IL2450 System Level Validation 7.5 credits

Validering på systemnivå

This is a translation of the Swedish, legally binding, course syllabus.

If the course is discontinued, students may request to be examined during the following two academic years

Establishment

Course syllabus for IL2450 valid from Autumn 2008

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Specific prerequisites

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

Verification is today the principal component in the development cost of embedded systems and is often the reason for cost overruns and project delays. The EDA(Electronic Design Automation) industry has responded to this challenge by coming with a wide range of methodology components to improve productivity and improve quality of verification.

The objective of this course is to teach students modern verification methodology for Embedded Systems. After taking this course the student will be:
a) Familiar with fundamentals of embedded system verification,
b) Familiar with technologies and methodologies for embedded sytem verification,
c) Able to Develop Verification Plan, Verification Environment, Debug Embedded Systems and run regression tests for realistic embedded system examples.

Course contents

- Verification and Validation Plan
- Verification and Validation Strategies and Environments
- Stimuli Generation
- Test Bench Structures
- Regression Analysis
- Simulation Based Verification
- Bit True Verification of DSP hardware and software
- Constraint Based Verification
- Code Coverage
- Hardware/Software co-verification
- Virtual Prototyping
- Formal Methods
- Assertion Based Verification
- Model Checking
- Equivalence Checking
- Embedded Software Verification
- Reuse aspects of Verification and Validation Environments
- Rapid System Prototyping, Emulation
- Debugging and Testing Embedded Systems

Course literature

Writing Testbenches Using Systemverilog ,
Janick Bergeron
Upplaga: Förlag: Springer-Verlag New York Inc.
År: 2006 ISBN: 0387292217

Examination

- LAB1 - Laboratory Work, 4.5 credits, grading scale: A, B, C, D, E, FX, F
- TEN1 - Examination, 3.0 credits, grading scale: A, B, C, D, E, FX, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

Other requirements for final grade

Passed examination (TEN1; 3hp)
Passed laboratory tasks (LAB1; 4,5hp)

The examination has two components. 3 points for Labs and 2 points for a written exam. Students will be awarded grades from A to F with labs and written having weightage in the proportion 3:2 respectively. Both the labs and written exam will have components that the students will have to successfully pass to get the pass grades. To get the higher grades, the labs and the exam will have components that will have successively higher challenge in terms of grasp of concepts, problem solving and engineering skills. Students are expected to finish their labs before written exams.

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.