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# PIEZOELECTRIC STRAIN-TUNING of QUANTUM PHOTONIC COMPONENTS

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# Abstract

A promising approach for the application of quantum technologies is through the implementation of quantum optical circuits on-chip that presents key advantages such as stability, scalability and high-density integration. To achieve this goal, the main building blocks of single-photon generation, guiding and manipulation, and detection mechanisms must be realized to a reliable extent. However, it is challenging to implement these points simultaneously with high efficiency, as the suitable systems for each type of component exhibits their own drawbacks. In this project, the challenge of bringing on-demand sources together with low-loss passive components was overcome with a hybrid approach. III-V quantum sources were integrated deterministically to silicon-based nanophotonic circuits. The emission of the integrated sources was coupled to the nanophotonic waveguides and furthermore, were strain-tuned by electrically driving an underlying piezoelectric substrate. This work marks a prominent step towards the application of reconfigurable quantum optical circuits, by showing on-demand light generation from single-photon sources, coupling the emission into high quality circuits and tuning reversibly in a precise manner.

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# List of Abbreviations

| | |
|---|---|
| LOQC: | Linear optical quantum computing |
| QD: | Quantum dot |
| NWQD: | Nanowire quantum dot |
| RR: | Ring resonator |
| PMN-PT: | Lead magnesium niobate- lead titanate |
| PZT: | Lead zirconate titanate |
| PIN: | P-type – Intrinsic – n-type |
| PECVD: | Plasma enhanced chemical vapor deposition |
| EBL: | Electron beam lithography |
| E-Beam: | Electron beam |
| FBMS: | Fixed beam moving stage |
| RIE: | Reactive ion etching |
| vdW: | Van der Waals |
| PCB: | Printed circuit board |
| TE: | Transverse electric |
| TM: | Transverse magnetic |
| FSR: | Free spectral range |

# I. Introduction

Among the applications of various quantum technologies, linear optical quantum computing (LOQC) stands out as a promising method to realize quantum information processing due to various advantages of photons, such as high mobility and low decoherence. The table-top components for realizing LOQC, however, exhibit inherent drawbacks such as excessive occupation of space, complexity and risk of instability. In contrast, the components within on-chip nanophotonics are integrated and intact, thus present stability and robustness. With further advantages such as miniaturization and scalability, realizing LOQC on nanophotonic chips is a topic of current research, to which many efforts are being invested (1).

The components of an optical quantum information circuit comprise of three major building blocks. The first component type is means for qubit (i.e. single-photons encoded in path, time, polarization, etc) generation. Furthermore, means for guidance and manipulation of the qubit is needed to convey the information and implement unitary operations. Examples of manipulation components for LOQC include directional couplers, delay lines and filters (2). Finally, means for determining the nature of the qubit, namely detection mechanisms are employed.

There are various demands for each component type. Firstly, the quantum sources should have high extraction efficiencies and low multi-photon emission probability to generate quantum light to a reliable extent. The emission should be directional and of Gaussian mode for reliable and efficient coupling between the nanophotonic components. Moreover, photon indistinguishability should be attained at high levels in order to obtain high fidelity operation. For second part of guidance and manipulation, nanophotonic components with low-losses are needed. In general, III-V semiconductors, atom-like on-demand emitters are not adequate for the fabrication of nanophotonic circuits. The growth procedure of these emitters occurs in such fashion that millions of emitters grow in randomly distributed locations, which results in the substantial risk of reabsorption of generated single photons, or emission from unwanted emitters (2). On the other hand, Si-based materials, which exhibit low propagation losses, prove to be deficient sources in terms of on-demand emission (3). Their emission is of probabilistic nature relying on nonlinear interactions, in opposition to the desired on-demand fashion.

In this work, a hybrid approach for realizing generation and, guidance and manipulation components of on-chip integrated quantum circuits was implemented. InAsP quantum-dots embedded in InP nanowires were employed as the single-photon sources. Nanophotonic chips with $SiO_2$-cladding and $SiN_x$-waveguide-core layers were fabricated on top of a piezoelectric substrate, which introduced strain to the whole chip upon application of voltage. The single-photon sources were transferred to the fabricated chips by means of a micromanipulator, done at TU Delft by Zadeh, I. For the measurements, the nanowire quantum-dots (NWQD) were excited from top with a laser and the resulting emission spectra were collected either from top or coupled to the on-chip waveguides and collected from the end facets by means of fiber-coupling. The spectra were detected by a liquid $N_2$ cooled Si charge coupled device (CCD) camera. As for the main scope of this project, the single-photon sources emission was tuned by applying strain, while simultaneously recording the spectra.

As a second part of the work, the concept of piezoelectric tuning was implemented further on passive nanophotonic components with the same compositional structure. Arrays of photonic circuits, comprised of through- and drop-ports coupled by ring resonator (RR) filters were designed and fabricated.

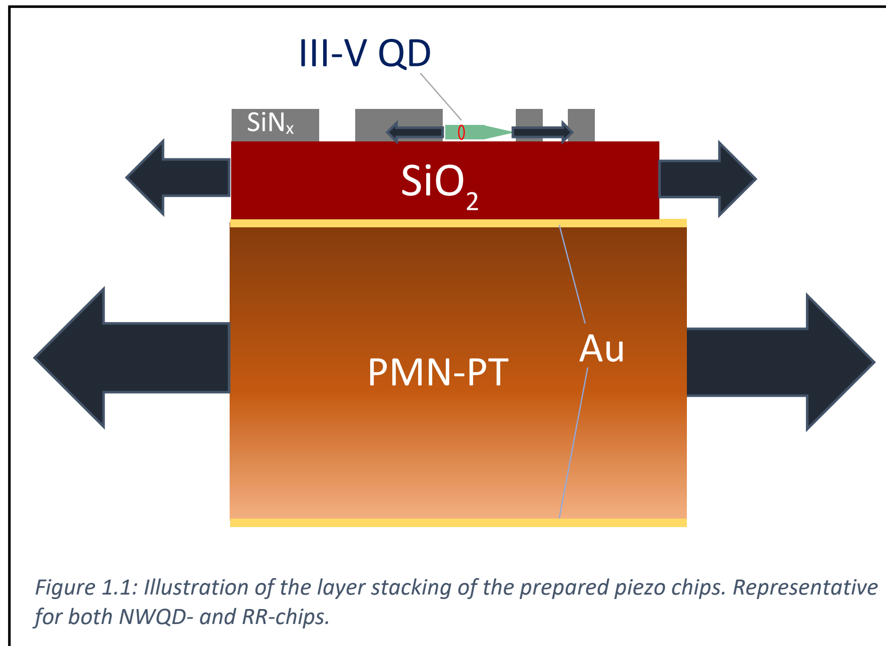



*Figure 1.1: Illustration of the layer stacking of the prepared piezo chips. Representative for both NWQD- and RR-chips.*

A schematic illustration of the fabricated chips can be seen on figure 1.1 with a NWQD integrated to the chip. For both NWQD- and RR-chips, lead magnesium niobate- lead titanate (PMN-PT) substrates were employed as the piezoelectric actuator. Gold contacts were fabricated on top and bottom of the piezoelectric substrates to serve as contacts for the application of an electric field throughout the material. On top of the top Au contact, a $SiO_2$ cladding layer of 2.5 μm and nanophotonic $SiN_x$ waveguides with 800 nm of width and 230 nm of height were fabricated. An electric applied through the piezoelectric substrate results in biaxial strain, indicated by blue arrows on the figure, which is transferred through the intermediate layers up to the NWQDs. Upon on-demand excitation of the NWQD's by laser radiation, the strain-tuned emission spectra were recorded over a voltage range between -600V and 600V once as-transferred and once after encapsulating in a bilayer of 30 nm $SiN_x$ and 200 nm of $SiO_2$.

The overall flow of actions was as follows:

1. Polishing of the PMN-PT chips
2. Evaporation of Cr/Au metallic bilayer
3. Deposition of $SiO_2$
4. Deposition of $SiN_x$
5. Electron Beam Lithography
6. Dry Etching
7. Cleaving
8. Source Integration (for NWQD chip)
9. Chip Integration
10. Electrical Functionalization
11. Measurement

# I.I Strain-Tuning

The energy band of materials arise from the cumulative interactions of the electrons and atoms in the lattice (4). Along with the electronic configuration of the atomic units, the crystallographic configuration has a decisive effect on the band configuration, as the crystal momentum of the energy band is given by periodicity of the lattice (5). Therefore, changes in the lattice parameters by e.g. heat result in the alteration of the band configuration, as the lattice of the crystal is subjected to change by such perturbations.

In optically active two-level systems such as single quantum dots (QD), electron-hole pairs that are bound by the Coulomb interaction constitute quantum states called excitons (6). Upon recombination of the bound electron-hole pairs, light is emitted with the emission wavelength that correspond to certain energy values defined by the various energy levels that the excitons are allowed to assume. The energy levels are determined by the excitation state of the excitons (7), the crystal momentum of the charge carriers and their respective lattice potential (8). Introducing interatomic distance changes (e.g. by applying strain) into the lattice of a QD alters the confinement potential and the crystal momentum of the excitons, which in turn leads to changes in their energy levels (9). This effect of strain manifests itself as a shift in the emission wavelength of the QD that can be observed by simultaneous excitation and emission collection.

## I.I.I Piezoelectricity

Piezoelectricity is the concept of electricity generation in a material upon applied stress or the reverse effect of stress generation by the application of an electric field throughout a piezoelectric material. It is a ubiquitously applied phenomenon. Almost every electronic device has a piezoelectric frequency generator (10); other daily applications of piezoelectrics include lighters or clocks. Near to these conventional uses, novel approaches of piezoelectrics in industry and in research are also being implemented. Prominent examples are energy harvesting applications (11), actuators for AFM stages, acoustic devices and thin film resonators (12-14).

The piezoelectric effect arises from the crystal structures of the piezoelectric materials, which are non-centrosymmetric, i.e. the lattice lacks inversion symmetry. In such structures, below the material-specific Curie-Temperature $T_c$ (6), the central ions within the lattice unit are located by an offset from the center. This results in the formation of a dipole, which collectively results in the spontaneous polarization of the material. Lattice units that are polarized in the same direction form the so-called (piezoelectric) domains, which are separated by the domain-walls defined by the equilibrium between the mechanical-, electrical- and thermal energy interplay of the domains (15).

In semiconductors research, piezoelectric materials bring together the advantage of tuning the optical properties of nanomaterials precisely and reversibly through the application of a voltage. This feature of piezoelectric substrates stands as a promising point for the future of quantum nano photonics, which demand fine control over the generation and manipulation components (6, 16).

### I.I.II Strain

The strain applied on a material can be described by the strain matrix $\varepsilon$, which comprises of the six independent strain components (8):

$$\varepsilon_{ij} \quad i, j \in \{1, 2, 3\} \tag{1}$$

where $\varepsilon$ is the 3x3 strain matrix and the numeric values represent the principal directions of the Cartesian coordinate system.

The strain parameters with the same indices ($\varepsilon_{11}, \varepsilon_{22}, \varepsilon_{33}$) indicate the strain acting on the atomic planes that lie normally to the applied stress, whereas the ones with different indices ($\varepsilon_{23}, \varepsilon_{13}, \varepsilon_{12}$) indicate the strain acting on the planes parallel to the applied stress. The strain acting on a material can be given by a 6x1 strain tensor and is the result of the externally applied stress together with the piezoelectric stress that arises from the electric field applied to the material:

$$\begin{bmatrix} \varepsilon_{11} \\ \varepsilon_{22} \\ \varepsilon_{33} \\ \varepsilon_{23} \\ \varepsilon_{31} \\ \varepsilon_{12} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} & S_{15} & S_{16} \\ S_{21} & S_{22} & S_{23} & S_{24} & S_{25} & S_{26} \\ S_{31} & S_{32} & S_{33} & S_{34} & S_{35} & S_{36} \\ S_{41} & S_{42} & S_{43} & S_{44} & S_{45} & S_{46} \\ S_{51} & S_{52} & S_{53} & S_{54} & S_{55} & S_{56} \\ S_{61} & S_{62} & S_{63} & S_{64} & S_{65} & S_{66} \end{bmatrix} * \begin{bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{31} \\ \sigma_{12} \end{bmatrix} - \begin{bmatrix} d_{11} & d_{12} & d_{13} \\ d_{21} & d_{22} & d_{23} \\ d_{31} & d_{32} & d_{33} \\ d_{41} & d_{42} & d_{43} \\ d_{51} & d_{52} & d_{53} \\ d_{61} & d_{62} & d_{63} \end{bmatrix} * \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{2}$$

Here, $S$ is the compliance tensor at zero electric field with units [1/Pa], $\sigma$ is the stress tensor with units [Pa], $d$ is the piezoelectric stress tensor with units [C/N] and $E$ is the electric field with units [V/m]. In the case of this project (and most of the other works), no external stress is applied to the piezoelectric substrate. Furthermore, the electric field is applied only in the third principal direction. These considerations simplify the above matrix equation to a large extent. Adding to these points, many of the piezoelectric coefficients (components of the piezoelectric stress tensor) are either equal to zero or each other, due to crystal structure symmetries. For PMN-PT, the non-zero piezoelectric coefficients are $d_{13}, d_{23}, d_{33}, d_{42}$ and $d_{51}$, where $d_{13}$ is equal to $d_{23}$ and $d_{51}$to $d_{42}$ (8).

Applying the simplifications mentioned above gives the following sub-equations:

$$\varepsilon_{11} = \varepsilon_{22} = d_{13} * E_3 \tag{3}$$
$$\varepsilon_{33} = d_{33} * E_3 \tag{4}$$

The other elements of the strain tensor equal zero.

These equations suggest that for a homogeneously applied electric field, the in-plane strain of the PMN-PT substrate will be biaxial and the values of the in- and out-of-plane strain will be proportional to the piezoelectric coefficients of the material, which are -699 pC/N and 1540 pC/N for $d_{13}$ and $d_{33}$, respectively (17).

### I.I.III PMN-PT

PMN-PT is a piezoelectric material that is a solid solution of lead magnesium niobate (PMN) and lead titanate (PT) with a perovskite lattice structure. The specific chemical formula of PMN-PT is given by $[Pb(Mg_{1/3}Nb_{2/3})O_3]_{(1-x)}$-$[PbTiO_3]_x$, where x is a value around 30%. This is the section of the morphotrophic phase boundary, where the most efficient piezoelectric performances are derived (18). Specifically, the best piezoelectric coefficients are obtained for a composition near x=33%, however, solutions with x=30% are usually applied due to their better compositional stability (6). The chips that were used during this project had a solid solution composition with x~30%. Lattice constants for PMN-PT (for x=29%) are a=b= 5.68 ± 0.91 Å and c= 4.03 ± 0.01 Å, and the coercive field is reported to be a value around 2 kV/cm (19).

There are many advantages for employing PMN-PT as strain-introducing components for experiments. As a relaxor ferroelectric (a subset of piezoelectric materials with extraordinarily high piezoelectric constants) it shows huge strain levels up to ~1.7% (20). The piezoelectric coefficients (electromechanical factor j, piezoelectric coefficient D, field-induced strain S) of PMN-PT are five to ten times higher than those of the common piezoelectric material lead zirconate titanate (PZT) (20). Further attractive features such as the large electromechanical coupling coefficient ($k_{33}$ =~90%), high dielectric constants and low dielectric losses make it an advantageous choice for non-resonant applications with large bandwidth and high sensitivity. These distinguished properties of PMN-PT, drop only negligibly at low temperatures, which makes it the excellent option to employ within quantum devices that operate at low temperatures (6).

# II. Research in Quantum Photonics and Tuning

For the successful accomplishment of this work, multiple aspects had to be considered as the work itself constituted the combination of different materials and techniques. Major points included the composition of the single-photon sources, their integration and coupling with the quantum nano photonic circuits, the material choice and design of the quantum nano photonic circuits, and the application of the tuning mechanism. A general approach for a systematic experimentation was strived for with the given parameter-scale, all of which could impose crucial effects on the results. In the following, the state-of-the-art research for these points is evaluated.

The tuning of the optical properties of materials can be done by various methods, i.e. by introducing thermal gradients, electric fields (21-23) or strain fields (24, 25). Thermal tuning suffers from introducing heat to the vicinity of the single photon sources, while tuning with electricity requires introducing electric fields to the QD, which either reduce the quality of emission or require the integration of the QD to a complex PIN device or similar structures (26). In contrast, within piezoelectric-tuning approach, the emission spectrum is tuned by merely altering the band configuration via strain, which is controlled precisely and reversibly, thereby inheriting no degradation potential.

PMN-PT has been recently employed in numerous works regarding tuning the properties of optically active nanomaterials (22, 27-30), where it is used as the strain-introducing substrate (8, 25, 27, 30-32). Many publications include work in strain-tuning of QDs that are either grown or etched on two-dimensional nanomaterials, which are subsequently bonded to the PMN-PT monolithic actuators by gold-thermocompression bonding (24, 27, 31). As an advancement of the monolithic substrates, the architecture of the PMN-PT chips can also be shaped by a combination of micromachining via femtosecond laser cutting and patterning the upper contact layer (8, 31). This results in multiple strain-introducing 'fingers' so that strain field can be manipulated more freely. This results in the independent control of multiple quantum properties such as the polarization, emission wavelength or the fine-structure-splitting of the excitons (27). Overall, this sophisticated control over multiple quantum properties heralds exciting opportunities for the future of on-chip quantum photonics, to implement significant LOQC experiments such as two-photon interference or entangled photon pair emission (25, 27).

### II.I.I Strain-Transfer

While achieving high values of strain within an actuator substrate is one thing, transferring the strain to the required layer is another. In this section, an approximation of the strain-transfer from the underlying piezoelectric substrate towards the above layers is discussed.

The strain-transfer of a material is correlated with its stiffness. Under uniaxial stresses, the Young's modulus $E$ is a good measure for the stiffness of a material, which in the simple case of an isotropic material is given as:

$$E = \frac{d\sigma}{d\varepsilon} \tag{5}$$

The above expression of Young's modulus is derived from the elastic regime of the macroscopic stress-strain behavior. Metaphorically, it is the top-down approach to define it. Microscopically (bottom-up approach), the elasticity of a material arises from the interatomic forces within the crystal. For a material structure that exhibits only primary bonds (i.e. van der Waals forces, dipolar interactions and Hydrogen bonds neglected), the Young's modulus is derived from the relation between the lattice potential and the lattice constant as (reference):

$$E = \frac{\delta F}{\delta a} = \frac{\delta^2 U}{\delta a^2} \quad (6)$$

Here, $F$ is the interatomic force, $a$ is the distance between two atoms and $U$ is the lattice potential. For crystals with higher lattice potential values and smaller lattice constants, the Young's modulus $E$ will be higher as the curvature of the potential-constant relation is higher towards these limits. This implies that materials with stronger bonds exhibit better stiffness and therefore the strain is transferred throughout the material more efficiently (50).

At this point, it should be noted that the above assumptions of uniaxial stress, a perfect crystal lattice composed solely of primary bonds are taken to evaluate an approximation for the strain-transfer. In reality, the crystal structure, i.e. the degree of crystallinity, and the purity of the materials will also have decisive effects on the strain-transfer. Defects such as substitutional- and interstitial atoms, stacking faults, dislocations together with the crystallographic considerations such as dangling bonds, coordination of atoms further impose effects on the strain-transfer within a material.

Finally, the third point to be considered for the strain-transfer are the design parameters of an experiment. The thickness and number of deposited layers for a chip's fabrication impose effects. The thickness of a layer determines, to what extent the defects within the layer are magnified. The number of defects is proportional to the volume of the layer, which is correlated to the thickness. Furthermore, the number interfaces between the various layers is crucial when transferring strain from one layer to another. Surfaces, where the atomic bonding structure deviates from the bulk form and boast many irregularities act literally as the 'weakest links' for the strain-transfer. It is therefore of best interest to keep the number of intermediate layers as low as possible and the quality of bonding the highest.

An interesting finding about the importance of the interfacial bonding is done by Ziss *et al.* (8, 19). In their work, the strain in a GaAs nanomembrane is investigated, which were bonded with an underlying PMN-PT substrate either through a Au layer through by gold-thermocompression bonding or with a polymer (SU8) through melting. It was expected that the strain-transfer in the former scenario would be higher, since the stiffness of Au is much higher than the soft polymer. However, their findings showed the contrary, which is explained by the inevitable presence of voids in the interfaces between the layers for the case of Au bonding. By comparison, SU-8 material is melted for bonding and therefore distributes evenly in a conforming fashion, which results in a much better strain-transfer between the layers, despite the material's lower stiffness.

In the case of this project, single-photons sources that lie on the surface of the piezoelectric chip is exposed to strain through the strain-transfer from the underlying PMN-PT substrate up to the nanowires on the surface. Imperfections within the intermediate layers and the interlayer boundaries cause screening of the transferred strain. Foremost, the PECVD $SiO_2$ contains defects such as dangling bonds and substitutional atoms (34), which are the primary reasons for shielding the strain-transfer. Also importantly, due to the low temperature nature of PECVD, the porosity in the $SiO_2$ layer is more pronounced compared to that of higher temperature deposition methods such as atomic layer deposition or low pressure chemical vapor deposition (51). Considering that the $SiO_2$ layer - being in the micron regime - is by far the thickest layer that plays a role in the strain-transfer (i.e. the PMN-PT and $SiN_x$ are excluded since they do not come into play for strain-transfer), the porosity and defects in this layer are the primary sources for a decreased strain-transfer.

Further defects that contribute to the decrease in the strain-transfer are the defects in the upper Cr/Au bimetal layer and the defects within each interlayer boundary. Stacking faults occur in evaporated thin Au films (33), which can be overcome by post-annealing. Moreover, mismatches between layers such as lattice mismatch or

mismatch in thermal expansion coefficient, and voids at the interlayer boundaries also contribute to the screening of the strain-transfer (19).

Finally, the strain transferred to the $SiO_2$ layer has to be further transferred up to the nanowires by means of weak intermolecular van der Waals (vdW) forces in the case of non-encapsulated nanowires, where in the case of encapsulated nanowires, it is transferred by additional interlayers. In each case, either the vdW forces or additional interlayer boundaries (and defects in these layers) will act as sources for further reduction in the strain-transfer.

### II.I.II Quantum Dots Embedded in Nanowires

The semiconductor quantum dots employed in this work are fabricated as embedded in nanowires, which act as waveguides for their emission. The NWQDs were previously grown, by Dalacu, D., and Poole, P.J., in a two-step bottom-up fabrication method combining selective area epitaxy and vapor-liquid-solid epitaxy (35). Through the control of the chamber parameters, the geometry and chemistry of the NWQDs can be precisely tuned. Thus, the size and position of the circular quantum dot, the length of nanowire and the tapering angle of the upper tip of the nanowire can be engineered to obtain desired emission properties.

Near to their multiple advantageous properties such as being high quality single-photon sources (36, 37), the pick-and-place mechanism of transferring them on to a destination quantum photonic chip enables site selection and controlled alignment. Moreover, the horizontal placement of the nanowires enables the in-plane emission coupling to the fabricated waveguides via butt-coupling through the waveguide facets, which is a prominent ability to realize efficient coupling on-chip sources to on-chip manipulation components.

# III. Materials & Methods

## 3.1 PMN-PT Chips

The single crystal PMN-PT chips were obtained from TRS Technologies (PA, USA). The chips comprised of surface 1x1 $cm^2$ surface area and thickness of 300 μm. This single-crystallinity of the chips enhances their fragility, of which the thickness is already in the micrometer regime. Although, dexterity and cautious handling were implemented overall when working with the chips, some chips broke in couple of occasions. In one incident, a chip shattered into pieces while put directly on the 300˚C hot holder of the plasma enhanced chemical vapor deposition (PECVD) chamber. In later operations that required heat, the chips were always heated gradually by steps of 50 ˚C, whenever the usage of a hot platform was required.

As the micrometer-regime thick chips were produced by a sawing procedure from the ingot, their surfaces exhibited large roughness values. An AFM image from a 10x10 $\mu m^2$ section of an unprocessed, as-obtained PMN-PT chip is given in figure 3.1. The sawing traces as well as the chunky material parts as result of the coarse sawing procedure are visible.

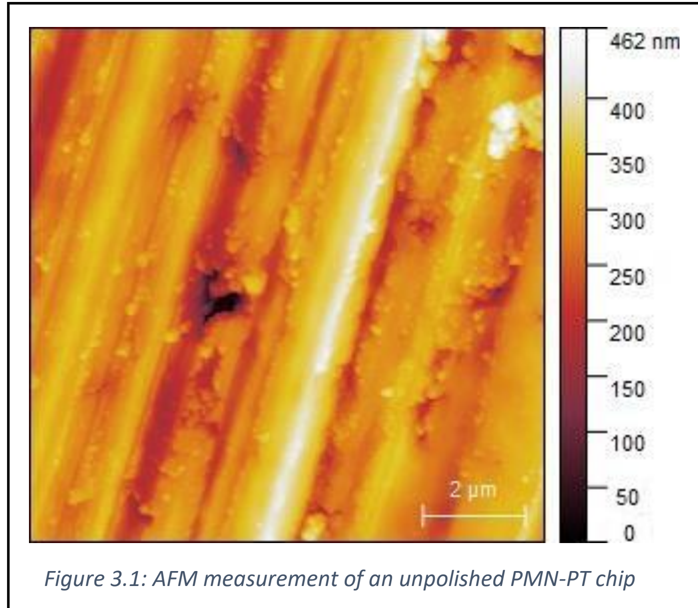


*Figure 3.1: AFM measurement of an unpolished PMN-PT chip*

The AFM measurements done on a total of four unpolished chips are given in table 3.1. Three of the investigated chips were from an old batch of shipment and had a thickness of 300 μm, whereas the fourth chip was from a newer batch and had a thickness of 200 μm. In total, 25 measurements were done on the unpolished chips within areas ranging from 2x2 $\mu m^2$ to 30x30 $\mu m^2$. The corresponding average $R_a$ roughness values are given.

*Table 3.1: AFM measurement results for various unpolished PMN-PT chips*

| Chip | Thickness | $R_a$ Average | Number of Measurements |
|---|---|---|---|
| ***Chip #1*** | 300 μm | 376,16 nm | 5 |
| ***Chip #2*** | 300 μm | 43,38 nm | 5 |
| ***Chip #3*** | 300 μm | 61,71 nm | 7 |
| ***Chip #4*** | 200 μm | 50,43 nm | 8 |
| ***Total*** | - | 49,32 nm | 25 |

## 3.2 Polishing

In order to make sure that the nano photonic waveguides that were to be fabricated on top of the piezoelectric chips, had smooth and straight profiles, the roughness in the roughness of the PMN-PT chips had to be polished away. This was done manually with a high-weight lapper (see figure 3.2). Initially, the chips were glued on to the cylindrical weight of the lapper. This was done by heating the metallic cylinder up to ~300 °C. After 10 minutes, the cylinder would become hot enough to melt the wax, which was applied on top of the cylinder to glue the PMN-PT chips by carefully placing to the middle. After gluing, the cylinder was put on the glass plate upside down to minimize the tilt of the chip upon the cylinder's surface as well as aid the sticking.

After this, polishing was done by tucking the cylinder into the balancing fragment (see figure 3.2) and moving in miscallenous ways. About 5 to 15 minutes polishing was done with each grinding paper, of which the set compised of multiple levels of diamond grain size distribution, decreasing sequentially from 30 μm, 15 μm, 6 μm, 3 μm, 1 μm, 0.5 μm up to a finest grind paper of which the diamond grain size is not given, but designated as "none". Finally, after polishing, the chips were scraped off from the cylinder. The chips were cleaned in the cleanroom by ultrasonication in acetone bath for about 2 minutes and dried with nitrogen gas. The cleaned and dried chips were reserved in Gel-packs.

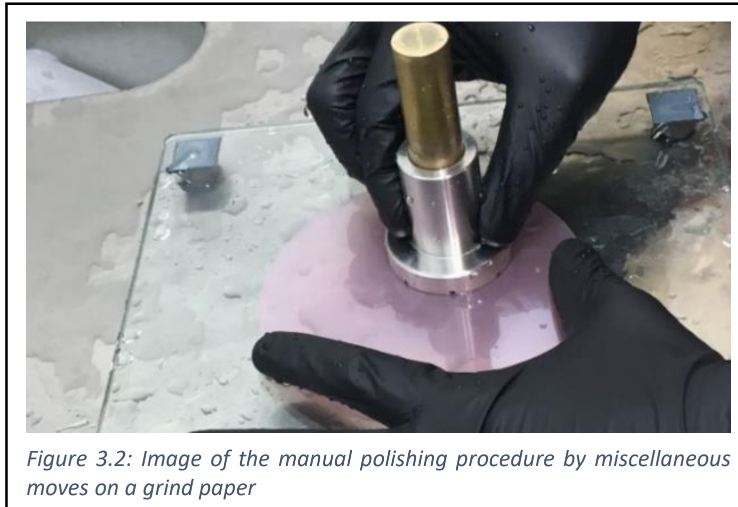


*Figure 3.2: Image of the manual polishing procedure by miscellaneous moves on a grind paper*

## 3.3 Evaporation

The next step after polishing was depositing thin Cr/Au bimetallic layers on both sides on both sides of the polished chips, which function as the contact layers for the application of electric field throughout the piezoelectric substrate.

The physical vapor deposition of electron beam (e-beam) evaporation was implemented. In e-beam evaporation, a source with the desired material to be deposited is heated via an electron beam. The atoms from the material are in turn locally evaporated and travel in the vacuum chamber in straight lines (38) to finally condense on the target substrate. The properties of the deposited film depend on the evaporation temperature and chemistry. As a rule of thumb, deposition at higher temperatures yield better films (39), since the adsorption and surface reaction procedures are thermally activated processes (38).

In the run of this project, multiple piezoelectric chips alongside with Si dummy chips were evaporated with bimetallic layers of Au and Cr. Prior to each evaporation session, the polished chips were cleaned in acetone and IPA for 1 minute each and blow-dried with nitrogen. Afterwards, the chips were fixated on to glass slides through application of photoresist S1818 to the sides and subsequent baking on hot plate at ~90˚C for 1 minute. The glass slides with the PMN-PT chips were further integrated in to the evaporator holder.

*Figure 3.3: Two piezo chips as-evaporated, glued to a glass slide, fixated to the evaporator's holder*

The e-beam evaporator used was an Edwards Auto 360 machine. Initially, a thin layer of Chromium with thickness values ranging between 5 and 30 nm was deposited. Being a good adherent to PMN-PT, Cr is conventionally used as an intermediate layer between Au and PMN-PT chips (6, 27). After the deposition of the thinner Cr layer, the Au layer was deposited on top of Cr, with thickness values ranging from 60nm to 100nm. Gold is an inert and a well diffusive material, therefore has good electrical and structural properties. In some of the recent works regarding the strain-tuning the out-of-plane emission of single-photon sources, Gold also brings the advantage of acting as a back-plane mirror enhancing the extraction efficiencies of the sources (24).

After the completion of evaporation, the glass slide was immersed into acetone bath and the chips were released such. The same procedure of the bimetallic layer evaporation was then implemented on the other side of each chip.

## 3.4 Chemical Deposition of Layers

Multiple requirements are to be fulfilled when choosing the right materials for the fabrication of nano photonic circuits. Ultimately, the refractive index difference between the core and the cladding layers has to be sufficiently high in order to confine the light in the photonic components to the extent of experiment specific reliability. The second most important point is the photonic performance of the circuit; propagation losses due to material-inherent absorption mechanisms or due to fabrication consequences (i.e. sidewall roughness) are to be kept as low as possible. Near to these points, ease of fabrication, compatibility for integration with other materials, mechanical robustness are further aspects to take into account for the choice of materials.

The chosen material system for the fabrication of the nano photonic waveguide components of this work was $SiN_x$ as the core and $SiO_2$ as the bottom cladding layer. There are several convenient aspects regarding the nitride-oxide material system for nano photonic applications. Firstly, the moderate refractive index contrast $\Delta n$~0.55 in the near infra-red provides good optical confinement, giving low scattering losses (40). Furthermore, the Si-based nature of the materials boasts the ability to tune the refractive indices by tuning the chamber parameters of the depositions (41). Recent efforts for the integration of high performance III/V sources on silicon-based photonic circuits (2), compatibility with deposition of single-photon detectors (42) and overall compatibility with microelectronics fabrication methods are the further crucial advantages of the $SiN_x$ / $SiO_2$ material duo, making it a promising candidate for the application of nano photonic processors of the future.

Plasma enhanced chemical vapor deposition (PECVD) was the chosen method due to its low-thermal budget, which include working temperatures usually below 400 ˚C by supplying the necessary deposition energy through the plasma. This low-thermal budget of PECVD is compliant with the need for low operating temperatures for the InP/InAsP nanowire quantum dots integrated into the chips. The QDs contain the volatile element Indium, are thus prone to diffusion and hence to deterioration at elevated temperatures.

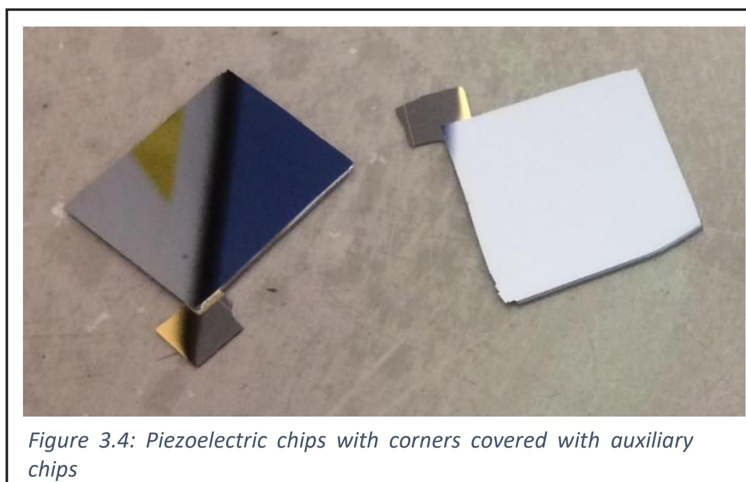


*Figure 3.4: Piezoelectric chips with corners covered with auxiliary chips*

Details about the chemistry and the chamber parameters regarding the deposition of the core and the cladding layers are given in appendix section. For the first piezoelectric chip with the NWQDs to be integrated on to, a bottom cladding $SiO_2$ of 2.5 μm thickness was deposited using $SiH_4/N_2O$ chemistry. The reason for this relatively high thickness value was to prevent coupling losses from the TE and TM modes in thewaveguides to the underlying Gold layer. The deposition of the $SiN_x$ waveguide core layer was implemented with a $SiH_4/NH_3$ chemistry. The value chosen for the deposition thickness of the core $SiN_x$ layer was ~230 nm. This value is slightly different than the waveguide height value of the previous works, which was 200 nm (43, 44). It was observed within the FDTD simulations ran for mode confinement measurements with Lumerical software (section 4.1) that higher values of $SiN_x$ layer thickness resulted in better confinement of the single modes and less propagation loss. This trend improved with higher thickness values for $SiN_x$, however came with a trade-off of confinement of higher modes. Therefore, 230nm was chosen as the upper limit for the waveguide core layer thickness. Furthermore, the simulations showed that the $SiO_2$ cladding could be decreased down to 2 μm without any compromise of coupling loss to the Au layer. This value for the $SiO_2$ layer thickness

was implemented in the fabrication of the second chip with ring-resonators, which was fabricated after the simulations.

### 3.4.1 Strain-Enhancement by Encapsulation

In the second part of the experiments for the chip with NWQDs, a 30 nm $SiN_x$ and a 200 nm $SiO_2$ layers were deposited on to the chip with the NWQDs, as an attempt for anchoring the nanowires to the surface and thus increasing the strain-transfer.

## 3.5 Lithography and Etching

After the deposition of the cladding $SiO_2$ and the core $SiN_x$ layers, the next step was to construct the photonic circuit design. This was done by reactive ion etching (RIE) the waveguide core layer. Initially, the chips were spun with e-beam resists that were subsequently patterned by electron beam lithography (EBL) according to the specific design that were prepared with softwares RaithApplication or AutoCAD.

A considerable effort was given for finding the optimal resist for the EBL. Initially, maN-2403 was used, which is an easy-to-operate negative resist. Although success was attained with the initial sample designs that comprised of waveguides shorter than a hundred micrometers, adhesion problems were encountered for the actual waveguide designs which comprised of length values of more than several hundred micrometers. HSQ was another candidate, however it was dismissed due to its long exposure times caused by high activation dose. It was finally decided to use the positive resist CSAR 6200 09. Since CSAR is a positive resist, it also acted as a protection layer throughout the chip after etching.

Both the design for the NWQD-chip and the RR-chip were implemented on multiple and many locations on the resist and stuffed side-by-side as dense as possible. This enhanced the probability of obtaining functioning circuits, which are prone to risks of contamination or unsuccessful cleaving. The different designs of the NWQD-chip and the RR-chip are evaluated under separate sections below.

### 3.5.1 Chip Design for Nanowire Quantum Dot Integration

The design of the nano photonic circuits for the NWQD-chip is given in figure 3.5. It consists of:

1- A basin for the NWQD integration with the micromanipulator.
2- A straight bus waveguide (through-port) with inverse tapered end, from which the quantum-dot emission is to be coupled
3- Ring resonator filters to couple specific wavelengths of emission to the drop-port waveguide
4- A U-shape drop-port waveguide

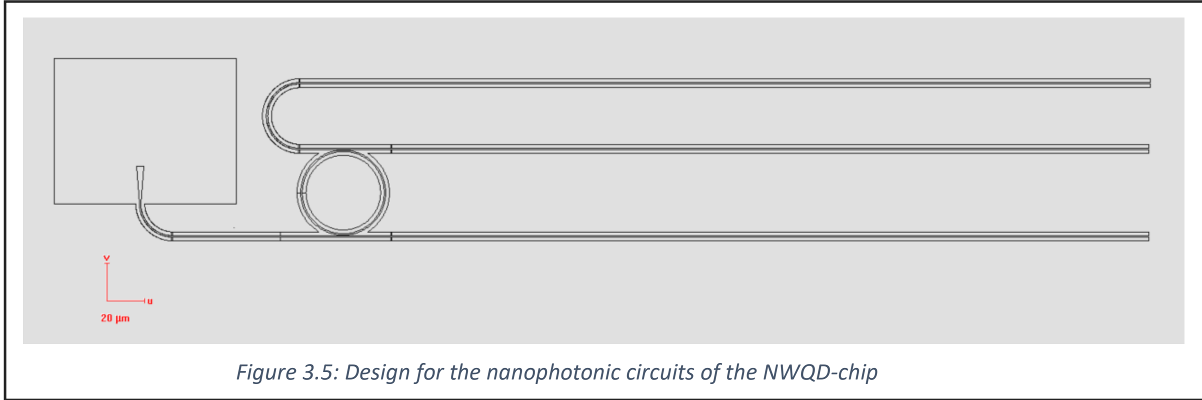



*Figure 3.5: Design for the nanophotonic circuits of the NWQD-chip*

The values for the dimensions within the design is given in the table 3.2. The waveguide dimensions of 800 nm width and 230 nm height are designed to give critical coupling for the transverse electric modes and transverse magnetic modes for distances between the waveguide and the ring resonator around 200 nm and 400 nm (44).

*Table 3.2: The dimensional values for the component features of the NWQD chip*

| Component | Feature | Size |
|---|---|---|
| **Through-port** | *Tail length* | ~500 µm |
| | *Bend radius* | ~20 µm |
| **Ring-resonator** | *Bus-to-ring distances* | 250 nm |
| | *Ring radius* | 40 µm |
| | *Tail length* | ~400 µm |
| **Tapered Coupler** | *Length* | 10 µm |
| | *Width* | 4 µm |

The EBL system that was used by the time the circuit design was prepared had two operation modes. For features that comprised of large straight distances with little or no curvature, the system was operated in the fixed beam moving stage (FBMS) mode. In this mode, the electron beam is kept stable and xyz-stage of the sample-holder is moved. For features that exhibit curvatures such as rings or bends, the system is operated under deflection mode, where the electron beam is deflected with magnetic coils according to the given design. The extent of deflection of the beam is limited and this defines the upper-limit of the system parameter write-field. Due to the limited write-field of deflection mode, it was only possible to design the ring-resonators with a radius of 40 µm, as opposed to the desired 70 µm radius values from previous works (44). However, for the NWQD-chip, the coupling of the NWQDs into the waveguides and the tuning of their emission was the main objective and this shortcoming was therefore not a major problem.

An optical micrograph of a dummy chip with the design for the NWQD-coupling is given in figure 3.6. Inset bar is 100 μm. The stacking of the circuits was not dense, since it was a dummy sample that was used. For the EBL of the actual chip, multiple of the same circuit grids were fabricated as densely as possible.

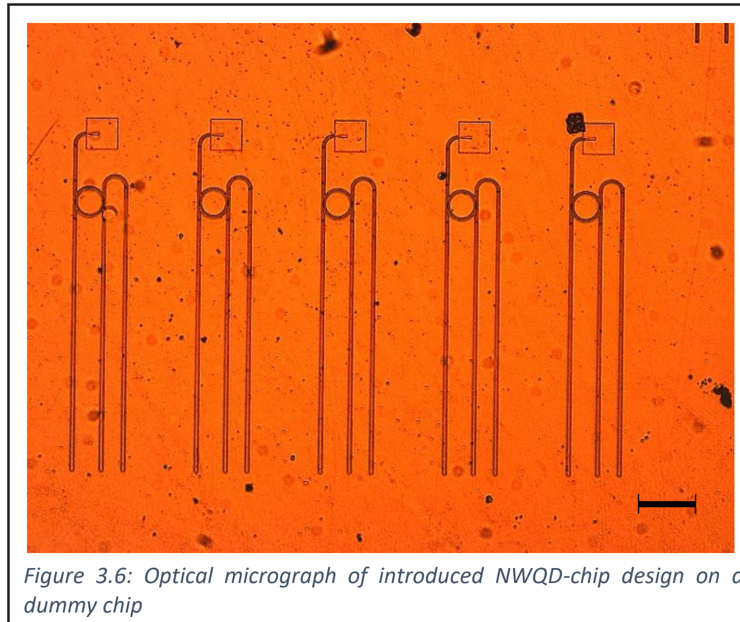


*Figure 3.6: Optical micrograph of introduced NWQD-chip design on a dummy chip*

### 3.5.2 Chip Design for Ring Resonators

In the second half of the project, a second chip with ring resonator filters was fabricated as an attempt to reproduce and advance the previous work accomplished by Elshaari, A. *et al.* (44) by means of piezoelectric tuning. A grid design of ring-resonators that couple through- and drop-ports was prepared. In figure 3.7, three arrays of this grid can be seen that were to be applied on ~4x4 mm$^2$ chips. In each grid, the bus-to-ring distance was increased gradually from 200 nm to 400 nm in steps Δd of 20 nm. The waveguide width and height were kept at 800nm and 230nm, respectively. As mentioned previously, these dimensions are calculated to give critical coupling for TE mode at ~d=200 nm and for TM mode at ~d=320 nm (44).

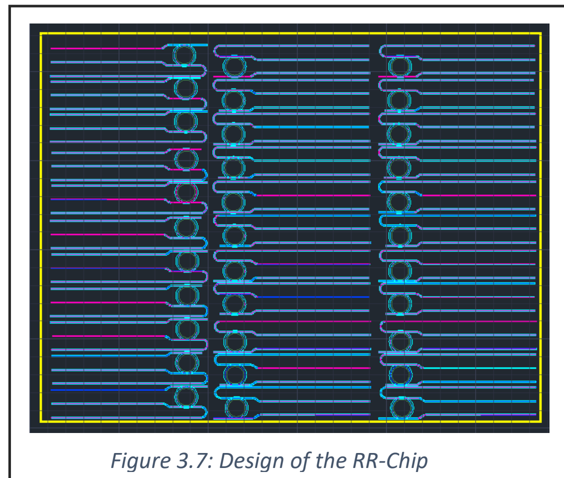


*Figure 3.7: Design of the RR-Chip*

As an improvement point in the second chip, the bottom cladding layer of $SiO_2$ was reduced to 2 μm. (with respect to the 2.5 μm in the NWQD-chip). Simulation results (see section 4.1) showed this value was the minimum limit for negligible loss and sound confinement of the fundamental waveguide modes.

## 3.6 Cleaving

In order to butt-couple light into and out of the waveguides, the tails of the waveguides had to be cleaved to expose the waveguides from the side through facets, in contrast to their embedded state as-fabricated.

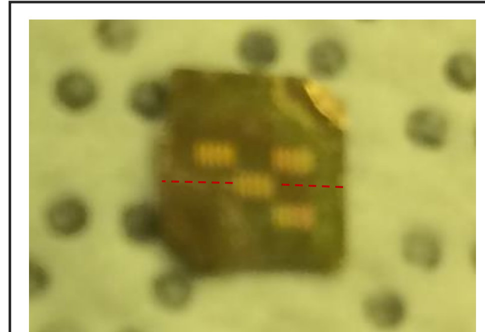


*Figure 3.8: A dummy chip with fabricated circuits. The red lines represent scribing*

Initially, the piezoelectric chips were scribed from both sides (dashed lines on figure 3.8) up until the waveguides, in order to not damage the waveguides. After scribing, the chips were cleaved into two by applying pressure from both sides of the scribing lines. The cleaving became a process of probabilistic nature that the crack propagation of the cleaving could occur in a crystallographic orientation but also can deviate, depending on the quality of the introduced scribes, homogeneity of the applied force and microscopic stress distribution effects.

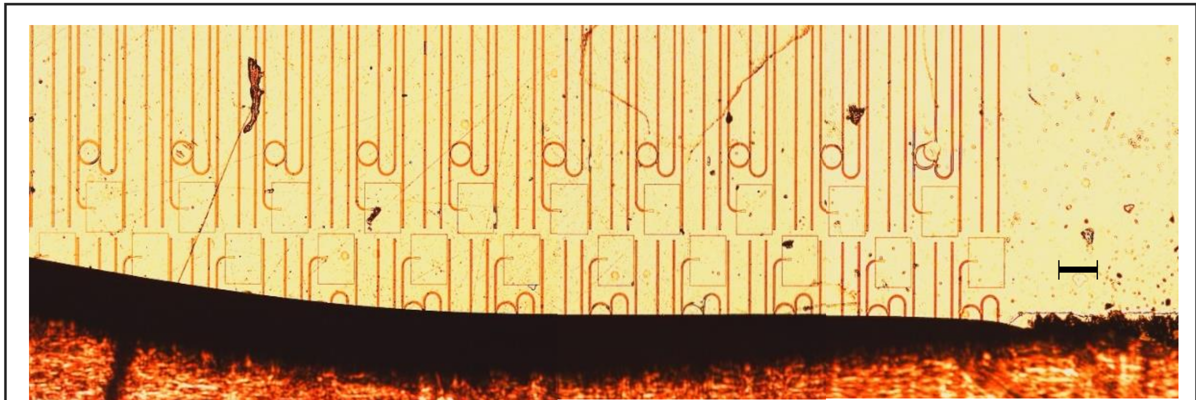


*Figure 3.9: Optical micrograph of the cleaved NWQD-chip, prior to integration of the NWQDs*

An optical micrograph of the cleaved chip on to which the NWQDs were transferred is given in figure 3.12. Inset bar is 100 µm. There was undesired cleaving through the ring-resonators, which meant that the function of this chip could only be to strain tune the NWQDs and couple their emission out-of-chip through the facets through-port waveguides but no coupling of emission to the drop-ports could be realized. A total of 11 nanowire basins, visible on the micrograph, were obtained with the possibility to integrate NWQD sources on to.

Means for deterministic cleaving of the chip and thereby exposing the waveguides through facets for butt-coupling is needed for the advancement of this type of work. Cleaving single-crystalline structures is a straightforward process resulting in ultra-smooth cleavage in the crystallographic directions. However, chips composed of multiple polycrystalline layers such as the one used in this work are hard cleave in a clean fashion. In order to obtain smooth waveguide facets in such devices, dicing of the chips can be applied with a following polishing procedure of the diced side. A more advanced method is the milling and shaping of the waveguide facet deterministically by focused ion beam milling, where exact control of the waveguide facet can be used to manipulate the out-coupling light distribution (45).

## 3.7 Single-Photon Sources

Single-photon sources to be integrated on to the fabricated NWQD-chip were circular InAsP quantum dots embedded within InP nanowires. The nanowire acts as a waveguide for the directional emission of the QD, of which the dipole axis lies on a plane perpendicular to the nanowire growth axis (43).

There are multiple advantages of the utilized single-photon sources. The NWQDs can be grown in a defect-free, ultra-pure Wurtzite structure (35), which manifests itself as high coherence values (29). Coherence times of 0.88 ns, and 1.2 ns (37) as well as a lifetime of 0.90 ns (25) are reported. In a two-step fabrication combined of selective area chemical beam epitaxy and vapor-liquid-solid epitaxy, the nanowire can be grown to precisely tune the dimensions of the QD and control its size and position within the nanowire. During the growth of the nanowires, the chamber parameters are altered abruptly for a briefly, in order to grow the InAsP QD instead of the InP nanowire. The parameters are then returned to the previous values to continue the growth of the nanowire waveguide. After a certain nanowire length value that exceeds the diffusion length of Indium, the nanowire growth front starts to taper with an angle depending on the chamber parameters. The precise control over the tapering length and angle present crucial the advantage for the control over the mode of light extraction, which has a Gaussian mode profile (36), enabling efficient coupling.

### 3.7.1 Deterministic Integration

Methods to integrate optically active materials on to piezoelectric substrates include among others bonding, integration (a.k.a. transferring) and epitaxial growth. Integration with a micromanipulator has the advantages of site-controlled placement of the quantum sources, as well as the alleviation of the need for extensive fabrication methods to grow sources on the nano photonic chip itself.

The InP/InAsP III-V single-photon sources were previously characterized as-intact on the growth chip, facing out-of-plane as grown. The sources with optimal emission properties – linewidth, brightness and homogeneity - were selected for transferring. The values for the largest emission peaks of each transferred NWQD are given in table 3.3. The characterization of the single-photon sources was done by Done by Ronan G. and Zadeh, I.
It should be noted that NWQD 3 exhibited two main peaks that were said to have same intensity values. For the sake of convention, only one of the peaks is reported.

*Table 3.3: The emission characteristics of the NWQDs as measured intact on the growth chip*

| Basin | NWQD | E | Linewidth | | Counts/second |
|---|---|---|---|---|---|
| **1** | - | - | | - | - |
| **2** | *NWQD 2* | 876,74 nm | 37.1 μeV | 0,023 nm | 14000 |
| **3** | *NWQD 3* | 886,34 nm | 30.8 μeV | 0,020 nm | 9000 |
| **4** | *NWQD 4* | 887,62 nm | 38.7 μeV | 0,025 nm | 5500 |
| **5** | *NWQD 5* | 888,11 nm | 31.4 μeV | 0,020 nm | 23000 |
| **6** | - | - | - | - | - |
| **7** | *NWQD 7* | 887,05 nm | 23.6 μeV | 0,015 nm | 8000 |
| **8** | *NWQD 8* | - | - | - | - |
| **9** | *NWQD 9* | 886,66 nm | 45.7 μeV | 0,029 nm | 17000 |
| **10** | - | - | - | - | - |
| **11** | - | - | - | - | - |

The transfer of the NWQDs with the micromanipulator was done, by Zadeh, I., in TU Delft. The machine consists of an xyz-movable differential stage, with a W-tip of 100 nm radius. As the tip approaches and contacts the nanowires, the vdW intermolecular forces come into play, strong enough to detach the nanowires from the growth chip (25). A detached and now to-the-tip-attached nanowire is then brought on to the chip surface towards the destinated NWQD basin. Upon contact, the nanowires attach to the surface to lie horizontally. Once placed, it is difficult to reclaim the nanowires from the surface. However, the nanowires can be poked from sides and such moved or rotated, which poses an additional advantage of the applied integration method, by making it possible to move and align the nanowires to optimize their coupling. The positioning and rotation accuracy of the micromanipulator is less than 250 nm and 0.5°, respectively.

## 3.8 Mounting and Poling

### 3.8.1 Mechanical Integration of the Piezo-chip

After the cleaving procedure - for the case of the NWQD-chip, following the integration of the sources - the chips were further processed to attain a mechanically integrable form-factor in order to mount them to the experiment setup and contact their top and bottom metallic layers electrically. The NWQD-chip was put on a Cu (~5x5 mm$^2$) holder of the Attocube cryostat, whereas the RR-chip was put on an Al (~10x10 mm$^2$) holder of a room temperature setup. As both holders were conductive and composed of similar dimensions, the procedure of the mechanical and electrical integration of the chips were the same for most of the part for both.

In the following, the mounting procedure is elaborated for the case of the NWQD-chip. Nuances with respect to the mounting procedure of the RR-chip are stated whenever necessary. The completed integration of the piezo (NWQD) chip to the Cu-holder of the cryostat is illustrated in figure 3.10. Initially, the piezoelectric chip was glued on to the conductive holder by Ag paste. Then a printed circuit board (PCB) with conductive layers on top was glued adjacently on to the holder, again with Ag paste. Wire-bonding was done between the PCB and the upper electrical Cr/Au bimetal layer, where a corner of the upper Au layer was previously left exposed during the PECVD of the waveguide cladding and core layers. Attention was paid to apply as little but sufficient Ag paste as possible. This yielded the moving freedom of the piezo chip to be able to exert strain. Furthermore, using little Ag paste made sure that no Ag paste climbed by surface tension forces and such contacted the upper Cr/Au bilayer, which would lead to fatal shortage of the electrical circuitry.

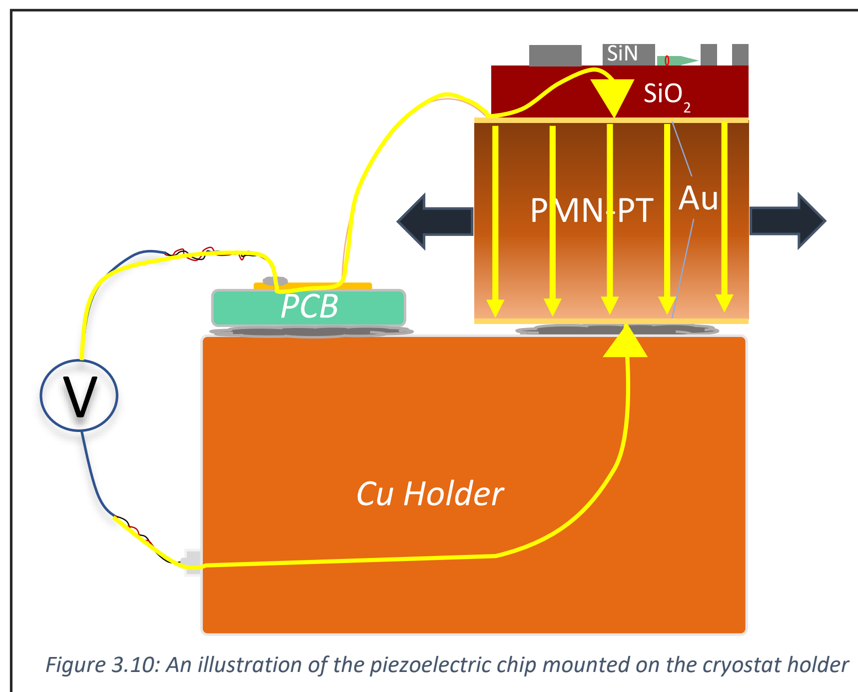



*Figure 3.10: An illustration of the piezoelectric chip mounted on the cryostat holder*

Afterwards, the PCB, which was previously soldered with an electric cable, was connected to the current compliant high voltage power source Keithley 1454. This was the electrical contact to the upper bimetal layer. For contacting the bottom bimetal layer, the electrical input of the Cu holder (see figure 3.10) was connected with the voltage source in the case of the NWQD-chip setup. For the case of the Al holder of the RR-chip setup, this was done by wrapping braded wires to the Al-holder - which did not consist of any electrical inputs - and connecting them to the voltage source.

A photographic image of the NWQD chip mounted on the Cu-holder can be seen in figure 3.11. The NWQD chip, labeled as ‘a’, lies to the south of the chip holder. Careful inspection reveals the 11 circuits cleaved to be butt-coupled with a fiber and the additional two arrays of waveguide circuits, which were in the embedded state, intact on the chip surface. The previously with electric cables soldered PCB are also visible, labeled as ‘b’. Not visible in the image are the wire-bonds between the conductive layer on the PCB and the exposed Au part of the piezo chip, since the diameter of these wires is in the micrometer regime. Labeled as ‘c’ is the rectangular holder with the square platform (5x5 mm$^2$) with the screw holes for fixing to the cryostat stage.

*Figure 3.11: A top-view photograph of the NWQD-chip as integrated on the Cu-holder of the cryostat*

### 3.8.2 Poling

The microscopic domains of a piezoelectric material as-manufactured align arbitrarily, i.e. the material is spontaneously polarized and therefore the piezoelectric performance is negligibly low (8). The "actual" piezoelectricity has to be activated by poling. During poling, an electric field throughout the material is ramped up to the specific threshold value corresponding to the electric field of domain switching, which refers to the rotation and the unidirectional alignment of the microscopic domains of the material.

An unpoled PMN-PT material exhibits spontaneous polarization in the [111]-direction. However, it is convenient to pole the PMN-PT materials in the [001]-direction which results in the best piezoelectric coefficients. Indeed, the PMN-PT chips that were used in this project were cut in the (001) direction.

The NWQD-chip was poled in vacuum conditions in the cryostat to prevent any electric sparks that could occur by the higher voltage values during poling. This poling under vacuum could not be done in the case of the RR-chip, since it was not a chamber setup. Nevertheless, no problem was encountered during the poling of either of the piezo chips.

In figure 3.12, the I-V curve for the poling of a piezoelectric chip is given. Ramping from 0V to more negative values, the current is initially in the nA regime, tracking a typical IV hysteresis that is characteristic for PMN-PT substrates (8). The current value starts to increase when the electric dipoles begin to rotate and align together, manifesting itself as a peak in the I-V curve attaining the μA regime. Once the domains are fully aligned, the current returns back to the nA regime. For the poling of the RR-chip, the domain-switch occurred at a voltage value at around ~63 V, whereas for the NWQD-chip, this value was around ~77V. The difference in the domain switching voltage indicates a difference in the thicknesses of both chips, since the domain switch electric field for both materials should be the same. This difference in thickness could be a result of the polishing procedures of the chips, applied in arbitrary durations for different chips.

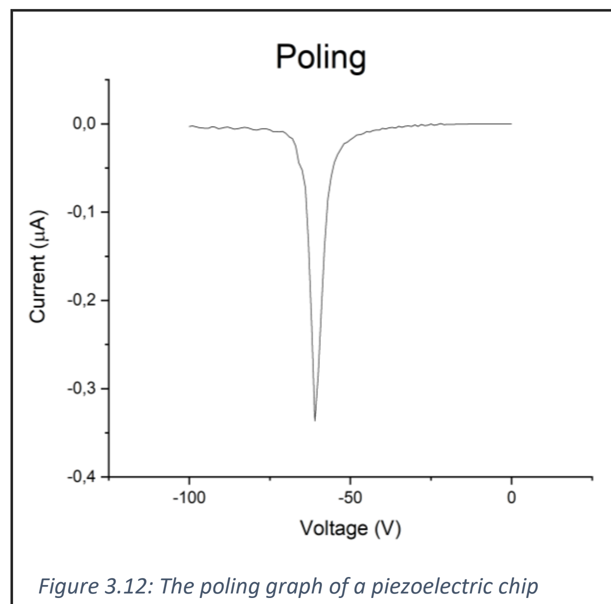



*Figure 3.12: The poling graph of a piezoelectric chip*

For the case of the NWQD-chip, the cryostat was ramped down to low temperature values only after the poling of the piezo chip. By doing so, the microscopic dipoles were "frozen", in the sense that the thermal energy of the domains was removed to a large extent. This facilitated the possibility to ramp the voltage further to values in magnitude that are much higher than the poling threshold voltage value at room temperature. Indeed, by freezing the piezo chip, the voltage could now be ramped between -600V and 600V, which is extensively large compared to the above given domain switching voltage of ~77V at room temperature.

## 3.9 Measurement Setups

Although the measurement of the RR-chip could not be implemented within the time period of this work, the tasks of setting up the optical setup and laser coupling into a dummy replica of the chip could be accomplished and are evaluated in this section, together with those of the NWQD-chip. Both the room temperature (RR -chip) and the cryostat (NWQD-chip) measurements were done on the same optical table.

### 3.9.1 Cryostat Setup for NWQD Chip

In this section, the configuration of the chip holder with respect to the fiber- and top-collection schemes and the piezoelectric moving stages within the cryostat will be elaborated. In a second part, the outer configuration of the excitation path and collection paths connected to the cryostat will be evaluated.

The inside of the cryostat can be seen on figure 3.13. Three major components are to be differentiated. The piezoelectric stage of the Cu holder standing in the middle with holder screwed from two sides is designated as ‘a’. To the right of the holder stage stands the coupling fiber, represented with dashed red lines; by careful observation, the silhouette of the fiber can be spotted, albeit faint. It is a tapered fiber specifically designed for single-mode coupling at 840nm wavelength, with a working distance of 13 μm. Thirdly, the platform for the objective lens on the upper side of the cryostat can be seen, designated as ‘b’. The stage of the chip-holder can be moved independently from the stage of the fiber, whereas the stage of the fiber moves together with the stage of the holder. In such operation manner, first the Cu-holder with the NWQD-chip is moved to couple the waveguide facets to the fiber. Then, the whole stage (fiber and holder) is moved to bring the laser beam collimated via the objective lens, on to the nanowire to be excited. This positioning procedure was repeated for each NWQD device.

In Figure 3.16 an image of the optical setup is given. The cryostat, designated as ‘a’ in the figure was ramped down to around 5,1 K and 4.7e-6 mbar of pressure. The red color indicates the excitation laser path, a wavelength tunable continuous wave source from Toptica with a maximum power output of 400 μW. The excitation laser is fiber coupled to the setup, directed towards an objective lens (confocal microscope, NA=0.82) through removable mirrors and beam splitters and finally collimated on to the chip with a spot size of ~1 μm. The working distance of the objective lens is 300 μm. The collection paths of the emission of the NWQDs are given in orange (top) and green (fiber-coupled). The fiber inside the cryostat is fiber-coupled through the coupling port of the cryostat, which was in turn coupled to the collection path towards the spectrometer, visible in figure 3.16. The path for the top collection was also coupled to the spectrometer through removable mirrors. The Acton SP2750 spectrometer from Princeton Instruments has a focal length of 0.750 mm, 1800 lines/mm grating and 50 μm slit entrance.

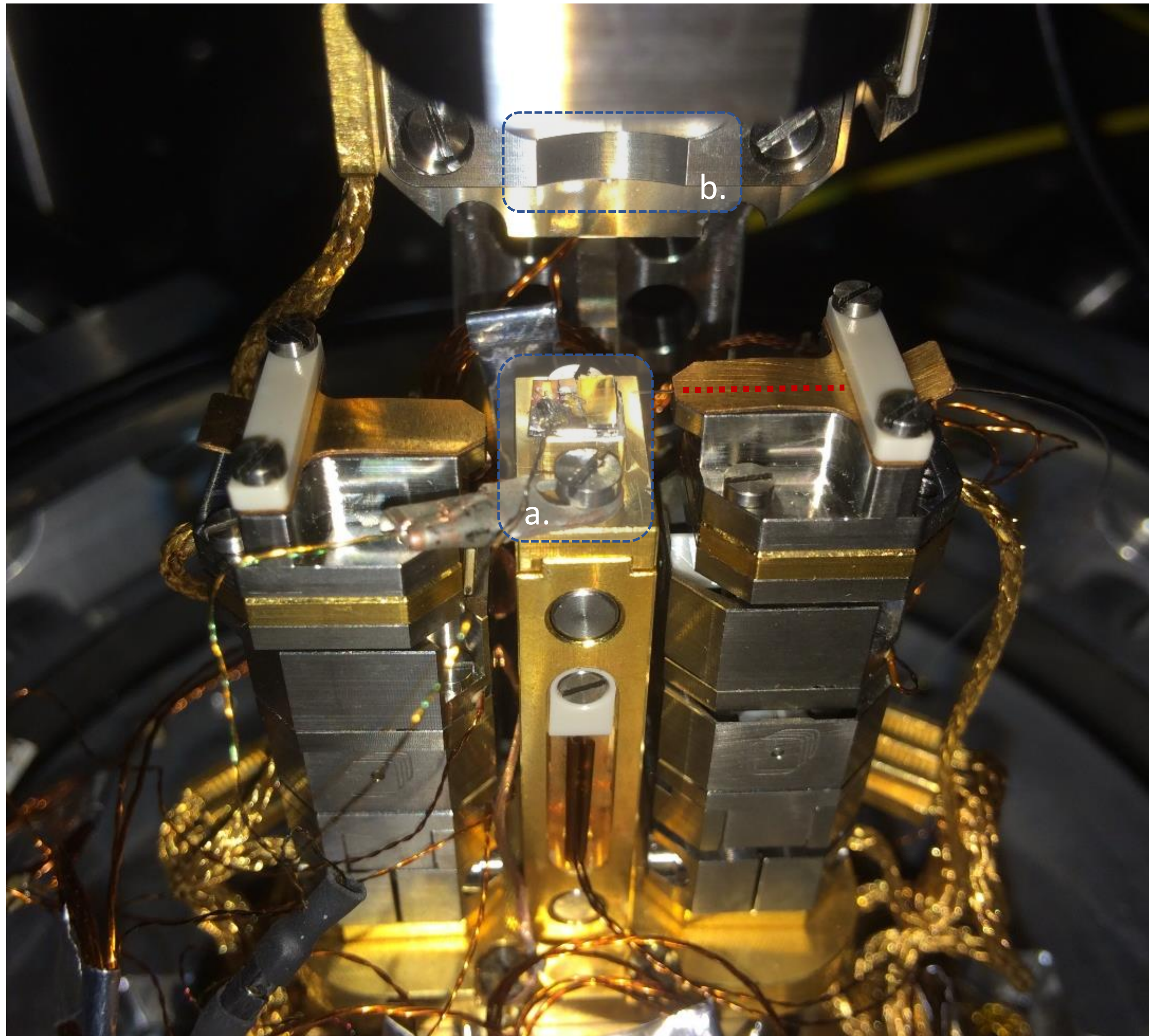



*Figure 3.13: The inner configuration of the cryostat. The platform for the objective lens (a), the Cu holder as screwed-in (b) and the tapered fiber (dashed line) are indicated*

The course of the experiments was as the following. The nanowires were excited with the laser non-resonantly, while simultaneously monitoring the emission spectrum around the expected emission value with the liquid-nitrogen-cooled Si CCD camera. Initially, the CCD camera was saturated with the NWQD emission by applying the laser at higher powers (μW regime). Through a powermeter, the laser power was gradually increased to excite the quantum dot below saturation. Then, the piezoelectric stage was moved in the horizontal plane to better locate the laser spot on the quantum dot section of the nanowires, which manifested itself as emission peaks getting sharper and brighter within the spectrum. By iteratively fine-tuning the lateral position of the nanowire and the illumination power, a sharp emission spectrum of the NWQD was obtained. Once the emission spectrum was set correctly, measurements were done by collecting the emission spectra while applying strain. This scheme of actions was repeated for each of the NWQD that was measured.

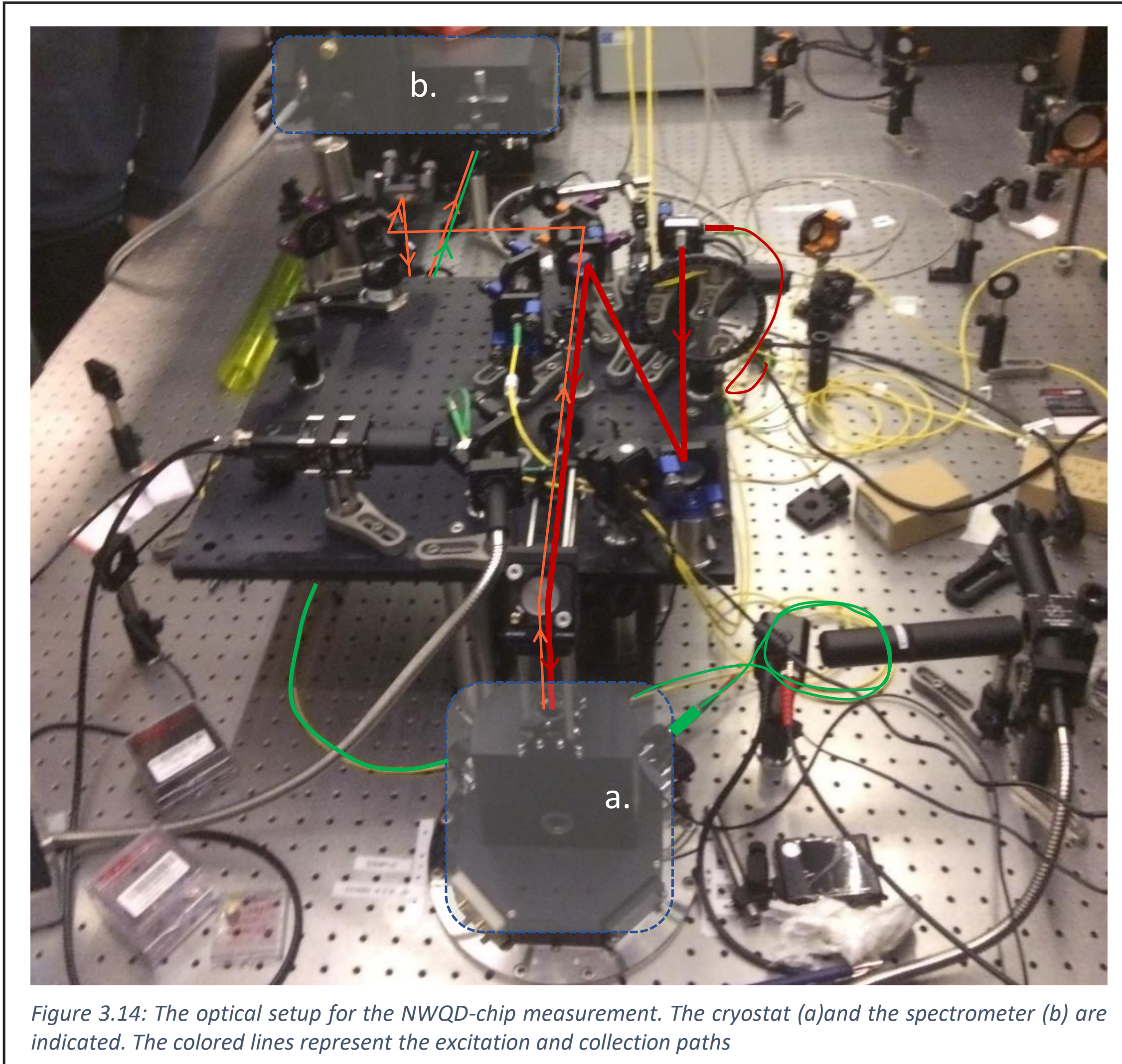



*Figure 3.14: The optical setup for the NWQD-chip measurement. The cryostat (a)and the spectrometer (b) are indicated. The colored lines represent the excitation and collection paths*

### 3.9.2 Room Temperature Setup for RR Chip

The microphotoluminescence setup of the RR-chip can be seen in figure 3.15. The piezoelectric chip is illustrated as the brown plate shown in the red circle, standing vertically as glued to the rectangular nose of the cylindrical Al holder. The two red and black cables from the high voltage power source can be seen on the bottom left. The cables were connected with braded wires, of which one was further connected to the soldered wire of the PCB (resulting in the upper layer contact) and the other one connected to the bottom layer by wrapping around the cylindrical Al holder. Notice that by the time the image was taken, the chip was not mounted on the Al holder, and therefore the electrical cables and the soldered braded wire cable are not visible. This setup was prepared together with Zhao, P. and Elshaari, A.

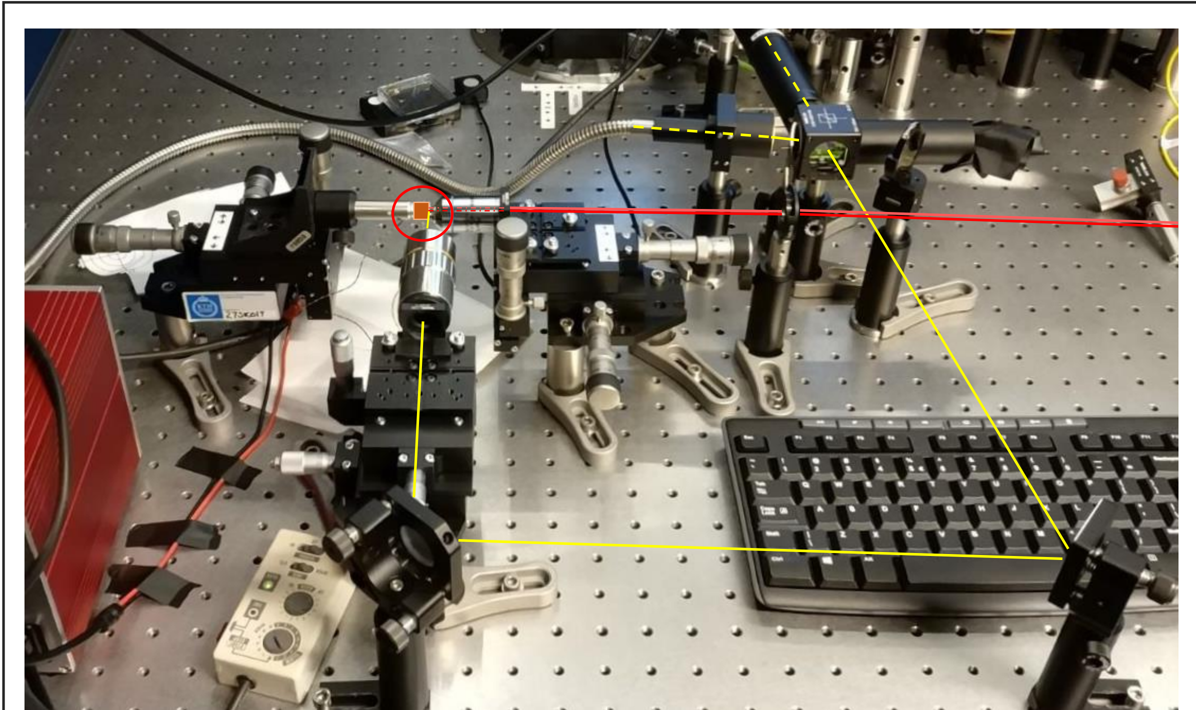


*Figure 3.15: The room temperature setup for the measurements of the RR-chip. Colored lines represent the laser excitation and collection (red and orange) and white light imaging (yellow) paths*

On the image of the RR-setup, the red line represents the excitation laser, coupled to the excitation path through fiber-coupling. The excitation laser is sent through a beam-splitter (not visible in the image), which is used to reflect the collection light from the chip towards the spectrometer. A pulsed supercontinuum laser from YSL was used, of which the wavelength was set around 850nm as designed for the RR-chip. Around one quarter of the total power (25% of 1,8 W) and a pulse rate of 0.5 MHz were used. The excitation beam is collimated through the objective lens with numerical aperture 0.65 and working distance of 600 μm. Through the manually movable xyz- micrometer stages, the chip position was aligned such that the laser beam would couple into the through-ports. In turn, light was coupled out from the drop-port, given by the orange line. The collected light is reflected towards the spectrometer Acton SP2750, which was used also for the cryostat measurements.

For the measurements with the RR-chip, the light was coupled in to the through-port and the light coming out from the drop-port was collected and monitored by the Si CCD camera. The xyz-stage of the piezoelectric chip was moved to fine-tune the collection spectrum, together with a polarizer.

# IV. Results & Analysis

## 4.1 Thickness Simulations

As mentioned previously, the biaxial strain exerted within the underlying PMN-PT piezoelectric substrate is transferred towards the overlying NWQDs through the interlayers between PMN-PT and Cr/Au, Cr/Au and $SiO_2$, and through the vdW-forces between the nanowire and the $SiO_2$ surface. These layers contain defects such as stacking faults in the evaporated gold (46) or dangling- and hydrogen bonds in the PECVD $SiO_2$ (38, 39). These types of disorder in the intermediate layers lead to a reduction in the strain-transfer, which is executed by the sum of the collective interatomic distance changes.

In order to increase the strain-transfer and so the tuning range of the NWQD emission, a strategy for reducing the thicknesses of the underlying layers (Au and $SiO_2$) was suggested. It was decided to focus not on the Au layer, since this was already at the nanometer regime. In contrast, the $SiO_2$ layer which was in the micrometer regime could be reduced. Therefore a lower boundary for the $SiO_2$ thickness value was sought by simulations, with the conditions that sound confinement of the fundamental TE mode within the core layer and low values of propagation loss would be obtained.

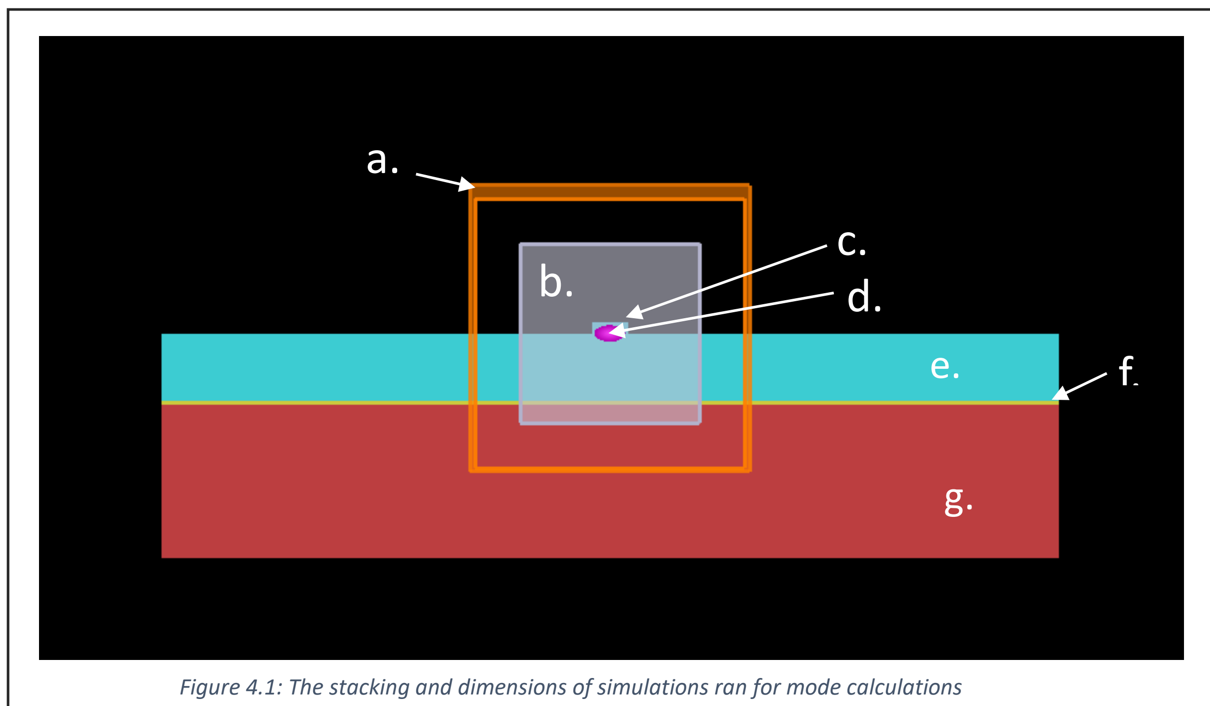



*Figure 4.1: The stacking and dimensions of simulations ran for mode calculations*

With regards to reasons evaluated above, mode calculations were run by simulating the physical stacking of the piezoelectric chips in the Lumerical software and parametrically sweeping the related thickness values of the $SiO_2$ and the $SiN_x$ layers. Although $SiN_x$ thickness value did not have a direct role on the strain-transfer, higher thickness values for this layer implied more tolerance on the reduction of the $SiO_2$ thickness, which meant a better trade-off with overall reduction of the total thickness. The cross-sectional illustration of the chip stacking is given in figure 4.1. The PMN-PT layer (g) lies at the bottom as the substrate with sufficiently large thickness to include the simulation region (a) for all the varying thickness values of the layers. On top of the PMN-PT substrate, a 100 nm Au layer (f) was set. The $SiO_2$ layer (e) and the $SiN_x$ waveguide (c) were varied in thickness from 1.5 microns to 2.5 microns and from 200 nm to 250 nm, respectively. The width of the $SiN_x$ waveguide was

kept at 800nm, in correspondence with the fabrication design, whereas the width of the other layers were kept at sufficiently large values to include the simulation region.

A cross-sectional eigenmode solver (d) was included at the middle of the waveguides (on z-axis) , which solves the Maxwell's equations at its defined 2D-layer. It calculates the mode field profiles with the respective effective refractive index and loss values. The geometry of the solver was set such to extend down until the Gold layer reaching to the PMN-PT chip, visible on figure 4.1 as the semi-transparent cross-section. Modes for sources with injection in the z-axis and a dipole plane (b) in the xy-plane were calculated. The wavelength around which the modes were calculated was set to 890 nm to find the corresponding modes for the NWQDs' emission, which had an average emission approximately around this value.

The refractive index for PMN-PT at a wavelength of ~880nm was taken from literature as a value close to 2.5 (47). The refractive index for $SiN_x$ and $SiO_2$ layers were set to 1.94 and 1.46, respectively, obtained from the resometry measurements previously implemented by Elshaari, A. Finally, the refractive index for the Au layer was set by the material database of the software, with a value of 0.8 at a wavelength ~886nm.

From the resulting lists of the calculated modes and the respective effective refractive index and loss values, the values for the modes of interest, i.e. the fundamental TE- and TM-modes were extracted.

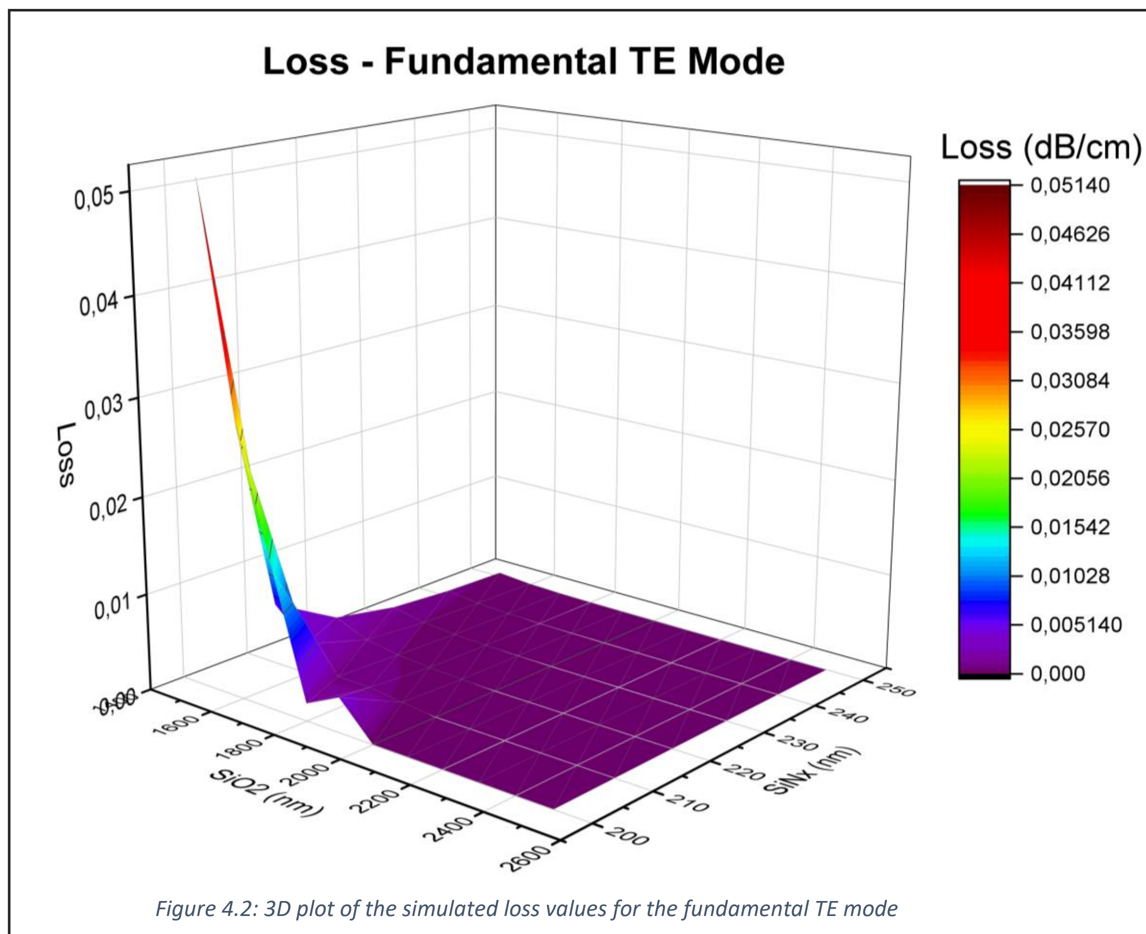



*Figure 4.2: 3D plot of the simulated loss values for the fundamental TE mode*

The loss values from simulation results for the fundamental transverse electric (TE) mode are given in figure 4.2. For each thickness value of the $SiN_x$ layer, a trend was observed such that the propagation loss started increasing below a certain thickness of the $SiO_2$ layer. This critical thickness value for the $SiO_2$ layer decreased with increasing thickness value of the $SiN_x$ layer. This meant that a higher value for $SiN_x$ could be implemented in order to further reduce the $SiO_2$ layer thickness. However, confinement of the higher modes were observed for higher values of the $SiN_x$ layer (values higher than 250nm were also investigated). Therefore, a moderately thick layer of 230nm $SiN_x$ was taken, which was the highest thickness value with no higher mode confinement. In accordance with this value for $SiN_x$, the value for $SiO_2$ layer was taken to be 2 microns, where the loss was still at low values of practically zero. The mode confinement profile of the fundamental TE mode for 2 micron of $SiO_2$ and 230nm of $SiN_x$ is given in figure 4.3.

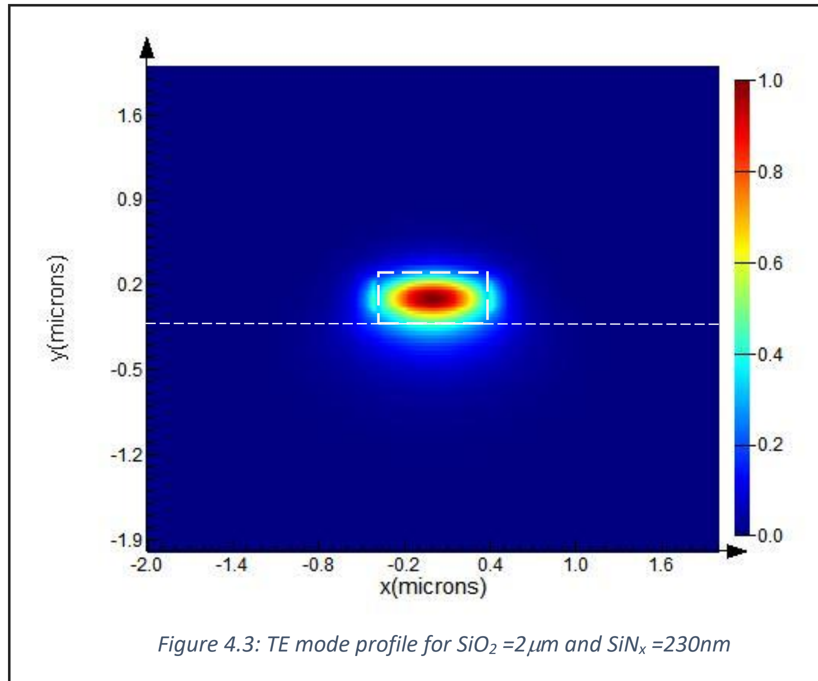



*Figure 4.3: TE mode profile for $SiO_2$ =2μm and $SiN_x$ =230nm*

Simulation for the confinement of the TM modes resulted in mode profiles with substantial leakage to the underlying $SiO_2$ layer within the given range of 200nm to 250nm of the $SiN_x$ layer. This problem can be overcome in the higher values of the $SiN_x$ layer such as 300nm. Since it was challenging to simultaneously have sound confinement of both the fundamental TE- and TM-modes, the confinement of the former was focused on during the project. The reason for this was that the profile of the TE mode exhibited polarization in the horizontal direction, in which the waveguide exhibits the larger dimension, thus giving more confinement in comparison with the fundamental TM-mode.

## 4.2 Strain-Tuning in NWQD Chip

In total, 7 NWQDs were transferred on to the NWQD-chip, by Zadeh, I. at TU-Delft. Out of the seven NWQDs, three showed tuning in their emission spectrum upon application of strain. The apexes of the sharp emission peaks of the NWQD spectrum was taken as the index to measure the strain-tuning. The magnitude of tuning of the three NWQDs were different. For a loop range between -600V and 600V, NWQD 7 showed emission peak tuning of Δλ=0.38nm, whereas NWQD 3 showed Δλ=0.22nm of tuning for the same voltage range. The emission peak tuning of the NWQD 9, which showed an order of magnitude less tuning of Δλ=0.015nm, was collected within a voltage range between -400V and 400V.

A scaled color image of the emission tuning of NWQD 7, collected from the top collection path is given in figure 4.1. The y-axis gives the wavelength range of which the emission was collected. Multiple peaks are visible which distinguished by higher brightness given by the color coding proportional to the photon counts. The x-axis is the voltage range which is swept between the high and low voltage boundaries of 600V and -600V. The emission of NWQD blue-shifts and red-shifts for increasing and decreasing voltage, respectively. The lowest and highest wavelength values that the brightest peak attains are ~885.15nm for 600V and ~884.76nm for -600V.

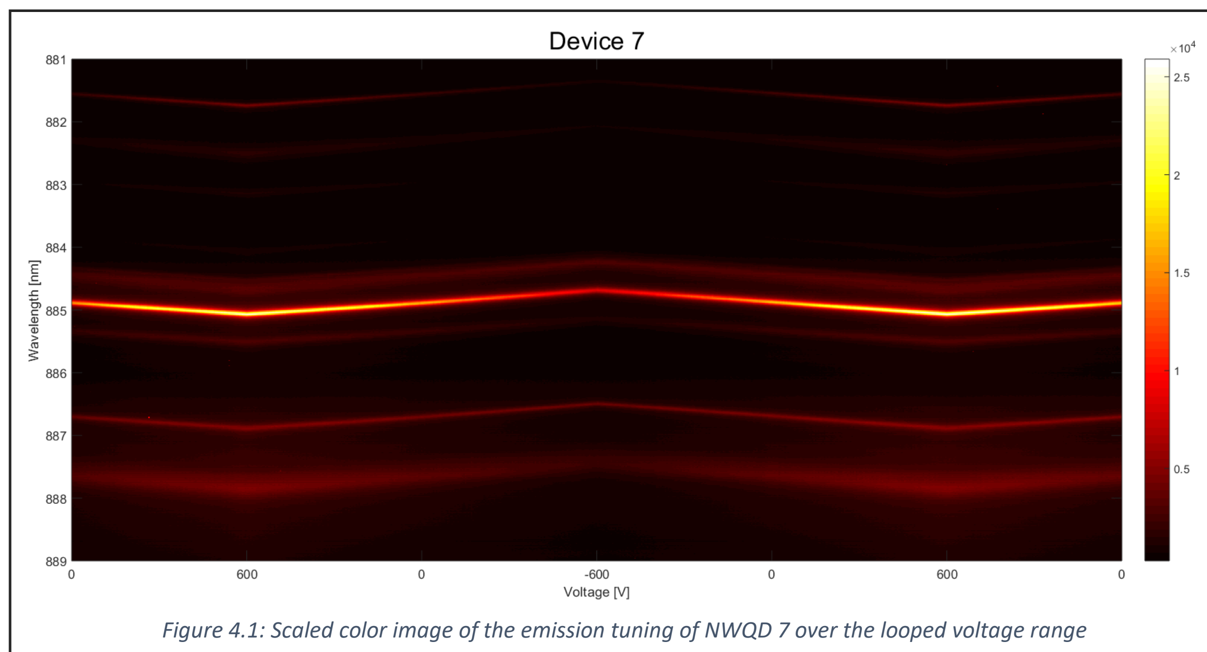



*Figure 4.1: Scaled color image of the emission tuning of NWQD 7 over the looped voltage range*

The emission peaks of NWQD 7 is shown in a stepwise illustration with steps of 300V's in figure 4.2. The normalized emission spectra are aligned on top of each other, starting from 600V towards -600V back to 600V again. The blue- and red-shift of the peak emission with decreasing and increasing voltage, respectively, are again visible. Furthermore, the other less bright emission peaks (dim lines in the scaled color image) can also be seen.

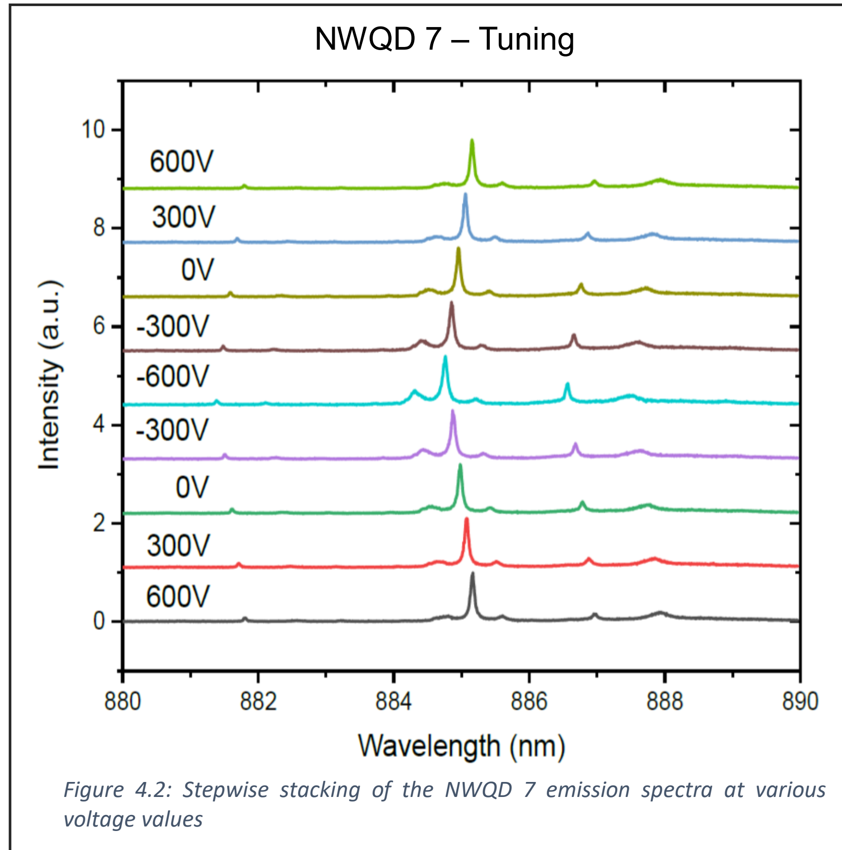


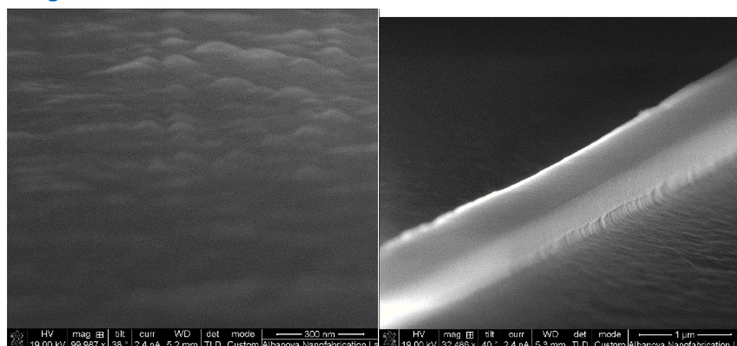

*Figure 4.2: Stepwise stacking of the NWQD 7 emission spectra at various voltage values*

*Table 4.1: Tuning and voltage ranges of the NWQDs*

| NWQD | Tuning Δλ | Tuning ΔE | Voltage ΔV |
|---|---|---|---|
| ***NWQD 2*** | - | - | 1200V |
| ***NWQD 3*** | 0,22nm | 0,35 meV | 1200V |
| ***NWQD 4*** | - | - | 1200V |
| ***NWQD 5*** | - | - | 1200V |
| ***NWQD 7*** | 0,384nm | 0,61 meV | 1200V |
| ***NWQD 8*** | - | - | - |
| ***NWQD 9*** | 0,015nm | 0,02 meV | 800V |

The tuning and voltage ranges of all NWQDs are given in table 4.1. Among the nine NWQDs that were transferred, 3 of them showed strain-tuning, in different magnitudes. The observation of difference in tuning ranges in these three NWQDs and no tuning in other NWQDs suggested either partial or no strain-transfer from the piezo chip to the NWQDs.

This is explained by the irrugularities in the SiN, so different nanowires have diffferent surface area contacted with the substrates which holds all the strain, so the strain transfer is very different. It all depends on the local toppology of the chip. Check the attached image that I took of the deposited SiN. The tool has issues, and it was not cleaned probably during the rings we made, so we ended up with lower quality SiN. Next image dhows SEM image of SiN surface



The maximal observed value for tuning of the emission energy belongs to NWQD7, with a value of 0,61 meV. This value is an order of magnitude smaller than those reported in the literature. In their work, Kremer, P.E., *et al.* report an average energy-tuning of 0.40 ± 0.33 meV over 40 measured NWQDs with a maximum emission tuning of 1.2 meV for one QD.

For comparison, Kremer's work consists of few differences. First, their NWQD material is GaAs/InGaAs. Firstly, no artifacts that has an impact on strain-transfer reduction, such as the polymer flakes in this work, were reported. Furthermore, differences in the design of the chip also has substantial effects. In their work, the chip of the NWQDs are flip-chip bonded to the underlying PMN-PT substrate by gold-thermocompression bonding. A total of 200 nm Au layer is the efficient strain-transfering layer, compared to bimetal layer of ~100 nm and 2.5 μm thick $SiO_2$ intermediate layers for strain transfer in this project. Furthermore in their work, strong chemical bonds are present where the Au is evaporated on the growth chip of GaAs, which is later on dry-etched to give NWQDs after the flip-chip bonding. In comparison, the nanowires in this work were either adhered by vdW-forces, or anchored by additional deposition of a bilayer of $SiN_x$ - $SiO_2$.

In a more recent work, the tuning of emission peaks of the same type of single-photon sources (i.e. InP/InAsP NWQDs) used in this work. (25). Specifically, the quantum sources were transferred on top of a PMN-PT substrate and excited from top while the collection was also implemented from top. The NWQD that showed the maximum tuning shifted ΔE= 6.3 meV in energy over a voltage range between -300V and 800V.

### 4.2.1 Light Coupling into the Waveguides

One of the most important points realized by this work was the coupling of the NWQD emission into the waveguide circuits. This is verified by comparison of the photoluminescence graphs coupled from the top collection and from the fiber collection. Such comparison is given for NWQD7 in figure 4.3. The left graph shows the photoluminescence as collected from top and the right graph as collected from the coupled fiber. The emission spectra is identical with background noise more prominent through fiber coupling and the distribution

of the intensities of some secondary peaks slightly differing, where the latter results from the difference in the applied laser power.

While the main emission peak of NWQD 7 gave count rates up to 64000 per second for top collection, this value was around ~1500 counts per 40 seconds for collection through fiber-coupling. The second device, of which the fiber coupling emission was also measured was NWQD 3. No fiber coupling measurements were done for NWQD9, since the emission of this device had strain-tuned one order of magnitude less than the NWQD 3 and NWQD 7, which was therefore not focused on. For NWQD 3 the ratio of counts between through top collection and through fiber collection was also extremely large as in the case of NWQD 7. These results suggest that the in-plane coupling of the NWQD emission is accompanied by large losses.

Several factors can have effect on the observed loss in the fiber-coupling scheme. The top collection is a straightforward process, where the emission from the quantum dot is directly coupled to the optical pathway of detection. By contrast, the collection through fiber-coupling scheme involves several more steps. First, the emission from the NWQD couples to the nano photonic waveguides. Here, two mechanisms, namely mode-size mismatch and effective refractive index mismatch between the waveguides and the single-photon sources come

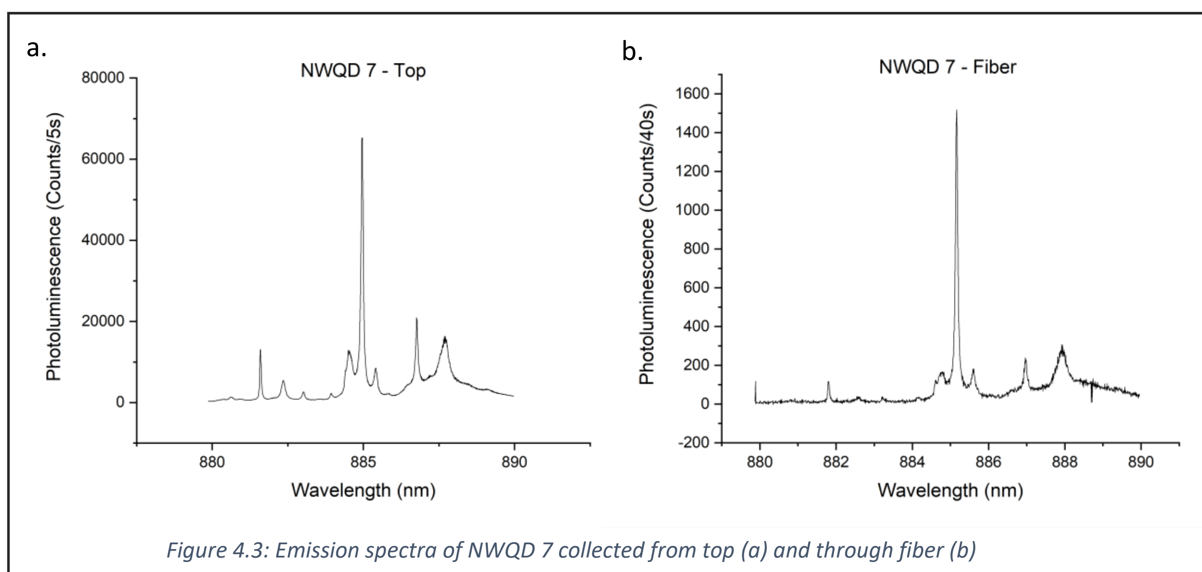



*Figure 4.3: Emission spectra of NWQD 7 collected from top (a) and through fiber (b)*

into play and lead to coupling losses (49). After coupling into the waveguide, the emission light is subjected to additional propagation loss, which are due to the loss coefficient of the waveguides, scattering from sidewall roughness and also from contaminating polymer deposition from the etching process, in addition to stitching error from connecting two different fields in the ebeam lithography. Finally, coupling-out from the waveguide to the collection fiber introduces additional loss where light distribution from the end of the waveguide depends on the quality of the cleaved facet.

The additional SEM investigations done by Elshaari, A., and Zhao, P. showed that the nano photonic waveguides were fabricated with a misalignment with the nanowire couplers. This error is expected to have the major contribution to the huge losses observed, as it distorts the modal mismatch between the nanowire and the waveguide mode.

Despite the substantial loss in intensity observed in the fiber-coupling scheme, the results show that the light emitted from the QDs could be successfully coupled in and out of the waveguides. The shortcoming of the huge losses can be improved by taking various measures; by improving the fabrication procedures, improving the tapering design and by introducing post-fabrication treatments such as annealing of the waveguides.

### 4.2.2 Strain-Tuning of the NWQDs after Encapsulation

As mentioned in the methods section, the NWQDs were encapsulated with a combined layer of 30nm $SiN_x$ and 200nm of $SiO_2$, in an attempt to anchor them to the surface of the piezo chip and thus increase the peak emission tuning by increasing the strain-transfer. The measurements after encapsulation showed that indeed the previously tuned NWQDs showed enhancement in their tuning range of emission wavelength/ energy. Specificall, NWQD 3 showed a peak emission tuning of 1.36nm, NWQD 7 of 1.59nm and with an astounding increase, NWQD 9 of 1.08nm. The emission tuning ranges before and after encapsulation are given in table 4.2.

*Table 4.2: Comparison of the tuning of the NWQDs before and after encapsulation*

| NWQD | Tuning Before | Tuning After | Increase Factor |
|---|---|---|---|
| ***NWQD 3*** | 0,22 nm | 1,36 nm | x 6,18 |
| ***NWQD 7*** | 0,38 nm | 1,59 nm | x 4,18 |
| ***NWQD 9*** | 0,015 nm | 1,08 nm | x 51,9 |

Notice that in order to get the increment factor in the tuning range of NWQD9, the initial wavelength tuning was extrapolated to 600V and -600V, where it was actually tuned between 400V and -400V. This extrapolation was done linearly for the fact that the emission peak tuning of all the devices were observed to tune linearly by voltage.

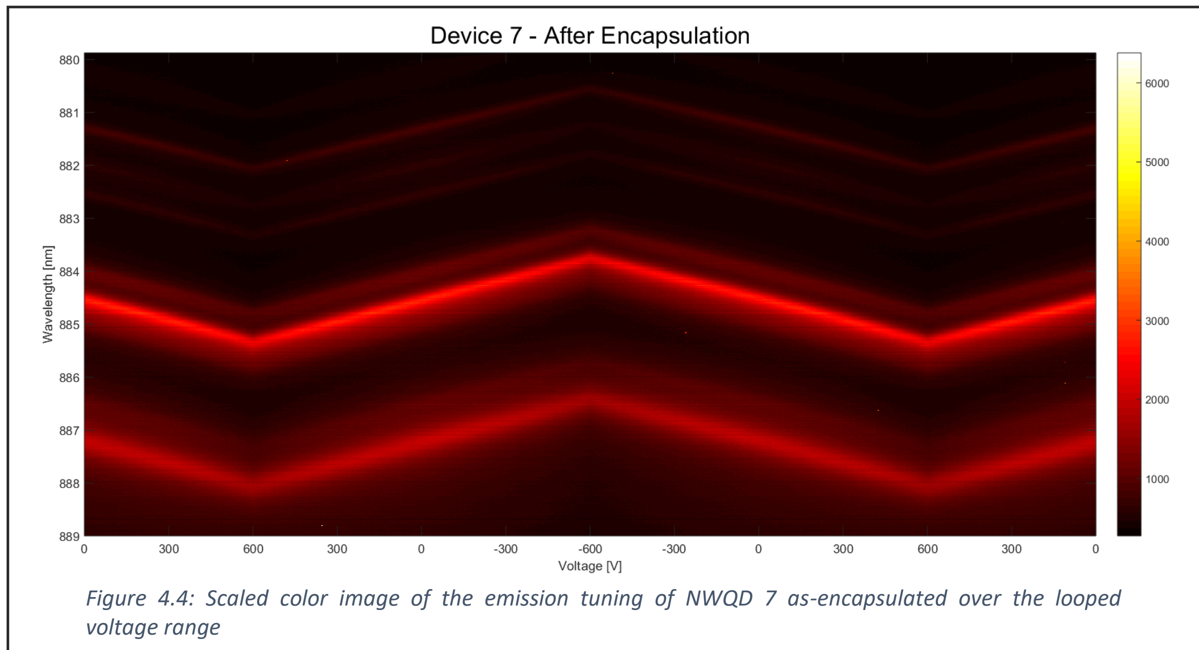



*Figure 4.4: Scaled color image of the emission tuning of NWQD 7 as-encapsulated over the looped voltage range*

In figure 4.4 and figure 4.5, the scaled color image and the stepwise stacking of the tuned emission spectra of NWQD 7 are given, respectively. For this device, the emission tuning range was enhanced ~4-fold as the peak emission blue-shifted from 885.41nm at 600V to 883.82nm at -600V.

An observation clear from figure 4.4 by the peak lines and more clear in figure 4.5 was that the emission peaks (of NWQD 7) after encapsulation were broadened and less bright. A confident explanation for this broadening behavior could not be found by the time of this reportation. One suggestion is that the deposited $SiN_x$ and $SiO_2$ introduces defects with surface states to the NWQD (this might actually be the case, the deposited materials have low quality, check my comment above), acting as traps for the charge carriers (24). However, the fact that the circular QD is embedded within the nanowire antenna constitutes a strong counter-argument for this, since the nanowire should shield the surface of the QDs.

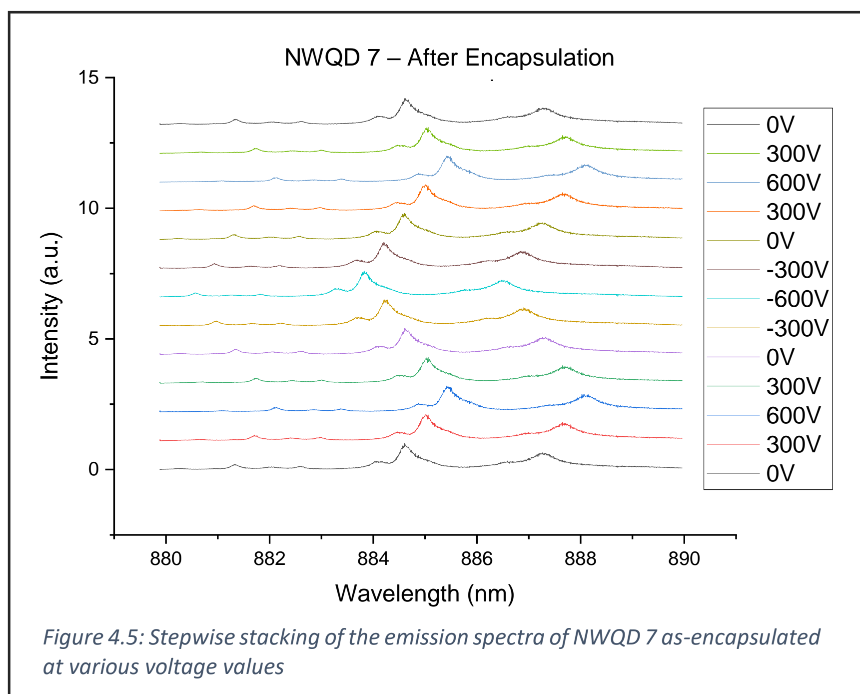



*Figure 4.5: Stepwise stacking of the emission spectra of NWQD 7 as-encapsulated at various voltage values*

Another possible explanation could be the diffusion of In atoms during the PECVD of the encapsulation layers. During encapsulation, the nanowires are exposed to the chamber temperature of 300 ˚C for around 5 minutes which is the total duration for the deposition of the $SiN_x$ and $SiO_2$. However in a previous work, Zadeh, I.E., *et al.*, worked with same type of NWQDs and encapsulated the devices within a $SiN_x$ layer of 200nm. Although PECVD at 300 ˚C was the applied deposition method with same precursor gases (PECVD, $SiH_4$ and $NH_3$), no fatal broadening of the NWQD emission was reported in their results (43). (our SiN have much lower quality, check above)

Another interesting point from the literature is the work of Chen *et al.* (25). *I*n their work, same type of InP/InAsP NWQD quantum sources and PMN-PT substrate are used. Additionally, some NWQDs were encapsulated in a thin layer of $SiN_x$, with the expectation of an increase in strain-transfer. Peculiarly, no difference in the strain-tuning order of magnitude was reported, nor any broadening in the emission spectra.

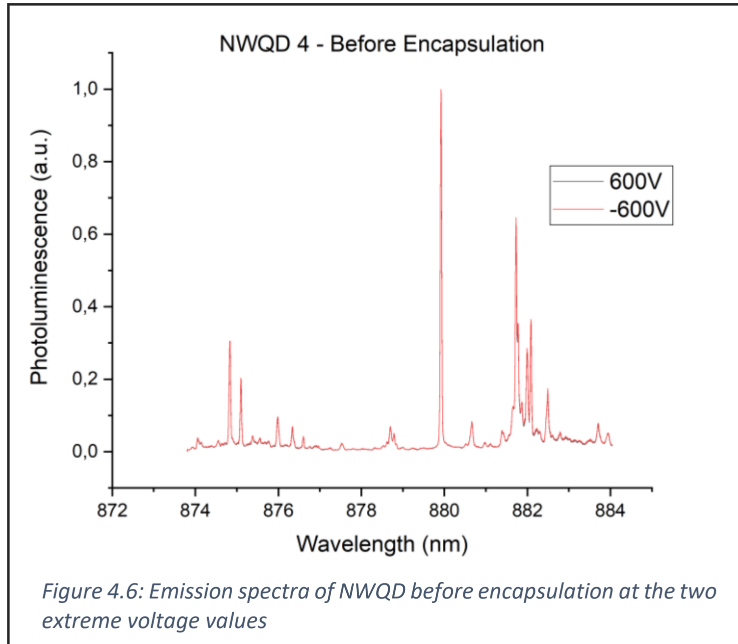



*Figure 4.6: Emission spectra of NWQD before encapsulation at the two extreme voltage values*

For comparison of the behavior after encapsulation of the previously-tuned and previously-not-tuned NWQDs, the emission spectra of NWQD 4 before and after encapsulation are given in figure 4.6 and figure 4.7, respectively. Above it was mentioned that the non-tuning of some of the NWQDs before encapsulation was attributed to no strain-transfer from the chip to the nanowires. This can be seen in figure 4.6 as the emission spectra recorded at the two extreme voltage values of 600V and -600V of NWQD 4 show no differences. This is an odd behavior (which was also observed with the other NWQDs that previously did not tune) suggesting that there was once again no strain-transfer towards these NWQDs. This lack of strain-transfer even after encapsulation is explained by the previously mentioned observation (most likely to the surface topology, check my previous comments) surface during the RIE of the waveguide layer. The integrated nanowires suggestively sit on a see of bumpy SiN which in turn screen the strain-transfer fully, so the deposited $SiO_2$ and $SiN_x$ anchoring

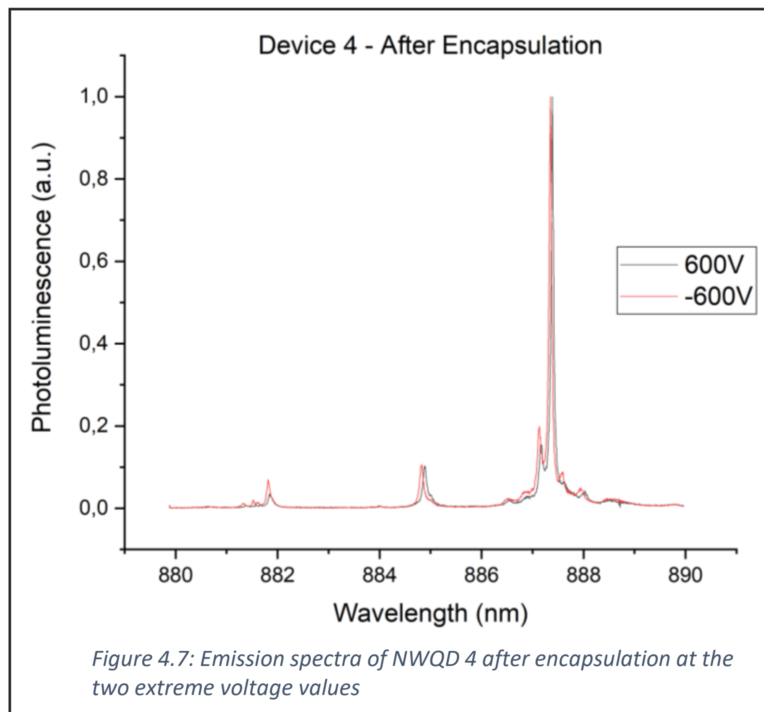



*Figure 4.7: Emission spectra of NWQD 4 after encapsulation at the two extreme voltage values*

bilayer in the vicinity of the NWQDs were themselves not exposed to strain, since the strain-transfer at these areas was blocked by the irrugular SiN surface.

Linewidth measurements of the NWQDs for prior to transferring to chip, after transfer and after encapsulation are given in table 4.3. It can be seen that the emission of these non-tuning NWQDs showed also no detrimental broadening after encapsulation (see figure 4.7 for NWQD 4) as opposed to the NWQDs that previously tuned. This gives a consistency in the interactions between the NWQDs and the $SiO_2$ chip surface or the deposited $SiN_x$-$SiO_2$-encapsulation layer. The only difference that is observed in the previously-not-tuned NWQDs is the displacement of the main emission peak, which is the manifestation of the static strain introduced by the encapsulation layer, meaning that these NWQDs were actually affected by this deposition.

*Table 4.3: The linewidth measurements and broadening of the NWQDs prior to and after encapsulation*

| NWQD | | Linewidth | | | Broadening by Encaps. |
|---|---|---|---|---|---|
| | | **As-Grown** | **Before Encapsulation** | **After Encapsulation** | |
| ***NWQD 2*** | | 37.1 μeV | 200 μeV | - | - |
| ***NWQD 3*** | 1st Peak | 30.8 μeV | 150 μeV | 670 μeV | x 4,46 |
| | 2nd Peak | | 220 μeV | 1020 μeV | x 4,63 |
| ***NWQD 4*** | | 38.7 μeV | 80 μeV | 90 μeV | x 1,12 |
| ***NWQD 5*** | | 31.4 μeV | 40 μeV | - | - |
| ***NWQD 7*** | Top | 23.6 μeV | 120 μeV | 700 μeV | x 5.83 |
| | Fiber | | 120 μeV | - | - |
| ***NWQD 8*** | | - | 60 μeV | - | - |
| ***NWQD 9*** | | 45.7 μeV | 70 μeV | 700 μeV | x 10 |

## 4.3 Strain-Tuning in NWQD Chip

In the second part of the project, a new piezo chip with ring-resonator structures with each coupling a through-port to a drop-port was fabricated. The $SiO_2$ cladding layer of this chip was reduced to 2.0 μm (with comparison to the 2.5 μm of the NWQD-chip), which was the lower boundary value for thickness obtained from the mode calculations (see section 4.1). Due to the random nature of the cleaving procedure that stems from the multiple-layered structure of the chips, only 5 circuits were cleaved nicely to have potential for successful butt-coupling. Other circuits were cut through at the ring-resonators, hence were not able to be be measured.

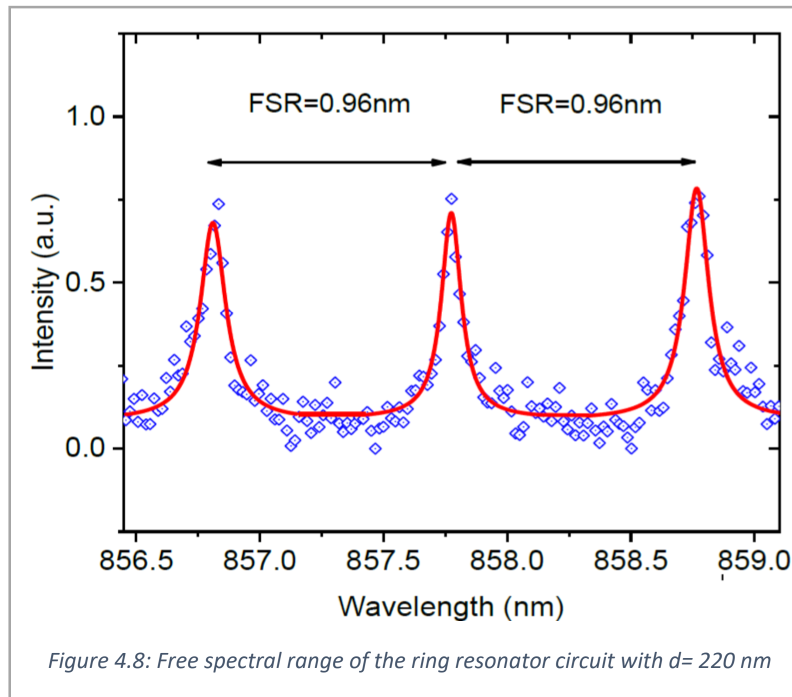



*Figure 4.8: Free spectral range of the ring resonator circuit with d= 220 nm*

In the following, transmission measurements were done by coupling light to the through-port of one of the circuits while simultaneously collecting from the corresponding drop-port. These measurements were executed by Zhao, P., The tranmission spectrum of the ring exhibit resonances with a free spectral range (FSR) of ~1 nm at ~850 nm wavelength (figure 4.8), the ring has a symmetric gap of 220nm for both drop and through waveguides. This value is in good agreement with the previous work of Elshaari, A., *et al.* (44), as in their case an FSR of 0,96 nm was obtained at wavelength values around 880 nm for similar chip design and compositional structure.

Having obtained resonance behaviour of the ring, the resonance condition can be controlled through piezoelectric tuning. Thepiezoelectric voltagewas ramped between -100 V and 30 V to tune the filtering wavelength (i.e. frequency). Notice that the voltage ramp range was smaller than that of the previous NWQD-chip, since the measurement setup of the RR-chip was in a room temperature setting, with no vacuum, which limits the applicable voltage range.

The ring-resonator filtering frequency was successfully tuned; it was red- and blue-shifted for increasing and decreasing voltage, respectively. Over the whole voltage range of ΔV= 130 V, a wavelength tuning of Δλ= 0.125 nm was achieved (figure 4.9). Furthermore, it was observed that the frequency of the ring-resonator showed a linear dependence on the applied voltage (see appendix: figure A.11).

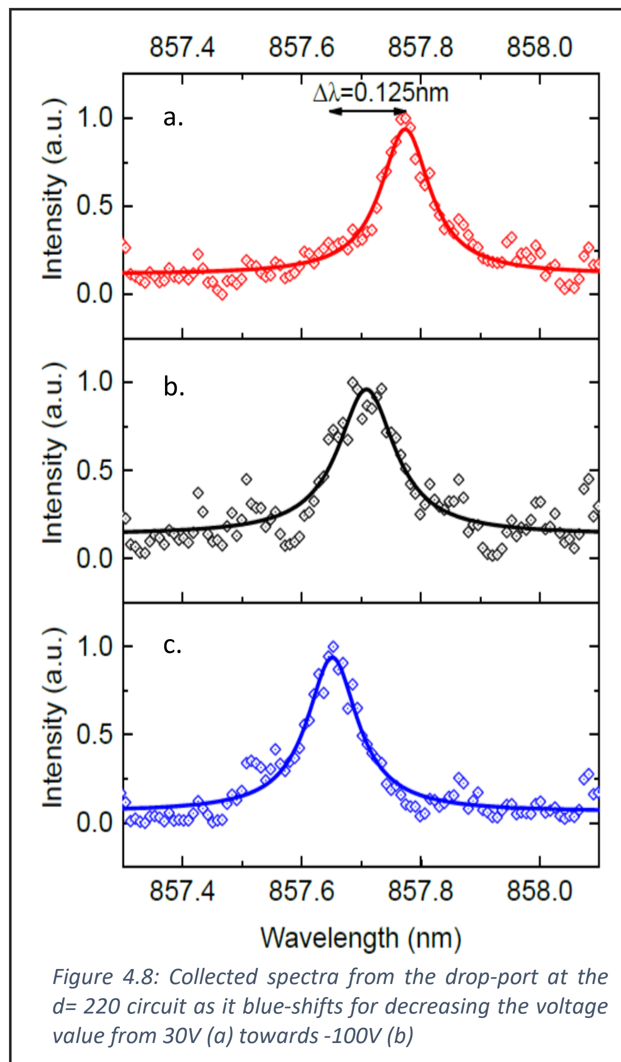



*Figure 4.8: Collected spectra from the drop-port at the d= 220 circuit as it blue-shifts for decreasing the voltage value from 30V (a) towards -100V (b)*

# V. Conclusions & Outlook

This project "Piezoelectric Tuning of Quantum Photonic Circuits" consisted of multiple goals and achievements. These can be divided into two major concepts. Firstly, quantum photonic circuits of reliable quantum sources and photonic components were fabricated and brought together to give successful coupling of emission from the sources to the waveguides. Within the hybrid approach, high emission quality III-V sources were integrated on to silicon-based photonic circuits, which overcomes the major problem of having the trade-off between these two components of generation and manipulation. Adding to the point of bringing these two material systems together, a third material type, namely the piezoelectric PMN-PT was also shown to be incorporated in to the system succefully. The PMN-PT chips underwent through major semiconductor fabrication methods such as EBL, PECVD and dry etching, and proved to work smoothly under the corresponding chamber parameters. In contrast to previous works where PMN-PT was also used as a bonded to preexisting substrates, our work shows that nano photonic circuits can be fabricated on top of PMN-PT directly. This material trio proves to be a promising system for the quantum optical tuning experiments of the future.

Correlating with the point mentioned about the compatibility of PMN-PT, the second major concept that was achieved within the project was the strain-tuning of both the quantum sources and passive optical components. The emission of the InP/InAsP NWQDs were tuned precisely and reversibly with applied voltage, although the strain had to be transferred through multiple layers, albeit large $SiO_2$ layer in the micrometer regime, in contrast to intermediate layers around few hundreds of nm for similar works in the literature. Future aspirations can be to bring the source tuning and tuning of manipulation components on to the same chip, or adding detection mechanisms to have a complete integrated circuit on-chip.

For the future of projects with same material compositions and fabrications, several improvement points can be implemented to further investigate the underlying problems that were encountered within this project, and to improve quality of the chip performance in general. Firstly, the post-fabrication processes can be implemented to enhance the quality of the layers. Annealing of the Au/Cr bimetallic layer, the amorphous $SiO_2$ layer or the $SiN_x$ layer can be implemented. The first two would aid to obtain a better-strain transfer to the above lying layers whereas increase the optical quality of the wavegudies.

The second potential improvement point is the improvement of the architecture of the chip. By introducing more sophisticated designs, multiple variables of a quantum source or passive components can be tuned independently. This can be implemented by introducing multiple "piezoelectric fingers" by means of micromachining or by means of patterning the electrical contact layers. In each case, independent tuning locations on the same chip can be fabricated which would yield higher integration density and lower footprint. Another crucial point where the architecture of the fabricated chip can be enhanced is the form of the PMN-PT substrate. In many works cited in this report, a monolithic PMN-PT substrate was used as the piezoelectric actuator. Thin film deposition of PMN-PT have been shown in previous works (48), which is a way to discard the rather exhaustive monolithic substrates. By growing epitaxial layers of PMN-PT (14, 28), the required voltage values for achieving the same strain (i.e. electric field) can be decreased substantially, but also much more sophisticated chip architecture and circuit designs can be implemented.

Another point that has to be investigated and evaluated is the adhesion of the nanowires to the integrated quantum chips. The III-V single photon sources, which have many advantages to be applied in quantum photonic circuits should be inspected in their straining behavior regarding their interactions with the substrate they are being integrated on to. The discoveries in this area will bring more knowledge about the emission properties of the sources and how the emission can be tuned more precisely. In this regard, atomic force microscopy measurements or acoustic microscopy measurements can be implemented to understand the adhesion

mechanisms of the structures precisely, whereas more conventional means such as SEM investigation can also prove to be enlightening.

As a final advancement point, the fabrication methods can be improved majorly. During the course of this work, especially the mechanical processing (i.e. polishing and cleaving) were the bottlenecks for the more rapid implementation of the fabrication. Several chips were lost to unsuccessful cleaving or shattering due to thermal shock, whereas the extensive procedure of polishing slowed down the process. If these two points can be improved to a level of semi-automated fabrication, rapid experimentation with systematic alteration of the parameters can be employed.

# VI. Appendices

## A.1 Fabrication

### VI.I.I Evaporation

Density, z-value and tooling factors for each material were input to the evaporator manually. A quartz crystal monitor within the evaporation chamber is simultaneously deposited during the evaporation. According to the input parameters, the thickness of the evaporated thin film is calculated from the deposition on to the quartz crystal and monitored. The tooling factor depends on the evaporated material and whether a rotating or stationary evaporation is conducted.

*Table A.1: Representative values for the parameters for evaporation of the bimetallic layer*

| Parameter | *Chromium* | *Gold* |
|---|---|---|
| **z-value** | 28,5 | - |
| **Tooling Factor** | 0,68 | 0,5 |
| **Current I** | 20mA | 80mA |
| **$P_{start}$** | 5 e-6 mbar | 0,7 e-6 mbar |
| **$P_{initial}$** | 3 e-6 mbar | 2,5 e-6 mbar |
| **Rate** | 0.1 nm/s | 0.18 nm/s |

### VI.I.II PECVD of $SiO_2$ and $SiN_x$

Plasma enhanced chemical vapor deposition (PECVD) was the applied deposition method for fabricating the waveguide core and cladding layers due its low thermal budget with operating temperatures around 250˚C - 300˚C, which is compatible with the low temperature demand of the In-containing single-photon sources.

The machinery used for PECVD was Plasmalab 80Plus Chamber A from Oxford Instruments. The chamber consisted of an Aluminum chuck of 20 cm chuck diameter. The RF frequency was 13.56 MHz.

For the PECVD of the fragile PMN-PT chips, which have low thermal shock resistance was gradually heated on hotplate to 300 ˚C with steps of 50 ˚C, before placing on to the hot chuck of the PECVD chamber.

### I. Bottom Oxide Cladding

The deposition recipe for the bottom cladding layer of $SiO_2$ is given in table A.2:

*Table A.2: Chamber parameters and values for the deposition of the bottom oxide cladding*

| Parameter | Value |
|---|---|
| **$SiH_4/N_2$ (8%)** | 710 sccm |
| **$N_2O$** | 425 sccm |
| **Pressure** | 800 mTorr |
| **Temperature** | 300 ˚C |
| **RF Power** | 24W |
| **Rate** | 65.5 nm/min |

### II. The Waveguide Core

The deposition recipe for the waveguide core layer of $SiN_x$ is given in table A.3:

*Table A.3: Chamber parameters and values for the deposition of the waveguide layer*

| Parameter | Value |
|---|---|
| **$SiH_4/N_2$ (8%)** | 800 sccm |
| **$NH_3$** | 16 sccm |
| **Pressure** | 650 mTorr |
| **Temperature** | 300 ˚C |
| **RF Power** | 24W |
| **Rate** | 16.3 nm/min |

Ellipsometry measurements were done to verify the refractive indices and the deposition rates. Around 850nm, the obtained values for n and k were 1.935 and 0 for $SiN_x$, respectively; for $SiO_2$, the obtained values for n and k were 1.46 and ~0.001, respectively.

### VI.I.III Resist Processing

Positive resist CSAR 6200 09 was spun at 4000 rpm for one minute, resulting in a thickness of 200 nm. Subsequent baking was done at 150˚C for one minute on hotplate. For development and removal of the resist, AR 600-546 (developer)- AR 600-60 (stopper) duo and AR-600-571 were used, respectively. The development took one minute of dipping for each process liquids whereas for removal, dipping of more than 24 hours was implemented.

### VI.I.IV Reactive Ion Etching

The dry etching of the piezo chips was implemented with a reactive ion etcher. The etch recipe was based on Fluoroform and Argon, which is given in table A.4.

*Table A.4: Dry etching parameters for the etching of the $SiN_x$ layer*

| Parameter | Value |
|---|---|
| **$CHF_3$** | 20 sccm |
| **Ar** | 10 sccm |
| **Pressure** | 7 mTorr |
| **RF Power** | 50 W |

### VI.I.V Oxygen Plasma Ashing

The surfaces of the chips were cleaned by applying oxygen plasma cleaning to the piezo chip prior to the evaporation and as-deposited with $SiO_2$ and $SiN_x$ prior to resist spinning.

*Table A.5: $O_2$-plasma ashing parameters and values*

| Parameter | Value |
|---|---|
| **$O_2$** | 20 sccm |
| **DC Bias** | 385 V |
| **Pressure** | 5,7 mTorr |
| **RF Power** | 49 W |
| **Water Temp.** | 20 ˚C |
| **Time** | 3 min |

### VI.I.VI Etch Rate Measurements

Etch rate measurements for the etching of the $SiN_x$ layer were conducted. Initially a photoresist (S1818) blob was put on top of dummy samples. The resist blob was then baked and etched with the Ar/$CHF_3$ based RIE. Finally, the profiles extending from the the etched area towards the protected-by-the-resist-area were measured by the surface profiler KLA Tencor P-15.

Throughout the course of the project, three different etch rate measurements were done separate in time: Initially, the etch rate for $SiN_x$ was found to be 22.5nm/min. A second etch rate measurement gave for $SiN_x$ and CSAR etch rates of 25nm/min and 9.5 nm/min, respectively. A final etch rate measurement for $SiN_x$ gave a value of 19.3 nm/min.

The fluctuations in the etch rate measurements were attributed to the fluctuations in the results measured by the surface profilometer, of which the leveling is done by the choice of the operator for lines that are sufficiently flat and furthermore, the measurement is not necessarily verified to extend fully throughout the etched profiles.

## A.2 Emission Spectra

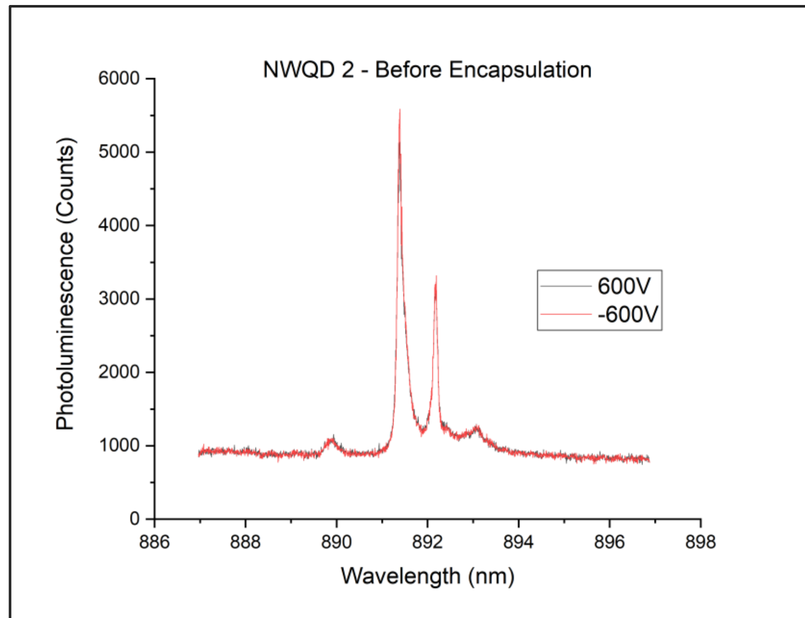



*Figure A.1: Emission spectra of NWQD before encapsulation at the two extreme voltage values*

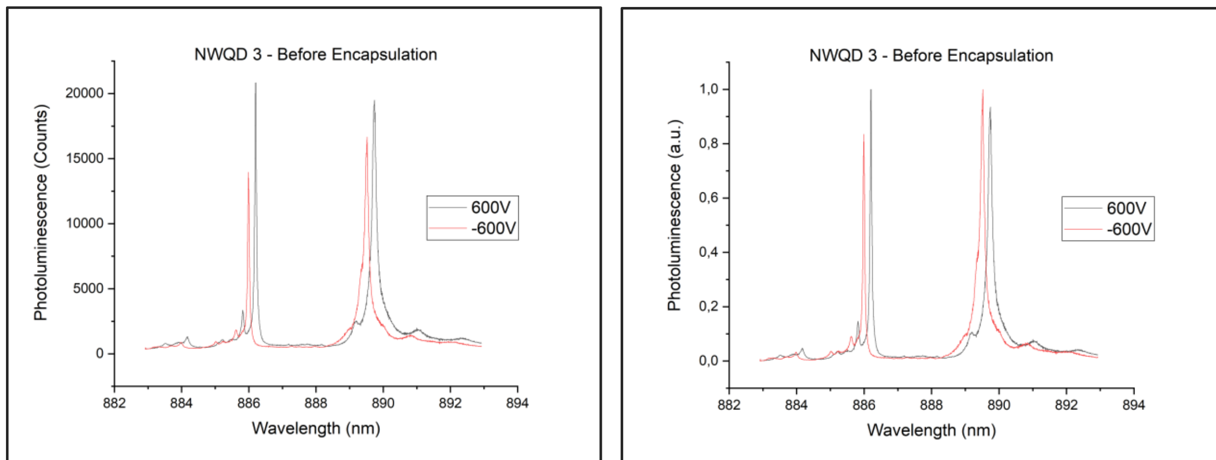



*Figure A.2: Emission spectra of NWQD 3 before encapsulation at the two extreme voltage values with actual photon counts (left) and normalized photon counts (right)*

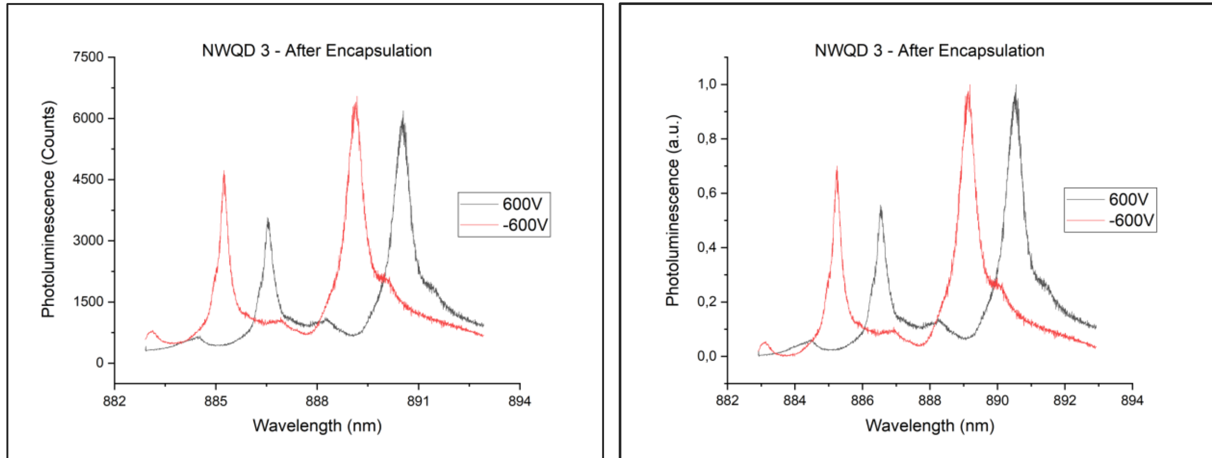



*Figure A.3: Emission spectra of NWQD 3 after encapsulation at the two extreme voltage values with actual photon counts (left) and normalized photon counts (right)*

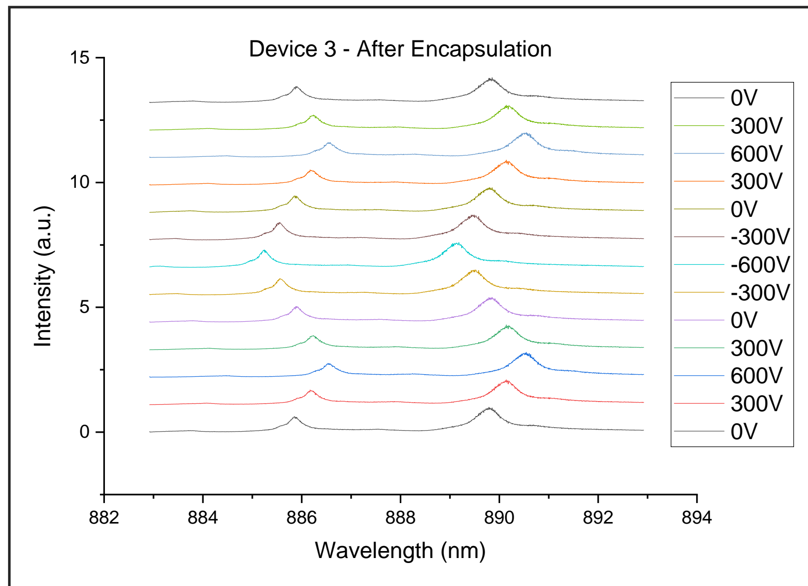



*Figure A.4: Stepwise stacking of the NWQD 3 emission spectra after encapsulation at various voltage values*

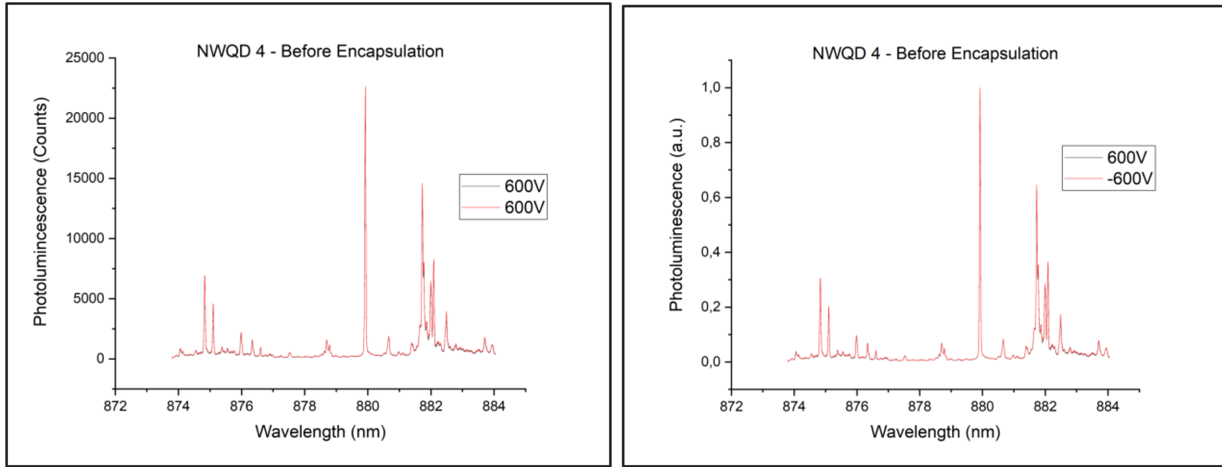



*Figure A.5: Emission spectra of NWQD 4 before encapsulation at the two extreme voltage values with actual photon counts (left) and normalized photon counts (right)*

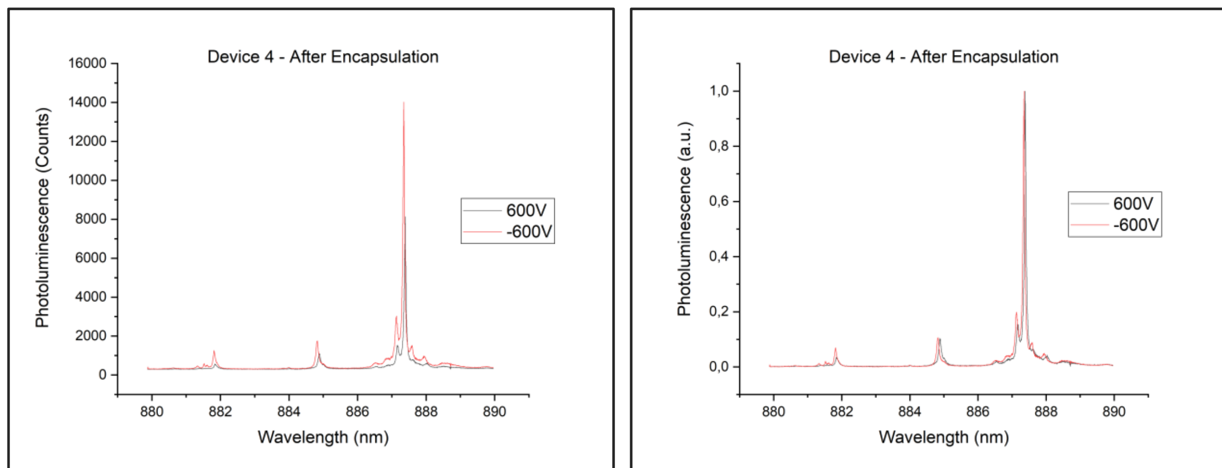



*Figure A.6: Emission spectra of NWQD 4 after encapsulation at the two extreme voltage values with actual photon counts (left) and normalized photon counts (right)*

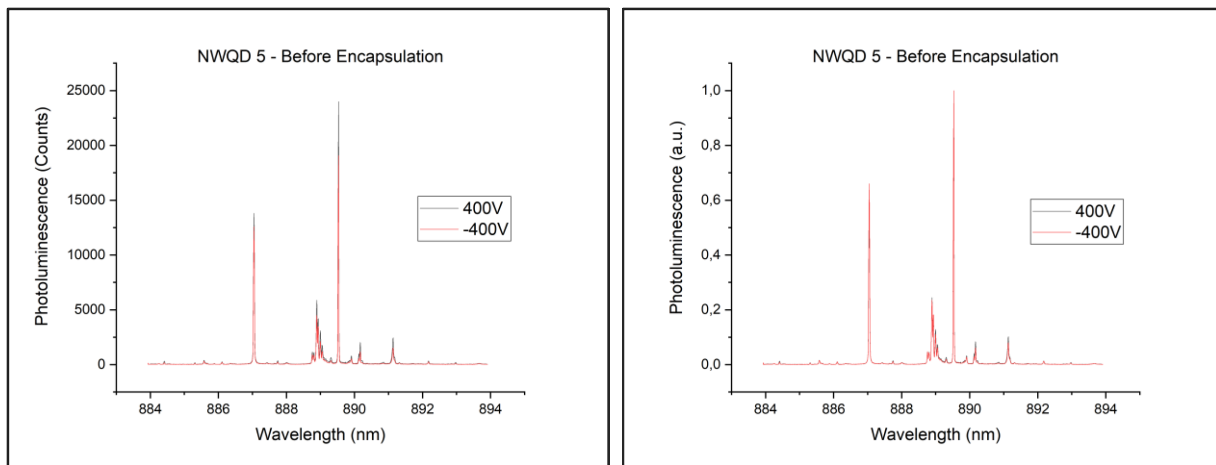



*Figure A.7: Emission spectra of NWQD 5 before encapsulation at the two extreme voltage values with actual photon counts (left) and normalized photon counts (right)*

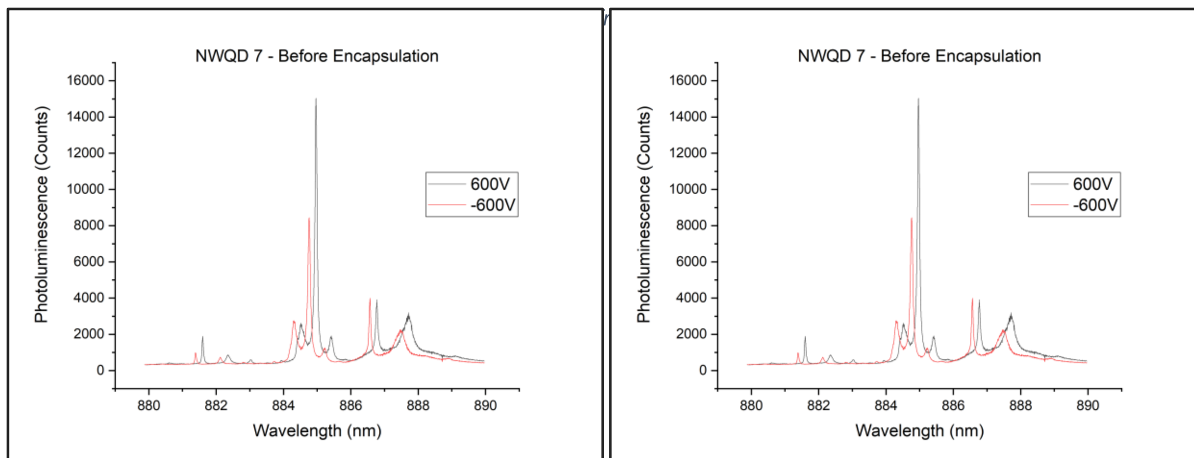



*Figure A.8: Emission spectra of NWQD 7 before encapsulation at the two extreme voltage values with actual photon counts (left) and normalized photon counts (right)*

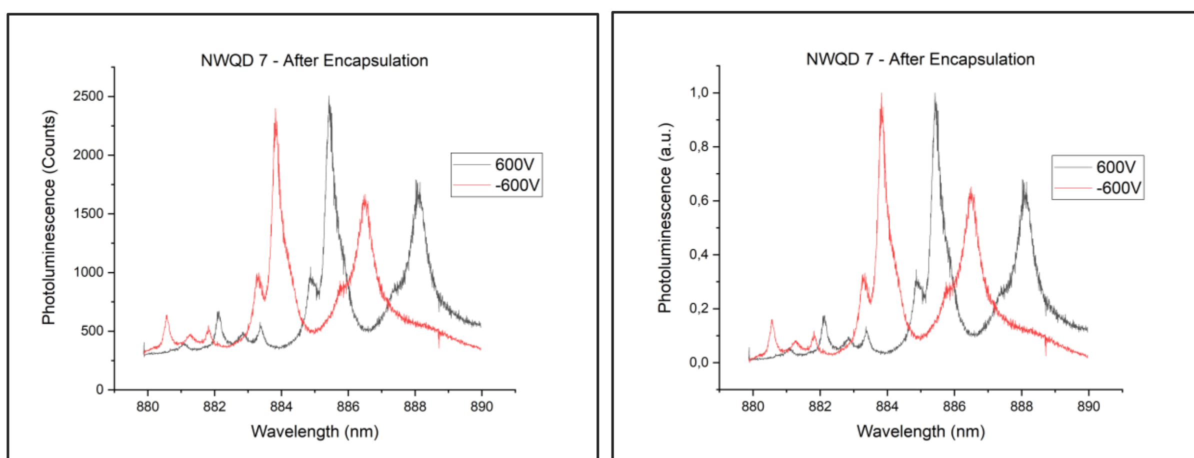



*Figure A.9: Emission spectra of NWQD 7 after encapsulation at the two extreme voltage values with actual photon counts (left) and normalized photon counts (right)*

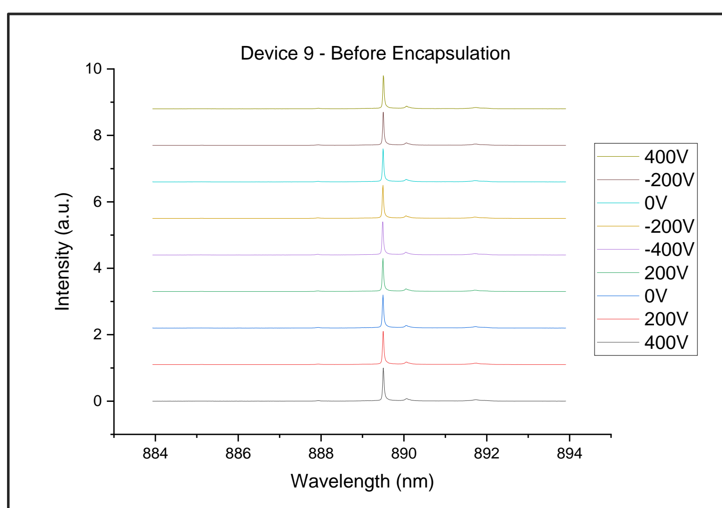



*Figure A.10: Stepwise stacking of the emission spectra of NWQD 9 before encapsulation at various voltage values*

## A.3 Ring-Resonator Filtering

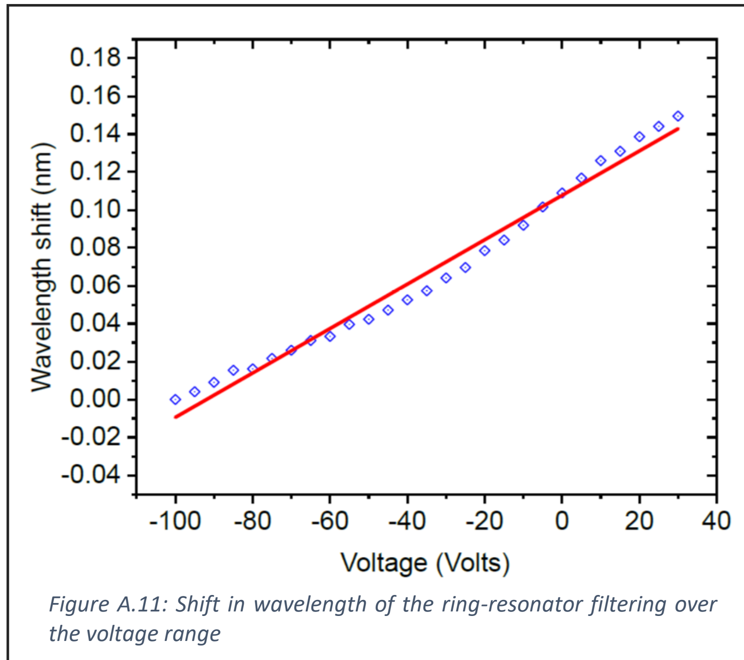



*Figure A.11: Shift in wavelength of the ring-resonator filtering over the voltage range*

# VII. Declaration of Originality

Eidgenössische Technische Hochschule Zürich
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The signed declaration of originality is a component of every semester paper, Bachelor's thesis, Master's thesis and any other degree paper undertaken during the course of studies, including the respective electronic versions.

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