A Very Low Loss 220–325 GHz Silicon Micromachined Waveguide Technology

Bernhard Beuerle, James Campion, Umer Shah and Joachim Oberhammer

***Abstract*—This paper reports for the first time on a very low loss silicon micromachined waveguide technology, implemented for the frequency band of 220 – 325 GHz. The waveguide is realized by utilizing a double H-plane split in a three-wafer stack. This ensures very low surface roughness, in particular on the top and bottom surfaces of the waveguide, without the use of any surface roughness reduction processing steps. This is superior to previous micromachined waveguide concepts, including E-plane and single H-plane split waveguides. The measured average surface roughness is 2.14 nm for the top/bottom of the waveguide, and 163.13 nm for the waveguide sidewalls. The measured insertion loss per unit length is 0.02 – 0.07 dB/mm for 220 – 325 GHz, with a gold layer thickness of 1 µm on the top/bottom and 0.3 µm on the sidewalls. This represents, in this frequency band, the lowest loss for any silicon micromachined waveguide published to date and is of the same order as the best metal waveguides.**

***Index Terms*—RF MEMS, micromachined waveguide, rectangular waveguide, submillimeter-wave, terahertz**

I. Introduction

The low insertion loss of rectangular waveguides, in particular when compared to planar transmission lines, makes them the ideal transmission medium for millimeter and submillimeter wave frequencies. Waveguide insertion loss depends on the surface roughness of the waveguide walls and the type and thickness of surface metallization. For split-block waveguides, the split geometry and joining technique also influence the insertion loss. CNC milling of metal split-blocks is the most established method to fabricate rectangular waveguides. The resulting milled surfaces have too high nonuniformity to allow for proper bonding of the split blocks. Low loss metal waveguides are therefore almost exclusively implemented in an E-plane split design, as this provides the lowest loss if the split cannot be ideally bonded together. Moreover, this design allows for relatively straightforward coupling to active devices using E-field probes [1]. An insertion loss of 0.20 – 0.25 dB/mm has been reported for aluminium split-block waveguides [2] in the WR-3.4 band, whereas a non-commercial gold electroplated split-block WR-3.7 waveguide achieved an insertion loss of 0.015 dB/mm [3]. By comparison, an insertion loss of 1.6 dB/mm for co-planar waveguides (CPW) on GaAs and 2.5 dB/mm for coplanar striplines on sapphire at 300 GHz have been reported [4]. Microstrip lines using BCB as dielectric achieve an insertion loss of 0.88 dB/mm at 330 GHz [5].

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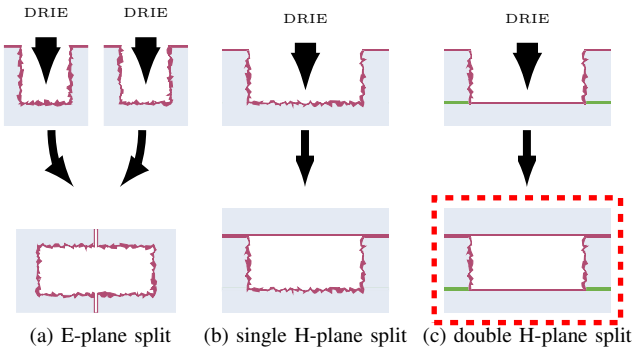

Fig. 1. Micromachined waveguide surface roughness: (a) E-plane split, waveguide halves DRIE along the waveguide width and subsequently joined together [6], [7]; (b) single H-plane split DRIE along the waveguide height [8], [6], [9]; and (c) double H-plane split DRIE along the waveguide height, as proposed in this paper.

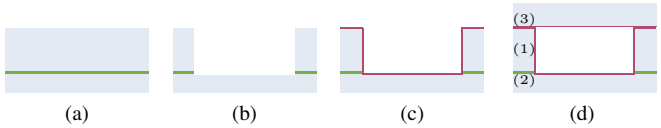

Fig. 2. Fabrication process: (a) bare SOI wafer; (b) waveguide structure after DRIE silicon etch and subsequent removal of the buried oxide layer; and (c) metallization using sputtering and (d) final waveguide after thermo-compression bonding.

Micromachining offers a number of advantages for the fabrication of waveguide components, which become particularly beneficial when approaching terahertz frequencies. The ability to implement small feature sizes with accurate tolerances allows for the integration of components of complex geometries [10]. These accurate tolerances, when combined with volume batch processing, result in high product uniformity and low fabrication costs. Micromachining also makes it possible to achieve low surface roughness and near ideal metallic bonding, reducing the insertion loss of a waveguide and allowing for the use of H-plane split designs. H-plane split waveguides are less sensitive to misalignment than E-plane split waveguides, simplifying waveguide assembly.

Insertion loss as low as 0.03 dB/mm has been shown for WR-3.4 micromachined waveguides using thick SU-8, either directly metallized or used as molds for electroplating [11]. However, it is difficult to apply SU-8 uniformly and stabilize it. Therefore, deep reactive-ion etching (DRIE) of trenches in silicon with subsequent metallization is the most common fabrication technique for micromachined waveguides. For

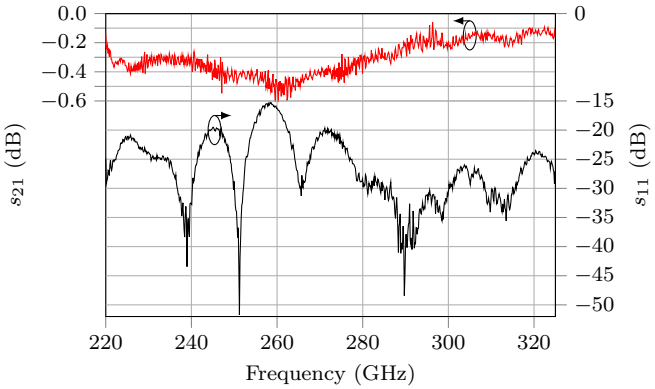

Fig. 3. Measured transmission and reflection coefficient of a waveguide line with a length of $l = 7.1\,\mathrm{mm}$.

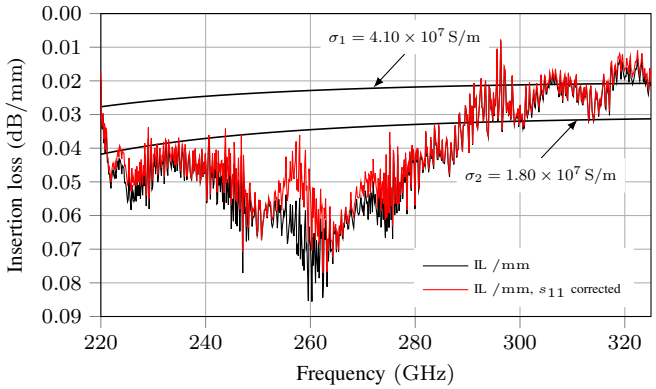

Fig. 4. Measured insertion loss and s_{11} corrected insertion loss per unit length of a waveguide line with a length of $l = 7.1\,\mathrm{mm}$, compared to the theoretical waveguide losses for a gold plated waveguide with an ideal conductivity of $\sigma_1 = 4.1 \times 10^7\,\mathrm{S/m}$ and a reduced conductivity of $\sigma_2 = 1.8 \times 10^7\,\mathrm{S/m}$, which provides a close fit to the measured data.

500 – 750 GHz, the reported insertion loss for E-plane and H-plane split micromachined waveguides is 0.08 – 0.12 dB/mm and 0.06 – 0.12 dB/mm, respectively [6]. In [7] an additional oxidation and etch-back step was added to decrease the surface roughness, reducing the insertion loss for an E-plane split waveguide to 0.05 – 0.07 dB/mm.

The DRIE process for an E-plane split waveguide results in high surface roughness on all four waveguide walls. The roughness of the sidewalls is particularly high since this is the bottom surface during DRIE (Fig. 1a). Single H-plane split waveguides are fabricated by etching the waveguide recess into a silicon wafer and bonding a cap wafer on top (Fig. 1b). Here, the cap wafer is not etched and therefore has a surface roughness of a few nanometers, but all three other walls are etched and contribute to the insertion loss.

In this paper we present, for the first time, a silicon micromachined WR-3.4 waveguide utilizing a double H-plane split (Fig. 1c). The proposed technique drastically reduces the overall surface roughness, resulting in the lowest insertion loss reported to date for any silicon micromachined waveguide in this frequency band.

II. Design and Fabrication

The implemented waveguide has the standard WR-3.4 waveguide width of 864 µm but a reduced height of 275 µm. The waveguide technology consists of a metallized three-wafer stack with two H-plane splits: (1) the handle layer of a silicon-on-insulator (SOI) wafer into which the waveguide channel is etched; (2) its device layer acting as the bottom of the waveguide; and (3) a silicon cap wafer as the top of the waveguide. The height of the waveguide can be controlled down to micrometer tolerances, since it is defined by the thickness of the SOI handle layer. Unlike for a single H-plane split, both the bottom and the top surface of the waveguide in this design have a surface roughness of a few nanometers, even after metallization. Furthermore, the surface roughness of the etched sidewalls is significantly lower than that of an E-plane split micromachined waveguide as the etch depth is significantly smaller (36% in our design).

The main steps of the fabrication process are illustrated in Fig. 2. The handle layer of the SOI wafer is etched using deep reactive ion etching with a three-step Bosch process (Fig. 2b). The SOI buried oxide (BOX) layer acts as an etch stop and is subsequently removed by plasma etching. Both the SOI wafer and the silicon cap wafer are then metallized with 1.0 µm of gold (waveguide top and bottom) using sputter deposition (Fig. 2c), resulting in a thickness of 0.3 µm on the waveguide sidewalls. Finally, the individual chips are bonded using thermo-compression bonding at 200 °C (Fig. 2d).

III. Characterization

To measure the scattering parameters and determine the insertion loss per unit length of the waveguide technology, a waveguide line with a length of 7.1 mm has been fabricated. This waveguide is characterized using a Rohde & Schwarz ZVA 24 Vector Network Analyzer with two Rohde & Schwarz ZC330 TxRx extension heads over the frequency band of 220 – 325 GHz. A micromachined on-chip Thru-Reflect-Line calibration kit is used to move the reference planes to the waveguide ports. The measured transmission and reflection coefficients for the waveguide line are shown in Fig. 3.

The measured insertion loss of the waveguide line is better than 0.6 dB across the band. Except for a single 15 dB peak, the return loss is better than 20 dB. The measured insertion loss per unit length is shown in Fig. 4, with and without correction by the measured return loss. It is between 0.02 – 0.07 dB/mm, averaging 0.039 dB/mm. The theoretical waveguide loss per unit length for a WR-3.4 waveguide with an ideal conductivity of $\sigma_1 = 4.1 \times 10^7$ S/m is plotted as reference. Assuming a conductivity of $\sigma_2 = 1.8 \times 10^7$ S/m the theoretical loss gives a close fit to the measured data.

As a reference, a commercially available gold-metallized E-plane split waveguide has been characterized with the same setup, with a measured insertion loss of 0.02 – 0.025 dB/mm in the frequency band of 280 – 330 GHz, which is of the order of values reported in the literature (Table I).

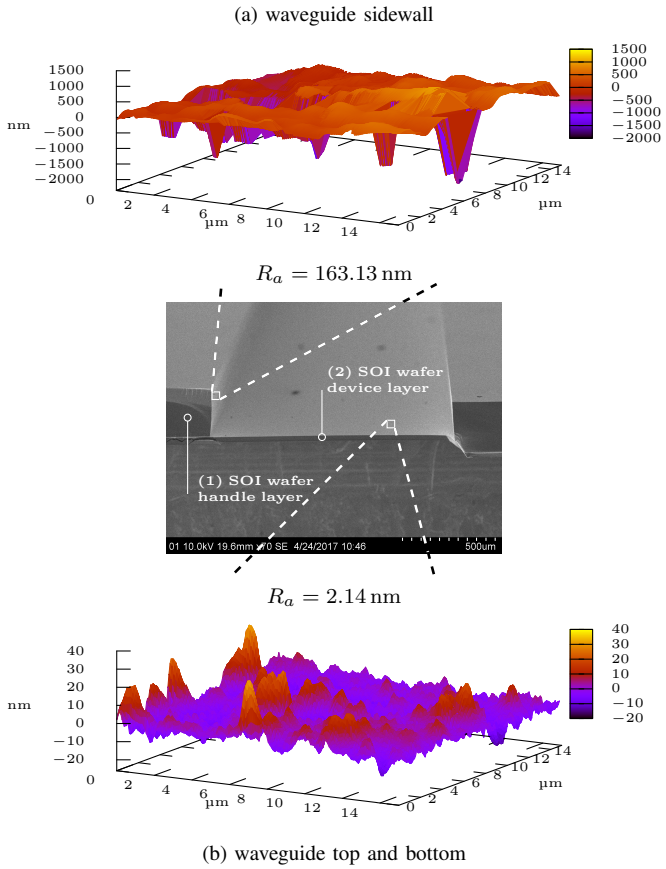

Fig. 5. Cross-sectional SEM image, unbonded waveguide after gold deposition: (1) SOI wafer handle layer (waveguide sidewalls); and (2) SOI wafer device layer (waveguide top and bottom). The measured average surface roughness (RMS) of the waveguide walls is (a) $R_a = 163.13\,\text{nm}$ for the waveguide sidewall; and (b) $R_a = 2.14\,\text{nm}$ for the waveguide bottom.

Assuming the same surface roughness for a WR-1.5 waveguide implemented in this technology without an additional oxidation step, the loss per unit length for the waveguide with conductivity $\sigma_2 = 1.8 \times 10^7\,\text{S/m}$ is expected to be between 0.07 dB/mm and 0.10 dB/mm for the frequency band of 500 – 750 GHz.

Fig. 5 shows a scanning electron microscope (SEM) image of a cross-section of the waveguide after gold deposition. The surface roughness was measured with an optical profilometer over a $15\,\mu\text{m} \times 15\,\mu\text{m}$ area. The measured average surface roughness (RMS) is 2.14 nm for the waveguide top/bottom (Fig. 5a) and 163.13 nm for the waveguide sidewalls (Fig. 5b).

The low insertion loss of the waveguide was achieved without an additional oxidation step (as was used in [7]) and is attributed to its design (Section II). The state of the art performance for different fabrication techniques is summarized in Table I.

IV. Conclusion

A double H-plane split silicon micromachined waveguide technology has been presented for the first time and implemented for the frequency band of 220 – 325 GHz. The measured insertion loss of the waveguide is 0.02 – 0.07 dB/mm over the whole frequency band, with an average of 0.039 dB/mm, without the use of additional surface roughness reduction methods. This represents, to the best of our knowledge, the lowest loss silicon micromachined waveguide in this frequency band to date.

Table I
State of the Art Waveguide Technologies

Reference	Technology	Split	h (nm)	f (GHz)	Loss (dB/mm)
[2]	CNC, Al	E	–	325 – 360	0.20 – 0.25
[12]	CNC, Au plated	E	–	220 – 330	0.03 – 0.06
[3]	CNC, Au plated	E	–	210 – 280	0.014 – 0.018
[11]	SU-8	E	–	220 – 325	0.03 – 0.05
[8]	DRIE	H	75 [1]	500 – 700	0.10 – 0.20
[6]	DRIE	E	110 [2]	500 – 750	0.08 – 0.12
[6]	DRIE	H	20 / 110 [3]	500 – 750	0.06 – 0.12
[7]	DRIE, ox. step	E	43 [4]	500 – 750	0.05 – 0.07
This work	DRIE double–	H	2 / 160 [5]	220 – 325	0.02 – 0.07

[1] measured sidewall scallops
[2] RMS
[3] RMS top / bottom and sidewall roughness
[4] RMS, 199 nm before surface roughness reducing oxidation step
[5] RMS top and bottom / sidewall roughness, without any oxidation step

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