VHDL-program with Quartus



Choose the right program version from the school's start menu :

```
Altera 13.0.1.232 Web edition\
Quartus II Web Edition 13.0.1.232\
Quartus II 13.0spl (32bit)
```



Start Quartus. You need no license and you do not need not buy anything.

If not be directly offered to start **New Project Wizard**, You may also select this option from the **File** menu.



Introduction

Clic on Next.



Project Name and Directory

In school, the entire project must be on your $H:\, eg. H:\MAXwork$ (at home on $C:\, eg. C:\MAXwork$)

Name: codelock

Top-Level Entity: codelock

(Note! the name codelock must "match" the name you later on specify as entity in your VHDL-file)

Proceed with Next.

Ht./MADIavark		144
What is the name of this project?		
codelock.		112
What is the name of the top-level design entity for t	his project? This name is case sensitive and must exactly match the entity name in the design file.	
codelock.		-01
Use Existing Project Settings		

Add files

We have no files to add to the project, so we proceed with Next.



Family and Device Settings

Here we specify which chip we intend to use during the lab.

Family: MAX3000A Available devices: EPM3032ALC44-10

Proceed with Next.

Device Family			Show in 'Asail	able devices' list	
Family: MAX3000	A.		Package:	Anv	-
Denirer Al			1	pro l	
Passas In			Pin count:	Any	-
Target device			Speed grader	Any	 *
C. Andre denistra co	lected by the filter		F show adv	whiced devices	
Auto device se	recised by the Pieter		-		
 Specific device 	selected in Wvallable	e devices' list	E HardCopy	compatible only	
C Other: n/a					
and a state of the second					
vallable devices:					
Name	Core Voltage	Macrocells			-
Name PM3032ALC44-4	Core Voltage	Macrocells 32			1
Vallable devices: Name PM3032ALC44-4 PM3032ALC44-7	Core Voltage 3.3V 3.3V	Macrocells 32 32			1
Vallable devices: Name DM3032ALC44-4 DM3032ALC44-7 DM3032ALC44-10	Core Voltage 3.3V 3.3V 3.37	Macrocells 32 33 33 33 33 34 35			1
Valiable devices: Name 94/3032ALC44-4 99/3032ALC44-7 97/3032ALC44-7 99/3032ATC44-7 99/3032ATC44-7	Core Voltage 3.3V 3.3V 3.3V 3.3V 3.3V	Macrocells 32 32 32 32 32 32 32 32 32 32 32 32 32			1
Name PM3032ALC44-4 PM3032ALC44-4 PM3032ALC44-7 PM3032ALC44-4 PM3032ALC44-4 PM3032ALC44-7	Core Voltage 3.3V 3.3V 3.3V 3.3V 3.3V 3.3V 3.3V 3.3	Macrocells 22 32 32 32 32 32 32 32 32 3			1
Vallable devices: Name PM3032ALC44-4 PM3032ALC44-7 PM3032ALC44-7 PM3032ALC44-7 PM3032ALC44-4 PM3032ALC44-10 PM3032ALC44-10	Core Voltage 3.37 3.37 3.37 3.37 3.37 3.37 3.37 3.3	Macrocells 32 32 32 32 32 32 32 32 32 32 32 32 32			1
Vallable devices: Name PM3032ALC44-4 PM3032ALC44-7 PM3032ATC44-4 PM3032ATC44-4 PM3032ATC44-7 PM3032ATC44-10 PM3032ATL44-10	Core Voltage 3.37 3.37 3.37 3.37 3.37 3.37 3.37 3.3	Macrocells 32 34 35 36 37 38 39 32 32 32 32 33 34 35 36 37 38 39 39 39 39 39 39 39 39 39 39 39 39			1
Valiable devices: Name EM3032ALC44-4 EM3032ALC44-7 EM3032ATC44-4 PM3032ATC44-7 PM3032ATC44-10 PM3032ATC44-10 PM3032ATC44-10 PM3032ATC44-2 EM304ALC44-4 Companies device	Core Voltage 3.37 3.37 3.37 3.37 3.37 3.37 3.37 3.3	Macrocells 32 32 32 32 32 32 32 32 32 32 32 32 34 35 36 37 38 39 32 32 34			1
Name Name EM43032ALC44-1 EM43032ALC44-7 EM43032ALC44-10 EM43032ALC44-10 EM43032ALC44-10 EM44-10 EM44-10 EM40032ALC44-4 Comparison device	Core Voltage 3.37 3.37 3.37 3.37 3.37 3.37 3.37 3.3	Macrocells 32 32 32 32 32 32 32 32 32 32 32 32 32			
Natible devices: Native EM5032342C44-4 EM5032342C44-7 EM503242C44-7 EM5032ATC44-4 EM5032ATC44-10 EM5032	Core Voltage 3.37 3.37 3.37 3.37 3.37 3.37 3.37 3.3	Macrocells 32 32 32 32 32 32 32 32 32 32 32 32 34			

EDA tools setting

Here you can create context with software tools from other vendors. We will simulate with the ModelSim program but that we need not enter. Proceed with **Next**.

EDA tools:				
Tool Type	Tool Name	Format(s)	188327	Run Tool Automatically
Design Entry/Synthesis	<tione></tione>	dionep	2000 7	Run this tool automatically to synthesize the current design
Simulation	<nane></nane>	diane>	100 F	Run gate-level simulation automatically after compilation
Timing Analysis	<none></none>	dipteb	22233 <u>¥</u>	Run this tool automatically after compliation
Formal Verification	dimes <u></u>]		
Board-Level	Timing	<none></none>		
	Symbol	<none></none>		
	Signal Integrity	<none></none>		
	Boundary Scan	<none></none>		

Summary.

Here you can see a summary of your selections, exit the "Wizard" with Finish.

New Project Wizard	
Summary [page 5 of 5]	
when you dick Pinish, the project will be created with the	following settings:
Project directory:	H: MAXImork
Project name:	codelock:
Top-level design entity:	codeloci:
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3032ALC44-10
EDA tools:	
Design entry/synthesis:	<hl><l< td=""></l<></hl>
Simulation:	chlone>(chlone>)
Timing analysis:	<pre>dlane>(dlane>)</pre>
Operating conditions:	
Core voltage:	3.3V
Junction benperature range:	0-85 °C
	<back arct=""> Pinish Cancel Help</back>

The project has been created



VHDL-code



Create a blank file for VHDL-code. File, New, VHDL File.

Copy the Template lockmall.vhd and paste it in Quartus text editor.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
entity codelock is
   port( clk:
                   in std_logic;
           к:
                   in std_logic_vector(1 to 3);
                   in std_logic_vector(1 to 4);
           R:
                   out std_logic_vector(4 downto 0);
           q:
           UNLOCK: out std_logic );
end codelock;
architecture behavior of codelock is
subtype state_type is integer range 0 to 31;
signal state, nextstate: state_type;
begin
nextstate_decoder: -- next state decoding part
process(state, K, R)
 begin
   case state is
      when 0 \Rightarrow if (K = "001" and R = "0001")
                                                   then nextstate <= 1;
                 else nextstate <= 0;</pre>
                 end if;
      when 1 => if (K = "001" and R = "0001") then nextstate <= 1;
                 elsif (K = "000" and R = "0000") then nextstate <= 2;</pre>
                 else nextstate <= 0;</pre>
                 end if;
      when 2 to 30 => nextstate <= state + 1;
      when 31 => nextstate <= 0;</pre>
   end case;
end process;
debug_output: -- display the state
q <= conv_std_logic_vector(state,5);</pre>
output_decoder: -- output decoder part
process(state)
begin
  case state is
     when 0 to 1 => UNLOCK <= '0';
     when 2 to 31 => UNLOCK <= '1';
  end case;
end process;
state_register: -- the state register part (the flipflops)
process(clk)
begin
  if rising_edge(clk) then
     state <= nextstate;</pre>
  end if;
end process;
end behavior;
```

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				Add life to current pro	ieck 👘		

Note that entity in the VHDL-file must "match" the project Top Level Entity!

Save the file: **File**, **Save As** and as VHDL-file. The name could be codelock.vhd (or another).

Add File to current project shall be checked!

Analysis and Synthesis

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System Processing Extra Infr Message:	Info / Warning / Critical W	arning / Error	Start VQM Writer Start Equation Writer (Post-synthesis) Start Equation Writer (Post-Stiting)	

When you have new code, it is unnecessary to run the entire tool chain - chances are that there are errors along the way ...

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From the start you only do Analysis & Synthesis.

Start Compilation

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Start Compilation runs the full tool chain.

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Message: 0 of 98 1	sations				Locate
				100%	00:00:09 //

The 3 warnings (moore with other program versions) are about "software tools" that are missing in our program version but we don't need them.

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