KTH Informations- och kommunikationsteknik

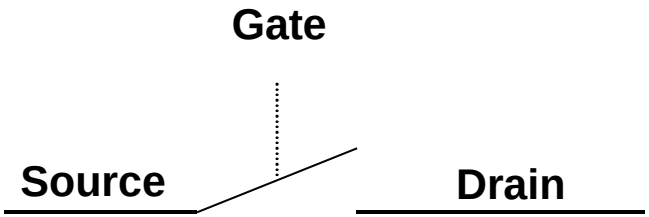
IE1204 Digital Design:

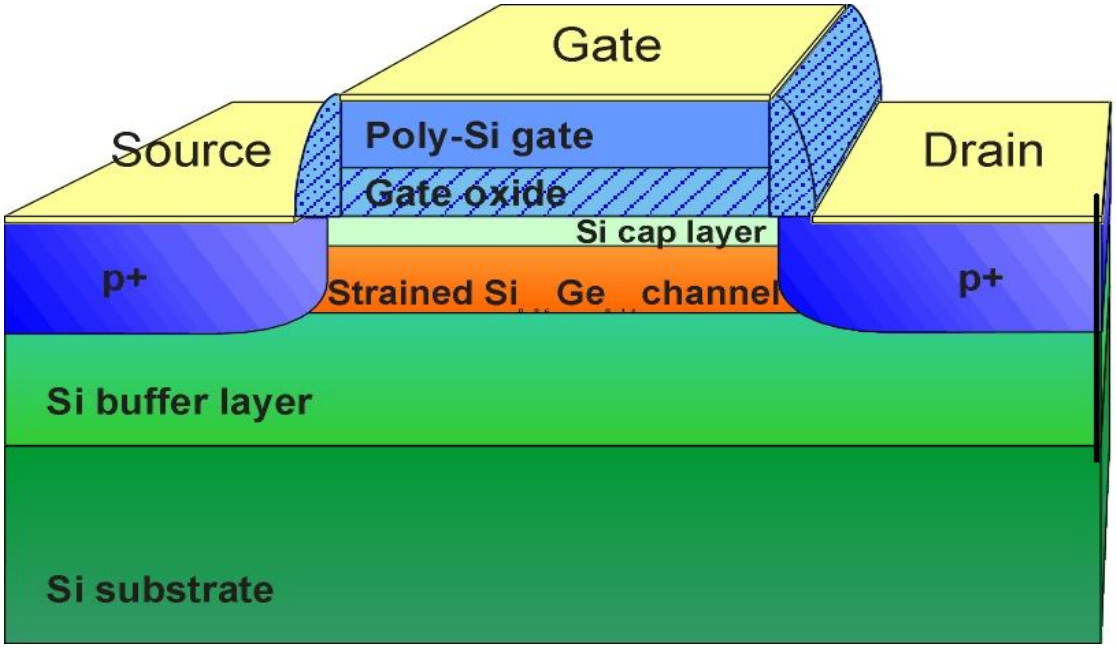
L3: CMOS circuits, Implementation Technologies

Masoumeh (Azin) Ebrahimi (masebr@kth.se)

Elena Dubrova(dubrova@kth.se)
KTH / ICT / ES

Transistor - a switch with no moving parts



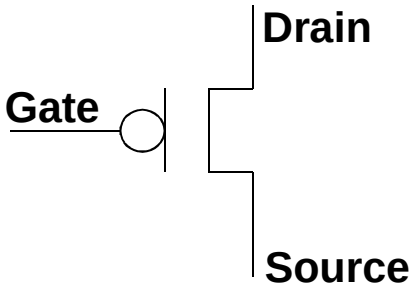


Schematic diagram of the SiGe transistor (KTH)

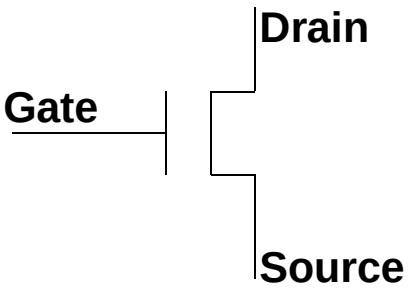
Why CMOS?

- CMOS transistors are easy to manufacture
- CMOS transistors are made from ordinary sand => cheap raw materials
- A transistor is easy to get to work as a switch

PMOS and NMOS



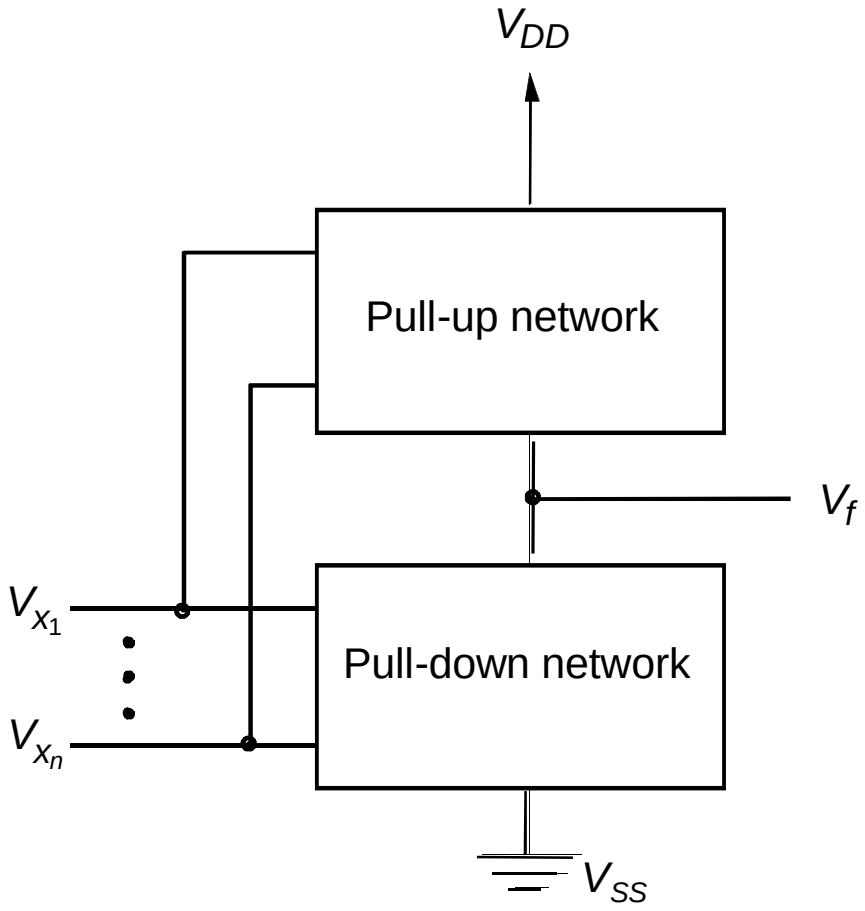
PMOS



NMOS

- A PMOS transistor (p-channel MOS) is conducting (switch is closed) if gate voltage (V_{GS}) is close to V_{SS}.
- An NMOS (n-channel) is conducting (switch is closed) if gate voltage (V_{GS}) is close to V_{DD}.

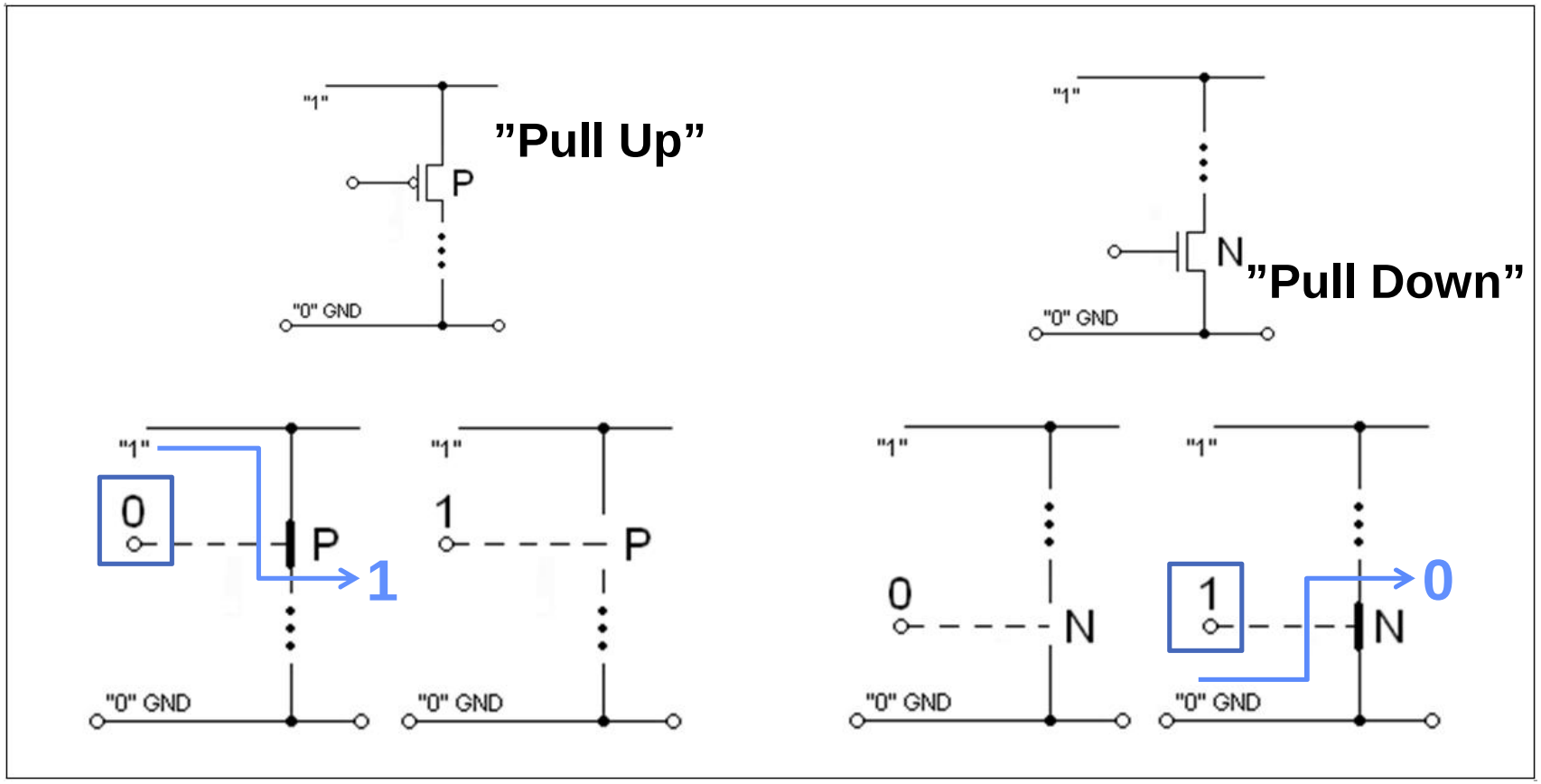
The structure of a CMOS circuit



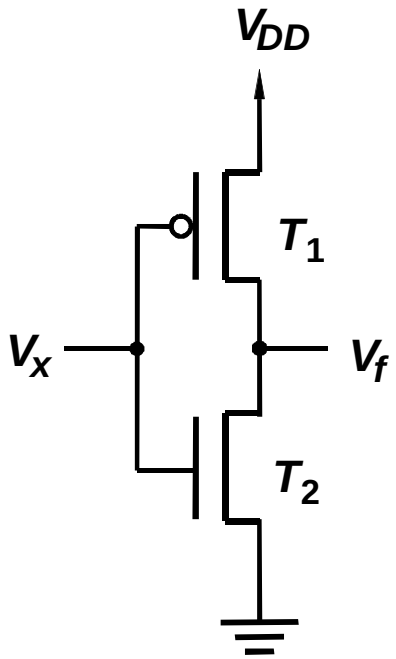
PMOS makes the output ”1”

NMOS makes the output ”0”

PMOS and NMOS Transistors



CMOS inverter



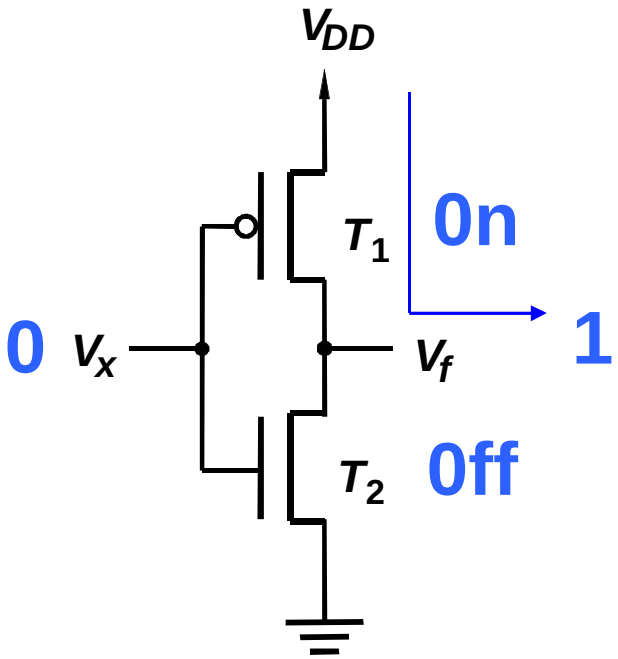
- CMOS circuits are composed of both PMOS and NMOS transistors
- CMOS stands for Complementary MOS
- **Area: $A_{Inverter}$= 2 Transistors**

x	T_1	T_2	f
0	on	off	1
1	off	on	0

(A) Circuit

(B) Truth table and transistor states

CMOS inverter



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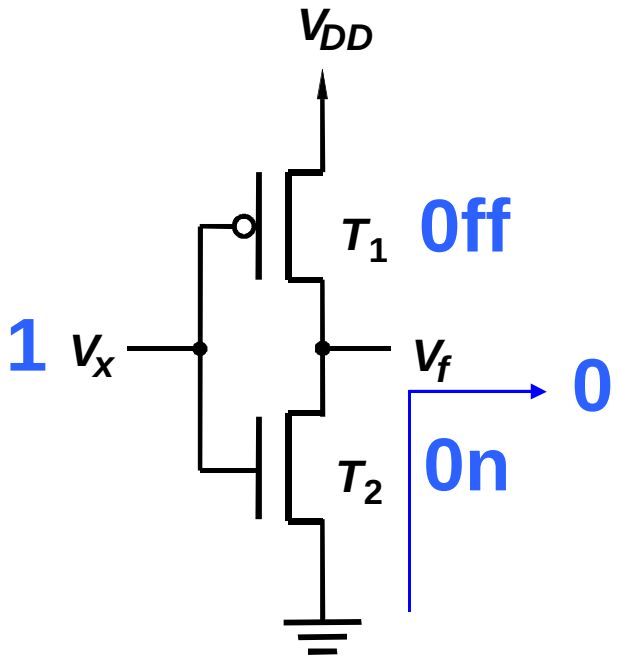

(A) Circuit

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- **Area: $A_{Inverter}$= 2 Transistors**

x	T_1	T_2	f
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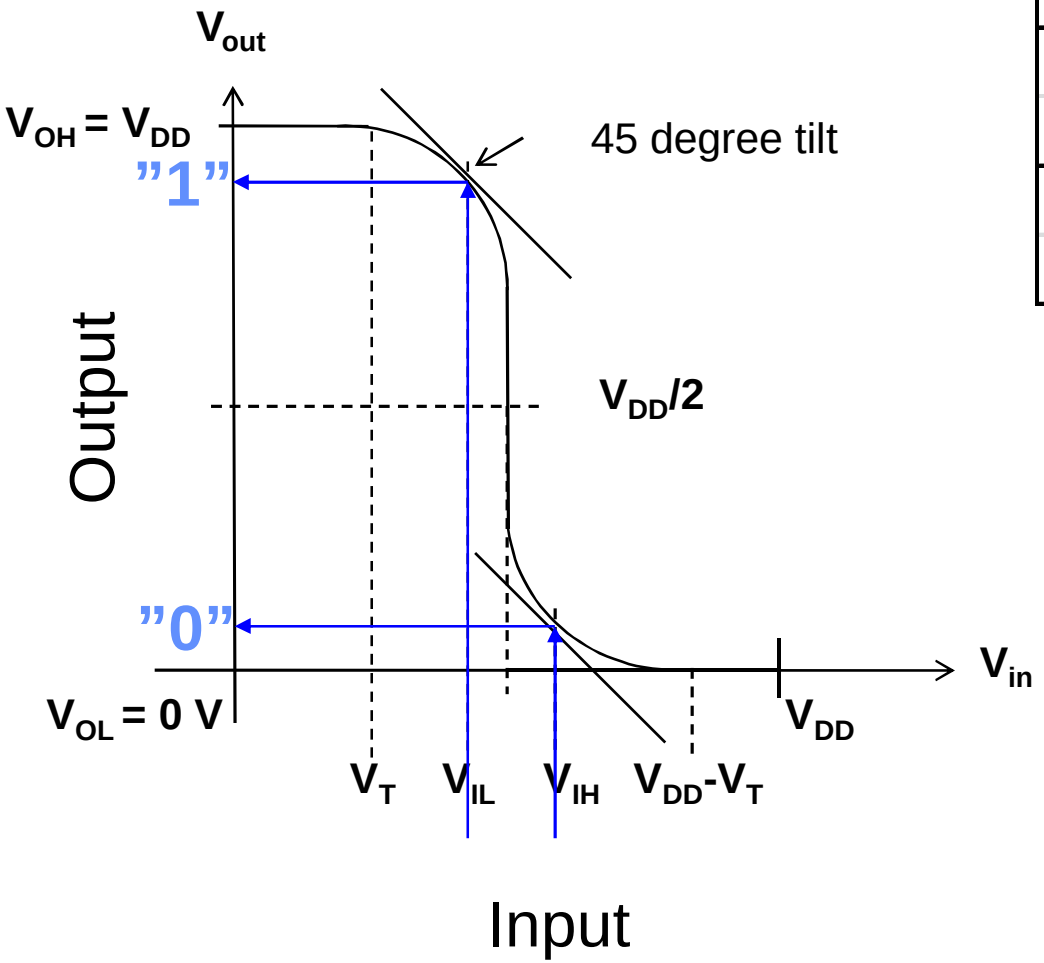
(B) Truth table and transistor states

CMOS inverter voltage transfer characteristic

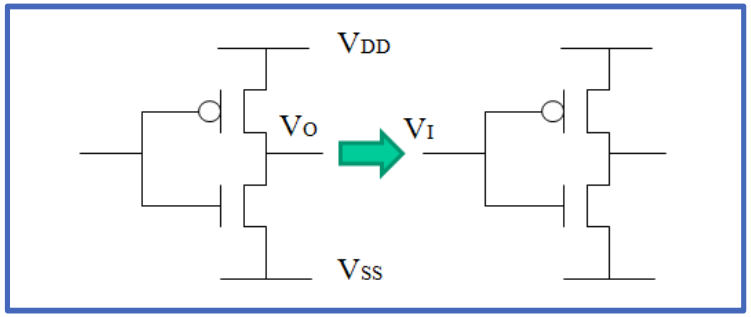


Power Supply	5.0V	3.3V	1.8V
V_{OH}	5.0	3.3	1,8
V_{IH}	2,9	1,9	1.0
V_{IL}	2,1	1,4	0.8
V_{OL}	0.0	0.0	0.0

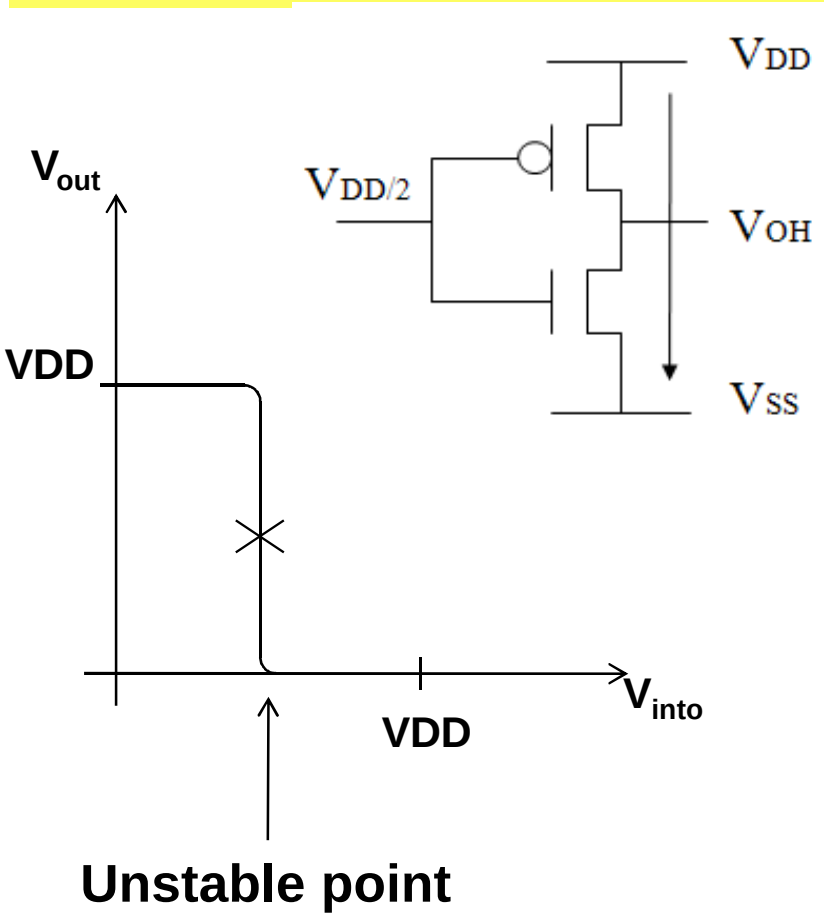
$V_T = 0.2V_{DD}$

Low Noise Margin: $NM_L = V_{IL}-V_{OL}$

High Noise Margin $NM_H = V_{OH}-V_{IH}$



One point is unstable!

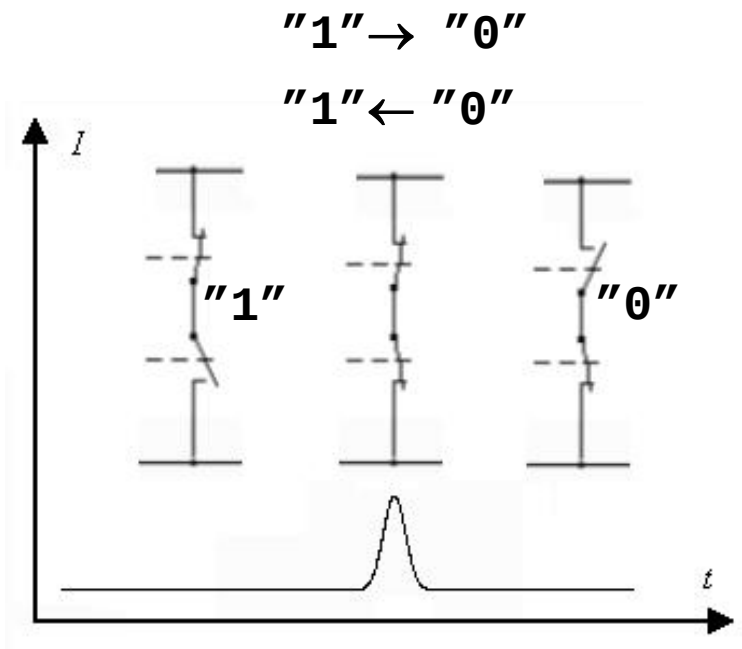


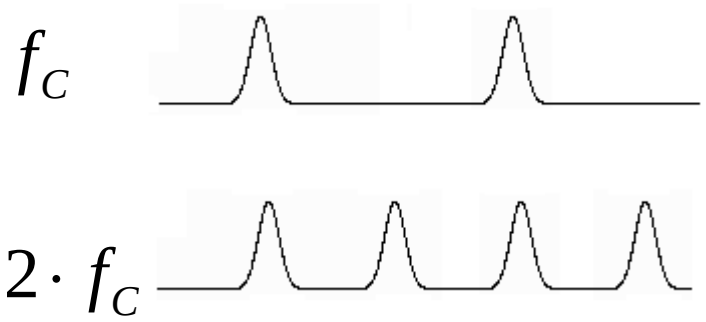
- CMOS circuit has a very stable transfer function
- At $V_{into} = V_{DD}/2$ there is an unstable point, then both T_1 and T_2 are conducting
- If a circuit temporarily stuck in this mode, it enters a state called *metastability*
- If this state lasts for a long time, the transistors in the circuit may be damaged by the high current

Metastability will be discussed in later lectures

CMOS–Dynamic power consumption!

Classical CMOS has *only* losses exactly at the vid *switching point*. The Power dissipation P_F is proportional to the clock-frequency!

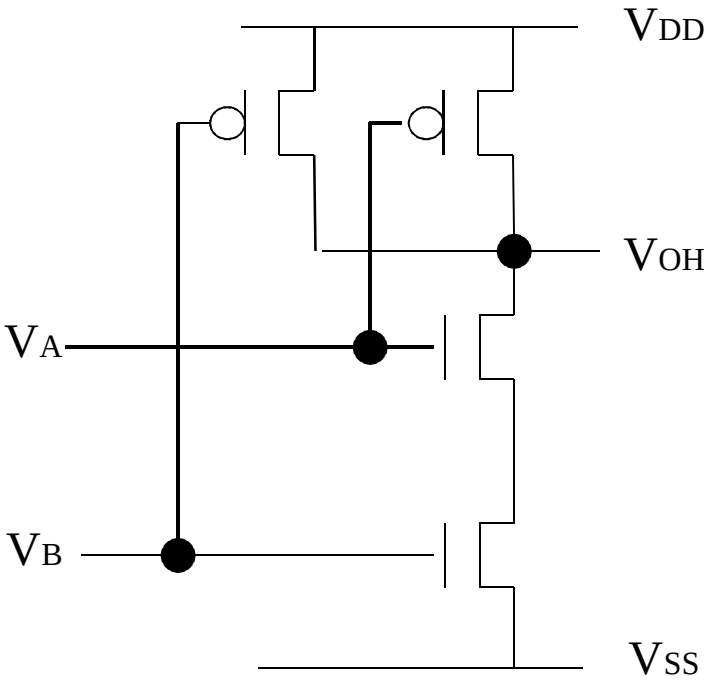




$$P_F \propto f_C \cdot V_{DD}^2$$

P_F	*Power losses*
f_C	*Clockfrequency*
V_{DD}	*Supply Voltage*

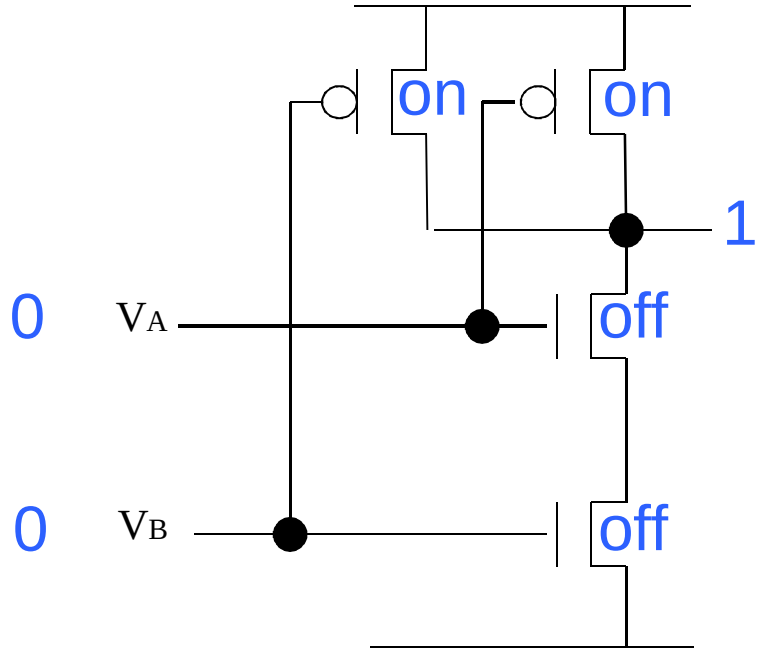
NAND gate



V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{SS}(0)$	$V_{DD}(1)$	$V_{DD}(1)$
$V_{DD}(1)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{DD}(1)$	$V_{DD}(1)$	$V_{SS}(0)$

Area: A_{NAND}= 4 Transistors

NAND gate



V_A	V_B	V_{OH}
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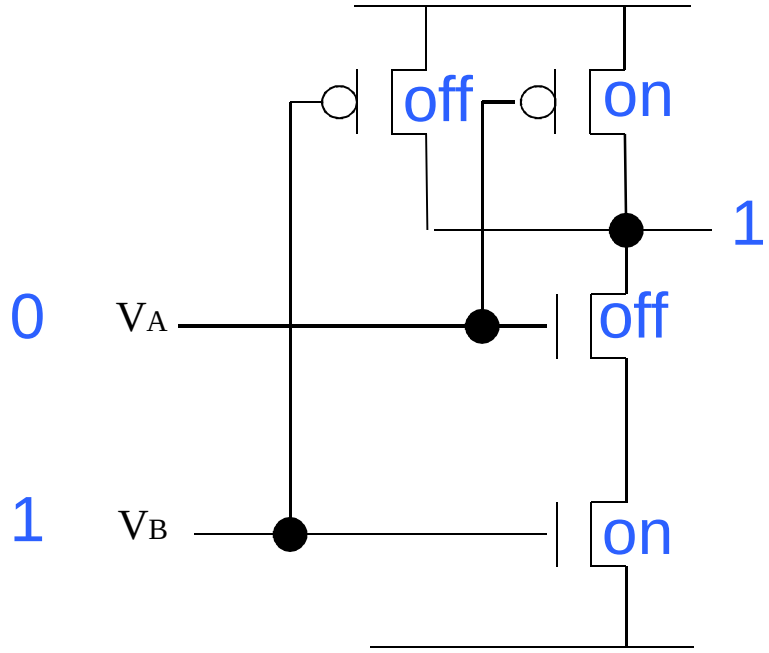
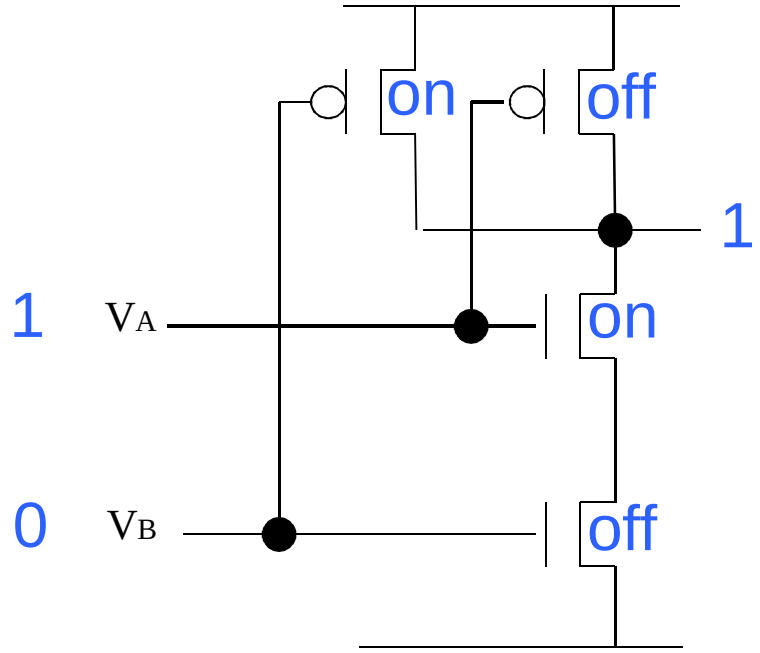


V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{SS}(0)$	$V_{DD}(1)$	$V_{DD}(1)$

Area: A_{NAND}= 4 Transistors

NAND gate



V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
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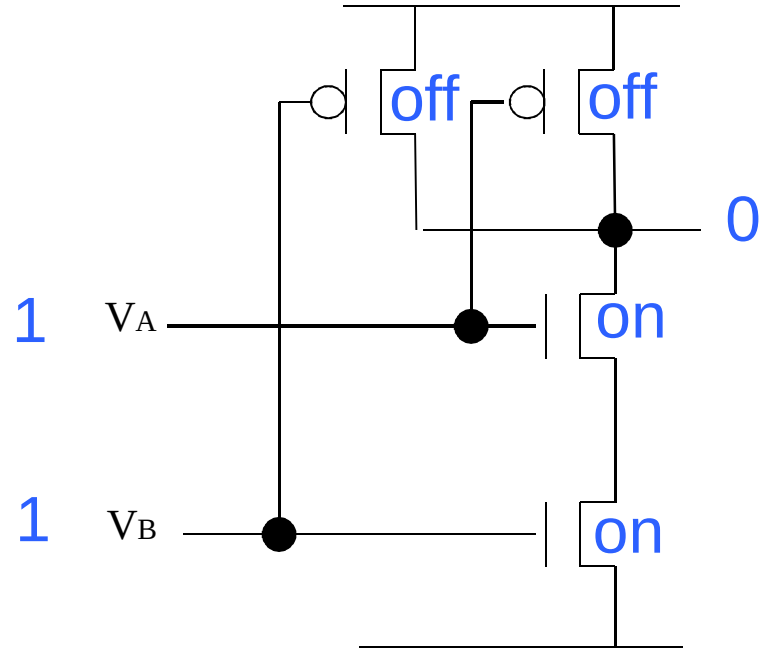
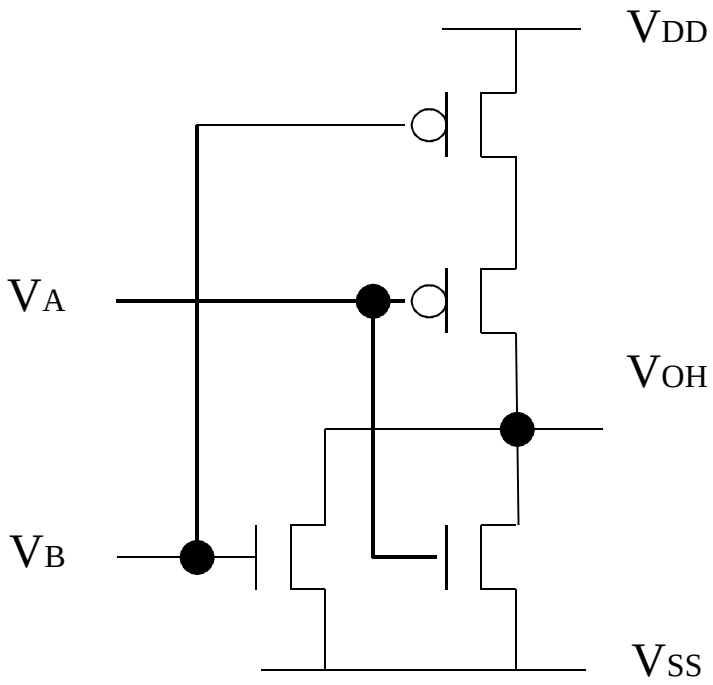


V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{SS}(0)$	$V_{DD}(1)$	$V_{DD}(1)$
$V_{DD}(1)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{DD}(1)$	$V_{DD}(1)$	$V_{SS}(0)$

Area: A_{NAND}= 4 Transistors

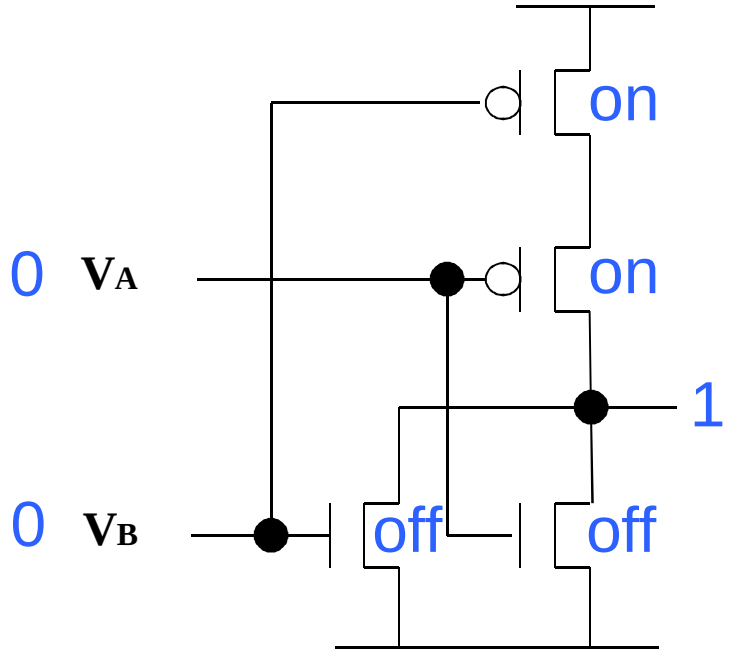
NOR gate



V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{SS}(0)$	$V_{DD}(1)$	$V_{SS}(0)$
$V_{DD}(1)$	$V_{SS}(0)$	$V_{SS}(0)$
$V_{DD}(1)$	$V_{DD}(1)$	$V_{SS}(0)$

Area: A_{NOR}= 4 Transistors

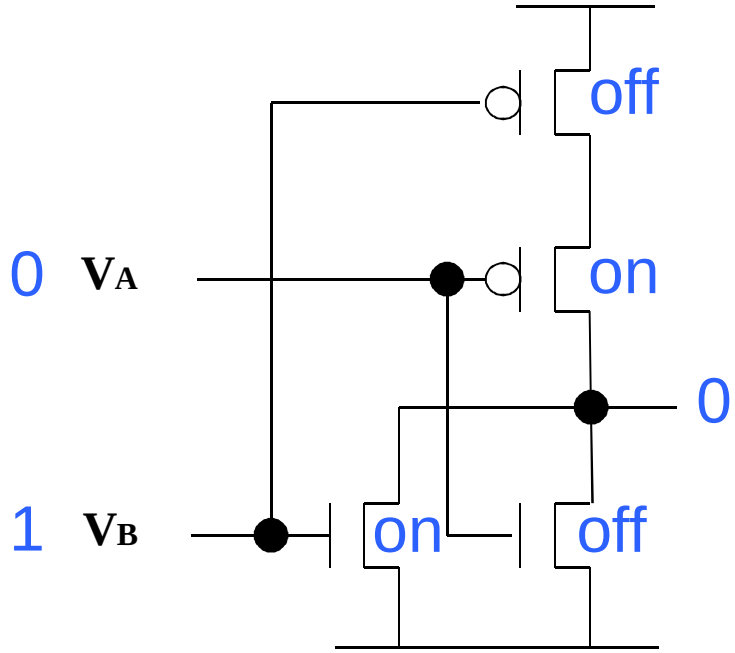
NOR gate



V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$

Area: A_{NOR}= 4 Transistors

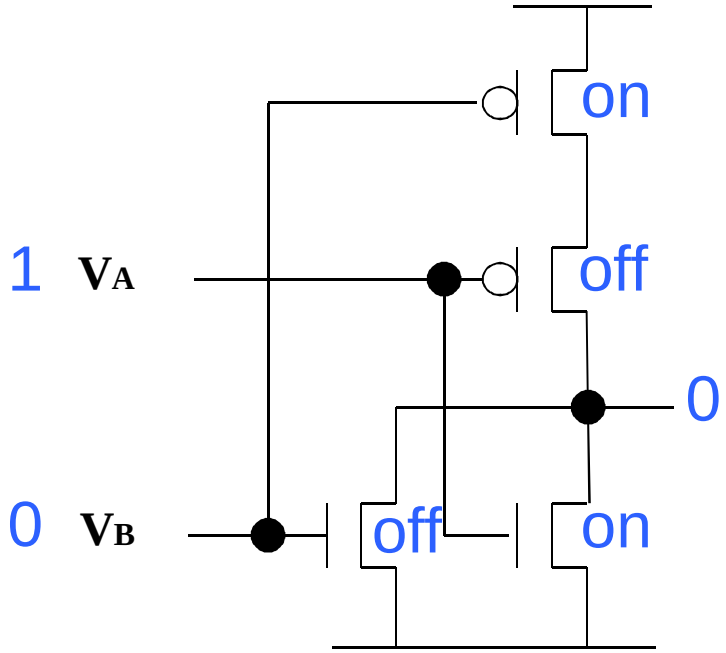
NOR gate



V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{SS}(0)$	$V_{DD}(1)$	$V_{SS}(0)$

Area: A_{NOR}= 4 Transistors

NOR gate



V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{SS}(0)$	$V_{DD}(1)$	$V_{SS}(0)$
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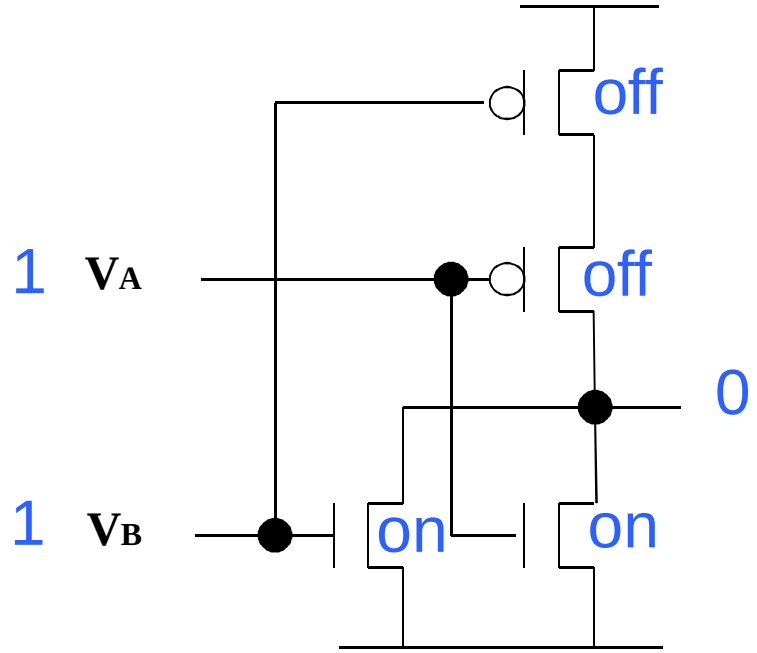
Area: A_{NOR}= 4 Transistors

NOR gate



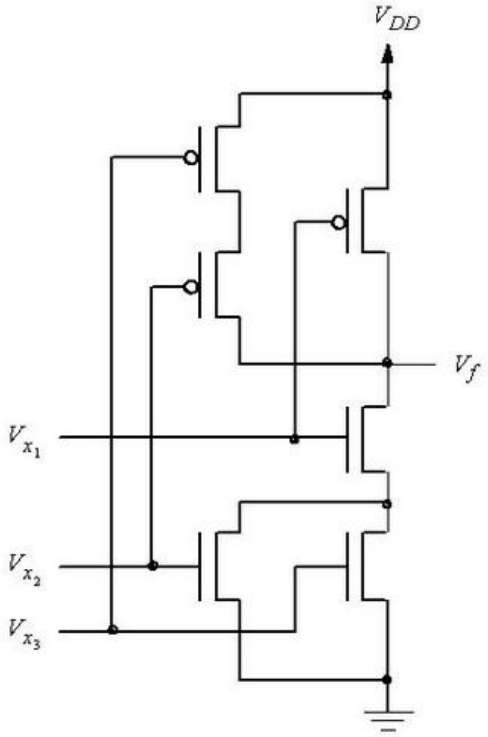
V_A	V_B	V_{OH}
$V_{SS}(0)$	$V_{SS}(0)$	$V_{DD}(1)$
$V_{SS}(0)$	$V_{DD}(1)$	$V_{SS}(0)$
$V_{DD}(1)$	$V_{SS}(0)$	$V_{SS}(0)$
$V_{DD}(1)$	$V_{DD}(1)$	$V_{SS}(0)$

Area: A_{NOR}= 4 Transistors

Group work

Illustrate the CMOS circuit of $F=\bar{X}_1+\bar{X}_2\bar{X}_3$

PDN network: $\overline{F=\bar{X}_1+\bar{X}_2\bar{X}_3} = X_1(X_2+X_3)$



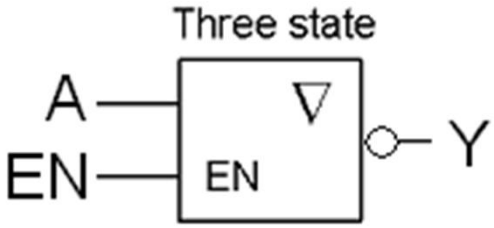
Negative logic

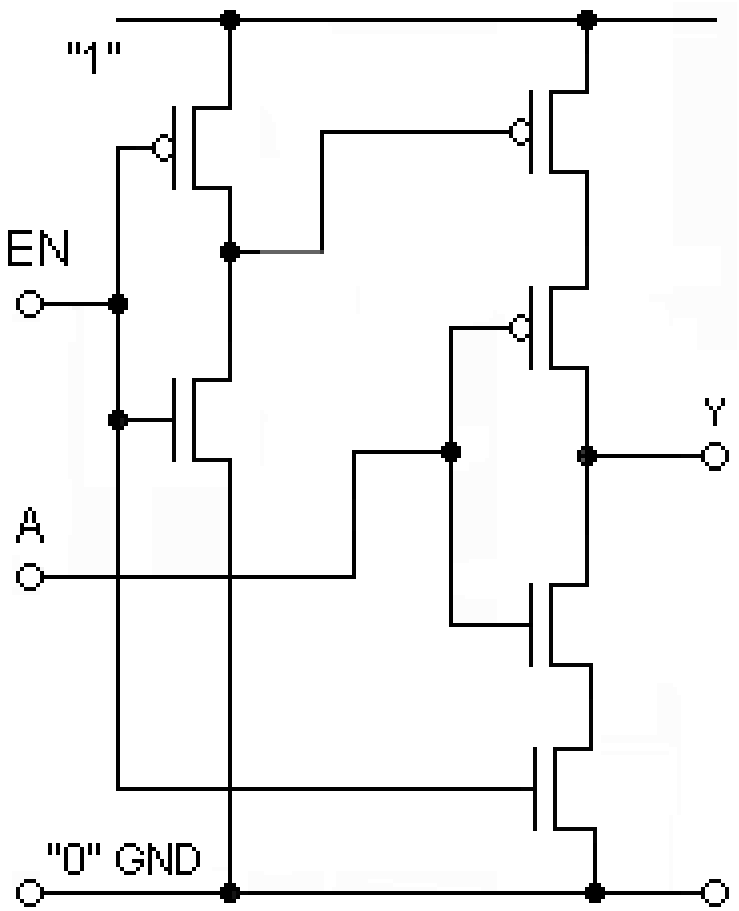
- You can also reverse the logic and let L (low voltage) represent the logic 1 and H (high voltage) represent the logic 0
  - This is called *negative logic*
- An AND function becomes an OR function and vice versa
  - It is not important which logic is used - negative or positive, but positive logic is more traditional

Three-state?

A CMOS-gate in addition to "1" or "0" is also provided with a third output state - the three-state ”Z”. (= unconnected output).

If many outputs are connected to the same line ("bus"), you can use one of the out-puts at a time . The other outputs are held in the Three-state condition.





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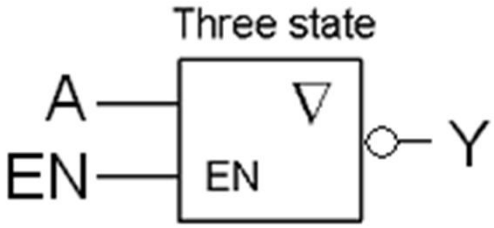

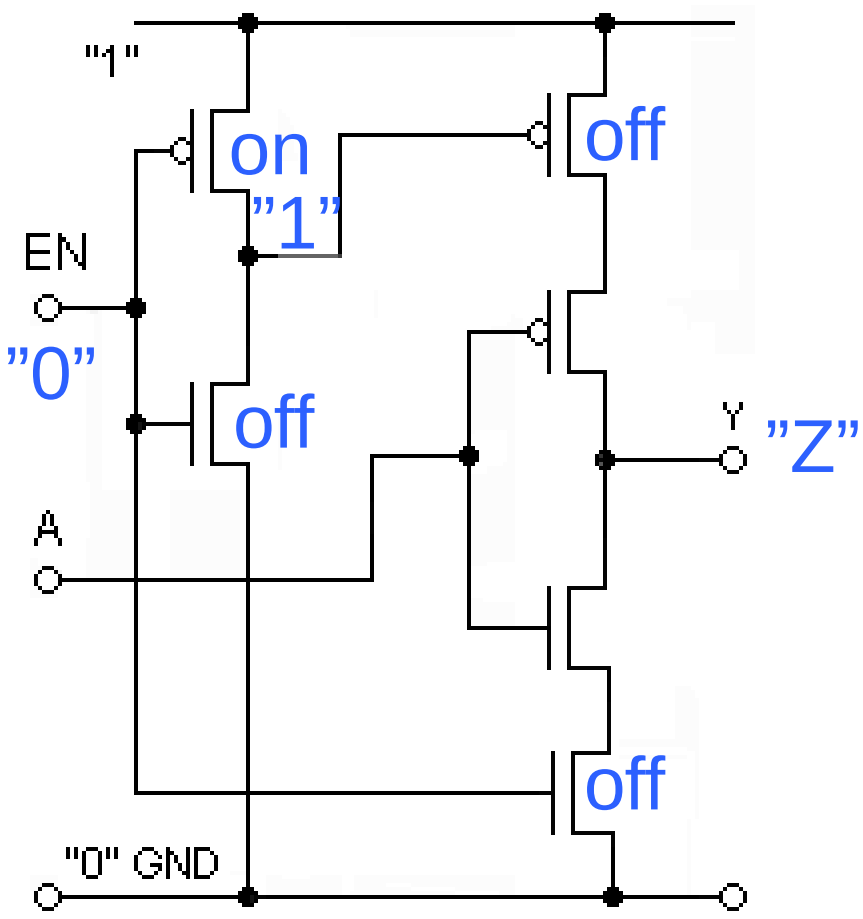

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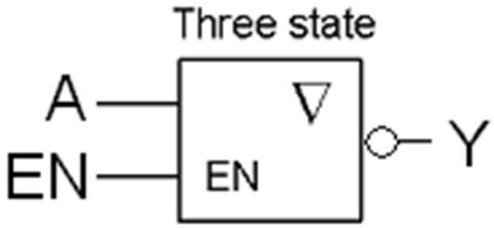
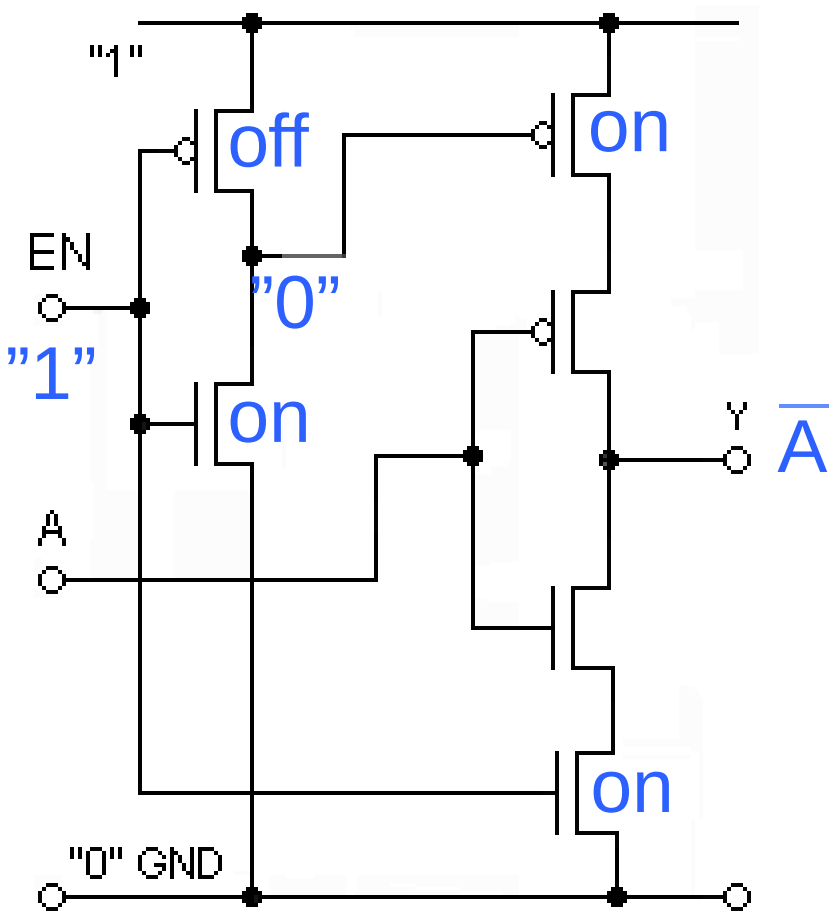
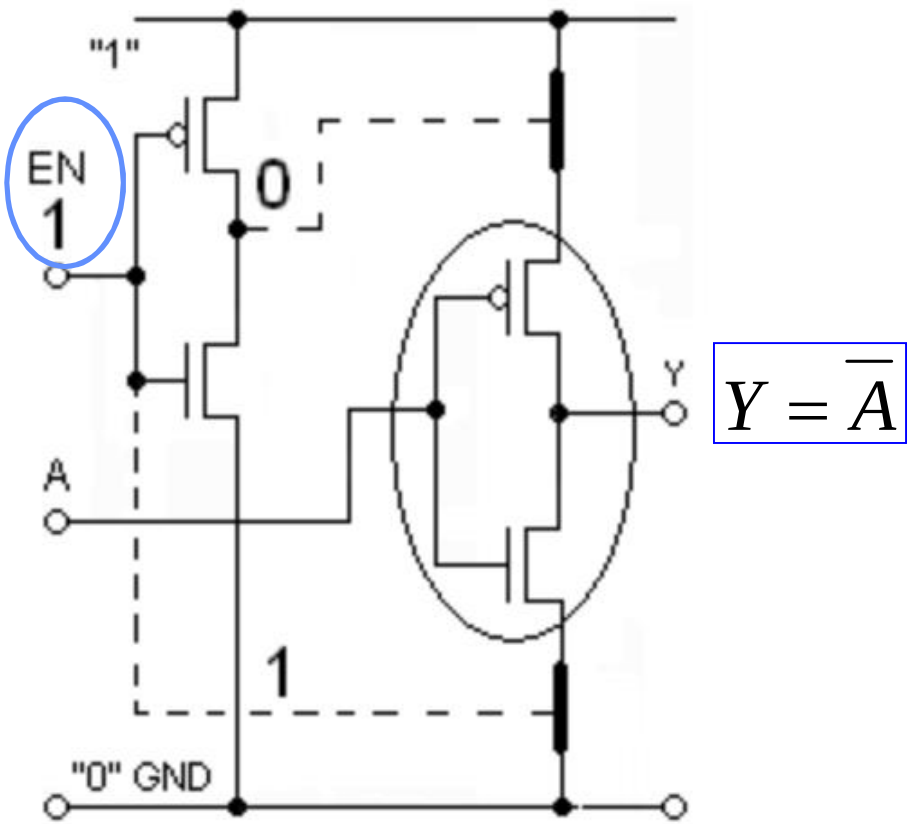
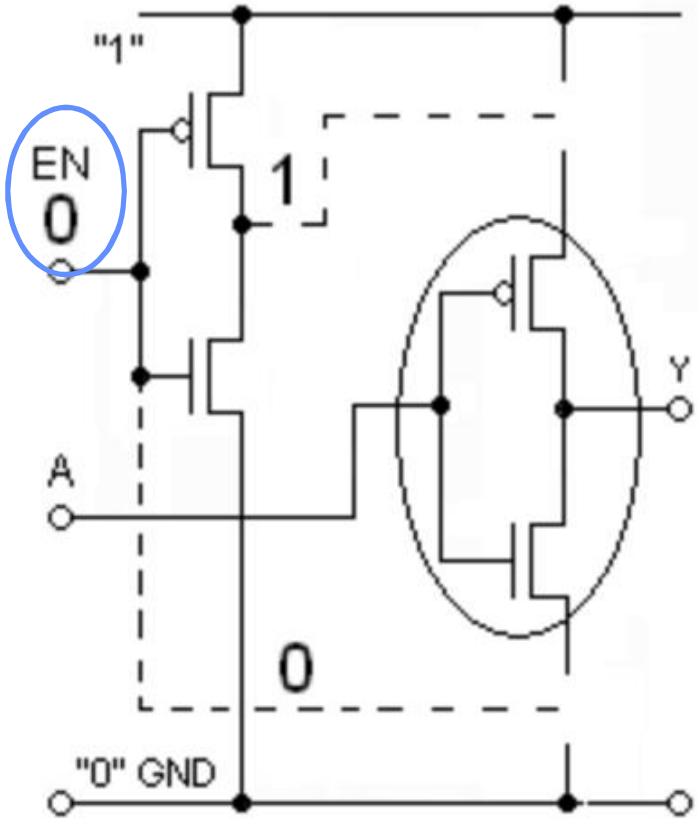




High Impedance ('Z')



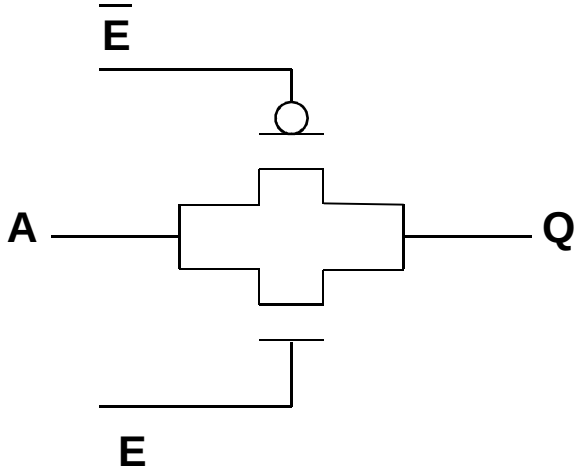
$Y = \overline{A}$

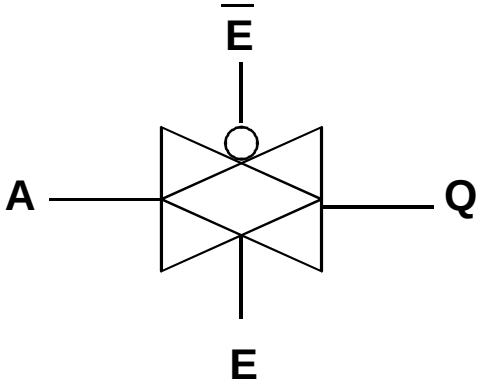


$Y = 'Z'$

Output is not connected

Transmission gate (pass gate)



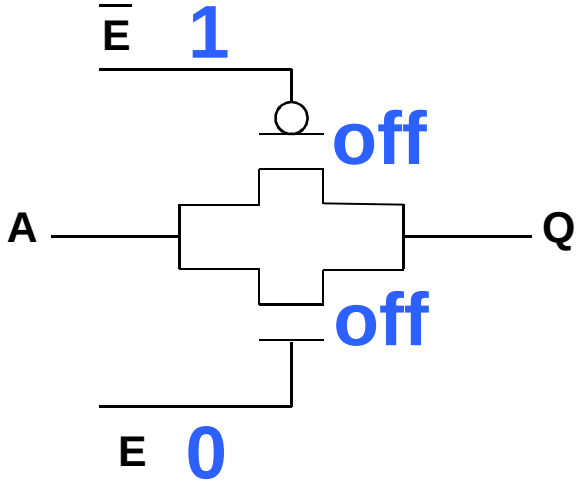


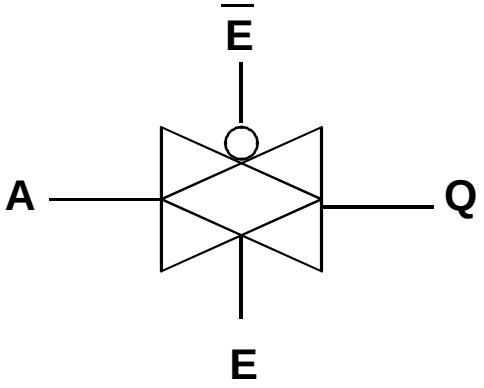
- The pass gate acts as a switch controlled by E
- If E = 0, the switch is open, Q = Z
- If E = 1, the switch is closed, Q = A
- Pass gates have a smaller driving capacity than ordinary gates

V_A	V_E	V_{OH}
L	L	Z
L	H	L
H	L	Z
H	H	H

Area: A_{TG}= 2 Transistors

Transmission gate (pass gate)





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V_A	V_E	V_{OH}
L	L	Z
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H	L	Z
H	H	H

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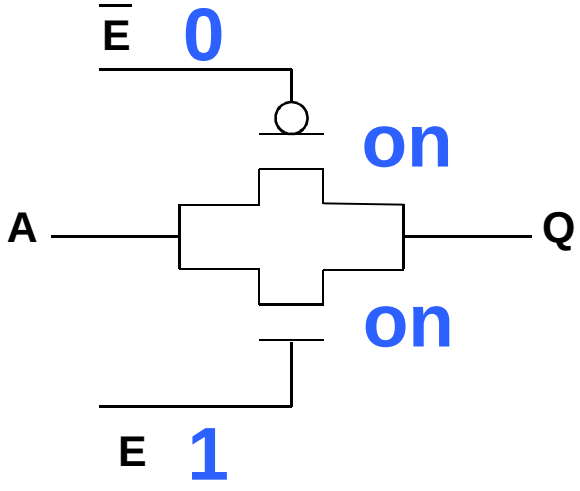
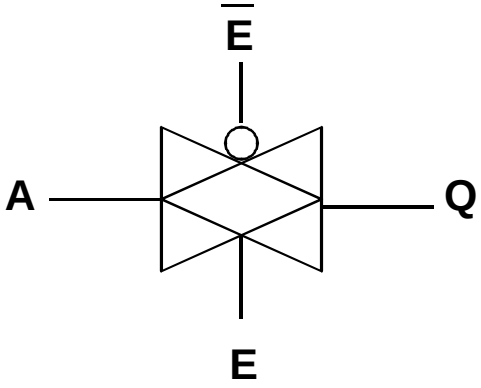
Transmission gate (pass gate)





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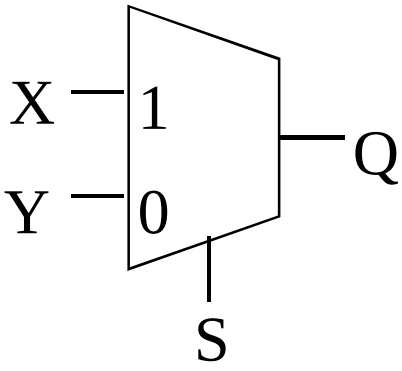
L	L	Z
L	H	L
H	L	Z
H	H	H

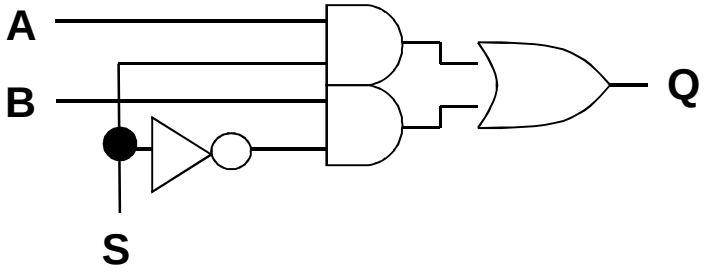
Area: A_{TG}= 2 Transistors

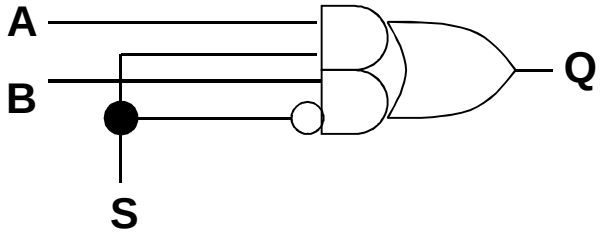
Multiplexer

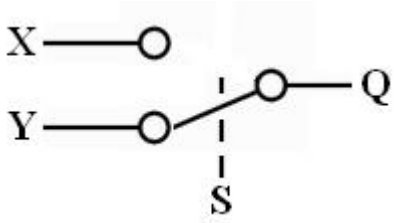
Example: MUX is a dataselector



$$Q = XS + Y\overline{S}$$

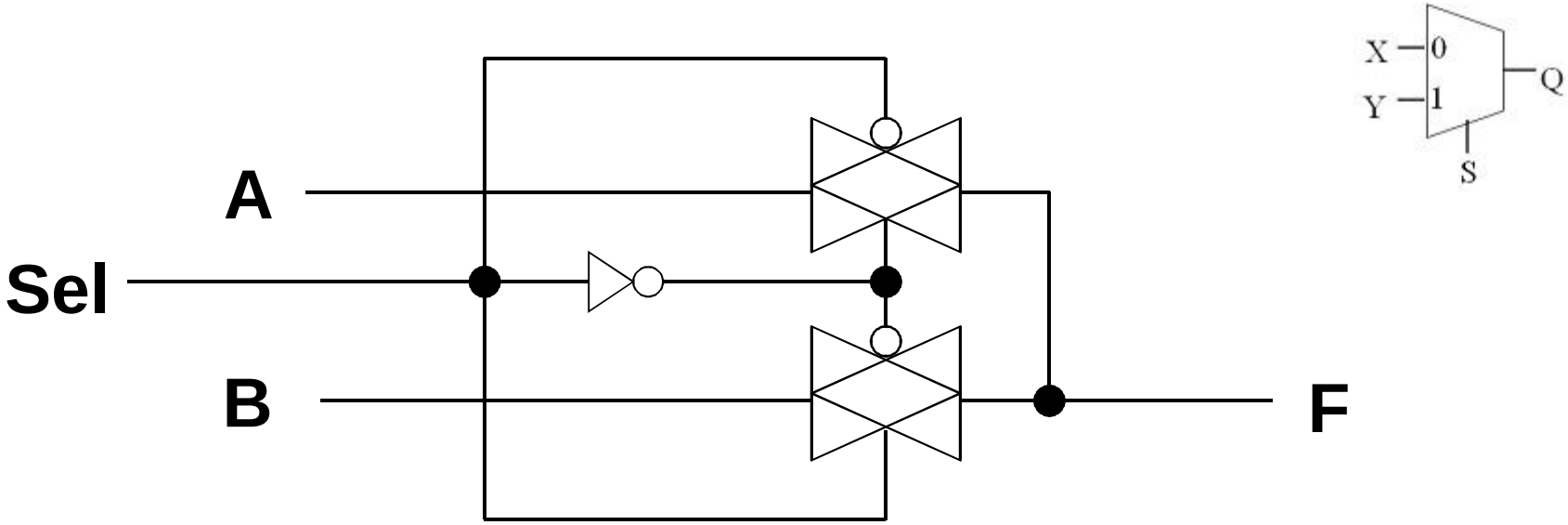






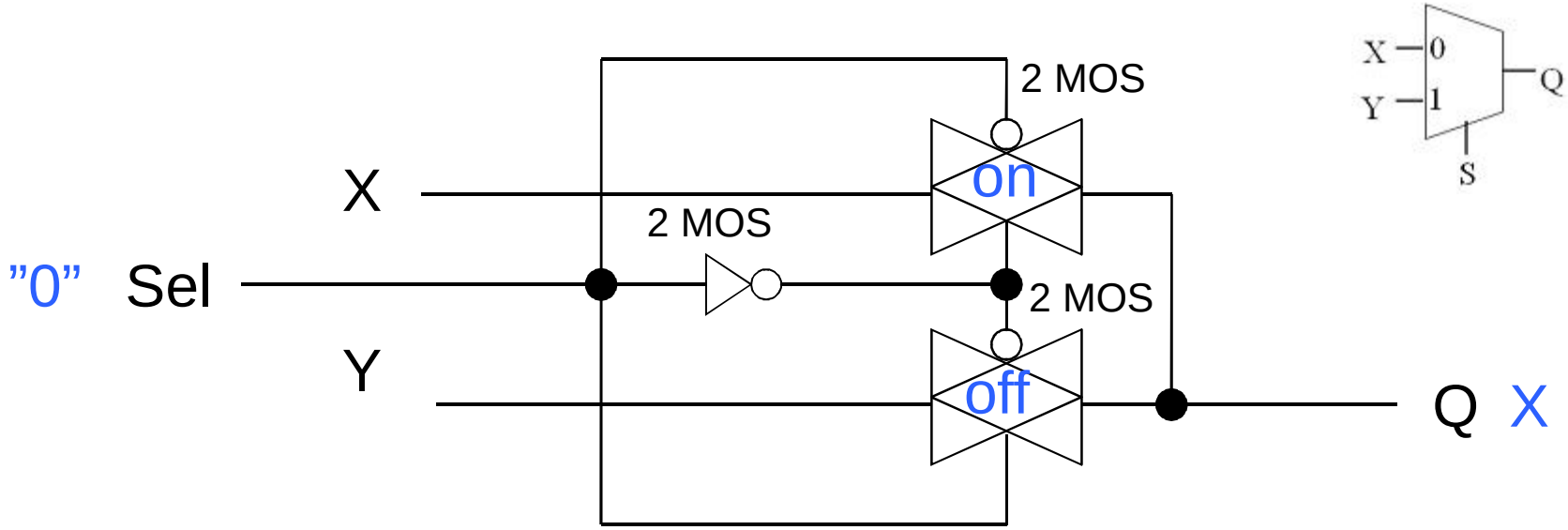
The inverter is denoted by a circle

Transmission gate MUX Implementation



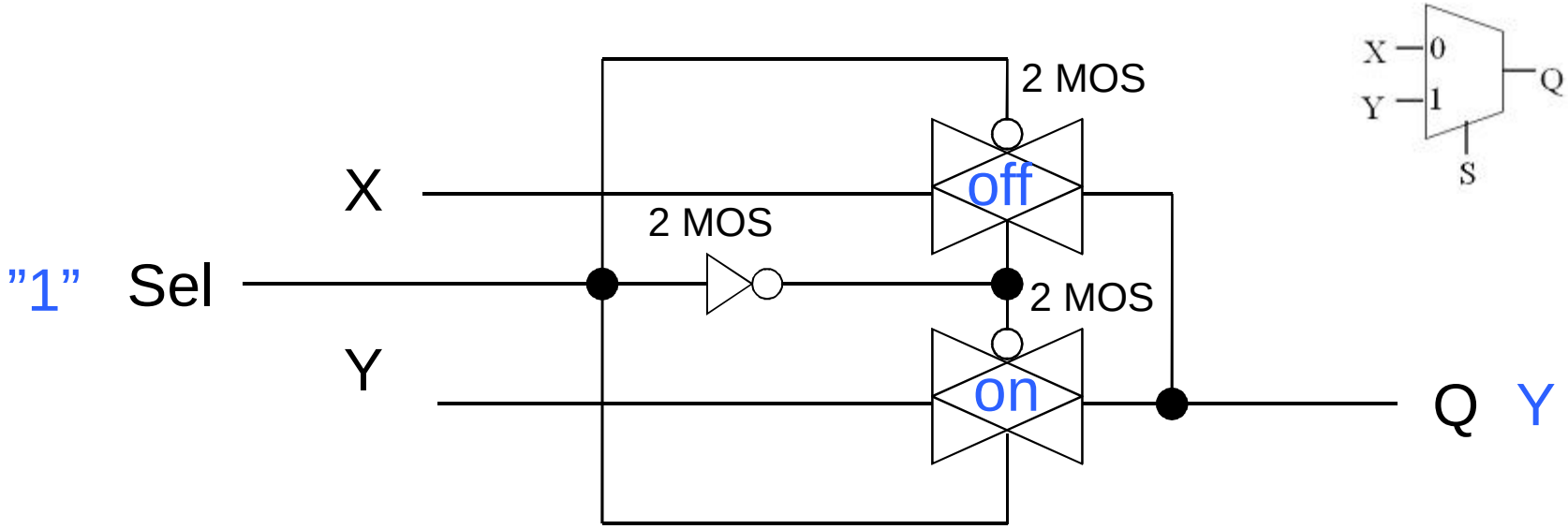
Area: A_{mux}= 6 Transistors

Transmission gate MUX Implementation



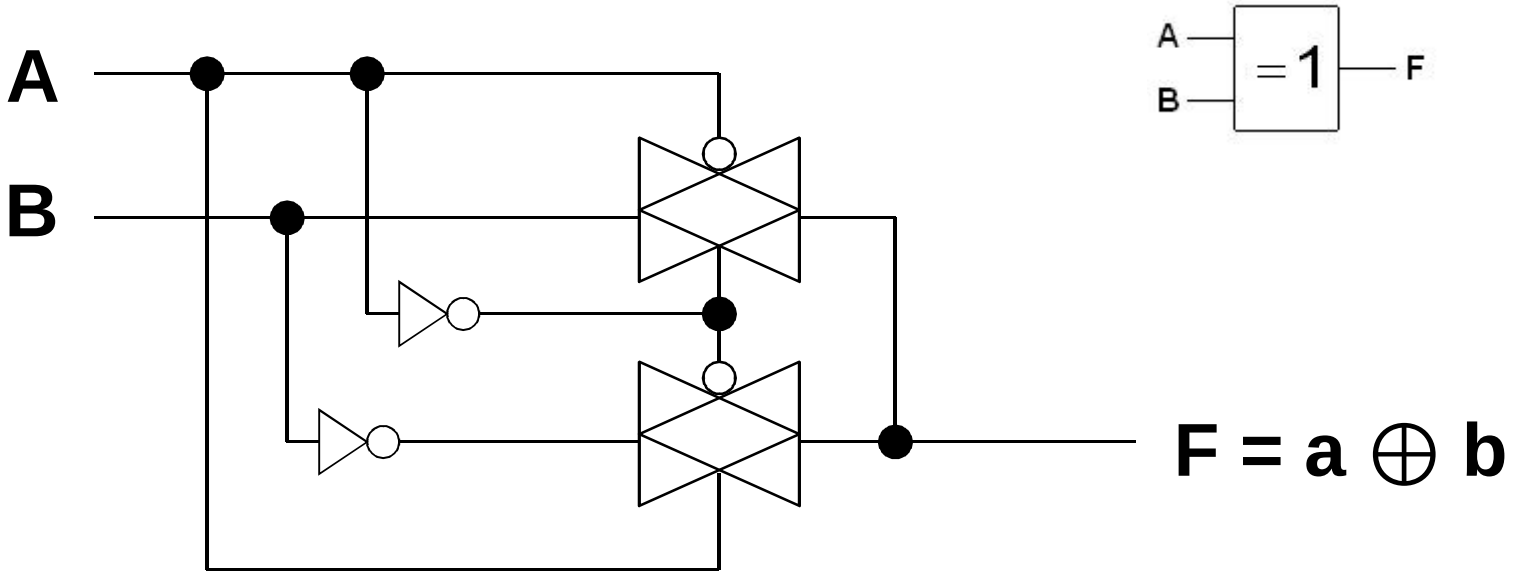
Area: A_{mux}= 6 Transistors

Transmission gate MUX Implementation



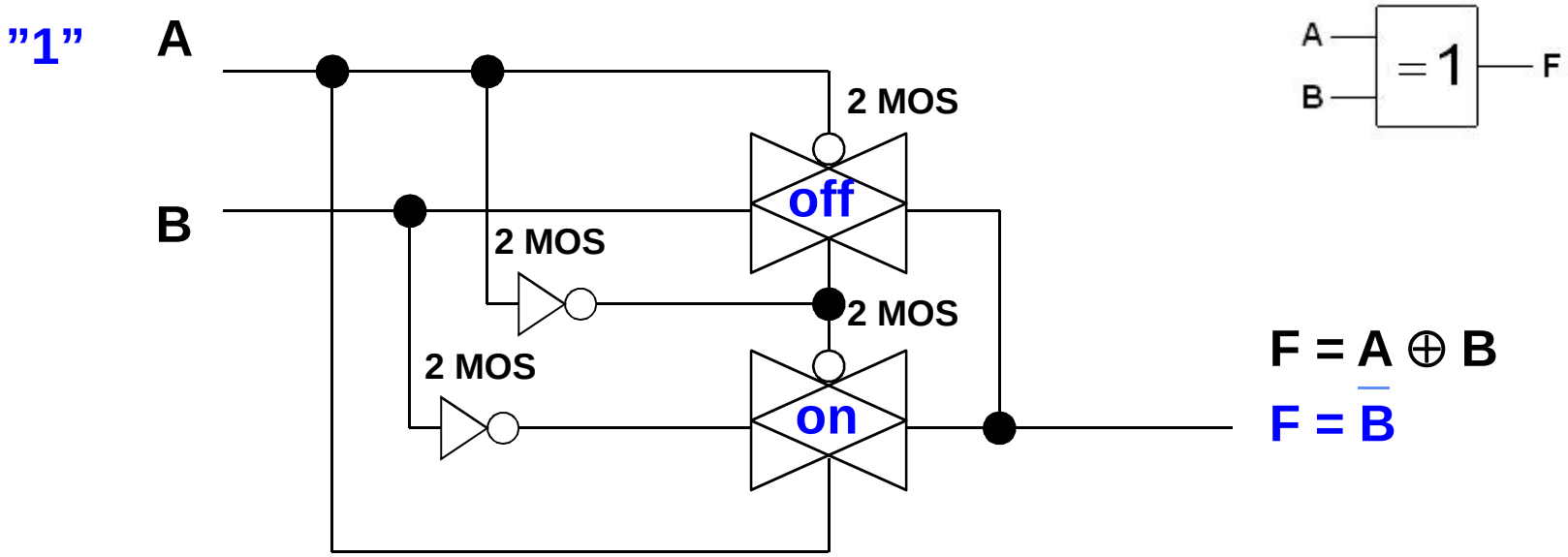
Area: A_{mux}= 6 Transistors

XOR implementation with pass gates



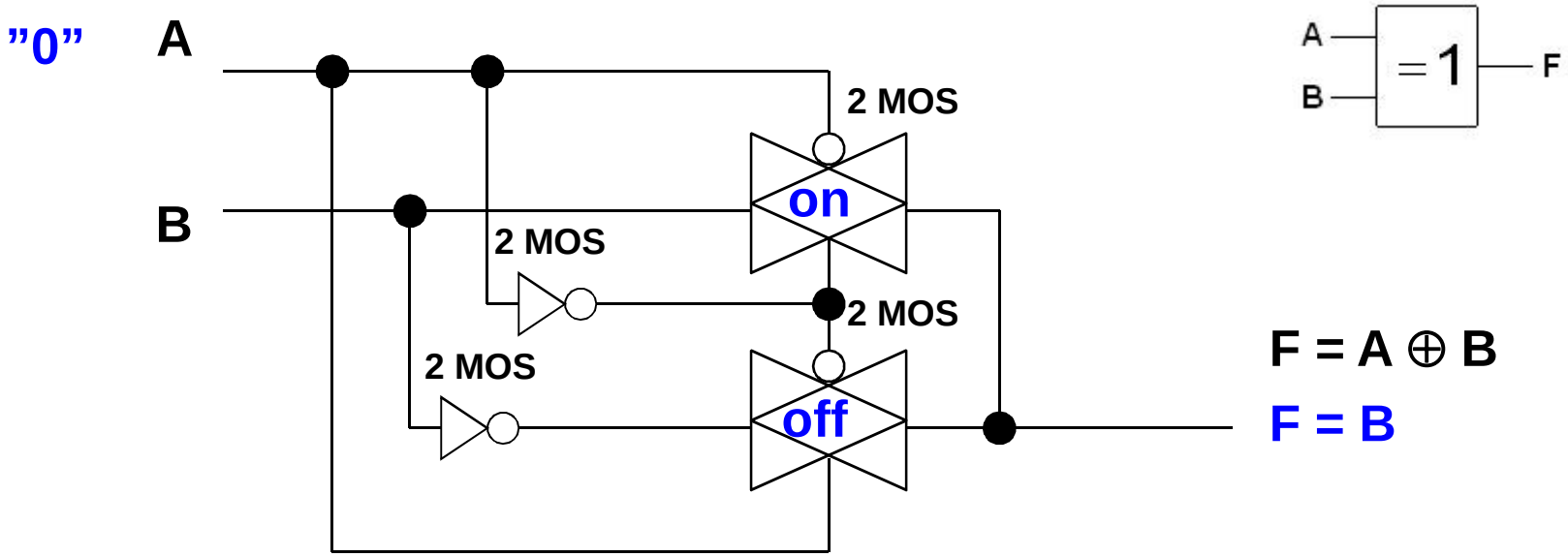
Area: A_{mux}= 8 Transistors

XOR implementation with pass gates



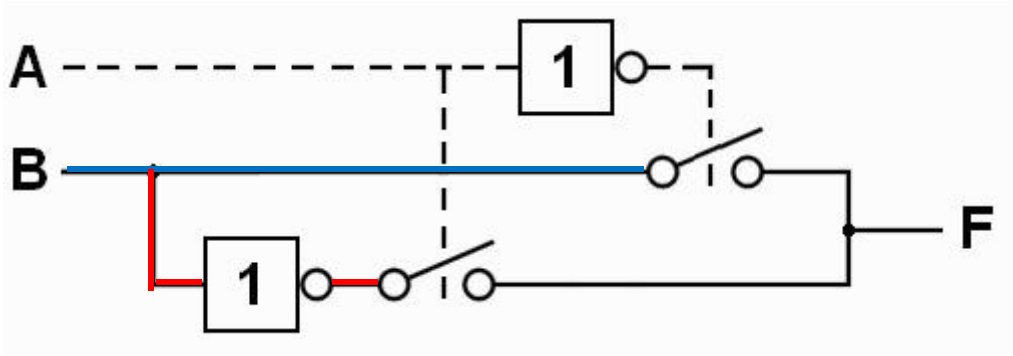
Area: A_{mux}= 8 Transistors

XOR implementation with pass gates



Area: A_{mux}= 8 Transistors

XOR implementation with pass gates

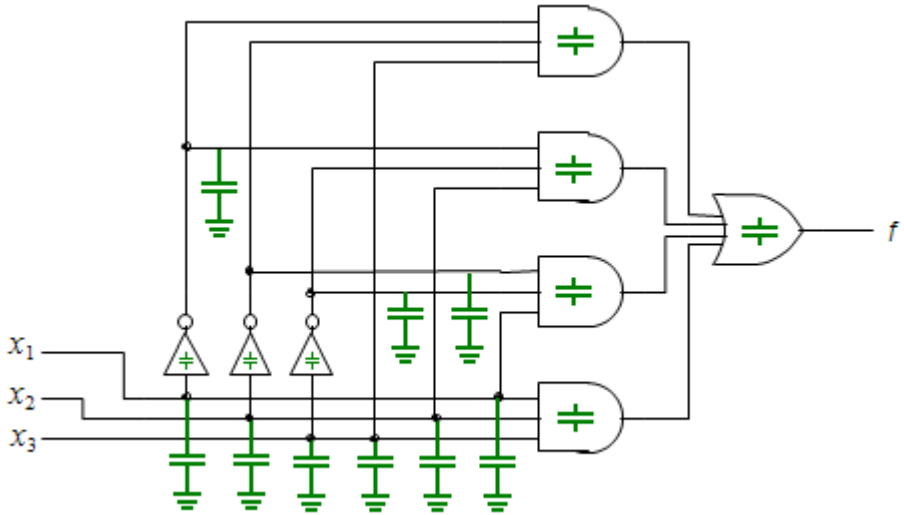


A	B	F	
0	0	0	$F = B$
0	1	1	
1	0	1	$F = \overline{B}$
1	1	0	

Things Take Time ...
About delays in circuits

Delays in circuits

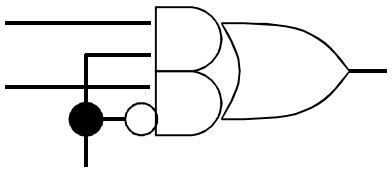
- Each wires in an electronic circuits has a capacitance
- Capacitance has a negative effect on the speed of operation of logic circuits



Typical delays

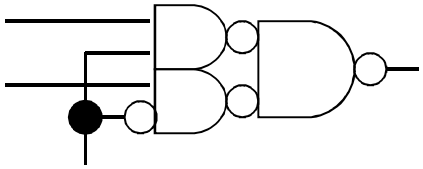
NAND, NOR	T
NOT	½ T, T (if implemented using NAND-gate)
AND, OR	2T (2 NANDs in a row)
XOR, XNOR, MUX	3T...5T
XOR, MUX (Pass-Gate)	2T

Optimized structures (MUX)

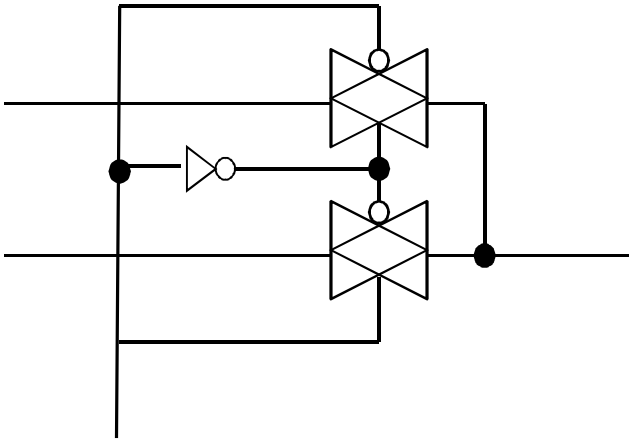


AND-OR

DeMorgan



NAND-NAND



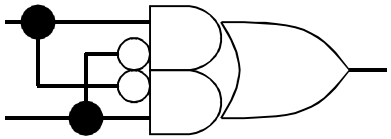
Area: A_{MUX}= 2+6+6+6=20
Transistors
Delay: T_{MUX}= $5T_{NAND}$

Area: A_{MUX}= 2+4+4+4 =14
Transistors
Delay: T_{MUX}= $3T_{NAND}$

Area: A_{MUX}= 2+2+2=6
Transistors
Delay: T_{MUX}= ~ $2T_{NAND}$

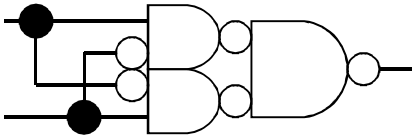
Best!

Optimized structures (XOR)



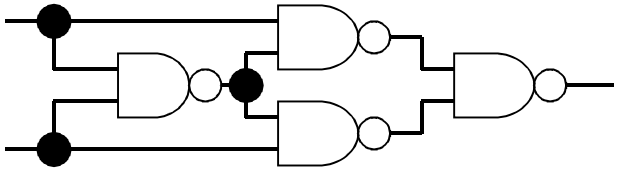
Area: A_{MUX}= 2+2+6+6+6=22 Transistors
Delay: T_{MUX}= $5T_{NAND}$

DeMorgan

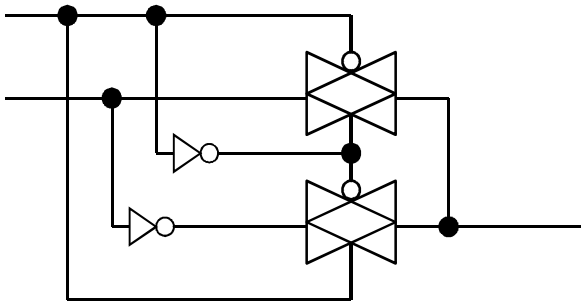


Area: A_{MUX}= 2+2+4+4+4=16 Transistors
Delay: T_{MUX}= $3T_{NAND}$

NAND only



Area: A_{MUX}= 16 Transistors
Delay: T_{MUX}= $3T_{NAND}$



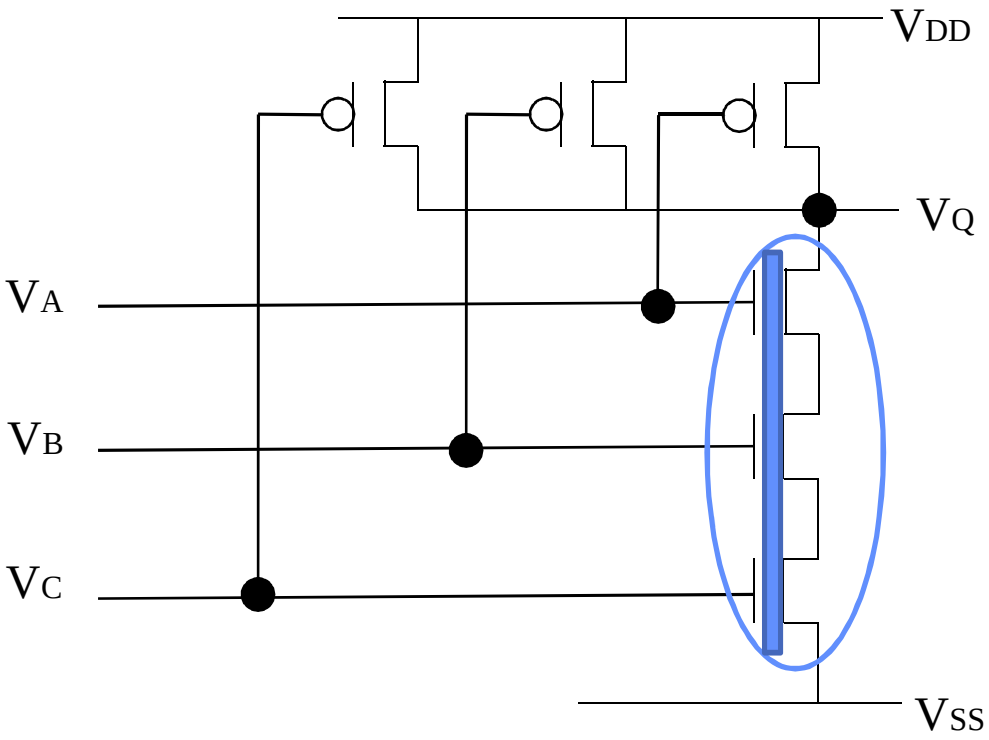
Area: A_{MUX}= 2x4=8 Transistors
Delay: T_{MUX}= ~ $2T_{NAND}$

Best!

Fan-in

- **Fan-in** is the number of inputs to the gate.
- If a gate has many inputs, it has a larger internal capacitance => its internal delay T_i (also called the intrinsic delay) becomes larger.

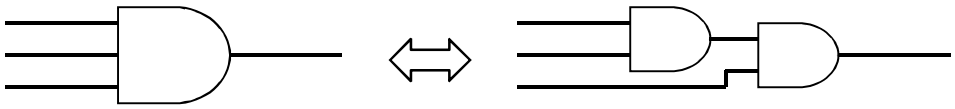
Gates with more than 2 inputs



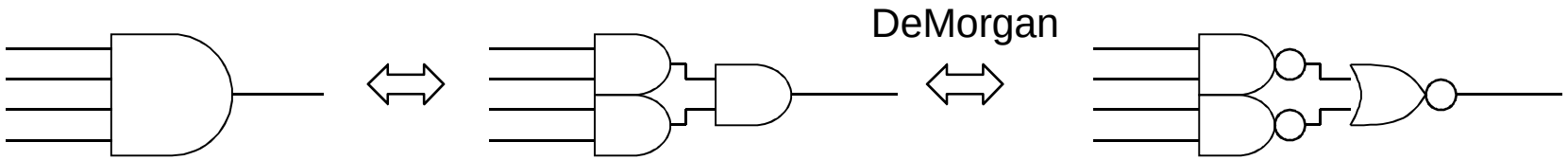
3-input NAND

- Gates with more than three or four inputs are used rarely
- The internal capacitance becomes too large and gates too slow
- A long line of transistors connected in series gives long delay!

High fan-in is solved with tree-structures



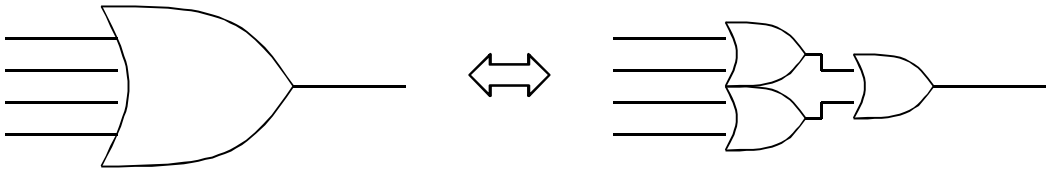
$$a \cdot b \cdot c = a \cdot (b \cdot c)$$



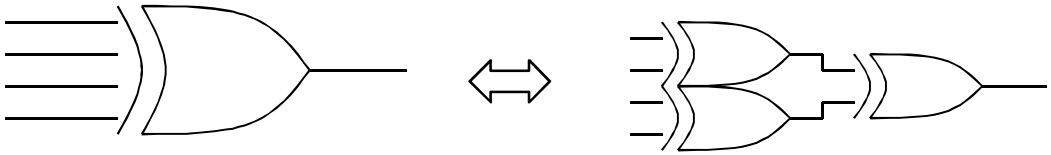
$$a \cdot b \cdot c \cdot d = (a \cdot b) \cdot (c \cdot d)$$

$$\overline{\overline{(a \cdot b)} + \overline{(c \cdot d)}} = a \cdot b \cdot c \cdot d$$

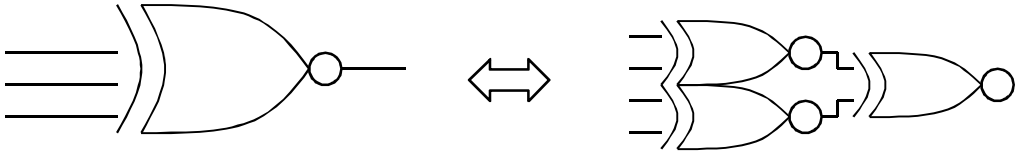
More tree structures ...



$$a+b+c+d=(a+b)+(c+d)$$



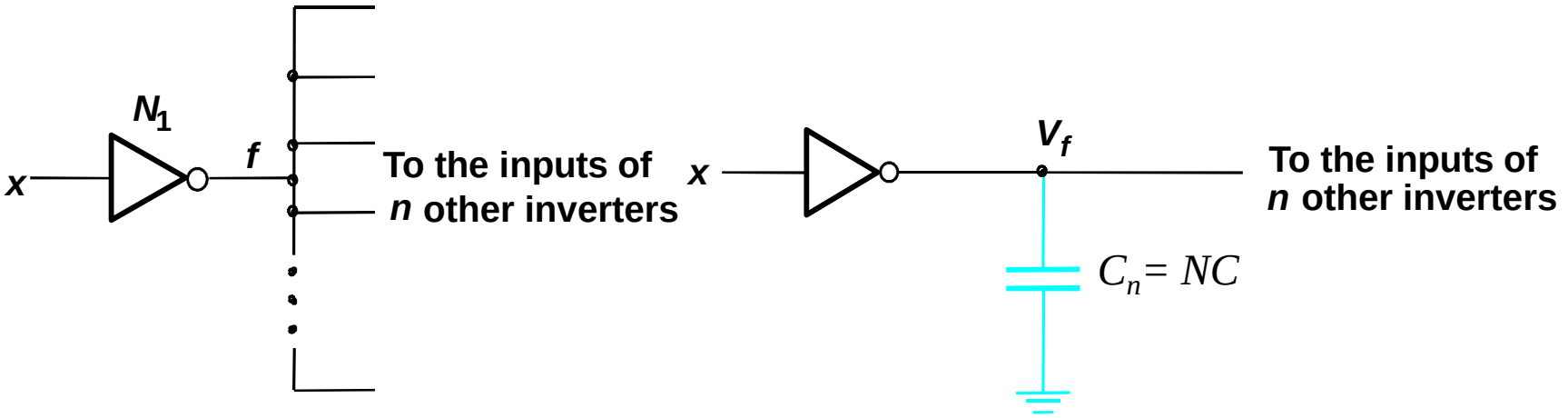
$$a \oplus b \oplus c \oplus d = (a \oplus b) \oplus (c \oplus d)$$



$$\overline{a \oplus b \oplus c \oplus d} = \overline{(a \oplus b)} \oplus \overline{(c \oplus d)}$$

Fan-out

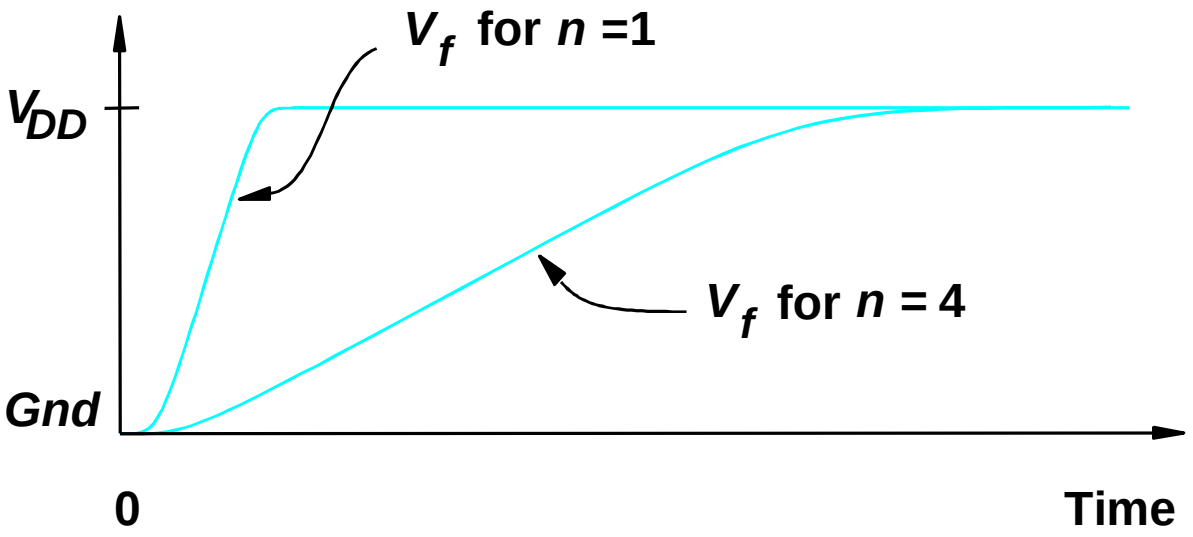
- Fan-out is number of other gates that a specific gate drives
- Each of driven gates increases the capacitive load on f



(A) Inverter that drives *n* other inverters (B) Equivalent circuit for timing purposes

Effect of fan-out on propagation delay

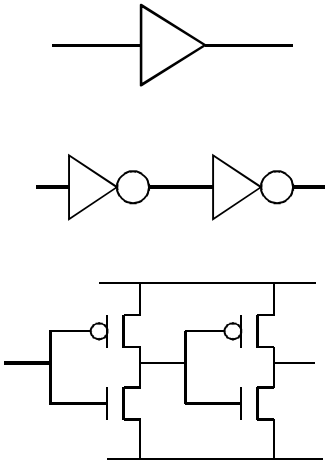
- The propagation time for different fan-outs



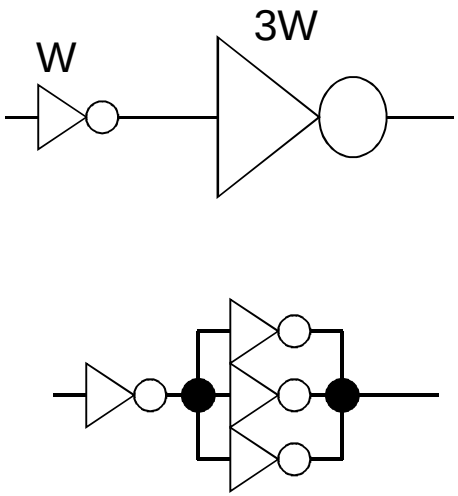
Buffering

- A buffer is a circuit that implements the function f(x) = x
- Buffers are used to increase performance
- They have larger transistors and can drive higher-than-normal capacitive loads
- They are also used when high current flow is needed to drive external devices

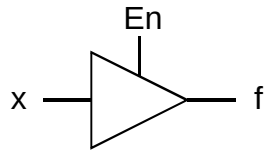
High Fan-out: Use Buffers



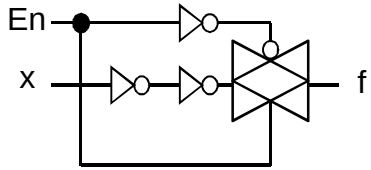
Non-Inverting Buffer



High-Fan-Out Buffer



x	En	f
0	0	Z
0	1	0
1	0	Z
1	1	1



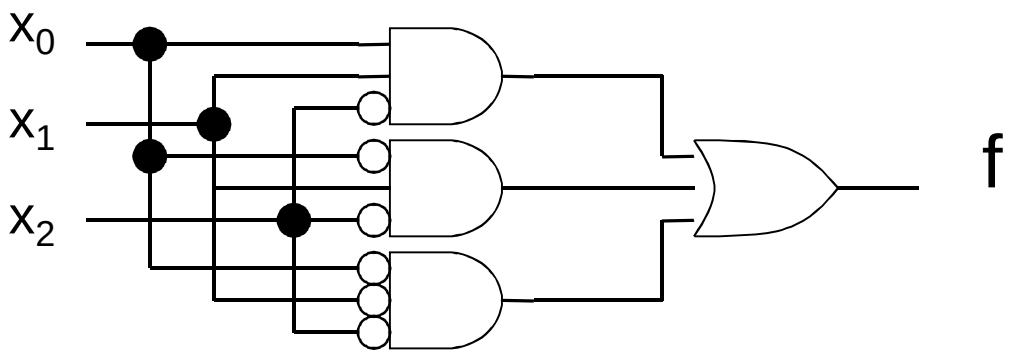
Tri-State Buffer

When En = 0, f is disconnected from x

When En = 1, f = x

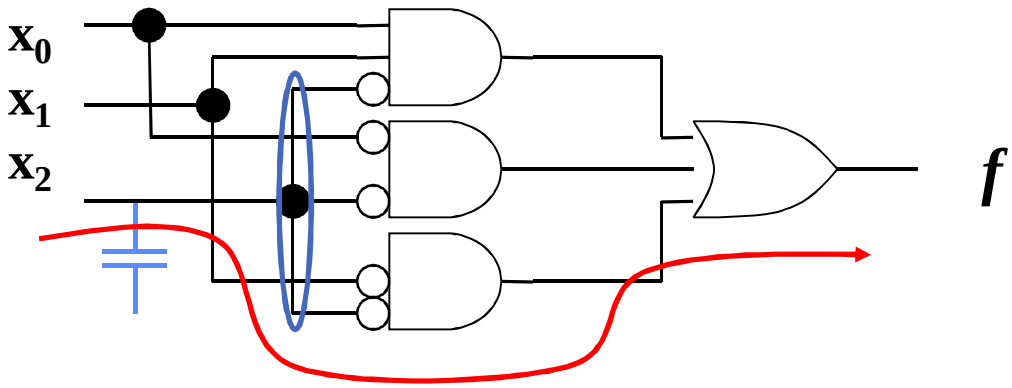
Critical Path (Longest path)

$$f = \Sigma m\,(3,2,0) = \overline{x}_2 x_1 x_0 + \overline{x}_2 x_1 \overline{x}_0 + \overline{x}_2 \overline{x}_1 \overline{x}_0$$



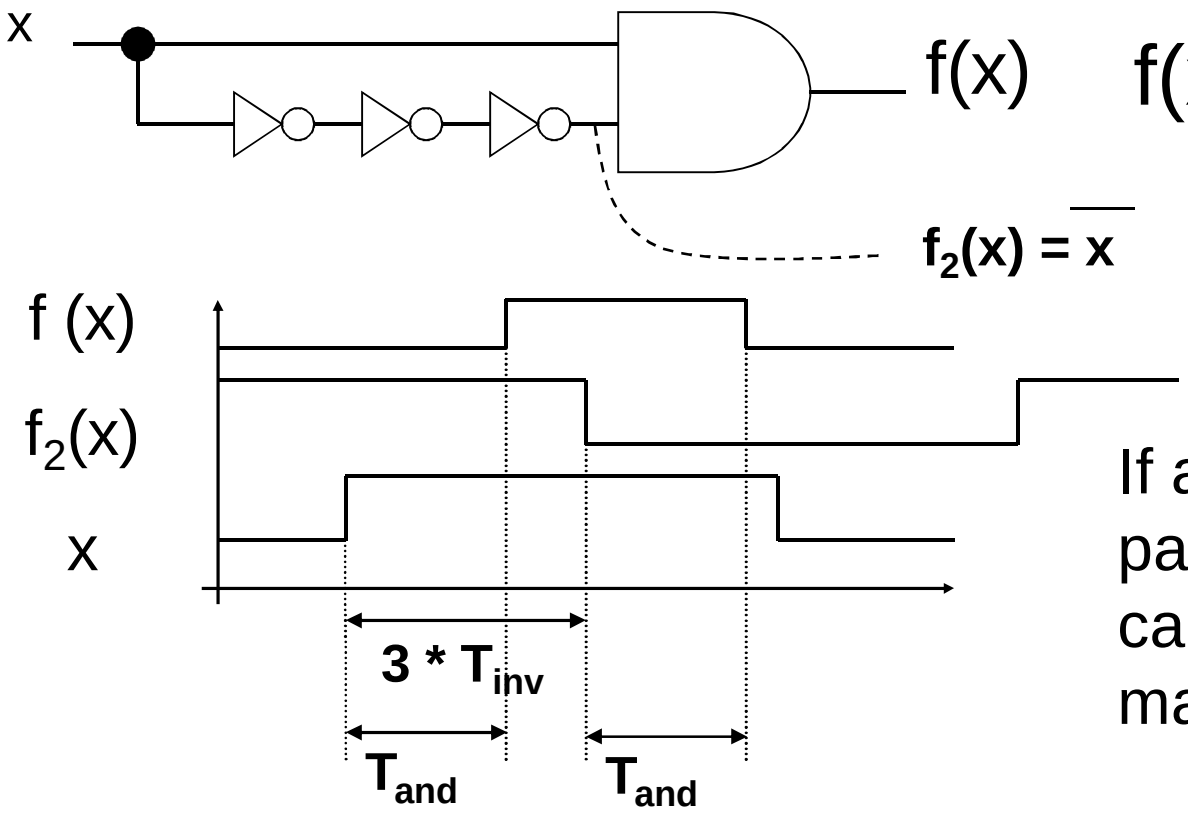
Critical Path (cont'd.)

$$f = x_0 x_1 \boxed{\bar{x}_2} + \bar{x}_0 \boxed{\bar{x}_2} + \bar{x}_1 \boxed{\bar{x}_2}$$



x_0 x_1 x_2 all pass NOT , AND, and OR, On their way to the output *f*, but x_2 has the load of *three* inputs (it is two for x_0 and x_1). "Critical path" becomes from x_2 to f!

Signal Racing



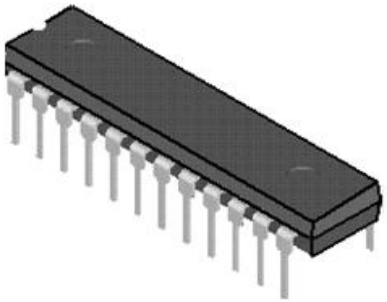
$$f(x) = x \overline{\overline{x}} = x \overline{x} = 0$$

If a signal has several paths to the exit, so called *signal racing* may happen

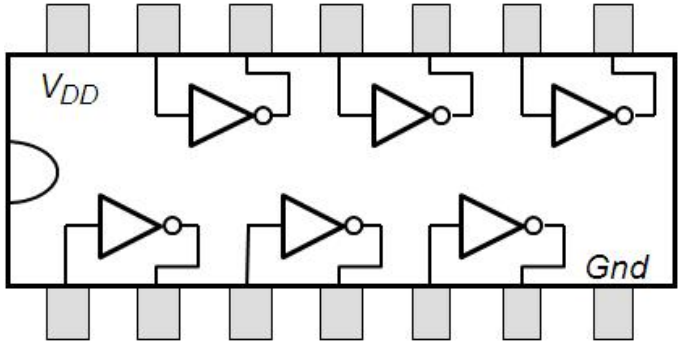
Power consumption of CMOS

- NMOS and PMOS circuits consume both static and dynamic power
  - Static power is dissipated by the current that flows in the steady state
  - Dymanic power is dissipated when the current flows because of changes in signal level
- CMOS circuits consume only dynamic power

7400 Series Standard Chips

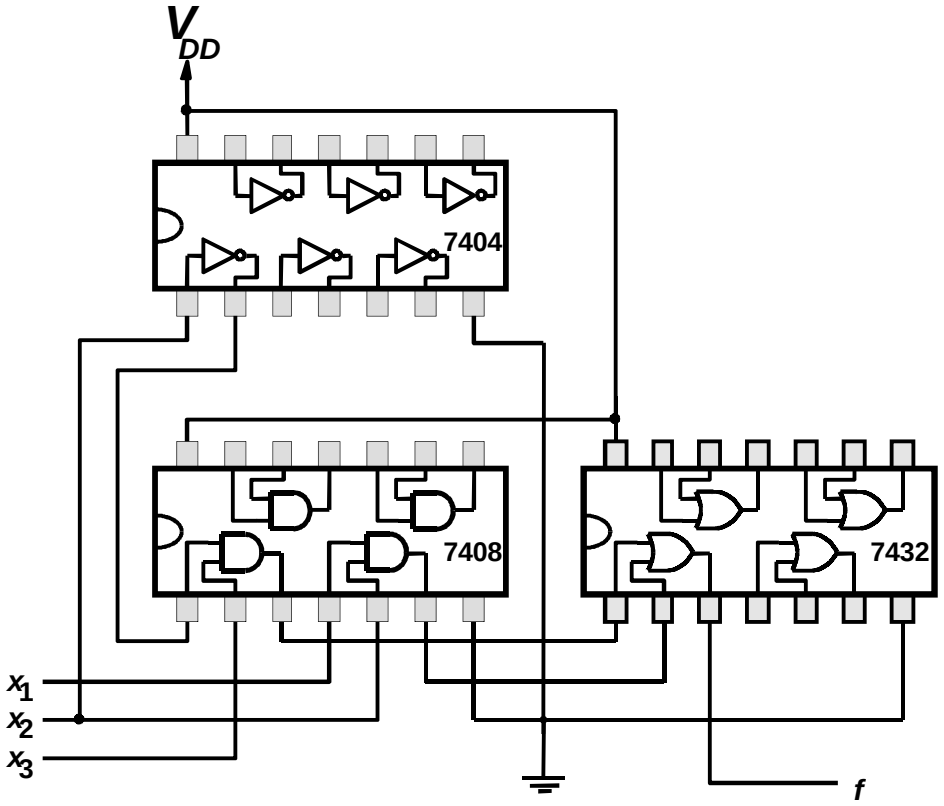


(a) Dual-inline package



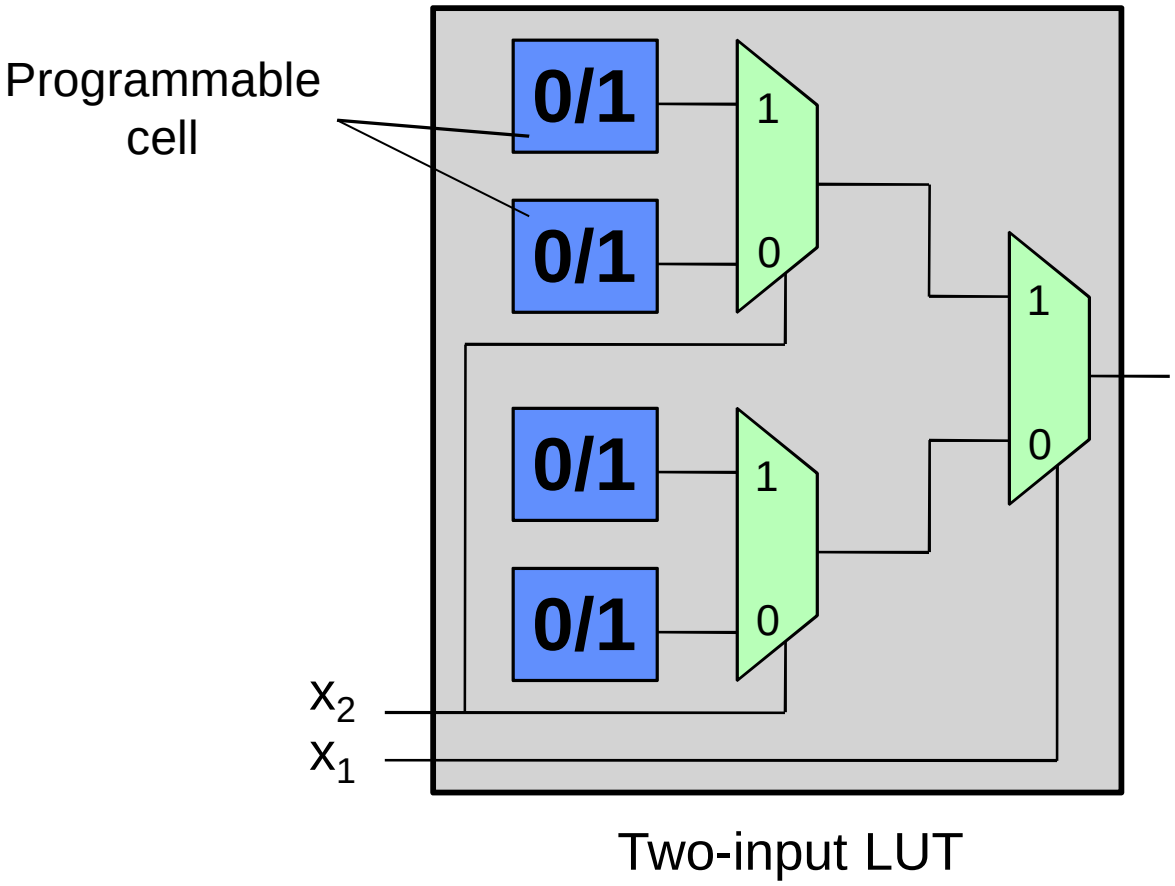
(b) Structure of 7404 chip

Implementation of a logic function



An implementation of $f = x_1x_2 + \overline{x}_2x_3$

Look-up tables (LUT)

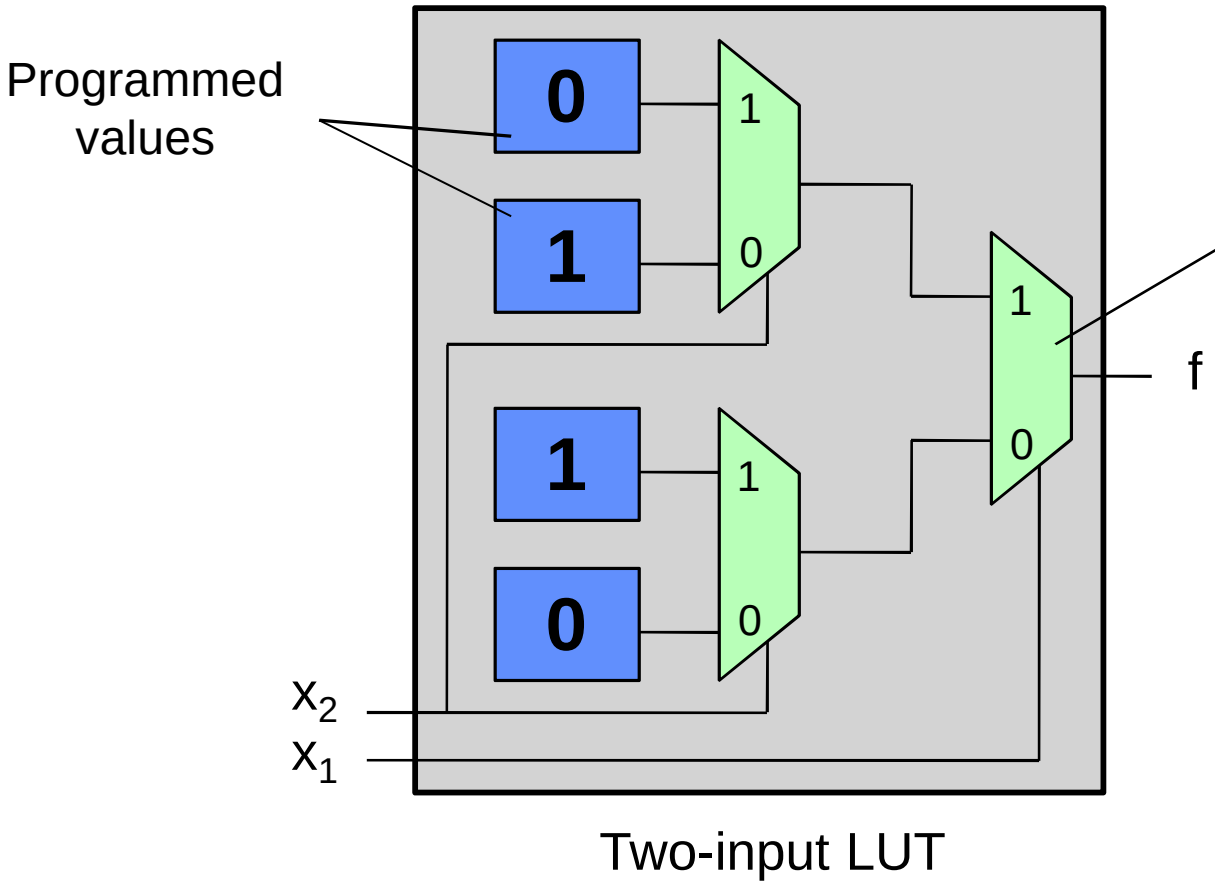


Two-input LUT

A LUT with *n* inputs can realize all combinational functions with up to *n* inputs

The usual size in an FPGA is $n = 4$

Example: XOR gate

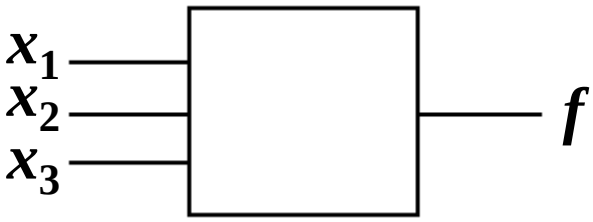


x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

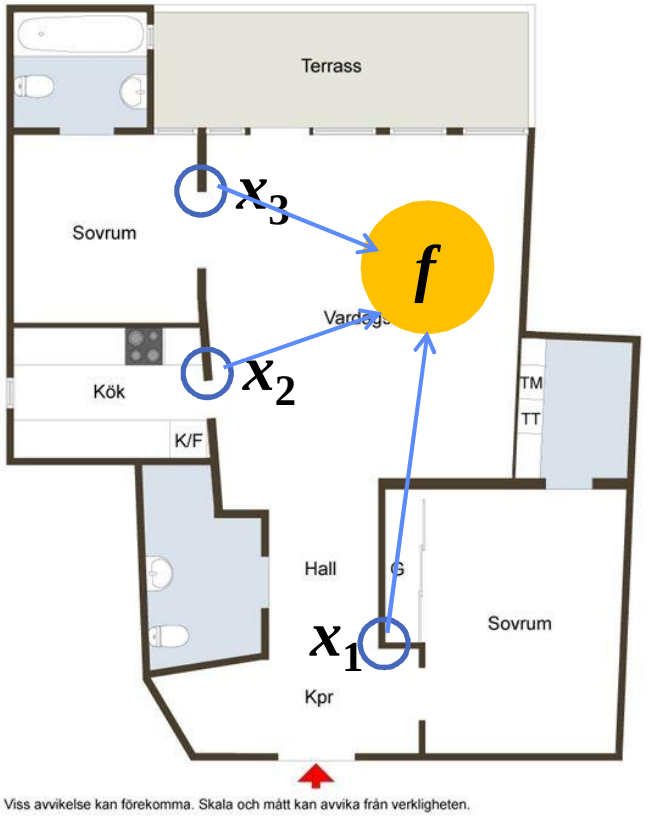
Three-way light control

Brown/Vranesic: 2.8.1

Suppose that we need to be able to turn on / off the lamp from three different places.

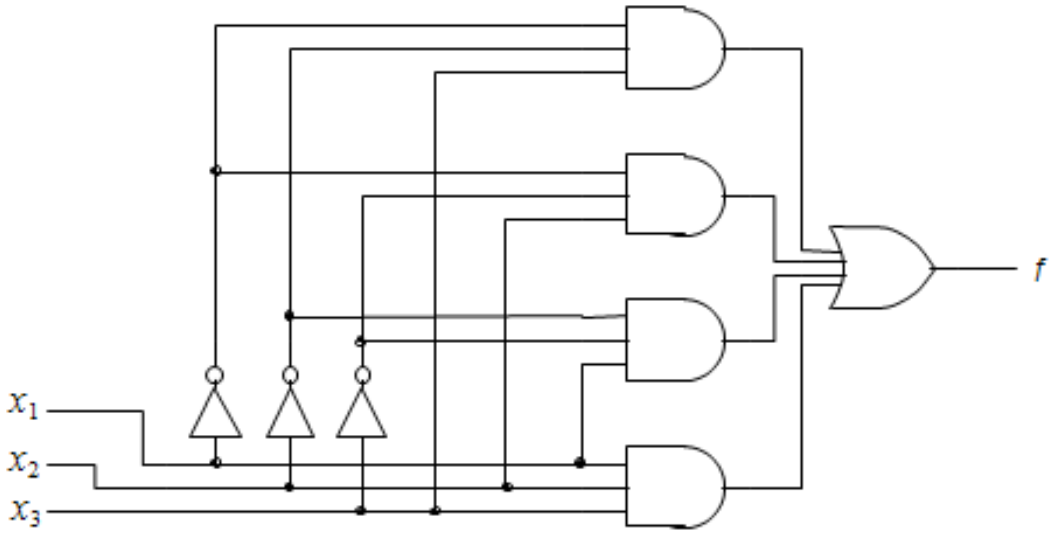


x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



Three-way light control

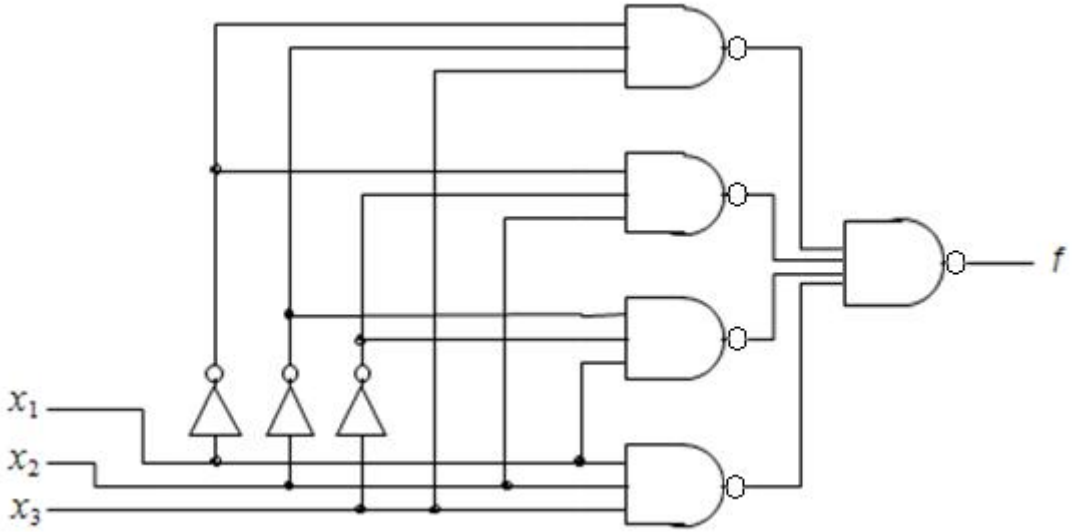
$$f = \sum m(1,2,4,7) = \bar{x}_1\bar{x}_2x_3 + \bar{x}_1x_2\bar{x}_3 + x_1\bar{x}_2\bar{x}_3 + x_1x_2x_3$$



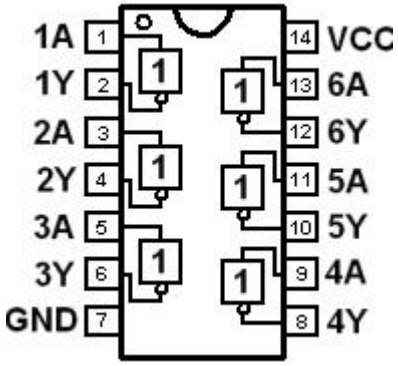
(a) Sum-of-products realization

NAND-NAND

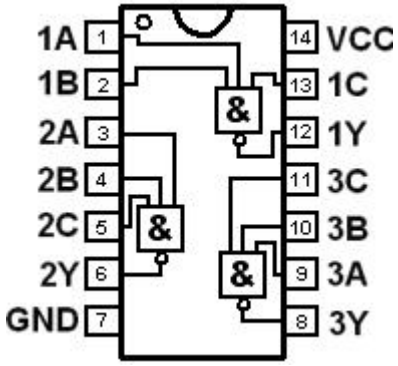
If we change to NAND-NAND all necessary gates are included with the simulator.



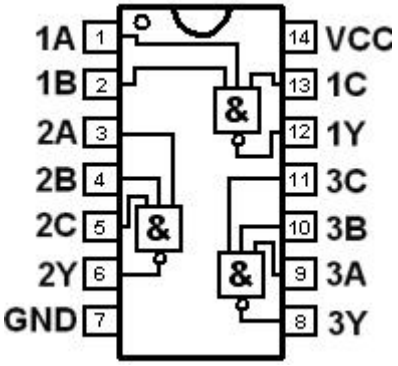
7404



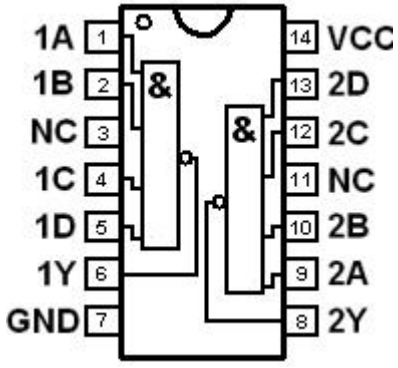
7410



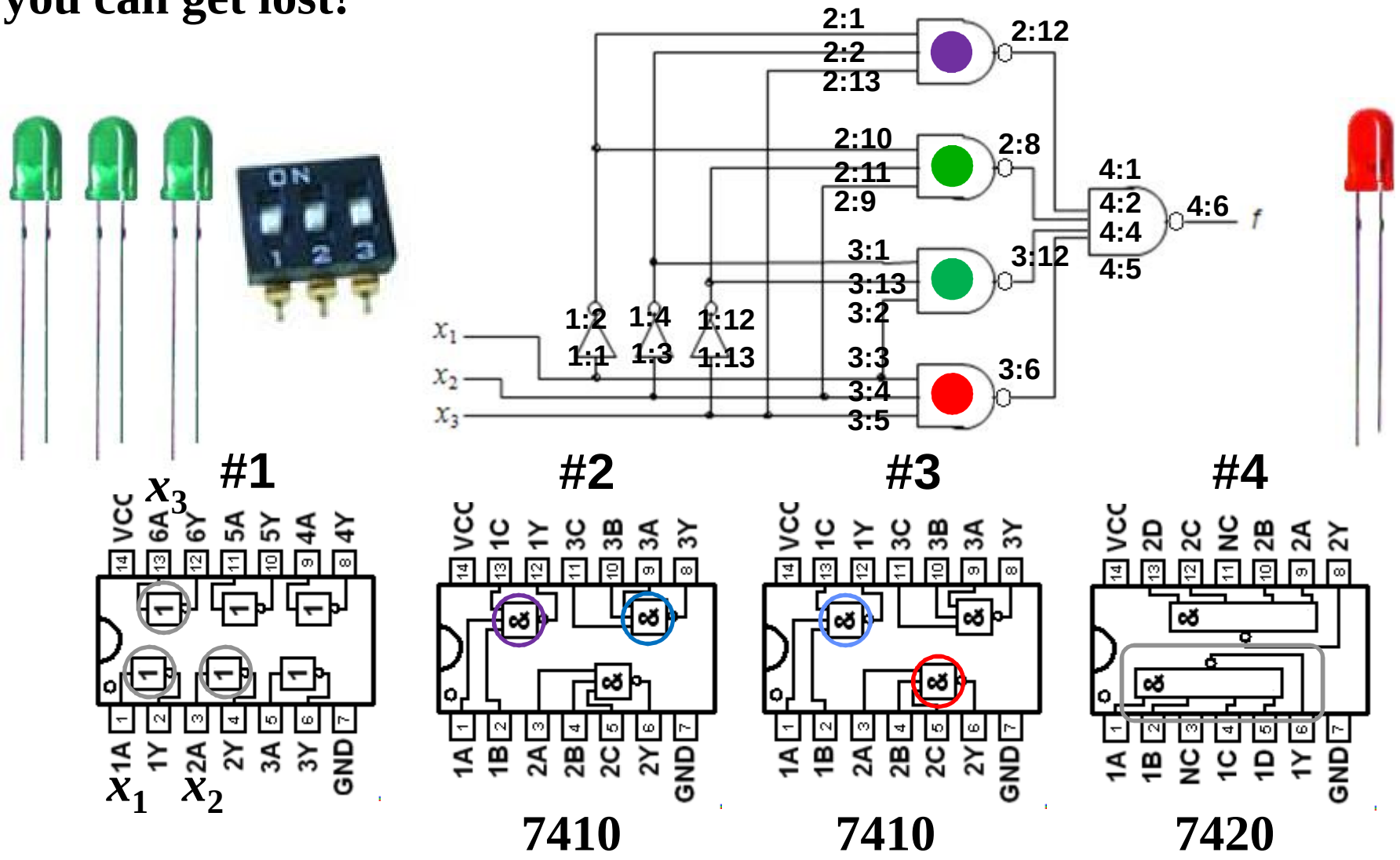
7410



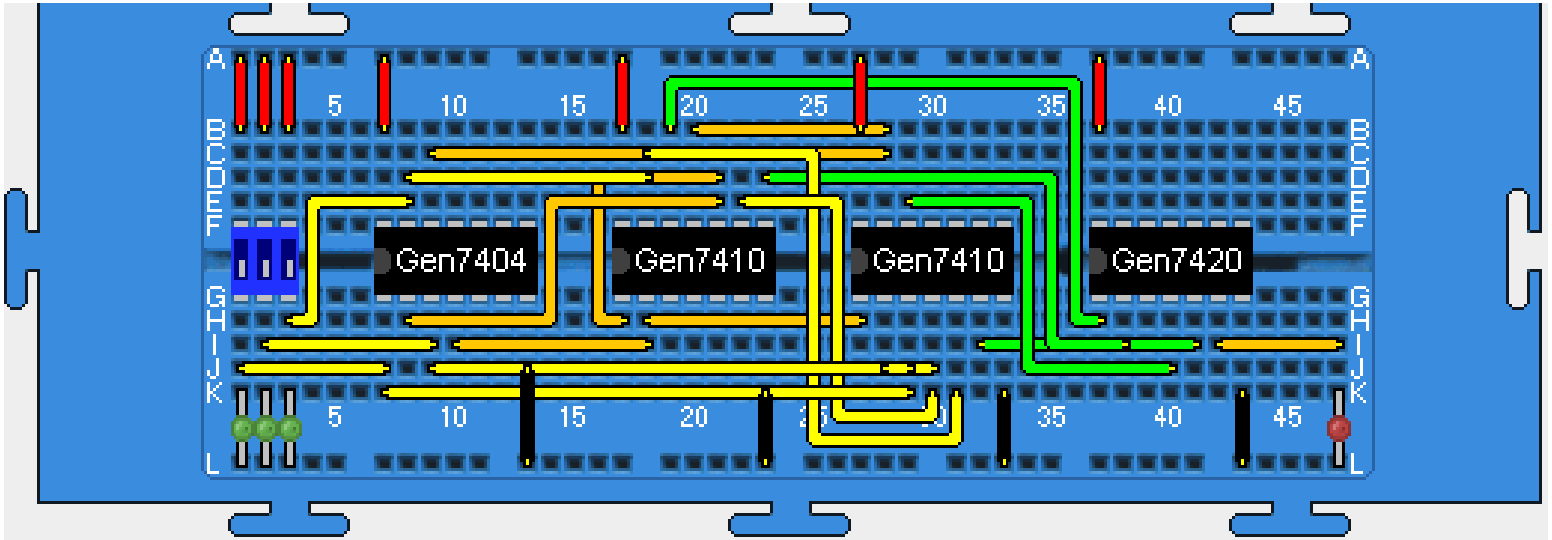
7420



You must enter the pin number in the schematic - otherwise you can get lost!



Simulate!


A
B
C
D
E
F
G
H
I
J
K
L
5
10
15
20
25
30
35
40
45
Gen7404
Gen7410
Gen7410
Gen7420

Make a guess!

How many transistors are inside an iPhone6?

2,000,000,000

What would the world be without the CMOS?!

Summary

- Logic gates can be implemented with CMOS technology
- Logic circuits have a delay
- CMOS circuits have relatively low power consumption