KTH Informations- och kommunikationsteknik

Written exam with solutions
IE1204-5 Digital Design
Friday 15/1 2016 14.00-18.00

General Information

Examiner: Ingo Sander.

Teacher: Kista, William Sandqvist tel 08-7904487
Teacher: Valhallavägen, Ahmed Hemani 08-790 4469

Exam text does not have to be returned when you hand in your writing.

Aids: No aids are allowed!
The exam consists of three parts with a total of 14 tasks, and a total of 30 points:

Part A1 (Analysis) containes ten short questions. Right answer will give you one point. Incorrect answer will give you zero points. The total number of points in Part A1 **is 10 points**. To **pass the Part A1 requires at least 6p**, *if fewer points we will not look at the rest of your exam.*

Part A2 (Methods) contains two method problems on a total of 10 points.

To **pass the exam** requires at least **11 points** from A1 + A2 , *if fewer points we will not look at the rest of your exam.*

Part B (Design problems) contains two design problems of a total of 10 points. Part B is corrected only if there are at **least 11p** from the exam A- Part.

NOTE ! At the end of the exam text there is a submission sheet for Part A1, which shall be separated and be submitted together with the solutions for A2 and B.

For a passing grade (**E**) requires at **least 11 points on the exam**. If exactly 10p from A1(6p)+A2(4p), (FX), completion to (E) will be offered.

Grades are given as follows:

0 –	11 –	16 –	19 –	22 –	25
F	E	D	C	B	A

The result is expected to be announced before Friday 15/2 2016.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p
A function *f*(x, y, z) is described by the expression:

$f(x,y,z) = z(\overline{x \oplus y}) + \bar{z}$

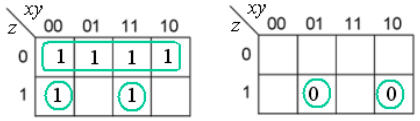
Write down the function maxterms, give the function as a product of sums.

$f(x,y,z) = \{PoS\} = ?$

---

1. Proposed solution.

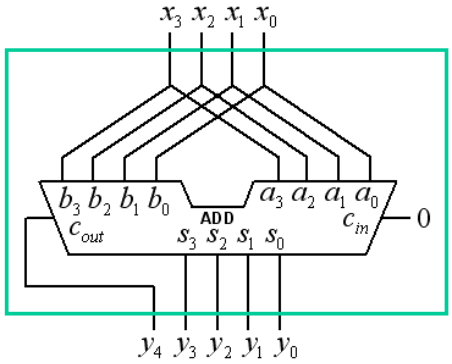
$f(x,y,z) = z \cdot (xy + \bar{x}\bar{y}) + \bar{z} = xyz + \bar{x}\bar{y}z + \bar{z}$

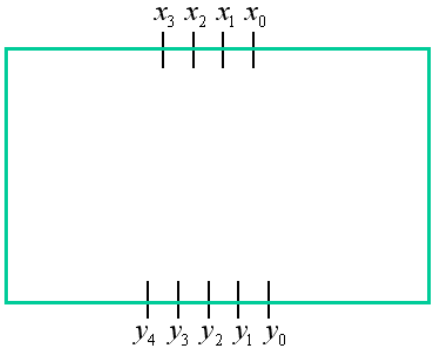


$f(x,y,z)_{PoS} = (\bar{z} + y + \bar{x})(\bar{z} + \bar{y} + x)$

---

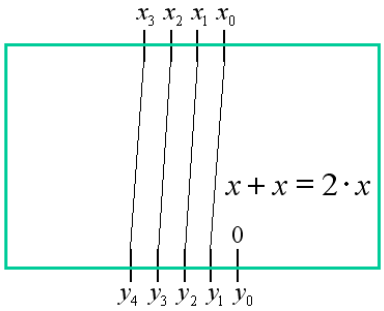
2. 1p/0p
A four bit unsigned integer x ($x_3x_2x_1x_0$) is connected to an 4-bit adder as in the figure. The result is a 5-bit number y ($y_4y_3y_2y_1y_0$). Draw the figure to the right how the same results can be obtained ***without using the adder***. There are also bits with the values 0 and 1 if needed. You will find a copy of the figure on the submission sheet.





---

2. Proposed solution.



---

3. 1p/0p
A two complement 4 bit number is x = 0101. Express $-x$ as a two complement 8 bit number. (Expanded to 8 bit). $-x$ = $?_2$

---

3. Proposed solution.
x = 0101 $-x$ = 1010+1=1011 1111**1011**

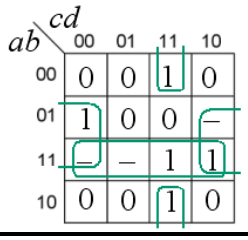
---

4. 1p/0p
Given is a Karnaugh map for a function of four variables $y = f(a, b, c, d)$.
Write the function as a minimized y_{min} sum of products, on **SoP** form.
"-" in the map means "don't care".

ab \ cd	00	01	11	10
00	0	0	1	0
01	1	0	0	–
11	–	–	1	1
10	0	0	1	0

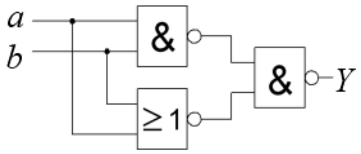
---

4. Proposed solution. $y = b\bar{d} + ab + \bar{b}cd$



---

5. 1p/0p
The figure bellow shows a circuit with two NAND gates and one NOR-gate. Simplify the function $Y = f(a, b)$ as much as possible.



---

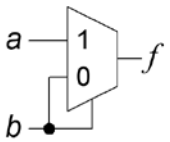
5. Proposed solution.

$$Y = \overline{\overline{a \cdot b} \cdot \overline{(a + b)}} = \{dM\} = \overline{\overline{a \cdot b}} + \overline{\overline{(a + b)}} = a \cdot b + a + b = a(b + 1) + b = a + b$$

---

6. 1p/0p
What logic function does this multiplexor circuit represent?

$f(b, a) = ?$

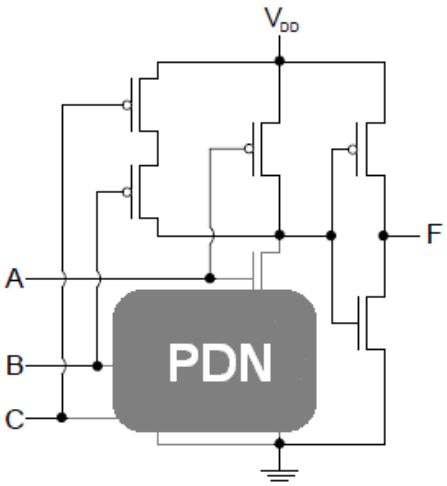


---

6. Proposed solution. $f(b, a) = b \cdot a + \bar{b} \cdot b = b \cdot a + 0 = b \cdot a$

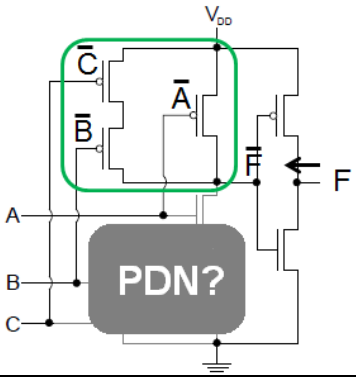
---

7. 1p/0p
Give an expression for the logical function realized by the CMOS circuit in the figure. One half of the circuit, the **P**ull **D**own **N**etwork, is hidden – but the circuit operation is still possible to determine with the help of the surviving parts.
Answer with sum of products, **SoP,** form. $F = f(A, B, C) = ?$



---

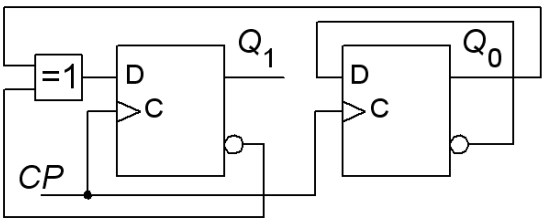
7. Proposed solution.



$$F = \overline{\overline{F}} = \overline{\overline{C} \cdot \overline{B} + \overline{A}} =$$
$$= \{dM\} = (C + B) \cdot A =$$
$$= AC + AB$$

---

8. 1p/0p



A synchronous counter starts in the state $Q_1Q_0 = 00$. Give the sequence of states for the following four clock pulses.

---

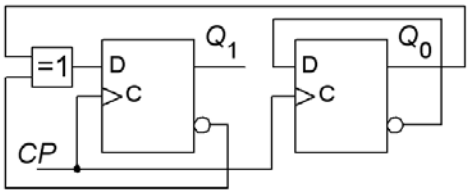
8. Proposed solution.

$Q_1^+ = Q_0 \oplus \overline{Q}_1 = \overline{Q_0 \oplus Q_1}$ (*equal*) $\quad Q_0^+ = \overline{Q}_0$ (*toggle*)

$Q_1^+ Q_0^+$: $\quad 00 \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00$

---

9. 1p/0p



For the flip-flops: setup time t_{su} = 4 ns, delay time for the flip-flop outputs t_{pdQ} = 3 ns. The XOR-gate has delay time t_{pdXOR} = 5 ns.

- How long does it needs to be between the clock pulses T_{CP} > ?, for the counter function to be safe?
- What value must the hold time have t_h for this circuit to work? t_h < ? ns.

---

9. Proposed solution.

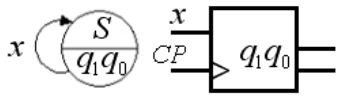
The clock period is determined by the longest path, the one with the XOR-gate.
$T_{CP} > t_{pdQ} + t_{su} + t_{pdXOR}$ = 3+4+5 = **12 ns**. Hold time is the time the data input must be stable after the clock edge. The flip-flop that has its *D*-input directly connected to the $\overline{Q}_0$ will get it's D-input changed first, directly after t_{pdQ} = 3 ns. t_h < **3 ns**.

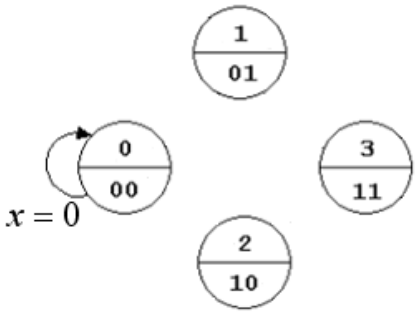
---

10. 1p/0p

Below is the VHDL code for a "**next state decoder**" for a Moore machine. To the right is an initiated state diagram. Finish the state diagram so that it complies with the VHDL code. The same figure is also on the submission sheet.

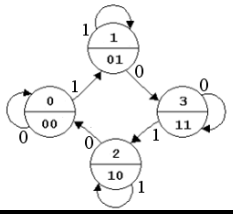
```
begin
next_state_decode:
process ( present_state, x )
begin
 if x = '1' then
   case present_state is
     when 0 => next_state <= 1;
     when 1 => next_state <= 1;
     when 3 => next_state <= 2;
     when 2 => next_state <= 2;
   end case;
else -- I = '0'
   case present_state is
     when 0 => next_state <= 0;
     when 1 => next_state <= 3
     when 3 => next_state <= 3;
     when 2 => next_state <= 0;
   end case;
 end if ;
end process ;
```





---

10. Proposed solution.



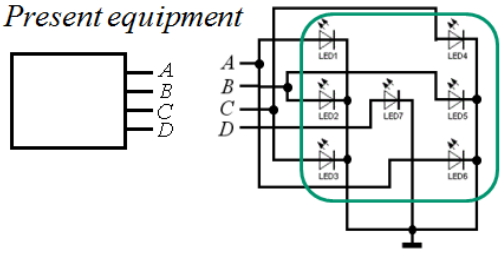
Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 (≥6p)

11. 4p

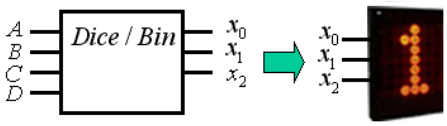
A display for an electronic dice consists of seven LEDs that are controlled by four signals A B C D. A B and C turns two LEDs on, while D turns one on.
(A=1 B=C=D=0 ⇒ "2")
The display shows the usual dot patterns of dice. (See the figure for the details).
One would now also be able to show the dice outcomes on a digital number display. The display uses the standard binary code for the digits.
You should construct a code converter (the circuit Dice/Bin) from **ABCD** to **binary code** $x_2x_1x_0$ for digits 1, 2, 3, 4, 5, 6.
Assume that nothing more than the usual dice dot patterns above occurs – use Don't Care.

Present equipment



Code converter for digit presentation

$ABCD \rightarrow x_2x_1x_0$



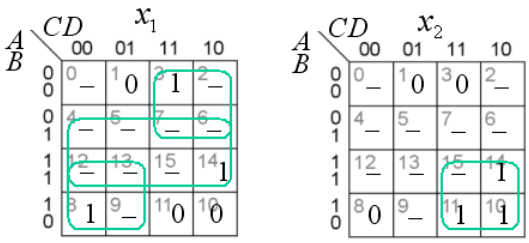
a) (1p) Set up the connection between ABCD and $x_2x_1x_0$ as a table (some kind of truth table).
b) (2p) Draw the karnaugh maps for the three bits of the binary-code and derive **minimized expressions** for x_2 x_1 x_0 on **SoP** form. Exploit don't care. (Possibly inspection of the table can directly provide one of the expressions).
c) (1p) Draw the schematic of the Dice/Bin code converter using optional types of gates.

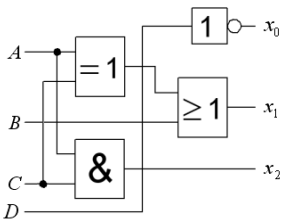
---

11. Proposed solution.

		$ABCD$	$x_2x_1x_0$	
	–	– – – –	– – –	–
•	1	0001	001	1
⁘	8	1000	010	2
⁙	3	0011	011	3
⁛	10	1010	100	4
⁜	11	1011	101	5
⁝	14	1110	110	6
	–	– – – –	– – –	–

Inspection of table gives: $x_0 = D$

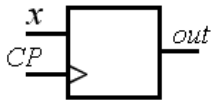




$x_0 = D \quad x_2 = AC$

$x_1 = B + A\overline{C} + \overline{A}C = B + A \oplus C$

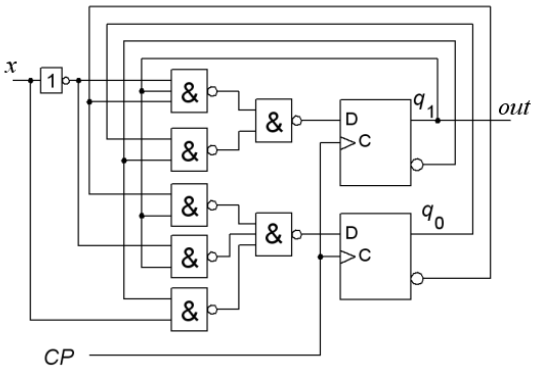
12. 6p



A synchronous sequential circuit, a Moore machine, has an input signal *x* and an output signal *out*. The circuit diagram is shown at right in the figure below.

a) (2p) Analyse the circuit and derive the **next state functions**

$q_1^+ = f(q_1 q_0, x) \quad q_0^+ = f(q_1 q_0, x)$



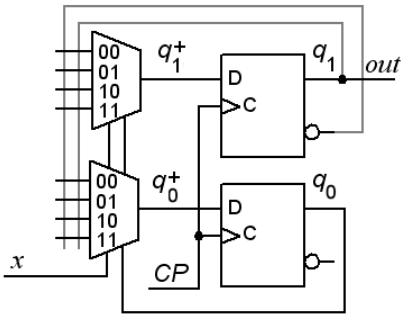
b) (2p) Set up the **coded state table**

$q_1^+ q_0^+ = f(q_1 q_0, x)$

and draw the **state diagram**.

c) (2p) Redesign the circuit, maintaining the function so that it uses **two 4:1 multiplexers** to the functions:

$q_1^+ = f(q_1 q_0, x) \quad q_0^+ = f(q_1 q_0, x)$



You should indicate what is to be connected to multiplexers data inputs. See the figure to the right.

$q_1^+ : mux_{00} = ?, mux_{01} = ?, mux_{10} = ?, mux_{11} = ?$

$q_0^+ : mux_{00} = ?, mux_{01} = ?, mux_{10} = ?, mux_{11} = ?$

---

12. Proposed solution a) $q_1^+ = \bar{x} q_1 \bar{q}_0 + \bar{q}_1 q_0 \quad q_0^+ = q_1 \bar{q}_0 + \bar{x} q_1 + x \bar{q}_1$

b)

q_1q_0	0	x	1
00	0		0
01	1		1
11	0		0
10	1		0

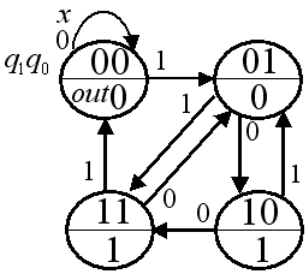
q_1^+

q_1q_0	0	x	1
00	0		1
01	0		1
11	1		0
10	1		1

q_0^+

state q_1q_0	next 0	next x	next 1	out
00	00		01	0
01	10		11	0
11	01		00	1
10	11		01	1

$q_1^+ q_0^+$



c) Multiplexers are using the select variables *x* and q_0 so therefore we change the variable order of the encoded state table.

$q_1 q_0\, x \rightarrow x q_0\, q_1$

Thereafter the mux data are given directly from tables.

$q_1^+ : mux_{00} = q_1, mux_{01} = \bar{q}_1, mux_{10} = 0, mux_{11} = \bar{q}_1$

$q_0^+ : mux_{00} = q_1, mux_{01} = q_1, mux_{10} = 1, mux_{11} = \bar{q}_1$

$q_1 q_0\, x \rightarrow x q_0\, q_1$

xq_0	0	q_1	1
00	00		11
01	10		01
11	11		00
10	01		01

$q_1^+ q_0^+$

xq_0	0	q_1	1	
00	0		1	$= q_1$
01	1		0	$= \bar{q}_1$
11	1		0	$= \bar{q}_1$
10	0		0	$= 0$

q_1^+

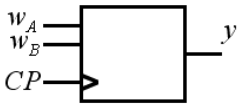
xq_0	0	q_1	1	
00	0		1	$= q_1$
01	0		1	$= q_1$
11	1		0	$= \bar{q}_1$
10	1		1	$= 1$

q_0^+

Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 (≥11p).

13. 6p Synchronous sequential circuit. Trafic control.



a) (2p) State minimize the state table to the right (*a*,*b*,*c*,*d*,*e*,*f*,*g*,*h*). Then draw the minimal state diagram.

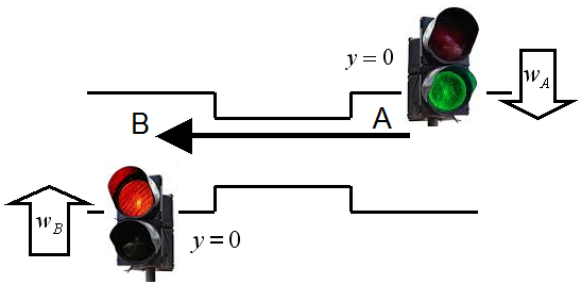
(To resolve this independent task may well prove to be a good use of time for the solving the rest of the task!)

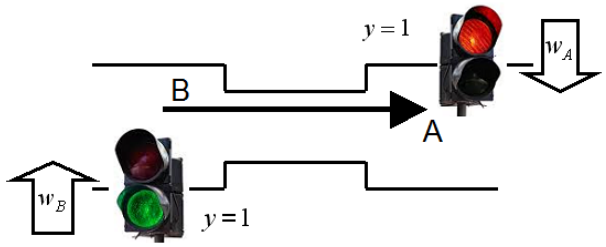
state	input w_Aw_B 00	01	11	10	
a	*c*	*f*	*c*	*f*	1
b	*b*	*b*	*a*	*c*	1
c	*c*	*g*	*d*	*c*	0
d	*g*	*b*	*b*	*b*	0

next state

state	input w_Aw_B 00	01	11	10	y
e	*g*	*g*	*b*	*b*	0
f	*f*	*b*	*e*	*f*	0
g	*g*	*g*	*h*	*f*	1
h	*f*	*f*	*c*	*f*	1

next state





At roadworks when forced to make a path so narrow that only cars in one direction at a time can pass, usually putting up traffic signals. You will design a synchronous sequential circuit, in the form of a positive edge-triggered Moore machine with D flip-flops for controlling such a traffic signal.

The sequential circuit has an output signal y that controls the trafic signals so that if $y = 0$ trafic in the direction A→B is let through, and when $y = 1$ trafic in the direction B→A (thus always only traffic in one direction).

The sequential circuit has two input signals w_A and w_B from sensors that indicates when/if there are vehicles (w=1) in directions A or B. Clock pulses will be every ten seconds.

Specification:
- alone car has red light → y = change
- alone car has green light → y = same
- cars from both directions → y = same, but change after the next clock edge (queue mode)
- no cars → y = same

(*Hint, four states are required*)

b) (2p) Derive the circuit **state table** and draw the **state diagram**.

c) (2p) Use binary code to encode the states and derive the **encoded state table**. Derive the minimized expressions for **next state** and for the **output**.

(*Wonder what the traffic safety administration would say about this traffic signal*?)

13. Proposed solution.

a)

$(abgh)(cdef)$

$a_{00} \to (\mathbf{c}def)\ a_{01} \to (cde\mathbf{f})\ a_{11} \to (\mathbf{c}def)\ a_{10} \to (cde\mathbf{f})$

$b_{00} \to (a\mathbf{b}gh)\ b_{01} \to (a\mathbf{b}gh)\ b_{11} \to (\mathbf{a}bgh)\ b_{10} \to (\mathbf{c}def)$

$g_{00} \to (ab\mathbf{g}h)\ g_{01} \to (ab\mathbf{g}h)\ g_{11} \to (abg\mathbf{h})\ g_{10} \to (cde\mathbf{f})$

$h_{00} \to (cde\mathbf{f})\ h_{01} \to (cde\mathbf{f})\ h_{11} \to (\mathbf{c}def)\ h_{10} \to (cde\mathbf{f})$

$(ah)(bg)(cdef)$

$(ah)(bg)(cdef)$

$c_{00} \to (\mathbf{c}def)\ c_{01} \to (b\mathbf{g})\ c_{11} \to (\mathbf{c}def)\ c_{10} \to (\mathbf{c}def)$

$d_{00} \to (b\mathbf{g})\ d_{01} \to (b\mathbf{g})\ d_{11} \to (b\mathbf{g})\ d_{10} \to (b\mathbf{g})$

$e_{00} \to (b\mathbf{g})\ e_{01} \to (b\mathbf{g})\ e_{11} \to (b\mathbf{g})\ e_{10} \to (b\mathbf{g})$

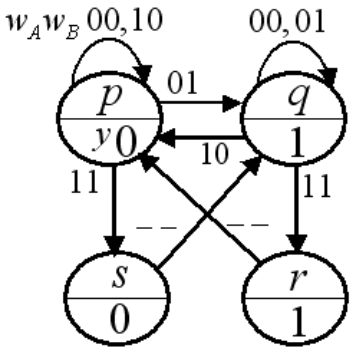
$f_{00} \to (cde\mathbf{f})\ f_{01} \to (b\mathbf{g})\ f_{11} \to (cde\mathbf{f})\ f_{10} \to (cde\mathbf{f})$

$(ah)(bg)(cf)(de)$ *other names* $(r)(q)(p)(s)$

b) **c**)

w_Aw_B	y		
00	0	$\to$	$y=0$
00	1	$\to$	$y=1$
01	0	$\to$	$y=1$
01	1	$\to$	$y=1$
10	0	$\to$	$y=0$
10	1	$\to$	$y=0$
11	0	$\to$	$y=0 \to y=1$
11	1	$\to$	$y=1 \to y=0$

	w_Aw_B 00	01	11	10	y
p	p	q	s	p	0
q	q	q	r	p	1
r	p	p	p	p	1
s	q	q	q	q	0



q_1q_0	w_Aw_B 00	01	11	10	y
00	00	01	11	00	0
01	01	01	10	00	1
11	01	01	01	01	0
10	00	00	00	00	1

$q_1^+q_0^+$

q_1q_0	w_Aw_B 00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	0	0
10	0	0	0	0

q_1^+

q_1q_0	w_Aw_B 00	01	11	10
00	0	1	1	0
01	1	1	0	0
11	1	1	1	1
10	0	0	0	0

q_0^+

q_1q_0 : $p:00\ q:01\ r:10\ s:11$

$y = \bar{q}_1q_0 + q_1\bar{q}_0 = q_1 \oplus q_0$

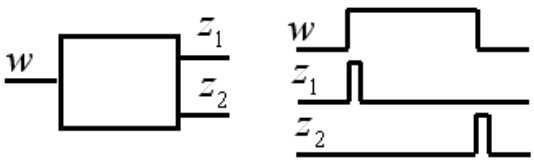
$q_1^+ = q_0w_Aw_B$

$q_0^+ = q_0\bar{w}_A + q_1q_0 + \bar{q}_1\bar{q}_0w_B$

---

14. 4p Edge detection.

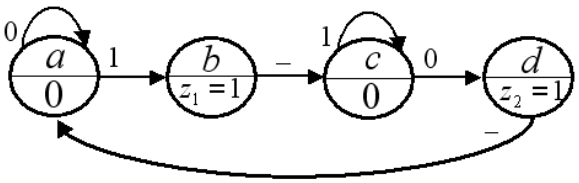
A asynchronous sequential circuit has one input w and two outputs z_1 and z_2. When the input w has a positive edge z_1 will indicate this with a short pulse (with the duration of a state transition). When the input has a negative edge this will in the same way be indicated with a short pulse on output z_2. See the figure.



a) Set up a proper **flow table** for the sequence circuit. Draw the **state diagram**.

b) Do a suitable **state assignement** with an exitation table which gives a circuit that is **free of critical race**. You should also derive **hazard free expressions** for the next state and an **expression for output**, and draw the **circuit diagrams** with optional gates.

13. Proposed solution.



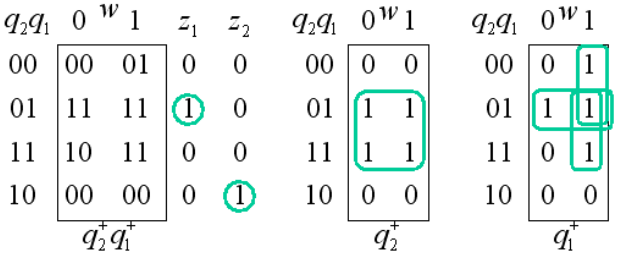
a:00 *b*:01 *c*:11 *d*:10

Gray code gives the states hamming distance 1

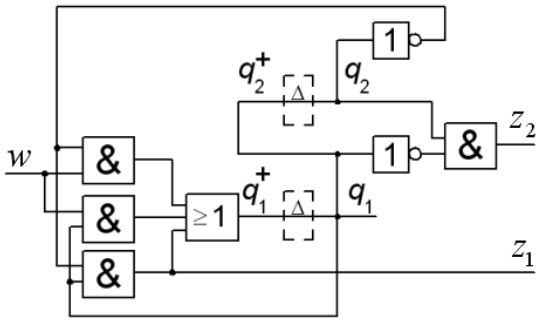
$z_1 = \bar{q}_2 q_1 \quad z_2 = q_2 \bar{q}_1$

$q_2^+ = q_1$

$q_1^+ = w\bar{q}_2 + wq_1 + \bar{q}_2 q_1$



Extra hazard cover is not needed



Hope all went well!

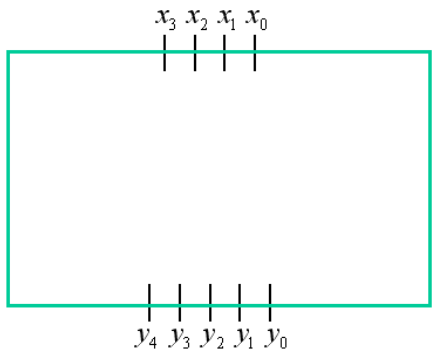
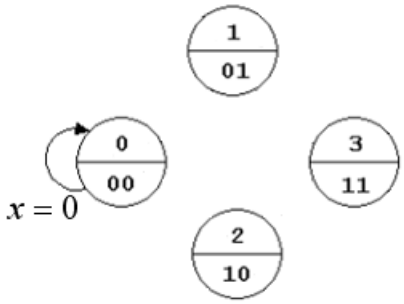
Submission sheet for Part A1 Sheet 1

(remove and hand in together with your answers for part A2 and part B)

Last name: _____ **Given name:** _____

Personal code: _____ **Sheet:** **1**

Write down your answers for the questions from Part A1 (1 to 10)

Question	Answer		
1	$f(x,y,z) = \{PoS\} = ?$		
2		**3**	-x = ? (8 bit 2-complement)
4	$f(a,b,c,d) = \{SoP\}_{\min} = ?$	**5**	$Y = f(a,b) = ?$
6	$f(b,a) = ?$	**7**	$Y = f(A,B,C) = ?$
8	$Q_1^+ Q_0^+$: 00 →		
9	T_{CP} > ? [ns]		t_h < ? [ns]
10			

This table is completed by the examiner!!

Part A1 (10)	**Part A2** (10)		**Part B** (10)		**Total** (30)	
Points	11	12	13	14	Sum	Grade