Written Re-exam with solutions for
IE1204/5 Digital Design
Friday 10/4 2015 8.00-12.00

General Information
Examiner: Ingo Sander.
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Exam text does not have to be returned when you hand in your writing.

Aids: No aids are allowed!
The exam consists of three parts with a total of 12 tasks, and a total of 30 points:

Part A1 (Analysis) contains eight short questions. Right answer will for six of the questions give you one point and for two of the questions one or two points. Incorrect answer will give you zero points. The total number of points in Part A1 is **10 points**. To pass the Part A1 requires at least **6p**, if fewer points we will not look at the rest of your exam.

Part A2 (Methods) contains two method problems on a total of 10 points.

To pass the exam requires at least **11 points** from A1 + A2, if fewer points we will not look at the rest of your exam.

Part B (Design problems) contains two design problems of a total of 10 points. Part B is corrected only if there are at least **11p** from the exam A-Part.

**NOTE**! At the end of the exam text there is a submission sheet for Part A1, which can be separated to be submitted together with the solutions for A2 and B.

For a passing grade (E) requires at least **11 points on the exam**.

Grades are given as follows:

<table>
<thead>
<tr>
<th></th>
<th>0 –</th>
<th>11 –</th>
<th>16 –</th>
<th>19 –</th>
<th>22 –</th>
<th>25</th>
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<tbody>
<tr>
<td></td>
<td>F</td>
<td>E</td>
<td>D</td>
<td>C</td>
<td>B</td>
<td>A</td>
</tr>
</tbody>
</table>

The result is expected to be announced before Monday 4/5 2015.
Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p
A function \( f(x, y, z) \) is described by the equation:
\[
f(x, y, z) = \overline{xy}z + yz + \overline{xyz} + \overline{xy}z
\]
Minimize the function.
\( f(x, y, z)_{\text{min}} = ? \)

1. Proposed solution
\[
f(x, y, z) = \overline{x}y\overline{z} + \overline{y}z + \overline{x}y\overline{z} + \overline{y}z = \{Kmap\} = \overline{y} + \overline{x}z
\]

2. 2p/1p/0p
When the numbers 0 ... 9 are coded with the usual 4 bit binary code it is called BCD code (binary code for 10 ... 15 are not included in the BCD code). Sometimes, a 4-bit code in which the BCD code words is reduced by 3, the so-called "excess-3 code", XS3, is used.
\[
(y_3y_2y_1y_0)_{\text{XS3}} = (x_3x_2x_1x_0)_{\text{BCD}} - 3_{10}
\]

a) Use a four-bit adder and, if necessary inverters to make a BCD→XS3 coder. The subtraction should be done with the two complement method. The constants 0 and 1 are available. Draw your solution in the figure on the answer sheet.

b) What binary XS3 code has the BCD number 9?

2. Proposed solution

a) \(-3=1101\).

b) BCD 9 is 1001. XS3 code gets \(1001 - 0011 = 0110\).
3. 1p/0p
Given is a Karnaugh map for a function of four variables \( y = f(x_3, x_2, x_1, x_0) \).
Write the function as a **minimized** sum of products, SP form. “-” in the map means “don’t care”.

\[
x_3x_2x_1x_0 & 00 & 01 & 11 & 10 \\
00 & 1 & 1 & 3 & 0 \\
01 & 1 & 0 & 7 & - \\
11 & 1 & 3 & - & 6 \\
10 & 1 & 1 & 1 & 0 \\
\]

3. Proposed solution

\[
x_3x_2x_1x_0 & 00 & 01 & 11 & 10 \\
00 & 1 & 1 & 3 & 0 \\
01 & 1 & 0 & 7 & - \\
11 & 1 & 3 & - & 6 \\
10 & 1 & 1 & 1 & 0 \\
\]

\[\neg x_0 + \neg x_2x_1 + x_3x_2x_1\]

4. 2p/1p/0p
The figure shows a circuit consisting of three gates.

\[
a \quad =1 \quad \& \quad =1 \quad f \\
\begin{align*}
  a & b & A & B & f \\
  0 & 0 & 0 & 1 & 0 \\
  0 & 1 & 1 & 1 & 1 \\
  1 & 0 & 1 & 0 & 0 \\
  1 & 1 & 0 & 1 & 0 \\
\end{align*}
\]

b) \( f = a \cdot (a \oplus b) \oplus (a \oplus b) \)
\( f = \neg a \cdot b \)
5. 1p/0p
Give an expression for the logical function realized by the CMOS circuit in the figure? Only the "pull-down" circuit appears, the "pull-up" circuit is symbolized by the square at the top of the figure.

5. Proposed solution
Pull Down circuit gives inverted function.
\[ \overline{V_{OUT}} = A \cdot (B + C) \quad V_{OUT} = \overline{A \cdot (B + C)} = \{dM\} = \overline{A} + (B + C) = \overline{A} + \overline{B} \overline{C} \]

6. 1p/0p
This sequence circuit consists of a T-flip-flop and a D-flip-flop, it starts in the state \(q_1q_0 \ 00\). Analyze the circuit and give the sequence for the following three clock pulses.

6. Proposed solution
\[ q_1^+ = T \cdot \overline{q_1} + \overline{T} \cdot q_1 \quad T = q_0 \quad \Rightarrow \quad q_1^+ = q_0 \cdot \overline{q_1} + q_0 \cdot q_1 = q_0 \overline{q_1} + q_0q_1 = q_0 \oplus q_1 \]
\[ q_0^+ = q_1 \]

\begin{array}{c|c|c|c|c}
   CP & q_1 & q_0 & \overline{q_0} & q_1^+\\
   \hline
   00 & 1 & 10 \\
   10 & 0 & 01 & 00 \rightarrow 10 \rightarrow 01 \rightarrow 00 \ldots \\
   01 & 0 & 00 \\
   00 & 1 & 10 \\
\end{array}
7. 1p/0p
The figure shows a type of asynchronous latch. It’s called the Earle latch (but it is not included in the course materials). Derive the circuit’s characteristic function.

\[ q^+ = f(q,e,d) = ? \]

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7. Proposed solution

\[ q^+ = f(q,e,d) = (e \cdot d) \cdot (q \cdot \overline{d}) \cdot (e \cdot \overline{q}) = \{dM\} = ed + qd + eq \]

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8. 1p/0p
The following is the VHDL code for a 2:1 MUX. Unfortunately, some of the code has fallen away, this is marked by ( ??? ?? )
Answer with making the line of code complete!

**ENTITY** MUX_2_1 **IS**

**PORT**

\[ d_{\text{in}} : \text{IN} \quad \text{STD} \_\text{LOGIC} \_\text{VECTOR}(1 \ \text{downto} \ 0) ; \]

\[ a : \text{IN} \quad \text{STD} \_\text{LOGIC} ; \]

\[ d_{\text{out}} : \text{OUT} \quad \text{STD} \_\text{LOGIC} ; \]

**END** MUX_2_1 ;

**ARCHITECTURE** beh **OF** MUX_2_1 **IS**

**BEGIN**

\[ d_{\text{out}} <= ( \text{NOT} \ a \ \text{AND} \ d_{\text{in}} (0) ) \ \text{OR} \ ( \ ??? ?? ) ; \]

**END** beh ;

---

8. Proposed solution

\[ d_{\text{out}} <= ( \text{NOT} \ a \ \text{AND} \ d_{\text{in}} (0) ) \ \text{OR} \ ( a \ \text{AND} \ d_{\text{in}} (1) ) ; \]
Note! Part A2 will only be corrected if you have passed part A1 (≥6p).

9. 5p

The figure shows a punched tape with the Baudot code. Your task is to make a decoder for vowels (our Swedish vowels Å Ä Ö are not included) that provides the output $V = 1$ only when the code is corresponding to a vowel. Assume that the paper tape to read is edited so that only the English alphabet letters A ... Z are appearing (letters from the line "Lowercase"). No special characters (Car. Return, Line Feed, Ltrs ...) can occur. Consider Y as a vowel. Hole = 1, no hole = 0.

a) (1p) Enter the truth table $V = f(x_4, x_3, x_2, x_1, x_0)$, or directly as Karnaugh maps. Specify “do not care”. One code word is missing on the character strip - which one? - It could also be used as “do not care”.

b) (2p) Minimize the function $V$ and express it as a sum of products (SP). Use do not care.

c) (2p) In order to reduce the number of gates a multiplexer is used. Realize the function $V$ with a 4:1 MUX and a minimized number of optional gates. As select variables $x_4$ and $x_3$ should be used.

9. Proposed solution

a) $V = 1$ for
A(3), E(1), I(6), O(24), U(7), Y(21).

b) $V$ is don’t care for
BLANK(0), LF(2), CR(8), SP(4), LTRS(31), FIGS(27).

It is the code for BLANK, "no holes" 00000 that is missing on the character strip. That don’t care position is not utilized in this solution.

c) $V = \overline{x_4} \overline{x_3} \overline{x_2} + x_4 x_3 x_2 x_1 x_0 + x_4 x_3 x_2 \overline{x_1} \overline{x_0} + x_4 x_3 x_2 x_1 x_0$
A counter (a Moore-machine) counts Graycode up “→” 00 01 11 10 or down “←” 00 10 11 01. With two mode-signals \(a b\) (00 01 11 10) you control to which the state counter should count, and then remain in this state until \(a b\) are changed, then it should go to the new state. Choose to follow up/down sequence so that the desired state \(a b\) is reached after as few steps as possible – if the choice up/down does not imply any difference in the number of steps, then choose to follow the up “→” sequence.

\[
\begin{align*}
ab \quad 00,01,11,10 & \quad q_1q_0 \\
\end{align*}
\]

a) (1p) Finish the initiated state diagram. Map the condition for all state transitions.

b) (2p) Write state table based on the state diagram. \(q_1^+q_0^+ = f(q_1q_0, ab)\)

Derive minimized expressions for the next state. \(q_1^+ = f(q_1q_0, ab)\) \(q_0^+ = f(q_1q_0, ab)\)

c) (2p) Realize the next state decoder with two 4:1 multiplexers. The control signals \(a\) and \(b\) are connected to the multiplexers select inputs. Derive the minimized function expressions for the multiplexers data inputs. See the figure.

10. Proposed solution

a) b)
Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 (≥11p).

11. 5p Synchronous serial two-complementer.

a) (1p) A synchronous sequential circuits, a Moore machine, has the state diagram to the right. Minimize the number of states, set up the minimized state-table and draw the minimized state diagram. (This may very well prove to be time well spent before the subtask b).

b) (1p) The Rapid method for the two complement of a binary number means that, in the direction from the least significant bit to the most significant bit, all the bits including the leading 1 are copied and then all of the following bits are inverted.

A synchronous sequential circuit, a Moore machine, will at the input $i$ for each clock pulse, get the bits in this serial order. After each clock pulse the sequential circuit output $z$ will present the corresponding bit copied or inverted according to the rule. After each complete data word the circuit is cleared with the (asynchronous) reset. Derive the circuit’s state table and draw the state diagram.

(2p) Derive the coded state table (select the code yourself) and derive the minimized functions for next state and output.

(1p) Draw schematic it is free to use any type of gates together with the D-flip-flops which has asynchronous reset input.

11. Proposed solution

State encoding is free, except that $a$ must have the code 00 as we use asynchronous reset.
Asynchronous edge triggered pulse gate

An asynchronous sequential circuits has two inputs and one output. On one input there is a pulse train $p$, on the other input there is a slow signal $w$ (slow in comparison to $p$). As soon as possible after each rising edge of $w$, the output $z$ will "let through" the next complete pulse (one complete pulse) from $p$. Output $z$ is 0 all other times. See the figure's example.

Your answer must include a state diagram, if necessary minimized, a flow table, and an appropriate state assignment with an excitation table that gives race-free net. You must also develop the hazard-free expressions for the next state and an expression for the output, but you don’t need to draw the gate circuit.

Proposed solution

The states can be coded with the gray code. Two of the don’t care entries occur because the signal $w$ is slow and then always will be $w = 1$ during the pulses from $p$. The other two don’t care entries occur because input signals can have no double changes.

$$z = q_1q_0$$

Good Luck!
Submission sheet for Part A1  Sheet 1
( remove and hand in together with your answers for part A2 and part B )

Last Name: ___________________________ Given Name: ___________________________

Personal code number: ___________________________

Write down your answers for the questions from Part A1 (1 to 8)

<table>
<thead>
<tr>
<th>Question</th>
<th>Answer</th>
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<tbody>
<tr>
<td>1 1p</td>
<td>( f(x, y, z) = {SP}_{\text{min}} = ? )</td>
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</tbody>
</table>
| 2 1+1p a) | \( x_{BCD} = x_3 x_2 x_1 x_0 \) \[\begin{array}{cccc}
1 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 \\
0 & 0 & 1 & 1 \\
0 & 1 & 1 & 0 \\
0 & 1 & 1 & 1 \\
1 & 1 & 1 & 0 \\
1 & 1 & 1 & 1 \\
\end{array}\] |
| b) \( x_{BCD} = 9 \rightarrow y_{XS3} = ?_2 \) (answer with a binary number) |
| 3 1p     | \( y = f(x_3, x_2, x_1, x_0) = \{SP\}_{\text{min}} = ? \) |
| 4 1+1p a) | Truth table \[\begin{array}{c|cc}
ab & f \\
\hline
00 & 10 \\
01 & 11 \\
\end{array}\] |
| b) Simplified function \( f(a, b) = ? \) |
| 5 1p     | \( V_{OUT} = f(A, B, C) = ? \) |
| 6 1p     | \( q_3q_0 = 00, \) |
| 7 1p     | \( q^+ = f(q, e, d) = ? \) |
| 8 1p     | \( d_{\text{out}} \leq ( \text{NOT} a \text{ AND} d_{\text{in(0)}} ) \text{ OR } ( \text{ }) \); |

This table is completed by the examiner!!

<table>
<thead>
<tr>
<th>Part A1</th>
<th>Part A2</th>
<th>Part B</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Points</td>
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<td>10</td>
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