Written exam
IE1204-5 Digital Design
Friday 21/10 2016 09.00-13.00

General Information

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Exam text does not have to be returned when you hand in your writing.

Aids: No aids are allowed!
The exam consists of three parts with a total of 14 tasks, and a total of 30 points:

Part A1 (Analysis) contains ten short questions. Right answer will give you one point. Incorrect answer will give you zero points. The total number of points in Part A1 is 10 points. To pass the Part A1 requires at least 6p, if you get fewer points, we will not look at the rest of your exam.

Part A2 (Methods) contains two methodology-related problems with a total of 10 points.

To pass the exam requires at least 11 points from A1 + A2, if you get fewer points, we will not look at the rest of your exam.

Part B (Design problems) contains two design problems with total of 10 points. Part B is corrected only if there are at least 11p from the exam A-Part.

NOTE! At the end of the exam text there is a submission sheet for Part A1, which should be separated and submitted together with the solutions for A2 and B.

A passing grade (E) requires at least 11 points on the exam. If you get exactly 10p from A1(6p)+A2(4p), (FX), completion to (E) will be offered.

Grades are given as follows:

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<td>0</td>
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<td>F</td>
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<td>A</td>
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The result is expected to be announced before Friday 11/11 2016.
Part A1: Analysis

Only final answers are required in Part A1. Write these answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p
A function \( f(x, y, z) \) is described by the expression:
\[
f(x, y, z) = (z \oplus x + z \oplus x) \cdot (y + y)
\]
Write down a minimized two-level sum-of-products (SoP) form for this function.
\[
f(x, y, z) = \{SoP\}_{\text{min}} = ?
\]

2. 1p/0p
A four-bit unsigned integer \( x = (x_3x_2x_1x_0) \) is connected to a 6-bit adder in the way that it is multiplied with a constant \( K \), so that the result is \( s = K \cdot x \) (see the diagram below to figure out the value of \( K \)). If the input \( x = (1111)_2 \) is applied to the diagram below, then what will the number \( s = ? \) Answer with \( s \) as a binary number.

3. 1p/0p
A four bit adder adds two 4 bit signed numbers represented as 2’s complements. If \( x = 0101 \) and \( y = 0111 \), then what will be the four bit sum \( s \) computed by the adder? Answer with a signed decimal number. \( \pm s_{10} \)

4. 1p/0p
Consider a Karnaugh map for a function of four variables \( y = f(a, b, c, d) \) given below. Write the function in a minimized \( y_{\text{min}} \) product-of-sums (PoS) form. “-“ in the map means “don’t care”.

\[
\begin{array}{cccc}
00 & 01 & 11 & 10 \\
00 & 0 & 1 & 0 \\
01 & 1 & 0 & 0 & - \\
11 & - & - & 1 & 1 \\
10 & 0 & 0 & 1 & 0 \\
\end{array}
\]
5. 1p/0p
The figure shows a circuit with four NOR gates. Simplify the function \( Q = f(A, B) \) as much as possible and write down the resulting expression for it.

![Circuit Diagram]

6. 1p/0p
What logic function does this multiplexor circuit represent?

\[ f(b, a) = ? \]

![Multiplexor Diagram]

7. 1p/0p
Give an expression for the logic function realized by the CMOS circuit in the figure. Answer with a sum of products (SoP) form. \( f(A, B, C) = ? \)

![CMOS Circuit Diagram]

8. 1p/0p
A synchronous counter with T flip-flops in the figure starts in the state \( Q_1Q_0 = 00 \). Give its sequence of states for the following four clock pulses.
9. 1p/0p

For the shift register with D flip-flops in this figure setup time is $t_{su} = 4$ ns, delay time for the flip-flop outputs is $t_{pdQ} = 3$ ns and the hold time is $t_h = 2$ ns.

● How long needs to be the time between the clock pulses, $T_{CP}$, for the counter function to be correct?

10. 1p/0p

Consider The following the VHDL code for a 2-input multiplexer given below. One line of the code in the circuit architecture is missing. Write the missing code line on the submission sheet.

Variabes are: $d_{in0}$, $d_{in1}$, $d_{out}$, $s$. Useful keywords are: and, or, not.

```
entity MUX2_1 is
  port( d_in0, d_in1, s : in std_logic;
        d_out       : out std_logic);
end entity MUX2_1;

architecture behave of MUX2_1 is
begin
  d_out <= Oooops! What should be here?
end architecture behave;
```
Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 (≥6p)

11. 4p

Japanese train signals are more complex than ours, but it is needed because Japan has some of the world's fastest train. The signals allow speed in six steps from stand still up to full speed.

Stop (R)  Restricted Speed (Y over Y)  Caution (Y)  Reduced Speed (Y over G)  Less reduced Speed (Y over G flashing)  Clear (G)

Design a signal decoder, a combinatorial logic network, which uses a three-bit mode signal \( M(m_2m_1m_0) \) to generate output signals controlling four colored lights \( (y_1r_y_0g) \).

Mode 0, \( m_2m_1m_0 \) 000, will mean that the signal off.

Mode 1…6, \( m_2m_1m_0 \) 001 … 110 (in binary), select signals for incrementally increasing allowable speed according to the standard shown in the figure above.

Flashing signal means that \( y_1 \) and \( g \) should blink in an alternating manner, controlled by the pulse \( x \) from a pulse generator.

a) (1p) Set up the relationship between the output signals \( y_1r_y_0g \) and the input signals \( x m_2m_1m_0 \) as a table (as a truth table).

b) (2p) Set up Karnaugh maps for the four lamp signals and produce the minimized expressions \( y_1r_y_0g \) in the SoP form. Make use of "don’t cares".

c) (1p) Draw the schematic diagram for one of the four signal decoder outputs (select the most complex network) using the optional gates of your choice.
12. 6p
A modulo-6 synchronous counter is implementing the sequence $q_1q_2q_3$: 000, 010, 011, 110, 101, 001.

![Diagram of the counter with states 000 to 101 and an arrow from 111 to question mark, and another arrow from 100 to question mark.]

**a)** (1p) Derive the **State table**. The two states 111 and 100 which are not included in the sequence can be treated as don’t cares, but they should lead to the modulo-6 sequence (in other words their next state should be one of the 6 states in the sequence above).

**b)** (1p) Derive **minimized** expressions for next state $q_1^* = ?$ $q_2^* = ?$ $q_3^* = ?$

**c)** (3p) The Synchronous Counter is constructed with three D flip-flops as in the figure. Implement the functions:
- $q_1^*$ with a 4:1 multiplexer
- $q_2^*$ with AND-OR gates
- $q_3^*$ with only NAND gates
by assigning the inputs in the figure on the right.

**d)** (1p) to which state in the modulo-6 sequence will 111 and 100 go to in your implementation?
Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 (≥11p).

13. 6p  Synchronous sequential circuit. Sequence detector.

a) (2p) Minimize the states in the state diagram on the right \((a,b,c,d,e,f,g,h)\). Then draw the minimal state diagram.

( To solve this independent task may well prove to be a good use of time for solving the rest of the task! )

b) (4p) A sequence detector is expected to detect each occurrence of a sub-sequence ... 1101 ... within a sequence of bits received by the input \(w\).

The sequence detector output signal \(z\) should be 1 in a clock pulse interval immediately after the sub-sequence 1101 has occurred (see the figure). Implement the sequence detector circuit as a Moore machine with positive edge-triggered D flip-flops with reset inputs. Derive the circuit state table and draw its state diagram.

Use binary code to encode the states and derive the encoded state table. Assume that no 1 can be received directly after Reset. Derive the minimized expressions for next state and for the output.

\[ q_2^+; q_1^+; q_0^+ = f(q_2q_1q_0, w) \Rightarrow q_2^+ = f(q_2q_1q_0, w) \quad q_1^+ = f(q_2q_1q_0, w) \quad q_0^+ = f(q_2q_1q_0, w) \]

\( z = f(q_2q_1q_0, w) \)

14. 4p  Single pulse generator.

Design an asynchronous sequential circuit which has an input \(w\) and an input \(c\). A sequence of pulses are arriving at the input \(w\). Each time the input \(w\) is 1, a complete pulse of the sequence \(c\) should appear at the output \(y\), as soon as possible. A pulse \(w\) is always longer than a pulse \(c\) (see figure on the right).

a) Set up a proper flow table for the circuit. Draw its state diagram.

b) Do a suitable state assignment with an excitation-table which gives a circuit that is free of critical race. You should also derive hazard free expressions for the next state and an expression for the output, and draw the circuit diagrams with the gates of your choice.

Hope all went well!
Submission sheet for Part A1  Sheet 1

( remove and hand in together with your answers for part A2 and part B )

Last name: ________________________  Given name: ________________________

Personal code: ________________________  Sheet: 1

Write down your answers for the questions from Part A1 ( 1 to 10 )

<table>
<thead>
<tr>
<th>Question</th>
<th>Answer</th>
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<tbody>
<tr>
<td>1</td>
<td>( f(x, y, z) = {SoP}_{\text{min}} = ? )</td>
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<tr>
<td>2</td>
<td>( s = K \cdot x )  ( x = 1111_2 )  ( s = ? ) [binary]</td>
</tr>
<tr>
<td>3</td>
<td>( x = 0101 )  ( y = 0111 )  ( s = x + y = s_{10} ) [number as signed decimal value]</td>
</tr>
<tr>
<td>4</td>
<td>( f(a, b, c, d) = {PoS}_{\text{min}} = ? )</td>
</tr>
<tr>
<td>5</td>
<td>( Q = f(A, B) = ? )</td>
</tr>
<tr>
<td>6</td>
<td>( f(b, a) = ? )</td>
</tr>
<tr>
<td>7</td>
<td>( f(A, B, C) = ? )</td>
</tr>
<tr>
<td>8</td>
<td>( Q_1Q_0 : 00 \rightarrow )</td>
</tr>
<tr>
<td>9</td>
<td>( T_{CP} &gt; ? ) [ns]</td>
</tr>
<tr>
<td>10</td>
<td>architecture behave of MUX2_1 is begin d_out &lt;= end architecture behave;</td>
</tr>
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<tr>
<td>Points</td>
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<td>12</td>
<td>13</td>
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