Assignment description, project 2

Objective

The purpose of this assignment is to get further acquainted with the hardware description language and the hardware simulator for *timed* logic.

Contract

You may start from the implementation of a data flip-flop, DFF, as explained in the book. You may also use all the combinational chips (the simulator uses built in versions that are more efficient).

Implement the following chips in HDL and verify your implementation by the hardware tool.

1. Bit, Register
2. RAM8, RAM64, RAM512, RAM4K (RAM16K is optional)
3. PC

Resources

You will need the HardwareSimulator tool; you find templates and test script for all chips in the folder projects/03.

Hints

- Fan out, use "out=a, out=b, …"
- To assign a value *true* or *false* to a pin of a bus, use b[i]=false or b[i]=true
- For PC, several control signals may be set at the same time; follow the if-clauses in the definition of the chip.

Submission

Your project must be mailed to your group leader no later than 8.00 on Tuesday March 28, 2017. Make sure that the subject field states *EP1200-seminar2-GroupN-Firstname-Familyname*, if you are in seminar group N.

All projects should be done individually.

One submission per student, in a zipped file named EP1200-seminarM-GroupN-firstname-familyname.zip including:

- The solutions (typically code).
- The list of the sub-projects you solved successfully and are able to present. Use the provided form. Do not forget to write your name on the form!

Copying and other forms of plagiarism and cheating will be reported for disciplinary action!