



KTH Informations- och kommunikationsteknik

Written exam IE1204 Digital Design Monday 15/1 2018 14.00-18.00

General Information

Examiner: Carl-Mikael Zetterling.

Responsible teacher at exam: Carl-Mikael Zetterling.

Exam text has to be returned when you hand in your writing.

NOTE! At the end of the exam text there are submission sheets for Part A1, which must be separated and submitted together with the solutions for A2 and B.

Aids: No aids are allowed!

The exam consists of three parts with a total of 14 tasks, and a total of 30 points:

Part A1 (Analysis) contains ten short questions. A correct answer will give you one point.

An incorrect answer will give you zero points. The total number of points in Part A1 is **10 points**.

To **pass Part A1 requires at least 6 points**, if you have fewer points we will not correct the rest of your exam.

Part A2 (Methods) contains two method problems with a total of 10 points.

To **pass the exam** requires at least **11 points** from A1 + A2, if you have fewer points we will not correct the rest of your exam.

Part B (Design problems) contains two design problems of a total of 10 points. Part B is corrected only if you have at **least 11 points** from the exam A- Part.

For a passing grade (E) at **least 11 points on the exam is required**. If you have exactly 10 points from A1(6p)+A2(4p), (FX) completion to (E) will be offered.

Grades are given as follows:

0 –	11 –	16 –	19 –	22 –	25 –
F	E	D	C	B	A

The result will be announced before Monday 5/2 2018.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p

A function $f(x, y, z)$ is described as:

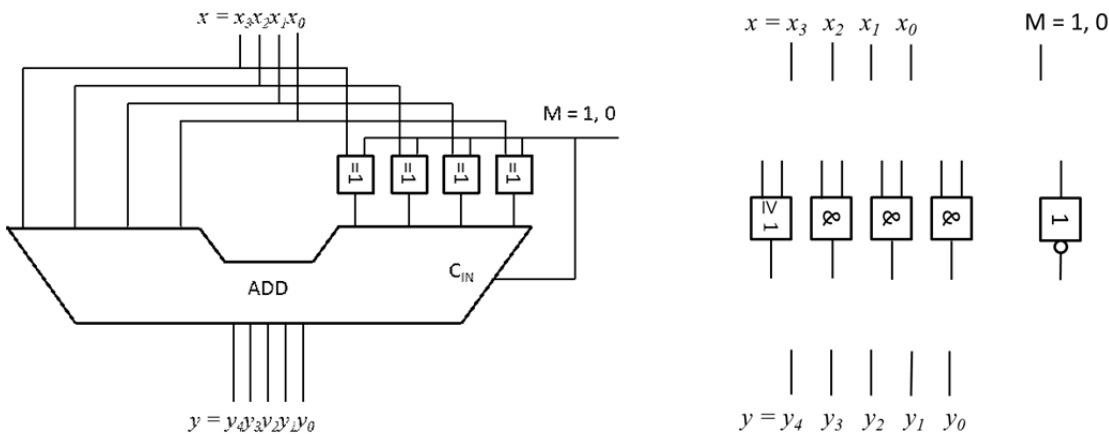
$$f(x, y, z) = (x + y + \bar{z})(x + \bar{y} + z)(\bar{x} + y + \bar{z})$$

Write down the function as a sum of products (minterms only).

$$f(x, y, z) = \{SoP_{\text{minterms}}\} = ?$$

2. 1p/0p

The following circuit consisting of a 4-bit adder and 4 XOR gates can be replaced by 3 AND gates, 1 OR gate and 1 inverter. Connect the signals with the gates. The constants 1 and 0 can also be used if needed.



3. 1p/0p

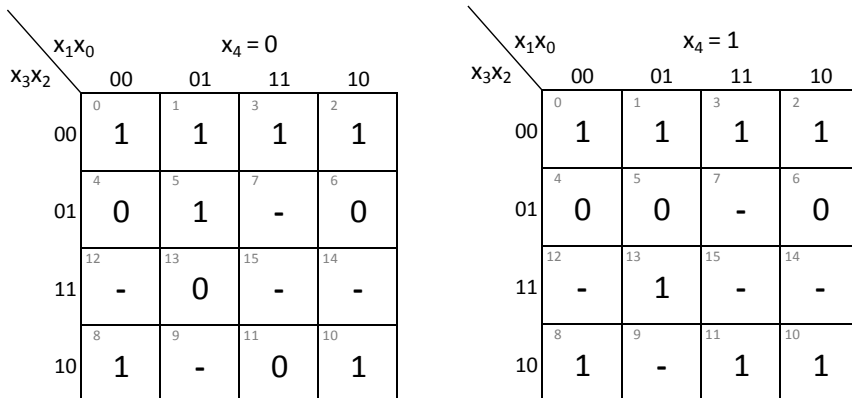
Two two's complement 16-bit hexadecimal numbers are $x = 0ABC_{16}$ and $y = 0BCD_{16}$.

What is the result of the subtraction $s = x - y$?

Express this number s as a two's complemented 16-bit hexadecimal number.

4. 1p/0p

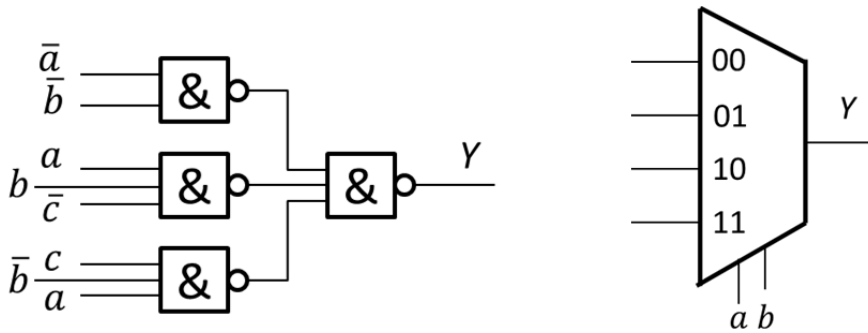
Below is a Karnaugh map for a function of five variables $Y = f(x_4, x_3, x_2, x_1, x_0)$. Write the minimized function Y_{min} , as a sum of products, on **SoP** form. "-" in the map means "don't care".



5. 1p/0p

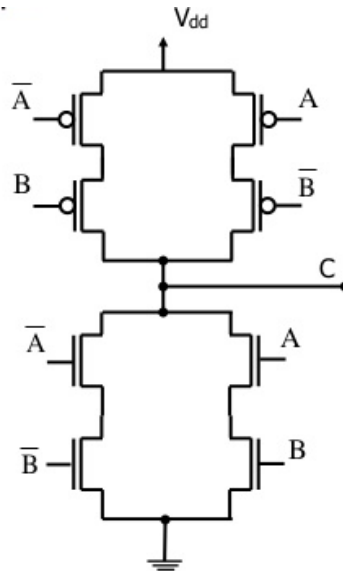
A function $Y = f(a,b,c)$ has been made with four NAND gates. Design it using a MUX instead.

You may connect the following to the MUX inputs as needed: $c, \bar{c}, 0, 1$



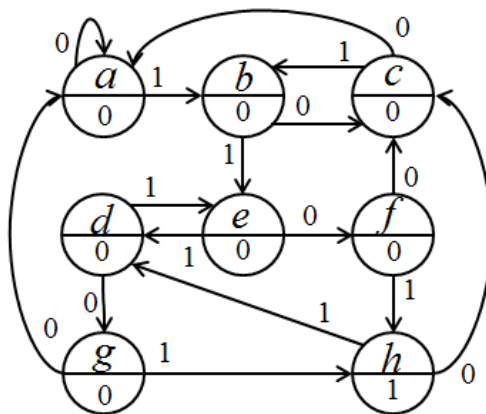
6. 1p/0p

What is the logic function of this CMOS gate? $C(A,B) = ?$



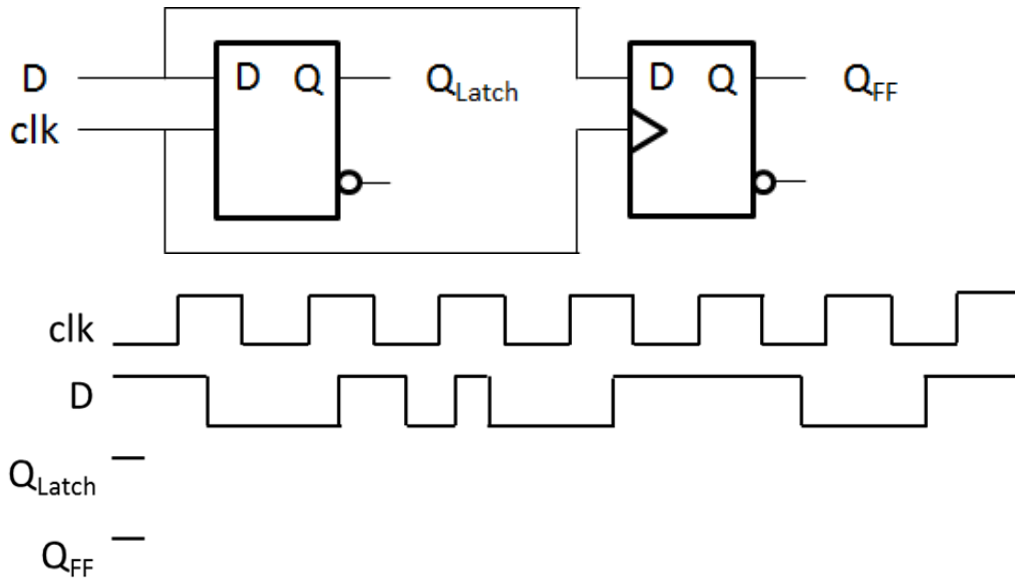
7. 1p/0p

A Moore type state machine has the input sequence 000010101101. The starting state does not matter but you may assume state "a". What is the final state after this input sequence?



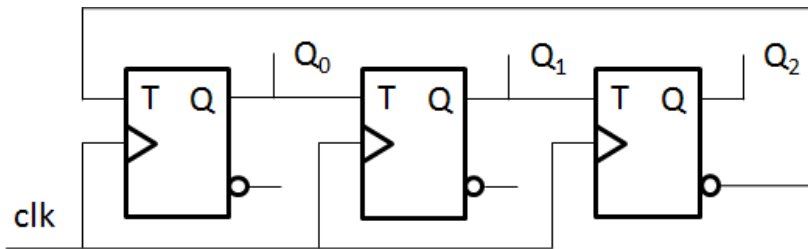
8. 1p/0p

A D latch and a D flip-flop both start with $Q = 1$. The same clk and D is connected to the inputs. Complete the timing diagram for the output signals Q_{Latch} and Q_{FF} . Answer on the submission sheet.



9. 1p/0p

A three bit counter is built with T flip-flops as below. Draw the state diagram for all possible states. Answer on the submission sheet.

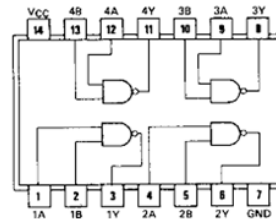


10. 1p/0p

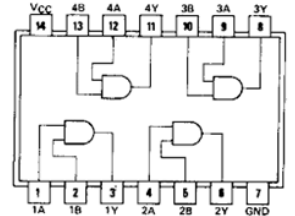
The VHDL code below describes a standard TTL gate. Which one of the four?

```
architecture behavior of chip is
begin
d5(1) <= not((d1(1) or d1(2)));
d5(2) <= not((d2(1) or d2(2)));
d5(3) <= not((d3(1) or d3(2)));
d5(4) <= not((d4(1) or d4(2)));
end behavior;
```

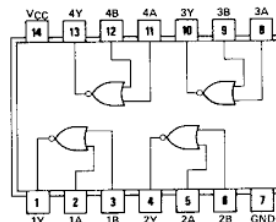
7400



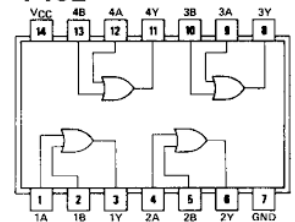
7408



7402



7432

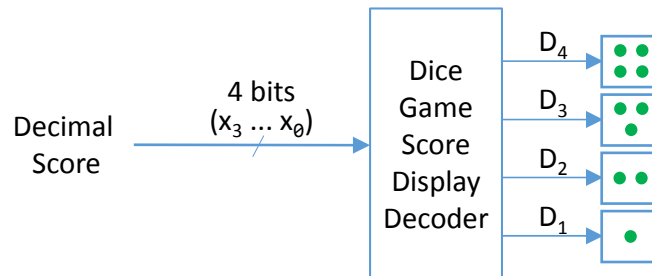


Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 ($\geq 6p$)

11. 5p

A dice based game score display has an unconventional display. The maximum that a player can score is 10 and minimum is 0. The game being based on dice, uses four electronic displays, each display showing one face of dice as shown below.



The scorer inputs the score through an interface, which encodes the score as 4 bit binary number. The Dice Game Score Display Decoder will then decode the 4-bit binary number into the 4 outputs D₄ to D₁. Each output is connected to a lightable dice face, as shown in the diagram above. The decoder has the following properties:

1. If the score is 0 no dice face is lit,
2. if the score is 10 all dice faces are lit and
3. if the score is in the range 1 to 9, the fewest number of dice that adds up to the score is lit, with priority to the highest dice values.
4. Assign the range 11 to 15 as don't cares.

a) (1p) Draw the truth table.

b) (2p) Derive minimum logic expressions for D₄, D₃, D₂ and D₁ using Karnaugh Maps and by exploiting the don't cares.

c) (2p) Design and draw the logic using only 2-input NAND gates.

12. 5p

Design a 4-bit synchronous counter that cycles through the odd prime numbers.

When the control input signal UP = 1 the sequence should be 3, 5, 7, 11, 13, 3 etc

When the control input signal UP = 0 the sequence should be 3, 13, 11, 7, 5, 3 etc

The signal UP can change at any state but is synchronous with the clock.

Design the counter using D flip-flops (with asynchronous set and reset inputs).

Hint: since all allowed numbers are odd, q₀ = 1, and only q₃, q₂ and q₁ need logic and flip-flops.

a) (1p) Make a state table for the allowed states.

b) (2p) Using Karnaugh Maps design the logic expressions for next state q₃₊, q₂₊ and q₁₊.

c) (1p) Draw a state diagram with all states, including the forbidden 1, 9, and 15.

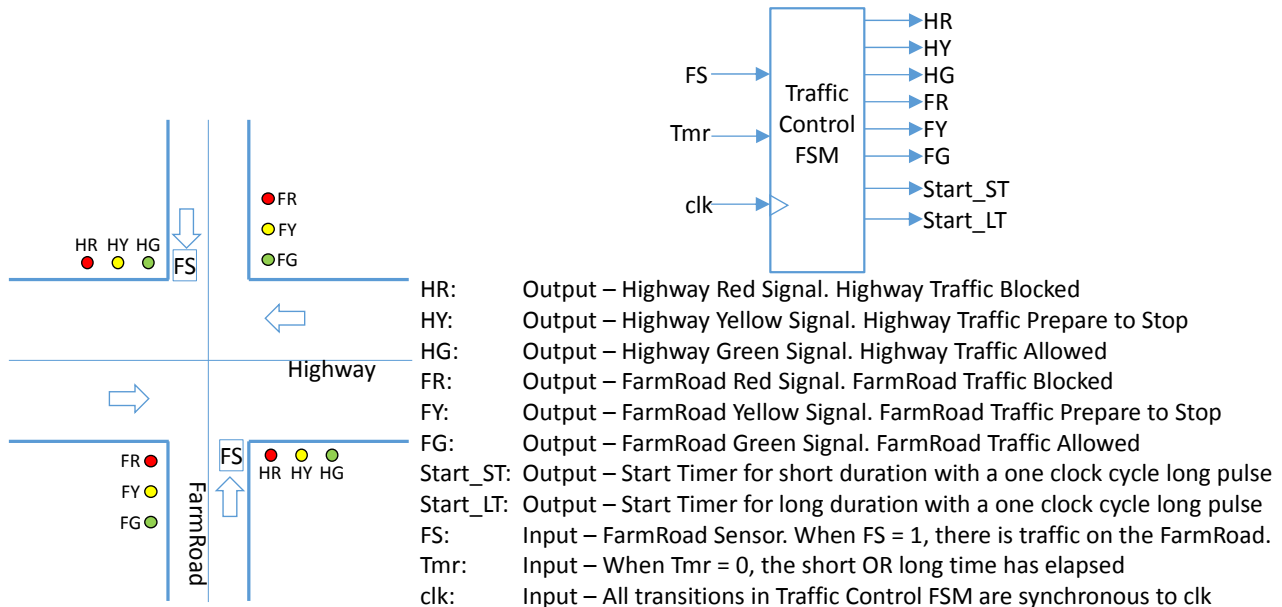
d) (1p) Design asynchronous set/reset logic so that the counter can always be set in state 3 at start.

Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 ($\geq 11p$).

13. (4p)

A finite state machine (FSM) traffic light controller controls the intersection of a Highway with that of a small Farmroad. Both roads are controlled by Red, Yellow and Green Lights. The illustration of the two roads, their signals and their operation is shown in the diagram and text below.



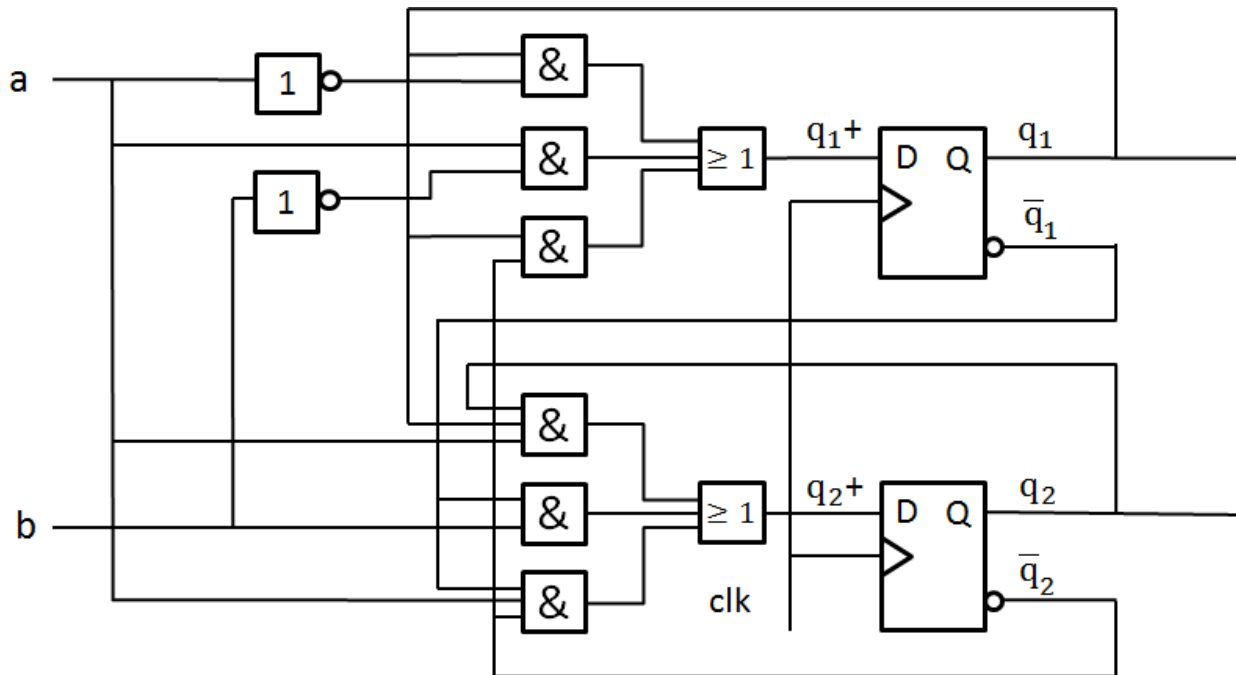
Design the traffic control FSM, taking the following into account:

- A traffic signal consists of three lights –Red, Yellow and Green. For each road and traffic direction, there is a traffic signal as shown in the diagram above.
 - The behavior of the two traffic signals for the two directions on the Highway is identical and this is also true for the two traffic signals for the two directions on the Farmroad.
 - For each traffic signal, only one light can be ON, the other two are OFF
 - To give priority to the Highway, by default the Highway green light HG is ON and the Farmroad red light FR is ON.
1. When the Highway traffic is enabled, if FS becomes 1, the traffic control FSM turns OFF HG and FR and turns ON HY and FY and starts a short timer by setting Start_ST to 1.
 2. When the short duration has elapsed, indicated by Tmr = 0, the traffic control FSM turns OFF the HY and FY lights, turns ON the HR and FG lights and at the same time starts the long timer by setting Start_LT to 1.
 3. When the long duration has elapsed, indicated again by Tmr = 0 it is time to block the Farmroad traffic again and enable the Highway traffic. This is done by turning OFF HR and FG and turning ON HY and FY and starting the short timer by setting Start_ST to 1
 4. When the short duration has elapsed, indicated by Tmr=0, the traffic control FSM turns OFF the HY and FY lights, turns ON the HG and FR lights and starts long term timer with a cycle long clock pulse.
 5. When Tmr=0, indicating that the long duration has elapsed and it is time to wait for the FS to become 1 again. And *when* it does, repeat the steps from 1 above.

Draw the state diagram and the state-transition table for a Mealy FSM.

14. (6p)

A synchronous state machine with inputs a and b has been designed with two D flip-flops, as seen below.



a) (1p) Calculate the maximum clock frequency.

Assume that $t_{\text{Setup}} = 5 \text{ ns}$, $t_{\text{Hold}} = 1 \text{ ns}$, $t_{\text{Gate}} = 5 \text{ ns}$, and $t_{\text{CLK2Q}} = 10 \text{ ns}$.

In an attempt to increase the reaction speed of the circuit and to reduce the gate count, the synchronous state machine is changed to an asynchronous state machine by removing the D flip-flops. For the analysis below, you can insert a delay element in place of each D flip-flop.

b) (2p) There is static hazard in at least one of the next-state functions. Specify new, hazard-free next-state functions for q_1^+ and q_2^+ . The excitation table must be unchanged.

Hint: Write down the next-state functions for q_1^+ and q_2^+ and draw Karnaugh maps.

c) (2p) There is at least one race condition in the sequential circuit. Specify all combinations of state and input that could trigger a race condition.

Hint: Draw the excitation table and transition diagram for the asynchronous machine and identify stable states.

d) (1p) Suggest a new state assignment that avoids the race condition.

Good Luck!

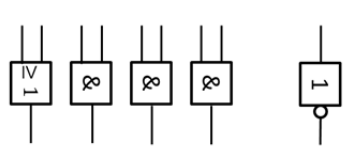
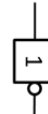
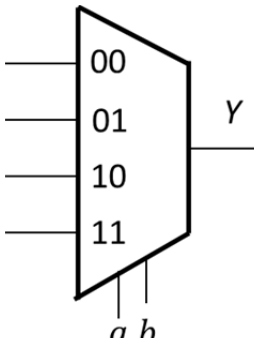
Submission sheet for Part A1 sheet 1

(remove and hand in together with your answers for part A2 and part B)

Last name: _____ Given name: _____

Personal code: _____ Sheet: 1

Write down your answers for the questions from Part A1 (1 to 10)

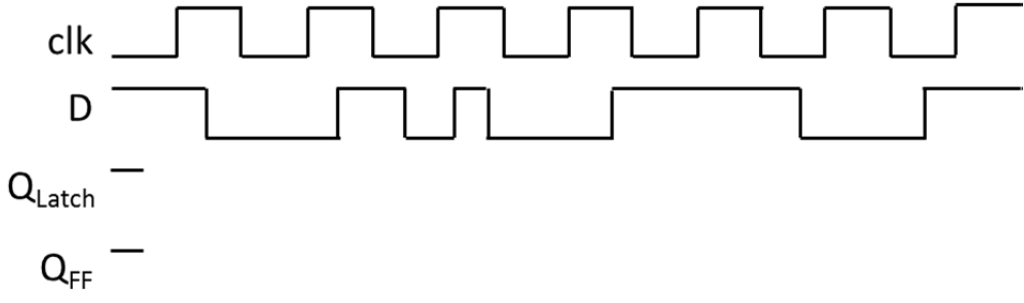
Question	Answer
1	$f(x, y, z) = \{SoP_{\min\ terms}\} = ?$
2	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> $x = x_3 \ x_2 \ x_1 \ x_0$  </div> <div style="text-align: center;"> $M = 1, 0$  </div> </div> <div style="margin-top: 20px; text-align: center;"> $y = y_4 \ y_3 \ y_2 \ y_1 \ y_0$ </div>
3	(Two's complement number) $s_{16} = ?$
4	$F(A, B) = \{SoP\}_{\min} = ?$
5	
6	$C(A, B) = ?$
7	Final state = ?

Submission sheet for Part A1 sheet 2

(remove and hand in together with your answers for part A2 and part B)

Last name: _____ Given name: _____

Personal code: _____ Sheet: 2

8	
9	State diagram:
10	Standard TTL gate:

This table is completed by the examiner!

Part A1 (10)	Part A2 (10)		Part B (10)		Total (30)	
Points	11	12	13	14	Sum	Grade