



KTH Informations- och kommunikationsteknik

Written exam IE1205 Digital Design Monday 15/1 2018 14.00-18.00

General Information

Examiner: Ahmed Hemani.

Responsible teacher at exam: Fredrik Lundevall.

Exam text has to be returned when you hand in your writing.

NOTE! At the end of the exam text there are submission sheets for Part A1, which must be separated and submitted together with the solutions for A2 and B.

Aids: No aids are allowed!

The exam consists of three parts with a total of 16 tasks, and a total of 30 points:

Part A1 (Analysis) contains ten short questions. A correct answer will give you one point.

An incorrect answer will give you zero points. The total number of points in Part A1 is **10 points**.

To **pass Part A1 requires at least 6 points**, if you have fewer points we will not correct the rest of your exam.

Part A2 (Methods) contains two method problems with a total of 10 points.

To **pass the exam** requires at least **11 points** from A1 + A2, if you have fewer points we will not correct the rest of your exam.

Part B (Design problems) contains four design problems for a total of 10 points. Part B is corrected only if you have at **least 11 points** from the exam A- Part.

For a passing grade (E) at **least 11 points on the exam is required**. If you have exactly 10 points from A1(6p)+A2(4p), (FX) completion to (E) will be offered.

Grades are given as follows:

0 –	11 –	16 –	19 –	22 –	25 –
F	E	D	C	B	A

The result will be announced before Monday 5/2 2018.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p

Schools are given snow days given specific circumstances. If there is ice on the roads, but no salt, then a snow day is given. If there is salt however, then a snow day is not given. Regardless of whether or not there is salt, whenever there is greater than 5 cms of snow, then a snow day is given. Write a truth table that describes these conditions.

Solution:

Inputs:

Ice on the road: x ; $x = 1$ means ice on the road

No salt: y ; $y = 1$ means no salt on the road

Greater 5 cms snow: z ; $z = 1$ means greater than 5 cms snow

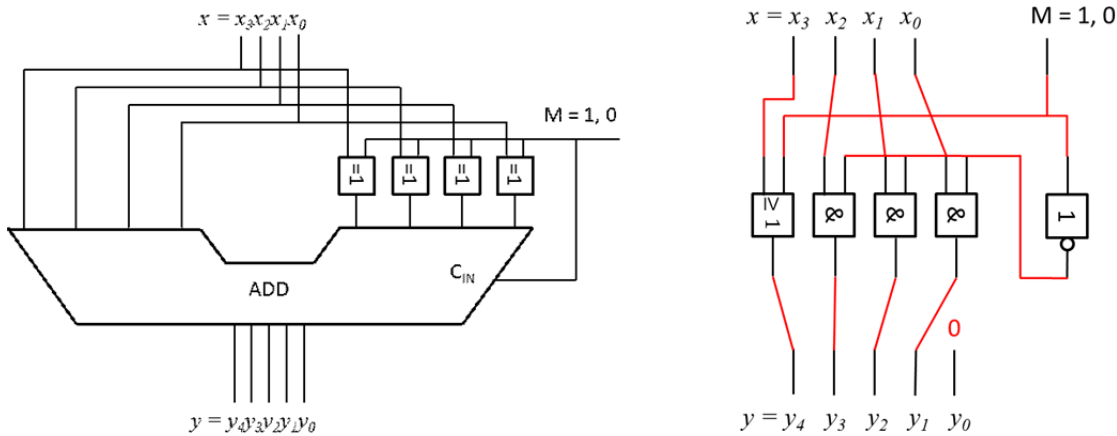
Output

Snow day: s

x	y	z	 	s
0	0	0		0
0	0	1		1 ; greater than 5 cms of snow
0	1	0		0
0	1	1		1 ; greater than 5 cms of snow
1	0	0		0 ; ice on the road and salt on the road
1	0	1		1 ; > 5 cms of snow
1	1	0		1 ; ice on the road and no salt
1	1	1		1 ; ice on the raod, no salt and > 5 cms of snow

2. 1p/0p

The following circuit consisting of a 4-bit adder and 4 XOR gates can be replaced by 3 AND gates, 1 OR gate and 1 inverter. Connect the signals with the gates. The constants 1 and 0 can also be used if needed.



Solution:

If $M = 0$ the adder performs the operation $2x$, or a left shift.

If $M = 1$ the adder performs $x - x$, with the 2-complement of x , which results in 0 in all bits except the carry out (y_4)

3. 1p/0p

Two two's complement 16-bit hexadecimal numbers are $x = 0ABC_{16}$ and $y = 0BCD_{16}$.

What is the result of the subtraction $s = x - y$?

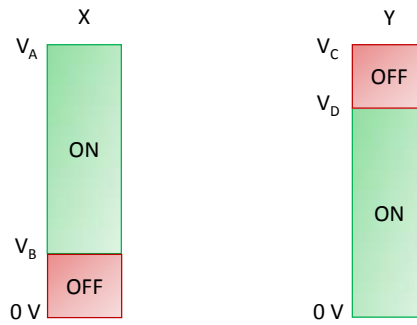
Express this number s as a two's complemented 16-bit hexadecimal number.

Solution:

The two's complement of $0BCD_{16}$ is $F433$. Add the two together to get $FEEF_{16}$

4. 1p/0p

The range bars are supposed to show the ON and OFF regions of PMOS and NMOS transistors.



Identify which range is for PMOS and which range is for NMOS by identifying X and Y as PMOS or NMOS

Write the Voltage values for V_A , V_B , V_C and V_D in terms of V_{DD} and V_t (threshold voltage)

Solution:

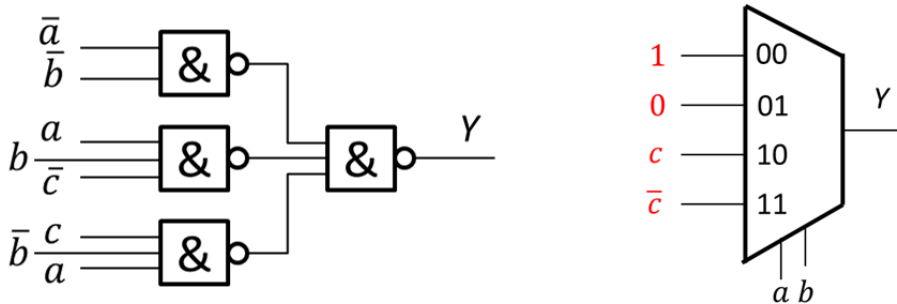
X: NMOS and Y: PMOS

$$V_A = V_{DD}, V_B = V_t, V_C = V_{DD}, V_D = V_{DD} - V_t$$

5. 1p/0p

A function $Y = f(a,b,c)$ has been made with four NAND gates. Design it using a MUX instead.

You may connect the following to the MUX inputs as needed: $c, \bar{c}, 0, 1$

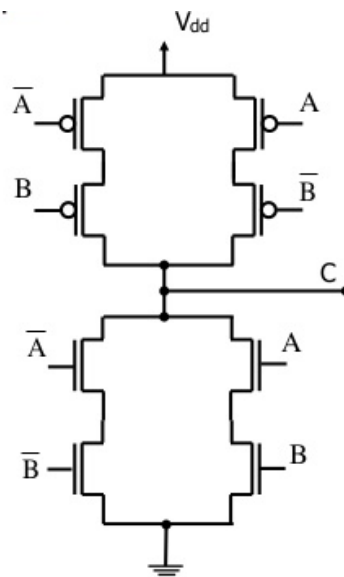


Solution:

		c			
		00	01		
ab	00	1	1	Gate 1	Row 1
	01	0	0		Row 2
	11	1	0	Gate 2	Row 4
	10	0	1	Gate 3	Row 3

6. 1p/0p

What is the logic function of this CMOS gate? $C(A,B) = ?$



Solution:

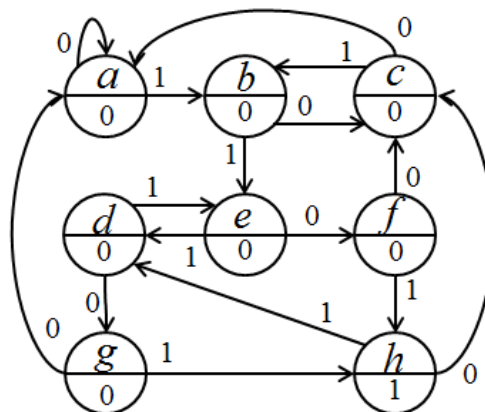
Pull down network:

$$\bar{C} = \bar{A}\bar{B} + AB \text{ \{De Morgan\}} \Rightarrow C = (\bar{A} + \bar{B})(A + B) = \bar{A}B + A\bar{B} = A \oplus B$$

It is an XOR gate.

7. 1p/0p

A Moore type state machine has the input sequence 000010101101. The starting state does not matter but you may assume state “a”. What is the final state after this input sequence?

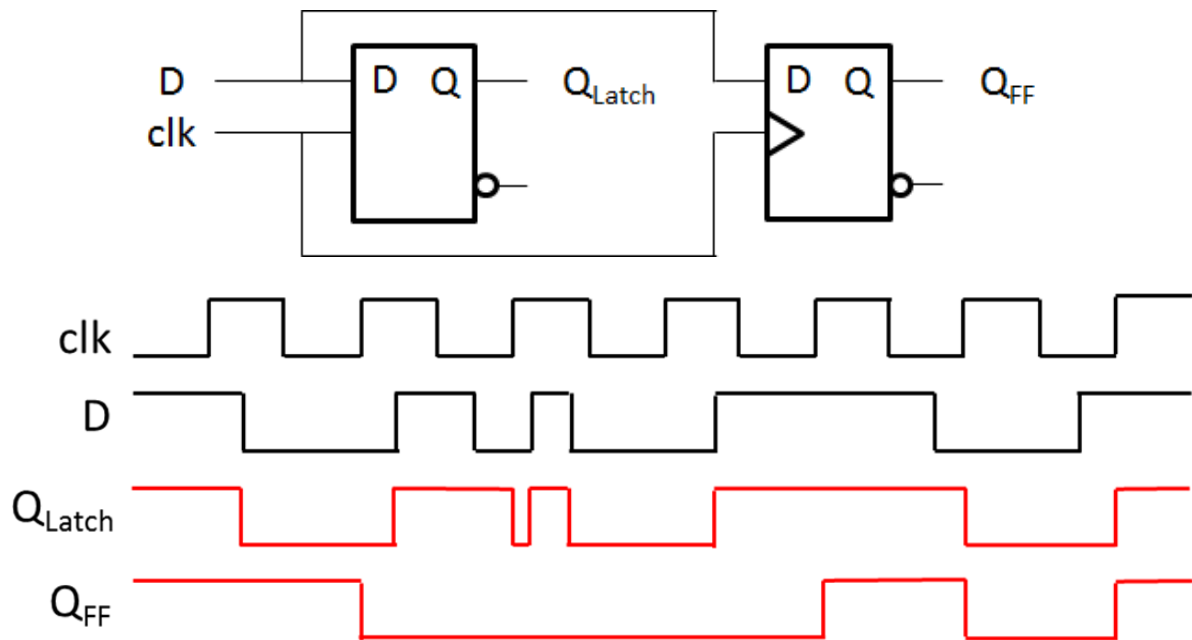


Solution:

The FSM will go through the sequence: a a a a b c b c b e f h, **final state = h**

8. 1p/0p

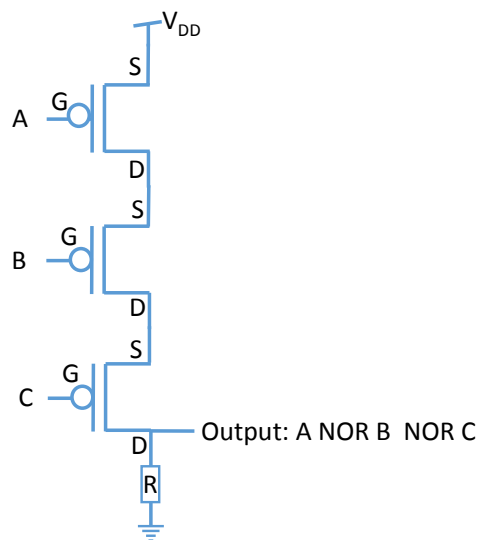
A D latch and a D flip-flop both start with $Q = 1$. The same clk and D is connected to the inputs. Complete the timing diagram for the output signals Q_{latch} and Q_{FF} . Answer on the submission sheet.



9. 1p/0p

Draw 3-inp NOR gate using PMOS transistors and a resistor. For each transistor mark the gate, source and drain terminals with symbols G, S and D respectively. Also clearly mark the three inputs as A, B and C and the output with "A NOR B NOR C". Finally show how the 3-input NOR gate is connected to VDD (Logic 1) and GND (Logic 0).

Solution:



10. 1p/0p

Identify the sequential element defined by the following VHDL description. Answer the following:

- i. Is it a Flop. If yes, is it sensitive to rising edge or falling edge
- ii. Is it a latch, if yes, is it transparent during the ON period when the clock is high or during the OFF period when the clock is low

```
ENTITY seq_element IS
    PORT (data_in; IN BIT;
          data_out: OUT BIT;
          clk: IN BIT);
END seq_element;
ARCHITECTURE behavioural OF seq_element IS
BEGIN
    IF clk = '0' THEN
        data_out <= data_in;
    END IF;
END behavioural;
```

Solution:

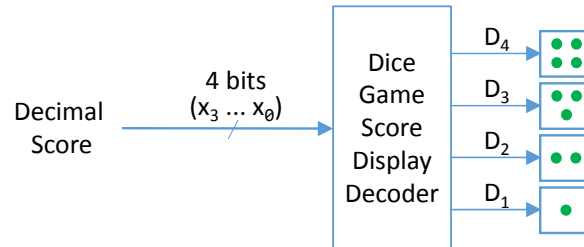
1. It is not a Flip-flop
2. It is a latch. It is transparent during the OFF period when the clock is low

Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 ($\geq 6p$)

11. 5p

A dice based game score display has an unconventional display. The maximum that a player can score is 10 and minimum is 0. The game being based on dice, uses four electronic displays, each display showing one face of dice as shown below.



The scorer inputs the score through an interface, which encodes the score as 4 bit binary number. The Dice Game Score Display Decoder will then decode the 4-bit binary number into the 4 outputs D_4 to D_1 . Each output is connected to a lightable dice face, as shown in the diagram above. The decoder has the following properties:

1. If the score is 0 no dice face is lit,
2. if the score is 10 all dice faces are lit and
3. if the score is in the range 1 to 9, the fewest number of dice that adds up to the score is lit, with priority to the highest dice values.
4. Assign the range 11 to 15 as don't cares.

a) (1p) Draw the truth table.

b) (2p) Derive minimum logic expressions for D_4 , D_3 , D_2 and D_1 using Karnaugh Maps and by exploiting the don't cares.

c) (2p) Design and draw the logic using only 2-input NAND gates.

Solution:

a)

x3	x2	x1	x0	D4	D3	D2	D1	#
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	2
0	0	1	1	0	1	0	0	3
0	1	0	0	1	0	0	0	4
0	1	0	1	1	0	0	1	5
0	1	1	0	1	0	1	0	6
0	1	1	1	1	1	0	0	7
1	0	0	0	1	1	0	1	8
1	0	0	1	1	1	1	0	9
1	0	1	0	1	1	1	1	10
1	0	1	1	-	-	-	-	11
1	1	0	0	-	-	-	-	12
1	1	0	1	-	-	-	-	13
1	1	1	0	-	-	-	-	14
1	1	1	1	-	-	-	-	15

b)

		x_1x_0			
		00	01	11	10
x_3x_2	00	0	0	0	0
	01	1	1	1	1
	11	-	-	-	-
	10	1	1	-	1

$$D_4 = x_3 + x_2$$

		x_1x_0			
		00	01	11	10
x_3x_2	00	0	0	1	0
	01	0	0	1	0
	11	-	-	-	-
	10	1	1	-	1

$$D_3 = x_3 + x_1 x_0$$

		x_1x_0			
		00	01	11	10
x_3x_2	00	0	0	0	1
	01	0	0	0	1
	11	-	-	-	-
	10	0	1	-	1

$$D_2 = x_3 x_0 + x_1 \bar{x}_0$$

		x_1x_0			
		00	01	11	10
x_3x_2	00	0	1	0	0
	01	0	1	0	0
	11	-	-	-	-
	10	1	0	-	1

$$D_1 = x_3 \bar{x}_0 + \bar{x}_3 \bar{x}_1 x_0$$

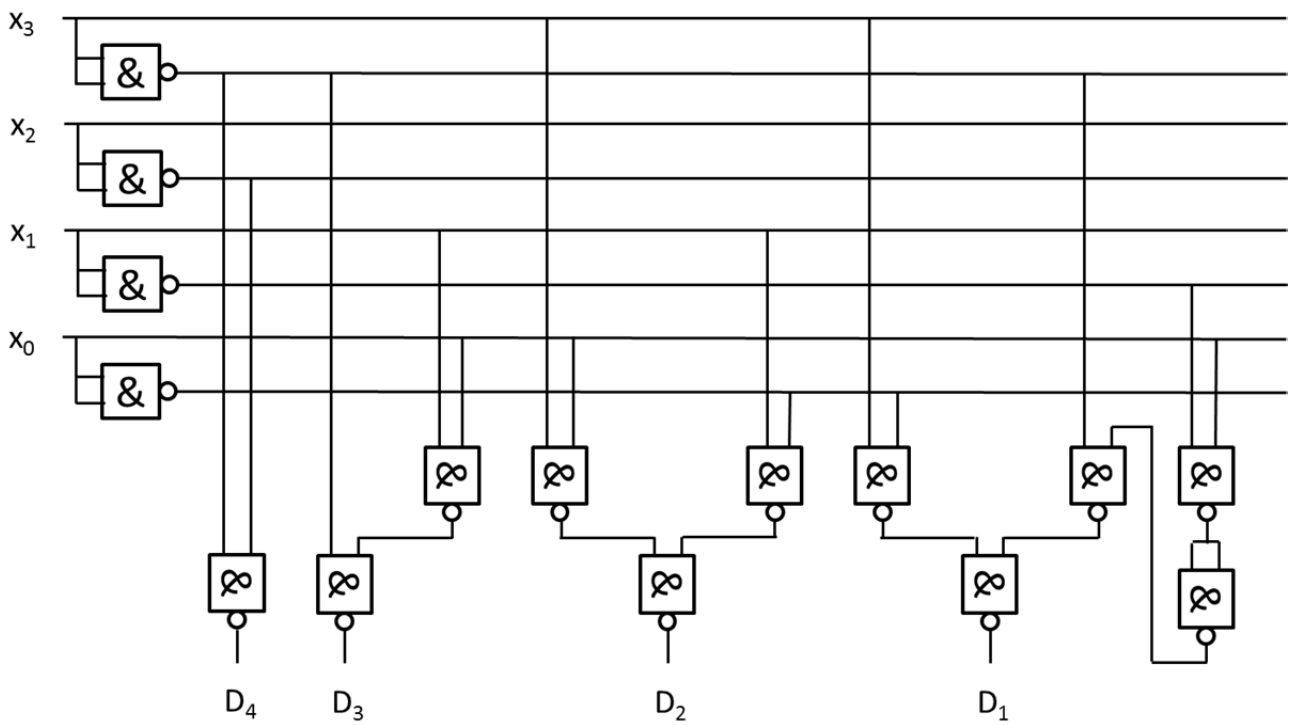
c)

$$D_4 = x_3 + x_2 = \overline{\overline{x_3} \overline{x_2}}$$

$$D_3 = x_3 + x_1 x_0 = \overline{\overline{x_3} \overline{x_1 x_0}}$$

$$D_2 = x_3 x_0 + x_1 \overline{x_0} = \overline{\overline{x_3 x_0} \overline{x_1 \overline{x_0}}}$$

$$D_1 = x_3 \overline{x_0} + \overline{x_3} \overline{x_1} x_0 = \overline{\overline{x_3 \overline{x_0}} \overline{\overline{x_3} \overline{x_1} x_0}} = \overline{\overline{x_3 \overline{x_0}} \overline{x_3} \overline{x_1} x_0}$$



12. 5p

Design a 4-bit synchronous counter that cycles through the odd prime numbers.

When the control input signal $UP = 1$ the sequence should be 3, 5, 7, 11, 13, 3 etc

When the control input signal $UP = 0$ the sequence should be 3, 13, 11, 7, 5, 3 etc

The signal UP can change at any state but is synchronous with the clock.

Design the counter using D flip-flops.

Hint: since all allowed numbers are odd, $q_0 = 1$, and only q_3, q_2 and q_1 need logic and flip-flops.

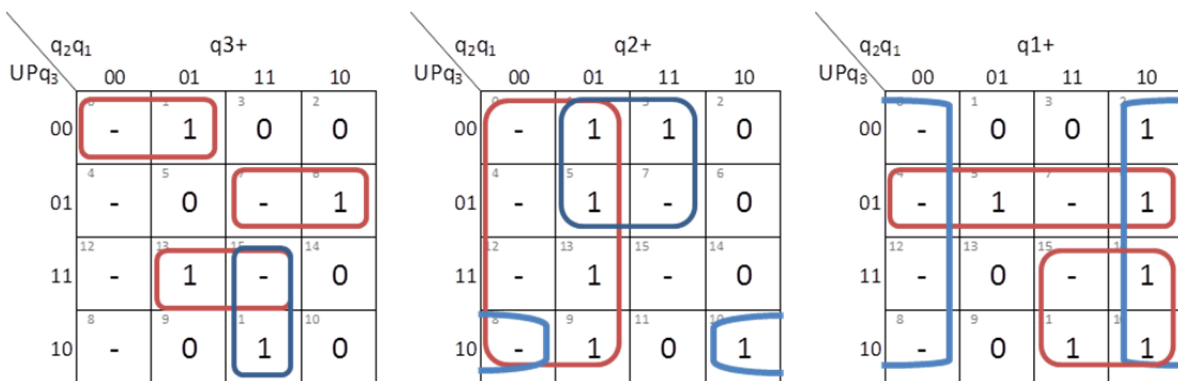
- a) (1p) Make a state table for the allowed states.
- b) (2p) Using Karnaugh Maps design the logic expressions for next state q_3+ , q_2+ and q_1+ .
- c) (1p) Draw a state diagram with all states, including the forbidden 1, 9, and 15.
- d) (1p) Design asynchronous set/reset logic so that the counter can always be set in state 3 at start.

Solution:

a)

#	Present state				next state			next state		
	q3	q2	q1	q0	UP = 0			UP = 1		
					q3+	q2+	q1+	q3+	q2+	q1+
1	0	0	0	1	-	-	-	-	-	-
3	0	0	1	1	1	1	0	0	1	0
5	0	1	0	1	0	0	1	0	1	1
7	0	1	1	1	0	1	0	1	0	1
9	1	0	0	1	-	-	-	-	-	-
11	1	0	1	1	0	1	1	1	1	0
13	1	1	0	1	1	0	1	0	0	1
15	1	1	1	1	-	-	-	-	-	-

b)



$$q_3+ = \overline{UP} \overline{q_3} \overline{q_2} + \overline{UP} q_3 q_2 + UP q_3 q_1 + UP q_2 q_1$$

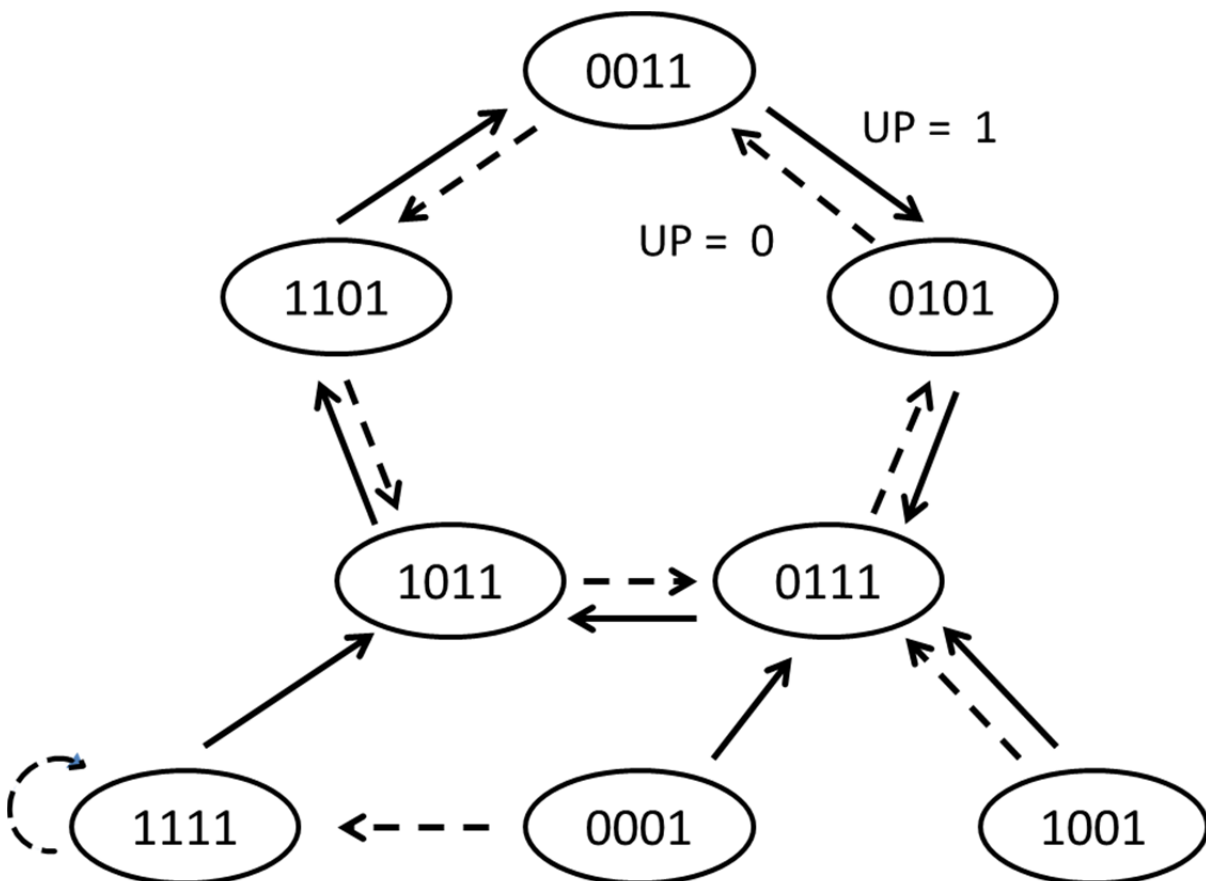
$$q_2+ = \overline{q_2} + \overline{UP} q_1 + UP \overline{q_3} \overline{q_1}$$

$$q_1+ = \overline{q_1} + \overline{UP} q_3 + UP q_2$$

c)

Insert the resulting 1s and 0s from the Karnaugh Maps to specify all don't cares:

#	Present state				next state			next state		
	q3	q2	q1	q0	UP = 0			UP = 1		
	q3+	q2+	q1+		q3+	q2+	q1+	q3+	q2+	q1+
1	0	0	0	1	1	1	1	0	1	1
3	0	0	1	1	1	1	0	0	1	0
5	0	1	0	1	0	0	1	0	1	1
7	0	1	1	1	0	1	0	1	0	1
9	1	0	0	1	0	1	1	0	1	1
11	1	0	1	1	0	1	1	1	1	0
13	1	1	0	1	1	0	1	0	0	1
15	1	1	1	1	1	1	1	1	0	1



d)

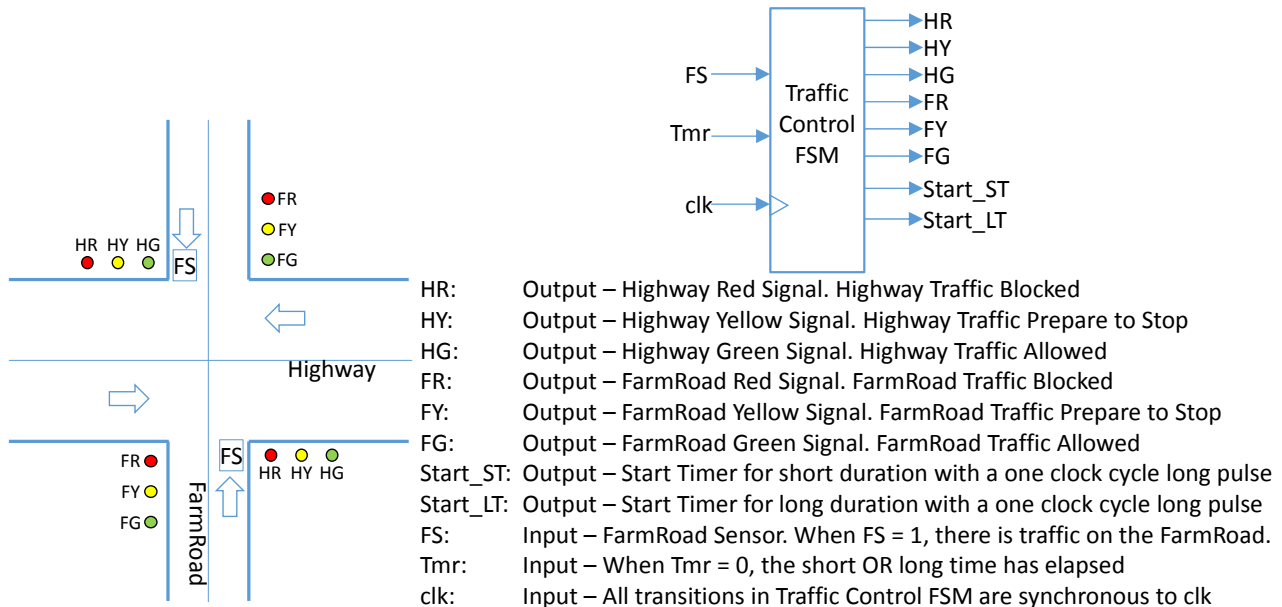
Connect reset to RES of q3 and q2, and to SET of q1.

Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 ($\geq 11p$).

13. (4p)

A finite state machine (FSM) traffic light controller controls the intersection of a Highway with that of a small Farmroad. Both roads are controlled by Red, Yellow and Green Lights. The illustration of the two roads, their signals and their operation is shown in the diagram and text below.

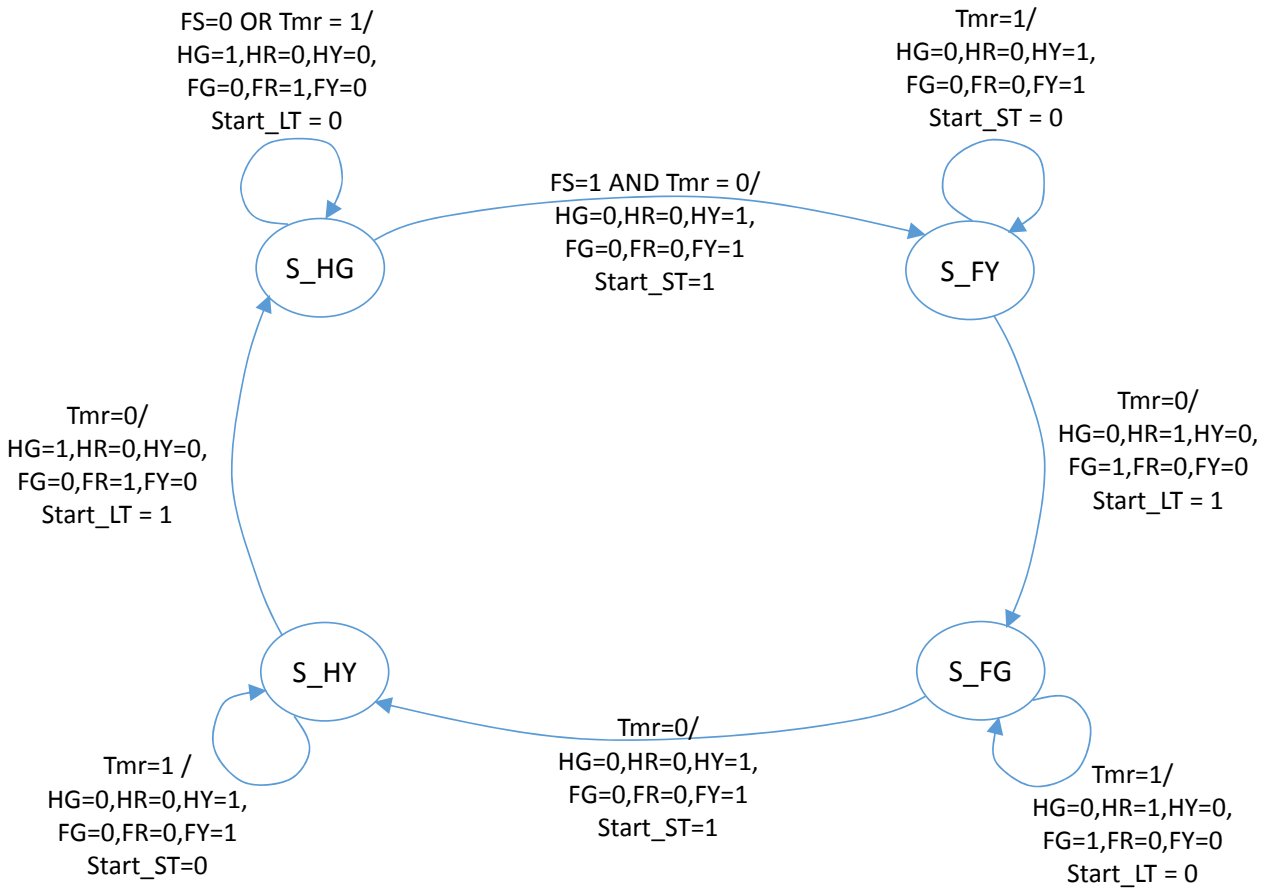


Design the traffic control FSM, taking the following into account:

- A traffic signal consists of three lights –Red, Yellow and Green. For each road and traffic direction, there is a traffic signal as shown in the diagram above.
 - The behavior of the two traffic signals for the two directions on the Highway is identical and this is also true for the two traffic signals for the two directions on the Farmroad.
 - For each traffic signal, only one light can be ON, the other two are OFF
 - To give priority to the Highway, by default the Highway green light HG is ON and the Farmroad red light FR is ON.
1. When the Highway traffic is enabled, if FS becomes 1, the traffic control FSM turns OFF HG and FR and turns ON HY and FY and starts a short timer by setting Start_ST to 1.
 2. When the short duration has elapsed, indicated by Tmr = 0, the traffic control FSM turns OFF the HY and FY lights, turns ON the HR and FG lights and at the same time starts the long timer by setting Start_LT to 1.
 3. When the long duration has elapsed, indicated again by Tmr = 0 it is time to block the Farmroad traffic again and enable the Highway traffic. This is done by turning OFF HR and FG and turning ON HY and FY and starting the short timer by setting Start_ST to 1
 4. When the short duration has elapsed, indicated by Tmr=0, the traffic control FSM turns OFF the HY and FY lights, turns ON the HG and FR lights and starts long term timer with a cycle long clock pulse.
 5. When Tmr=0, indicating that the long duration has elapsed and it is time to wait for the FS to become 1 again. And *when* it does, repeat the steps from 1 above.

Draw the state diagram and the state-transition table for a Mealy FSM.

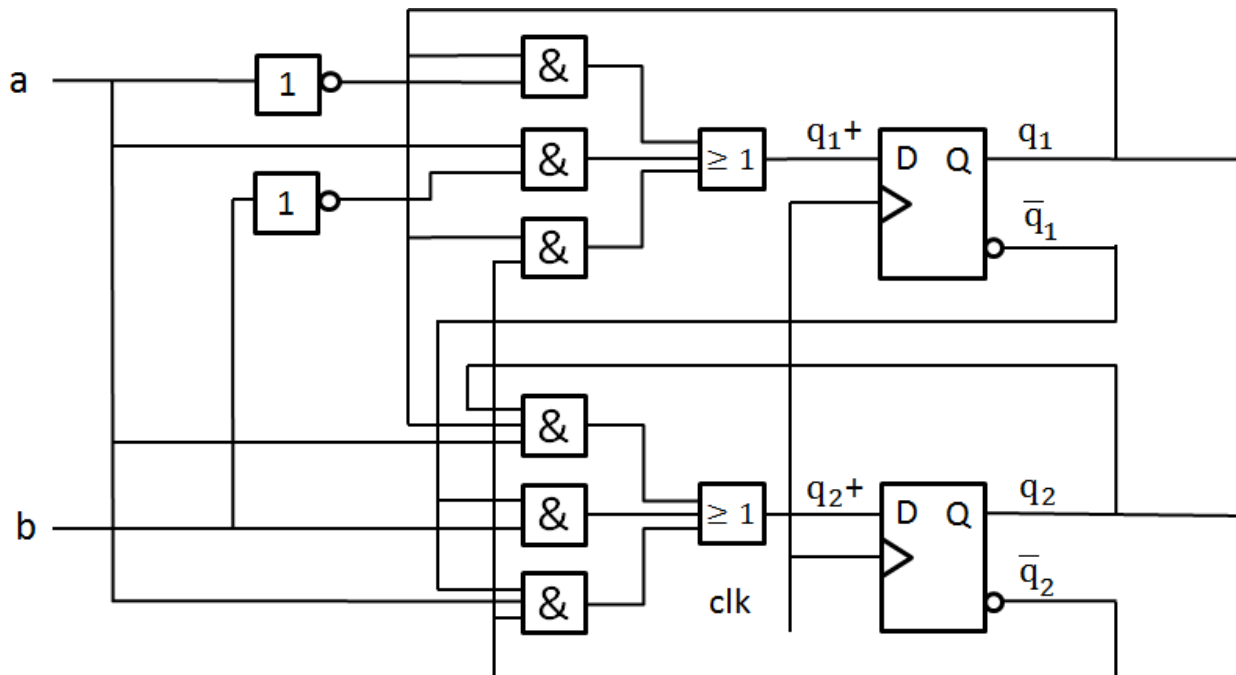
Solution:



Inputs		Present State	Next State	Outputs							
FS	Tmr			Start_ST	Start_LT	HG	HY	HR	FG	FY	FR
-	1	S_HG	S_HG	0	0	1	0	0	0	0	1
0	-	S_HG	S_HG	0	0	1	0	0	0	0	1
1	0	S_HG	S_FY	1	0	0	1	0	0	1	0
-	1	S_FY	S_FY	0	0	0	1	0	0	1	0
-	0	S_FY	S_FG	0	1	0	0	1	1	0	0
-	1	S_FG	S_FG	0	0	0	0	1	1	0	0
-	0	S_FG	S_HY	1	0	0	1	0	0	1	0
-	1	S_HY	S_HY	0	0	0	1	0	0	1	0
-	0	S_HY	S_HG	0	1	1	0	0	0	0	1

14. (2p)

A synchronous state machine with inputs a and b has been designed with two D flip-flops, as seen below.



a) (1p) Calculate the maximum clock frequency.

Assume that $t_{\text{Setup}} = 5 \text{ ns}$, $t_{\text{Hold}} = 1 \text{ ns}$, $t_{\text{Gate}} = 5 \text{ ns}$, and $t_{\text{CLK2Q}} = 10 \text{ ns}$.

In an attempt to increase the reaction speed of the circuit and to reduce the gate count, the synchronous state machine is changed to an asynchronous state machine by removing the D flip-flops. For the analysis below, you can insert a delay element in place of each D flip-flop.

b) (1p) There is static hazard in at least one of the next-state functions. Specify new, hazard-free next-state functions for q_1+ and q_2+ . The excitation table must be unchanged.

Hint: Write down the next-state functions for q_1+ and q_2+ and draw Karnaugh maps.

Solutions:

a)

Since t_{Hold} is much smaller than the other delays, this imposes no limitation.

T_{clock} should be greater than $t_{\text{Setup}} + 2 \times t_{\text{Gate}} + t_{\text{CLK2Q}} = 5 + 10 + 10 \text{ ns} = 25 \text{ ns}$

f_{max} is less than the inverse of T_{clock} so $1/25 \text{ ns} = 40 \text{ MHz}$

b)

From the circuit diagram:

$$q_2 += q_2 q_1 a + \bar{q}_1 b + \bar{q}_2 \bar{q}_1 a$$

$$q_1 += q_1 \bar{a} + \bar{b} a + \bar{q}_2 q_1$$

		ba			
		00	01	11	10
q ₂ q ₁	00	0	1	1	1
	01	0	0	0	0
	11	0	1	1	0
	10	0	0	1	1

		ba			
		00	01	11	10
q ₂ q ₁	00	0	1	0	0
	01	1	1	1	1
	11	1	1	0	1
	10	0	1	0	0

Add Hazard cover (indicated by dashed circling):

$$q_2 += q_2 q_1 a + \bar{q}_1 b + \bar{q}_2 \bar{q}_1 a + q_2 b a$$

$$q_1 += q_1 \bar{a} + \bar{b} a + \bar{q}_2 q_1 + q_1 \bar{b}$$

15. (1p)

A 4 bit two's complement adder has operands (a₃, a₂, a₁, a₀) and (b₃, b₂, b₁, b₀) to produce the sum (s₄, s₃, s₂, s₁, s₀). Write boolean expression to detect a) overflow and b) underflow.

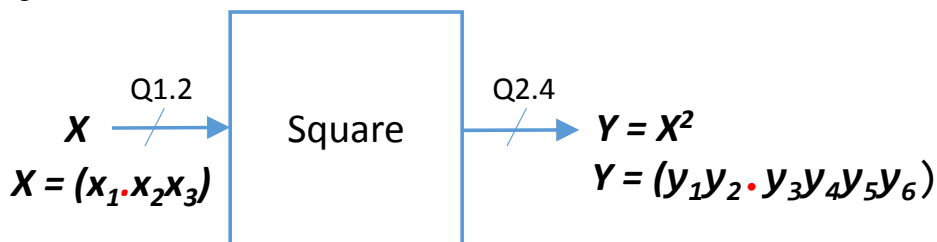
Solution:

Overflow = $\bar{a}_3 \text{ AND } \bar{b}_3 \text{ AND } s_3$

Underflow = $a_3 \text{ AND } b_3 \text{ AND } \bar{s}_3$

16. (3p)

A variable X is represented in two's complemented fixed point representation in the format Q1.2 (One integer bit and two fractional bits) and it is squared X^2 and represented in Q2.4 format as shown in the diagram below



- a) (1p) Perform X^2 and represent it in Q2.4 format. Hint: You need to perform only three binary multiplication of positive numbers. Note that $(-X \cdot -X) = X \cdot X$
- b) (1p) Draw the truth table to implement the Square function based on your results in the previous step. The truth table will have three input columns corresponding to (x_1, x_2, x_3) and six output columns corresponding to $X^2 = Y = (y_1, y_2, y_3, y_4, y_5, y_6)$
- c) (1p) Write the logic equations for the outputs as sum of minterms from the truth table. No need for minimization using Karnaugh Map or boolean identities.

Solution:

X	$x_1x_2x_3$	y_1	y_2	y_3	y_4	y_5	y_6	X^2
0.00	0.0 0	0	0.	0	0	0	0	0.0000
0.25	0.0 1	0	0.	0	0	0	1	0.0625
0.50	0.1 0	0	0.	0	1	0	0	0.2500
0.75	0.1 1	0	0.	1	0	0	1	0.5625
-1.00	1.0 0	0	1.	0	0	0	0	1.00
-0.75	1.0 1	0	0.	1	0	0	1	0.5625
-0.50	1.1 0	0	0.	0	1	0	0	0.2500
-0.25	1.1 1	0	0.	0	0	0	1	0.0625

$$y_1 = 0$$

$$y_2 = x_1 x_2' x_3'$$

$$y_3 = x_1' x_2 x_3 + x_1 x_2' x_3$$

$$y_4 = x_1' x_2 x_3' + x_1 x_2 x_3'$$

$$y_5 = 0$$

$$y_6 = x_1' x_2' x_3 + x_1' x_2 x_3 + x_1 x_2' x_3 + x_1 x_2 x_3$$

Submission sheet for Part A1 sheet 1

(remove and hand in together with your answers for part A2 and part B)

Last name: _____ Given name: _____

Personal code: _____ Sheet: 1

Write down your answers for the questions from Part A1 (1 to 10)

Question	Answer
1	$f(x, y, z) = \{SoP_{\text{min terms}}\} = ?$
2	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> $x = x_3 \ x_2 \ x_1 \ x_0$ $y = y_4 \ y_3 \ y_2 \ y_1 \ y_0$ </div> <div style="text-align: center;"> $M = 1, 0$ </div> </div>
3	(Two's complement number) $s_{16} = ?$
4	$F(A, B) = \{SoP\}_{\text{min}} = ?$
5	
6	$C(A, B) = ?$
7	Final state = ?

