KTH Informations- och kommunikationsteknik

Written exam
IE1204/5 Digital Design
Monday 23/10 2017 14.00-18.00

General Information

Examiner: Ingo Sander.

Teacher: Kista, William Sandqvist

Exam text has to be returned when you hand in your writing.

Aids: No aids are allowed!
The exam consists of three parts with a total of 14 tasks, and a total of 30 points:

Part A1 (Analysis) containes ten short questions. Right answer will give you one point. Incorrect answer will give you zero points. The total number of points in Part A1 **is 10 points**. To **pass the Part A1 requires at least 6p**, *if fewer points we will not look at the rest of your exam.*

Part A2 (Methods) contains two method problems on a total of 10 points.

To **pass the exam** requires at least **11 points** from A1 + A2 , *if fewer points we will not look at the rest of your exam.*

Part B (Design problems) contains two design problems of a total of 10 points. Part B is corrected only if there are at **least 11p** from the exam A- Part.

NOTE ! At the end of the exam text there is a submission sheet for Part A1, which shall be separated and be submitted together with the solutions for A2 and B.

For a passing grade (**E**) requires at **least 11 points on the exam**. If exactly 10p from A1(6p)+A2(4p), (FX), completion to (E) will be offered.

Grades are given as follows:

0 –	11 –	16 –	19 –	22 –	25
F	E	D	C	B	A

The result is expected to be announced before Monday 13/11 2017.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

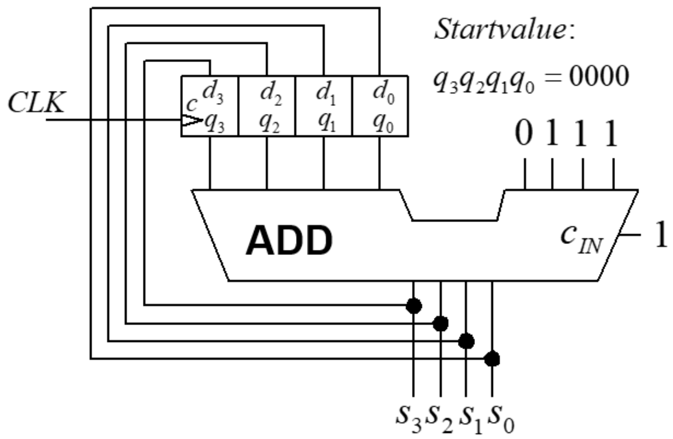
1. 1p/0p
A function $f(x, y, z)$ is described as:

$$f(x, y, z) = y\left(\overline{x \oplus z}\right) + x \oplus z$$

Write down the function as a product of sums (maxterms).

$$f(x, y, z) = \{PoS_{Maxterms}\} = ?$$

2. 1p/0p
A counter consists of four D-flip-flops and a 4-bit adder. The flip-flops are clocked simultaneously. See the figure. The counter starts with all flip-flop at zero $q_3q_2q_1q_0$ = 0000. What will the sequence bee from start and for the following four clockpulses?
$s_3s_2s_1s_0 = \quad \rightarrow \quad \rightarrow \quad \rightarrow \quad \ldots ?$



3. 1p/0p
Two, two's complement 4-bit numbers are (hexadecimal) $x = B_{16}$ och $y = E_{16}$. What will the subtraction $s = x - y$ be? Express this number s as a decimal number with sign $\pm s_{10}$ = ?

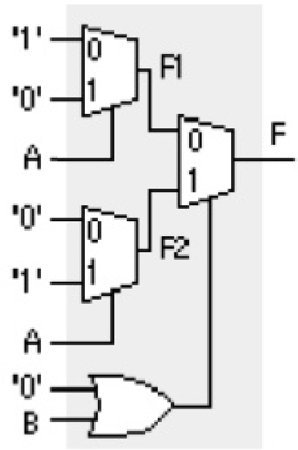
4. 1p/0p
Given is a Karnaugh map for a function of four variables $Y = f(x_3, x_2, x_1, x_0)$. Write the function Y_{min}, as a minimized product of sums, on **PoS** form. "-" in the map means "don't care".

x_3x_2 \ x_1x_0	00	01	11	10
00	0: -	1: 1	3: 0	2: 1
01	4: -	5: -	7: 0	6: 0
11	12: 0	13: 1	15: 0	14: -
10	8: 1	9: 0	11: 0	10: -

5. 1p/0p

ACT1 are cheap programable circuits with multiplexors. The figure shows how such a logic element is constructed.
Which function $F(A, B)$ is implemented with this logic element?
Write the function on minimized SoP-form.

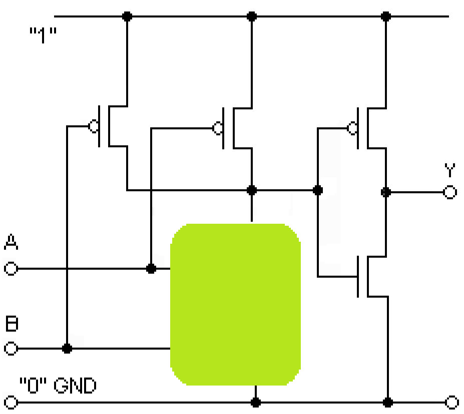
$$F(A,B) = \{SoP\}_{\min} = ?$$



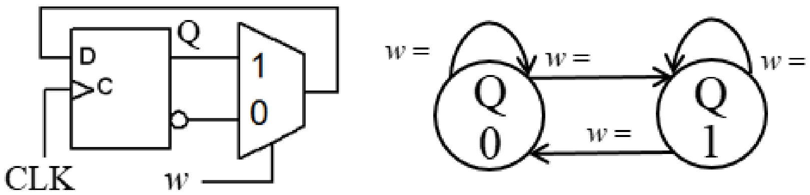
6. 1p/0p

What function has this CMOS gate? Unfortunately some part of the PullDown net is unreadable (coated with green color), but probably you can still figure out the function?

$$Y(A,B) = ?$$

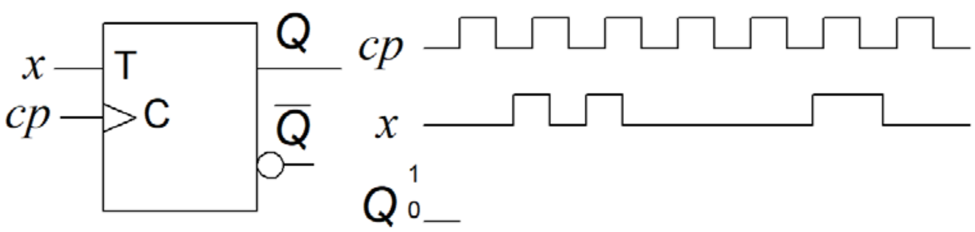


7. 1p/0p



Write the transition conditions for $\boldsymbol{w}$ at the arrows in the state diagram.
Answer on the submission sheet.

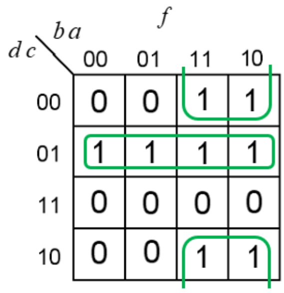
8. 1p/0p



A T-flip-flop starts with $Q = 0$. The signal x is connected to the T-input. Complete the timing diagram for the output signal Q. Answer on the submission sheet.

9. 1p/0p

The function f in the Karnaugh map is to be used in an asynchronous sequence circuit. Two groupings (terms) are done in the map. Which extra term has to be added as a Hazard Cover?



$HazardCover = \ ?$

10. 1p/0p

The VHDL code below describes some kind of ”frequency divider”. Suppose that the **Input clock** `clk` has the frequency 100 MHz. What will then the frequency for **Output clock** `cout` be?

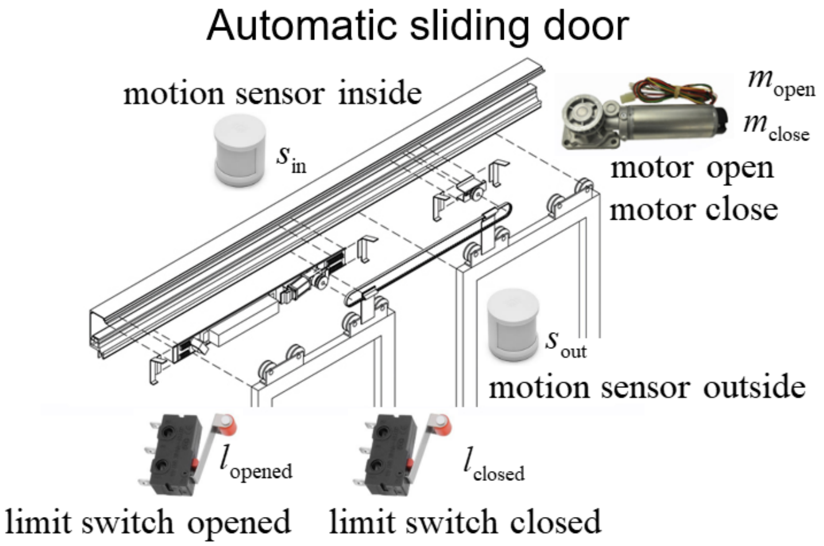
```
ENTITY clk_div IS
PORT (
        cout   :out std_logic; -- Output clock
        clk    :in  std_logic; -- Input clock
     );
END ENTITY;

ARCHITECTURE rtl OF clk_div IS
     SIGNAL flipflop_q :std_logic;
BEGIN
     PROCESS(clk) BEGIN
          IF (rising_edge(clk)) THEN
            flipflop_q <= not flipflop_q;
          END IF;
     END PROCESS;
     cout <= flipflop_q;
END ARCHITECTURE;
```

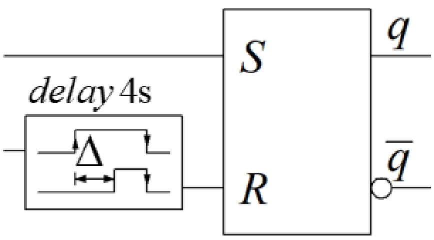
Part A2: Methods

Note! Part A2 will only be corrected if you have passed part A1 (≥6p)

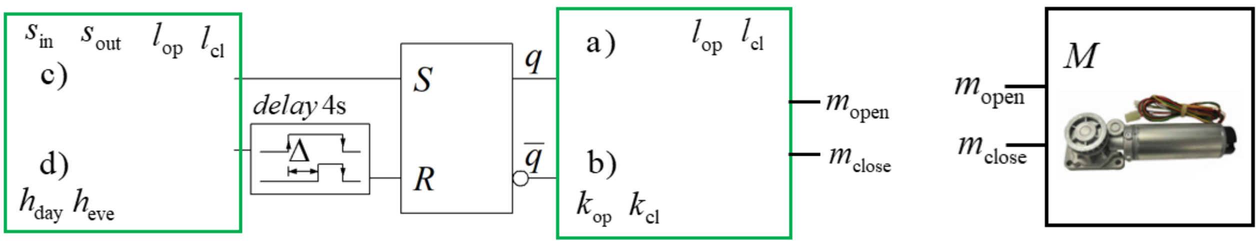
11. 4p

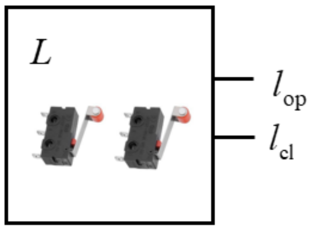


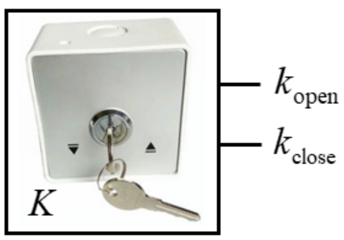
An automatic door is controlled by a SR-latch. The S input opens the door and the R input closes the door, but after at least a 4 seconds delay (this delay circuit is included in the figure and will not have to be constructed).
You will have to construct the logical circuits needed in step a) b) c) d). Use any optional gates. You don't need to minimize the logic, but strive to not use unnecessary many gates.



The block diagram below shows where the gates from the different sub tasks (a, b, c, d) will fit in.



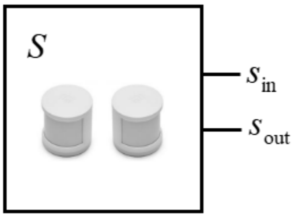




a) Signal q opens the door by having m_{open} = 1 until the door reaches the limit switch l_{opened} . Signal $\bar{q}$ closes the door by having m_{close} = 1 until the door reaches the limit switch l_{closed} .
Limit switches: l_{opened} = 0 when the doors are full open. l_{opened} = 1 otherwise. l_{closed} = 0 when doors are closed. l_{closed} = 1 otherwise.

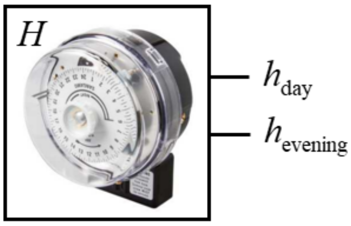
Draw gates for this function.

b) An operator should be able to open and close the doors directly, with a key, *K*, regardless of the signals from the SR-latch.
k_{open} = 1 door must open.
k_{close} = 1 door must close.
When k_{open} and k_{close} = 0 the operator will not effect the function any more. Draw gates for this function.



c) Motion sensors s_{out} and s_{in} becomes = 1 when any person is close to respective sensor. This should activate the latch S input to open the door.

If *no* person is close to the sensors, and if the door is fully open, this should activate the latch R input (after the 4s delay) to close the door. Draw gates for this function.



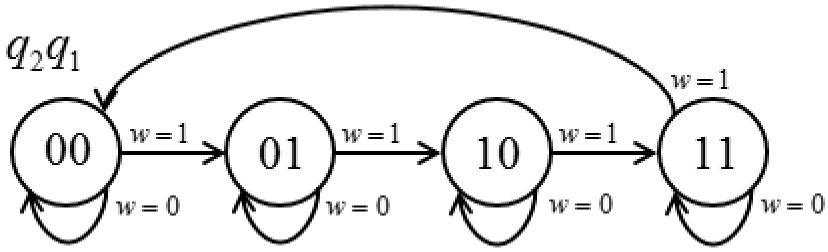
d) A timer *H* (with two separate actions/output signals per day) controls the door during the day. The door will be closed at night

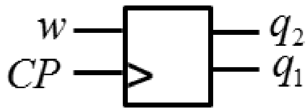
h_{day} = 1 during open daytime. The door should then open by the motion sensors for visitors to ***enter*** or to ***leave*** the building. h_{day} = 0 all other time (at night).

$h_{evening}$ = 1 during 30 minutes after the building closes. Door should then ***open*** for visitors ***leaving*** the building, but be ***closed*** for visitors to ***enter***. $h_{evening}$ = 0 other time. Draw gates for this function..

12. 6p

Construct a synchronous binary code counter with an input signal *w* that follows the state diagram below.



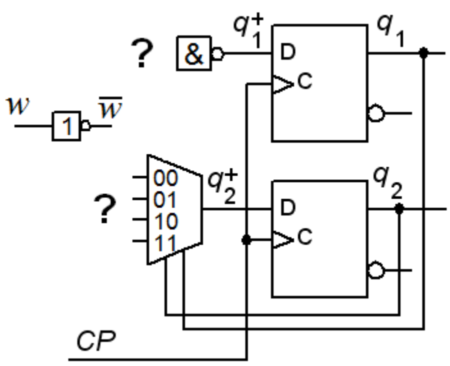


a) (1p) Set up the encoded state table.

$q_2^+ q_1^+ = f(w q_2 q_1)$

(2p) Derive minimized expressons for next state

$q_2^+ = ?$ $q_1^+ = ?$



b) (1p) Realize the sequence network with D flip-flops. Use NAND-gates for function q_1^+ according to the figure.

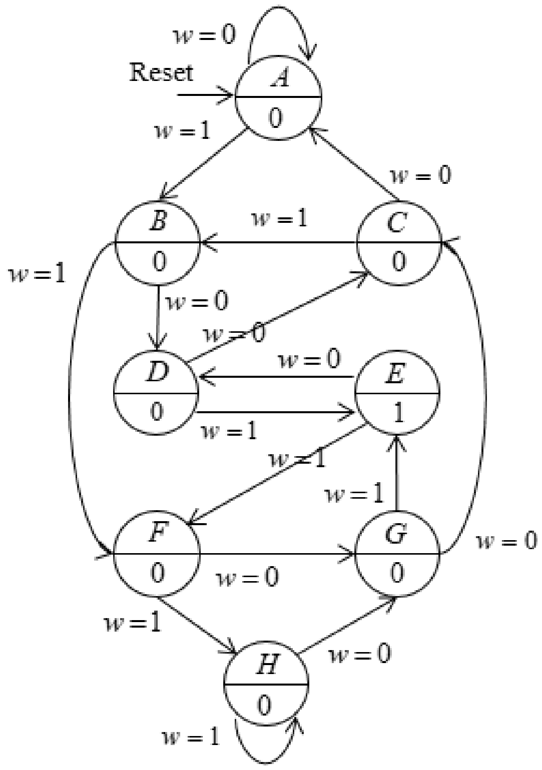
(1p) Use a 4:1 Multiplexor for function q_2^+ according to the figure. The answer must be motivated. Draw your solution.

$q_2^+(q_2 q_1, w): mux_{00} = ?, \quad mux_{01} = ? \quad mux_{10} = ?, \quad mux_{11} = ?$

c) (2p) At right there are a state diagram for ***another*** synchronous sequential circuit with eight states (A … H).

State minimize this diagram.

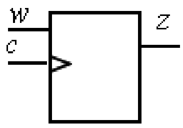
Answer with the *minimized* **state table** and **state diagram**.



Part B. Design Problems

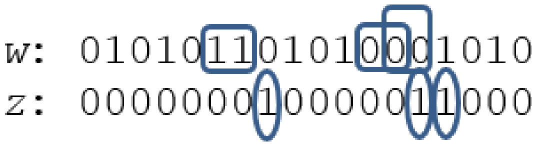
Note! Part B will only be corrected if you have passed part A1+A2 (≥11p).

13. 5p Synchronous sequential circuit. Detector for specific events.
Detect when there are at least two zeroes following after each other ..00.. or at least two ones ..11.. in the sequence of synchronous bits entering the input *w*.



The circuit starts with *w* = 0 which means that one zero has entered the input.

Detector output *z* should be '1' in the clock interval directly after the sequences has occurred.



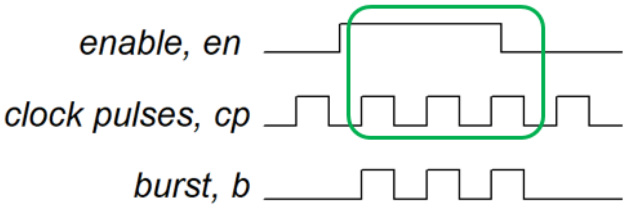
The sequence circuit is a Moore machine with positive edge triggered D-flip-flops.

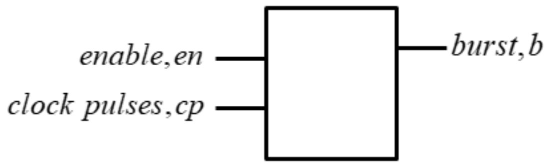
a) (2p) Draw the **State Diagram** and set up the **State Table**.

b) (2p) Set up the **Encoded State Table**, and use optional state code. Derive minimized expressions for **Next State decoder** and **Output decoder**

c) (1p) Draw **Schematic**, use any optional gates.

14. 5p Synchronized burst.





An **asynchronous sequential** circuit has two inputs, *enable* ***en*** and *clock pulses* ***cp***. As long as ***en*** = 1 complete pulses (synchronized with ***cp***) should be output as *burst* ***b***. This should happen as fast as a complete pulse (***cp*** = 1) is possible. If ***en*** gets = 0 during an ongoing pulse then this pulse will also be output completly. The signal ***en*** is allways longer than the pulse ***cp*** and the signal ***en*** will arrive with long intervals. See the timing diagram for a typical case.

a) (2p) Draw the **state diagram** and set up a proper **flow table** for the sequential circuit.

b) (2p) Make a suitable **state assignment** with an **exitation table** that provides circuits that are free from critical race (comment on how you achieved this). You will also develop the hazard free **expressions** for the **next state** (comment on how you achieved this) as well as an expression for **output**.

c) (1p) Draw the circuit diagram. (Use optional gates).

Good Luck!

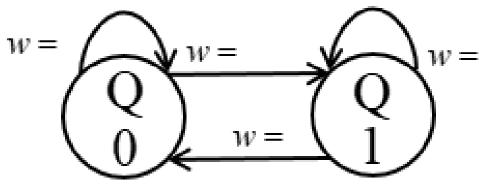
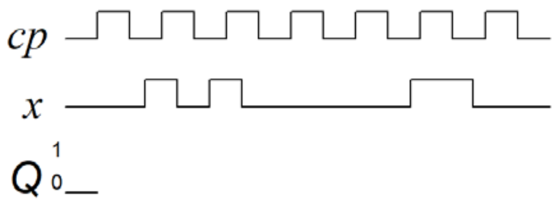
Submission sheet for Part A1 Sheet 1

(remove and hand in together with your answers for part A2 and part B)

Last name: ______________________________ **Given name:** ______________________________

Personal code: ______________________________ **Sheet:** 1

Write down your answers for the questions from Part A1 (1 to 10)

Question	Answer
1	$f(x,y,z) = \{PoS_{Maxterms}\} = ?$
2	$s_3 s_2 s_1 s_0 =$ $\rightarrow$ $\rightarrow$ $\rightarrow$
3	(Two complement numbers) $B_{16} - E_{16} = \pm s_{10} = ?$
4	$Y = \{PoS\}_{\min} = ?$
5	$F(A,B) = \{SoP\}_{\min} = ?$
6	$Y(A,B) = ?$
7	
8	
9	$HazardCover = ?$
10	$f_{cout} =$ [MHz]

This table is completed by the examiner!!

Part A1 (10)	**Part A2** (10)		**Part B** (10)		**Total** (30)	
Points	11	12	13	14	Sum	Grade