Lösningar Skriftlig Tentamen
IE1204 Digital Design
2022-04-21

Examiner/Examinator: Carl-Mikael Zetterling
Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

Swedish/Svenska:
Tentamenstexten ska lämnas in när lösningarna lämnas in.
Inga tillåtna hjälpmedel utom linjal.
Examen består av två delar:
Del 1 har 16 uppgifter med max 1 poäng per uppgift som ska besvaras på ”Answer Form”.
Del 2 har 4 uppgifter med max 4 poäng per uppgift som ska besvaras på separat papper.
Lämna in båda delar samtidigt. Disponera tiden själv mellan delarna.
Uppgifterna är inte ordnade efter svårighetsgrad.
Om slutsumman av tentan har halvpoäng avrundas det uppåt.

X = 1 om studenten har minst 8 poäng på del 1
Y = 1 om studenten har minst 16 poäng totalt
P = 1 om studenter får godkänt på tentamen
Fx = 1 om studenten kan godkännas efter en extra uppgift

X	Y	P	Fx
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Totalt max 32 poäng på tentamen.
För godkänt krävs
(minst 8 poäng på del 1) OCH (minst 16 poäng totalt)
Fx om något villkor ej är uppfyllt med en poängs marginal.

Betygskalan för tentamen förutsatt att studenten har minst 8 poäng från del 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

Resultat meddelas inom tre veckor.

Extended Solutions Written Exam
IE1204 Digital Design
2022-04-21

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English:
The exam text should be handed in after the exam.
No aids allowed except ruler.
The exam consists of two parts:
Part 1 has 16 exercises for max 1 point per exercise to be answered on the "Answer Form".
Part 2 has 4 exercises for max 4 points per exercise, to be answered on a separate paper.
Hand in both parts at the same time. Plan the time yourself between the parts.
The exercises are not in order of difficulty.
If the total sum of the exam has half points this will be rounded up.

X = 1 if student has at least 8 points from part 1
Y = 1 if student has at least 16 points in total
P = 1 if student passes exam
Fx = 1 if a student can pass after an extra task

X	Y	P	Fx
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

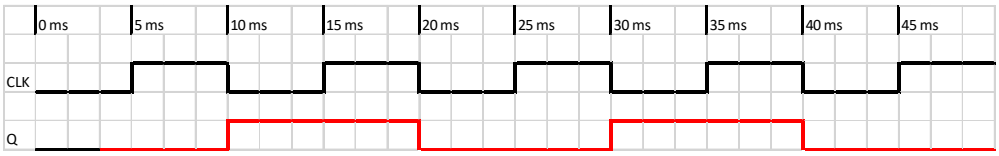
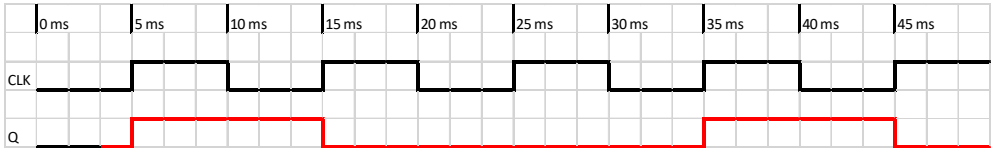
Total max of 32 points on the exam.
To pass the exam requires
(at least 8 points from part 1) AND (at least 16 points in total)
Fx if any condition is not fulfilled by one point's margin.

Grades are given as follows provided the student has at least 8 points from part 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

The result will be announced within three weeks.

IE1204 Digital Design Answer Form 2021-2022

Full Name		Personal Number								Program
Exam 2022-04-21		YYYYMMDD-XXXX								NN
#	Answer with	Answer								Points
1	Hexadecimal number	D6F2								1
2	8 bit two's complement binary number	0	1	1	1	0	0	1	0	1
3	8 bit two's complement binary number	1	1	0	1	0	1	1	0	1
4	Circuit number(s)	#4 and #5								1
5	Boolean expression, Y =	$\overline{C} \cdot D + B \cdot C$								1
6	Boolean expression, Y = $B \cdot \overline{C} + \overline{C} \cdot D + C \cdot \overline{D} = B \cdot \overline{C} + C \oplus D = (B + C + D)(\overline{C} + \overline{D})$									1
7	MUX connections									1
	Row CD = 00	$\overline{A \cdot B}$								
	Row CD = 01	$\overline{B}$								
	Row CD = 10	$A \oplus B$								
	Row CD = 11	$A \cdot B$								
8	Timing diagram									1
9	Timing diagram									1
10	Maximum clock frequency =	5 GHz								1
11	Next state $Q_D Q_C Q_B Q_A$ =	1000								1
12	16 bit two's complement Product A x B MSB	1	1	1	1	1	1	1	0	1
	LSB	0	1	1	1	1	0	1	0	
13	8 bit two's complement Quotient A / B	0	0	0	0	0	1	0	0	1
	Remainder	0	0	0	0	0	0	1	0	
14	Decimal number	-6.5								1
15	5 result bits (S4 S3 S2 S1 S0)				0	0	1	0	1	1
16	ALUControl (2 bits)	(Add)						0	0	1
TOTAL POINTS		Examiner sign								16

Del 1/Part 1, 1 point per exercise, fill in on "Answer Form"

1 Number Conversion

Swedish: Talet A är ett 16 bitars binärt tal.
Konvertera till ett hexadecimal tal.

English: The number A is an 16-bit binary number.
Convert to a hexadecimal number.

$A = 1101\ 0110\ 1111\ 0010_2$
Divide into groups of four bits, and convert each group to hexadecimal → D6F2

2 Addition

Swedish: Konvertera A och B från decimala till 8 bitars två-komplement kodade tal.
Beräkna A + B (binärt) och svara med ett 8 bitars två-komplement kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: Convert A and B from decimal to 8-bit binary (two's complement) numbers.
Calculate A + B (binary) and answer with an 8-bit binary (two's complement) number.
You can check your calculations using decimal numbers.

$A = 71_{10}$ 01000111
$B = 43_{10}$ + 00101011
A + B = 01110010 = 114_{10}

3 Subtraction

Swedish: Konvertera A och B från decimala till 8 bitars två-komplement kodade tal.
Beräkna A - B (binärt) och svara med ett 8 bitars två-komplement kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: Convert A and B from decimal to 8-bit binary (two's complement) numbers.
Calculate A - B (binary) and answer with an 8-bit binary (two's complement) number.
You can check your calculations using decimal numbers.

$A = 38_{10}$ 00100110
$B = 80_{10}$ 01010000
$-B = -80_{10}$ + 10110000
A - B = 11010110 = -42_{10}

4 CMOS

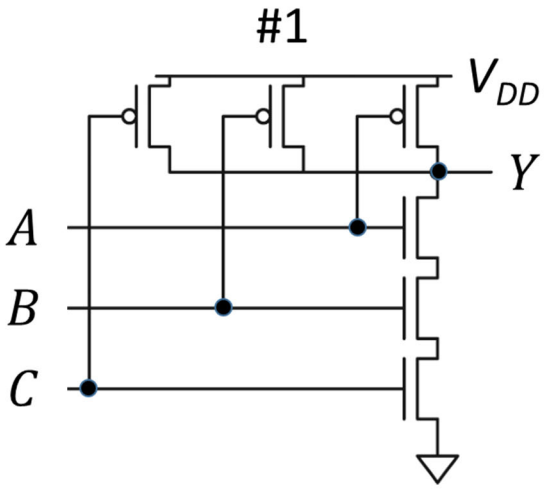
Swedish: Bestäm vilken/vilka av CMOS-grindnäten nedan som har den logiska funktionen Y.
Det kan finnas mer än ett korrekt svar.

English: Determine which of the CMOS-circuits below have the logic function Y.
There may be more than one correct answer.

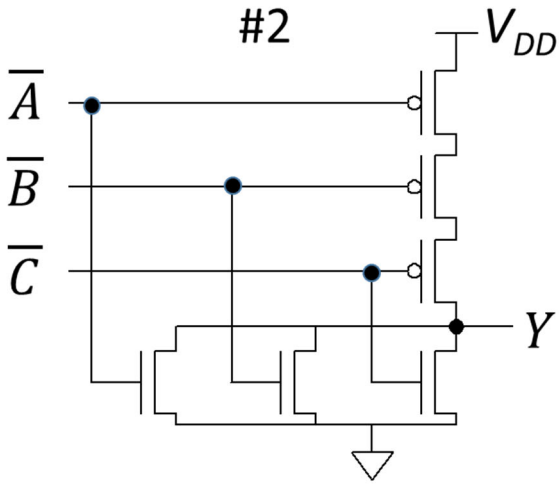
$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} = \overline{A + B + C}$$

(De Morgan's theorem), 3 input NOR

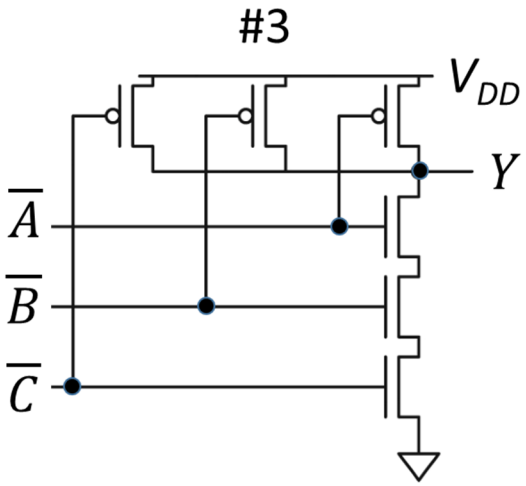
#1 $Y = \overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$ 3 input NAND



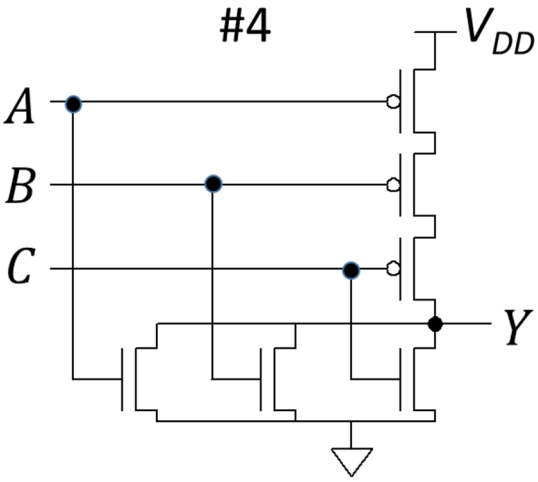
#2 $Y = \overline{\overline{A} + \overline{B} + \overline{C}} = A \cdot B \cdot C$ 3 input AND



#3 $Y = \overline{\overline{A} \cdot \overline{B} \cdot \overline{C}} = A + B +$ 3 input OR

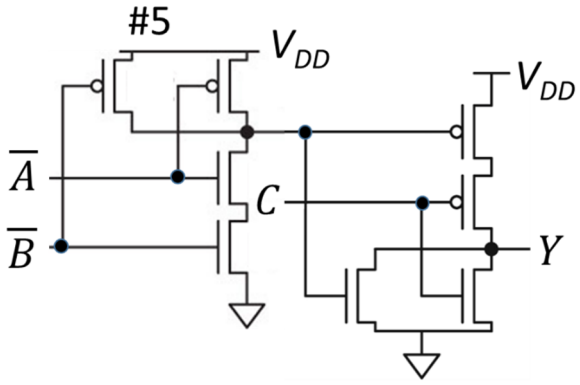


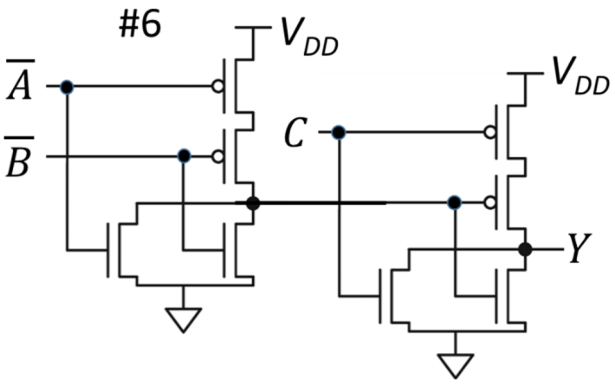
#4 $Y = \overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$ 3 input NOR



#5 $Y = \overline{\overline{\overline{A} \cdot \overline{B} + C}} = \overline{A} \cdot \overline{B} \cdot \overline{C} = \overline{A + B + C}$ 3 input NOR

#6 $Y = \overline{\overline{\overline{A} + \overline{B} + C}} = (\overline{A} + \overline{B})\overline{C} = \overline{A} \cdot \overline{C} + \overline{B} \cdot \overline{C}$





Answer: #4 and #5

5 Boolean Algebra

Swedish: Ta fram enklast möjliga booleska uttryck.

English: Derive the simplest possible Boolean expression.

$$
\begin{aligned}
Y &= \overline{A} \cdot B \cdot \overline{C} \cdot D + A \cdot B \cdot C \cdot D + \overline{C} \cdot D + B \cdot D + B \cdot C \\
&= \overline{C} \cdot D\left(\overline{A} \cdot B + 1\right) + B \cdot D(A \cdot C + 1) + B \cdot C \\
&= \overline{C} \cdot D + B \cdot D + B \cdot C = \overline{C} \cdot D + B \cdot D\left(C + \overline{C}\right) + B \cdot C \\
&= \overline{C} \cdot D + B \cdot \overline{C} \cdot D + B \cdot C \cdot D + B \cdot C \\
&= \overline{C} \cdot D(1 + B) + B \cdot C(1 + D) = \overline{C} \cdot D + B \cdot C
\end{aligned}
$$

Can be verified with a K-Map:

$$Y = \overline{A} \cdot B \cdot \overline{C} \cdot D + A \cdot B \cdot C \cdot D + \overline{C} \cdot D + B \cdot D + B \cdot C = \overline{C} \cdot D + B \cdot C$$

Y	CD 00	CD 01	CD 11	CD 10
AB 00		1		
AB 01		1	1	1
AB 11		1	1	1
AB 10		1		

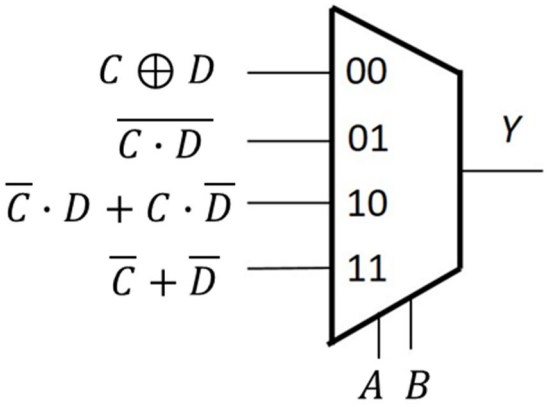
Y	CD 00	CD 01	CD 11	CD 10
AB 00		1		
AB 01		1	1	1
AB 11		1	1	1
AB 10		1		

6 MUX to K-map

Swedish: Fyll i K-Map från MUX-kopplingen.
Ta fram enklast möjliga booleska uttryck för Y från K-map. Välj PoS eller SoP.

English: Fill in the K-Map from the MUX circuit.
Derive simplest possible Boolean expression from the K-map. Select PoS or SoP.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	0	1	0	1
AB 01	1	1	0	1
AB 11	1	1	0	1
AB 10	0	1	0	1



$$B \cdot \overline{C} + \overline{C} \cdot D + C \cdot \overline{D} = B \cdot \overline{C} + C \oplus D = (B + C + D)(\overline{C} + \overline{D})$$

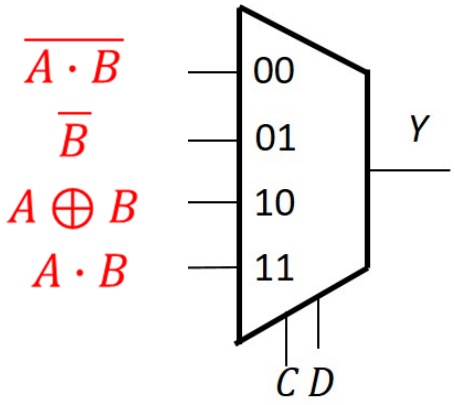
$$B \cdot \overline{C} \ \ can \ \ be \ \ replaced \ \ with \ \ B \cdot \overline{D} \ \ above$$

7 K-Map to MUX

Swedish: Använd en 4:1 MUX och valfria grindar eller 0 och 1 och gör en krets för K-map med CD som select-signaler.

English: Use a 4:1 MUX and any logic gates or 0 or 1 to draw a circuit for the K-map with CD as select signals.

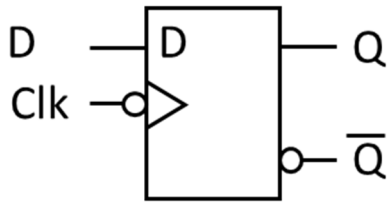
Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	1	0	0
AB 01	1	0	0	1
AB 11	0	0	1	0
AB 10	1	1	0	1



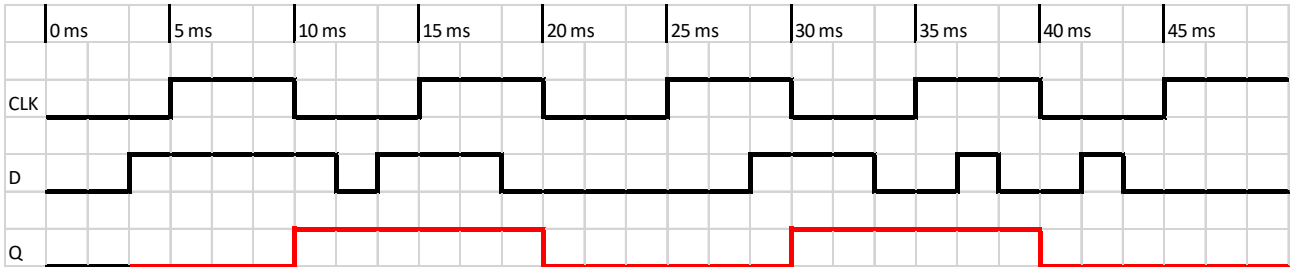
8 Timing diagram

Swedish: Rita tidsdiagram för D-vippan (D flip-flop) i ”Answer Form”.

English: Draw the timing diagram for the D flip-flop in the “Answer Form”.



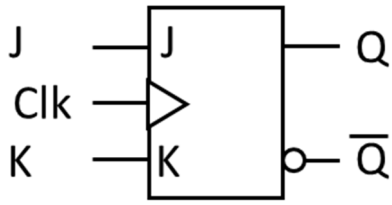
NOTE: negative edge



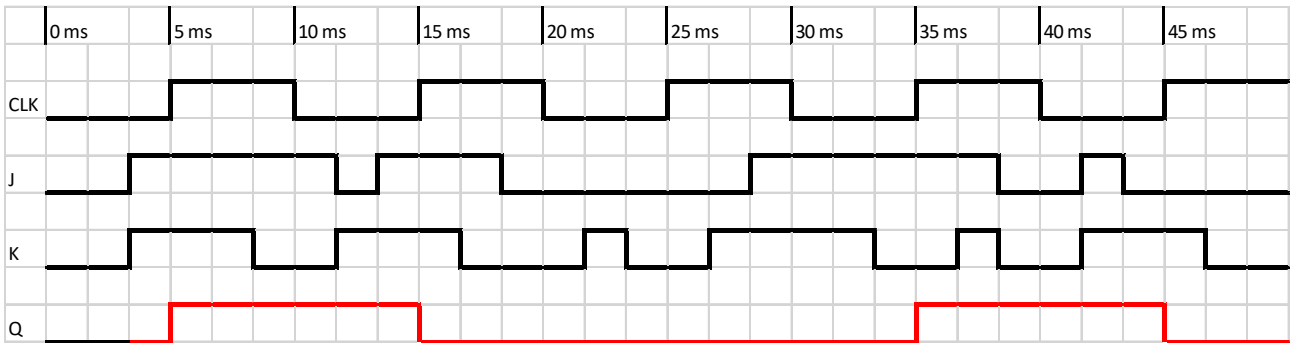
9 Timing diagram

Swedish: Rita tidsdiagram för JK-vippan (JK flip-flop) i ”Answer Form”.

English: Draw the timing diagram for the JK flip-flop in the “Answer Form”.



NOTE: positive edge



10 Timing calculation

Swedish: Beräkna maximal klockfrekvens för kretsen nedan.

English: Calculate the maximum clock frequency for this circuit.

Delay Per Register

t_{pcq} = 50 ps

t_{ccq} = 30 ps

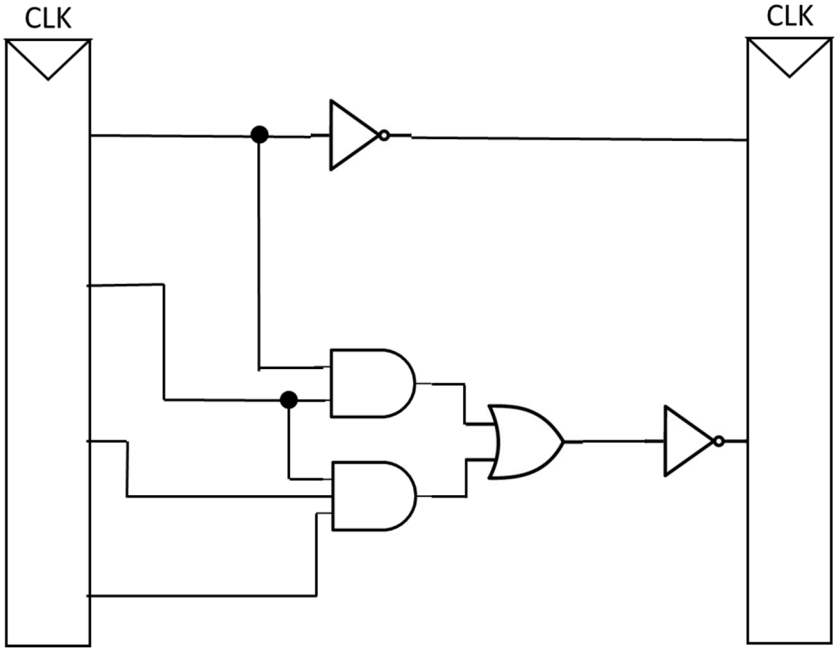
t_{setup} = 60 ps

t_{hold} = 60 ps

Delay Per gate:

t_{pd} = 30 ps

t_{cd} = 20 ps



The longest path is three gates

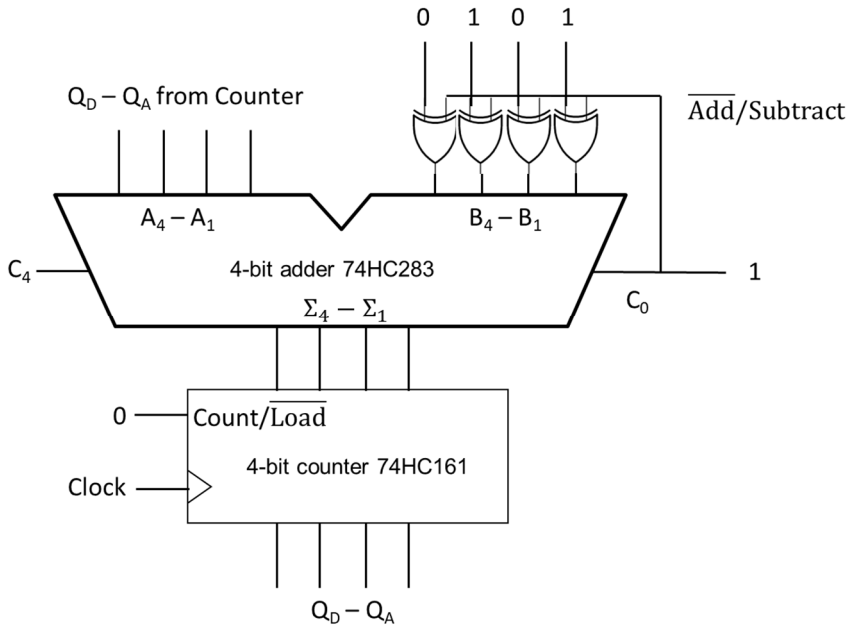
$T_c \geq t_{pcq} + t_{pd} + t_{setup} = 50 + 3 \times 30 + 60 = 200$ ps

$f_c = 1/T_c = 5$ GHz

11 Counter

Swedish: Räknaren nedan har kommit till tillstånd $Q_DQ_CQ_BQ_A = 1101$
Vad blir nästa tillstånd?

English: The counter below has counted to state $Q_DQ_CQ_BQ_A = 1101$
What is the next state?



Add 11 (subtract 5) for each clock, after 1101 (=13) comes 1000 (=8)

12 Multiplication

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A x B (binärt) och svara med ett 16 bitars två-komplement kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A x B (binary) and answer with a 16-bit binary (two's complement) number.
You can check your calculations using decimal numbers.

$A = 11110011_2$
$B = 00011110_2$ $=30_{10}$

A is negative, convert to positive: $-A = 00001101_2 = 13_{10}$
Multiply –A x B = B x (-A):

```
        00011110
      x 00001101
        00011110   1st multiplication
    + 00011110     2nd multiplication
      0010010110   add intermediate result first two rows
   + 00011110      add 3rd multiplication
0000000110000110   = 390₁₀  = 30 x 13

1111111001111010   Two's complement = A x B
```

13 Division

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A / B (binärt) och svara med kvot och rest (8 bitars två-komplement kodade tal).
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A / B (binary) and answer with quotient and remainder (8-bit binary two's complement numbers).
You can check your calculations using decimal numbers.

A = 00111010_2 $=58_{10}$
B = 00001110_2 $=14_{10}$

(A and B are both positive, nothing to convert)

```
         100  Quotient = 4, check: 4 x 14 = 56
1110/00111010
   -  1110
       00010  Remainder of 2
```

14 Fixed point

Swedish: Ett format för fixed point tal med tecken är att använda två-komplementtal med 4 bitar för talet och 4 bitar för bråkdelen. Omvandla A till ett decimalt tal.

English: One format for fixed point signed numbers is to use two's complement numbers with 4 bits for the integer and 4 bits for the fraction. Convert A to a decimal number.

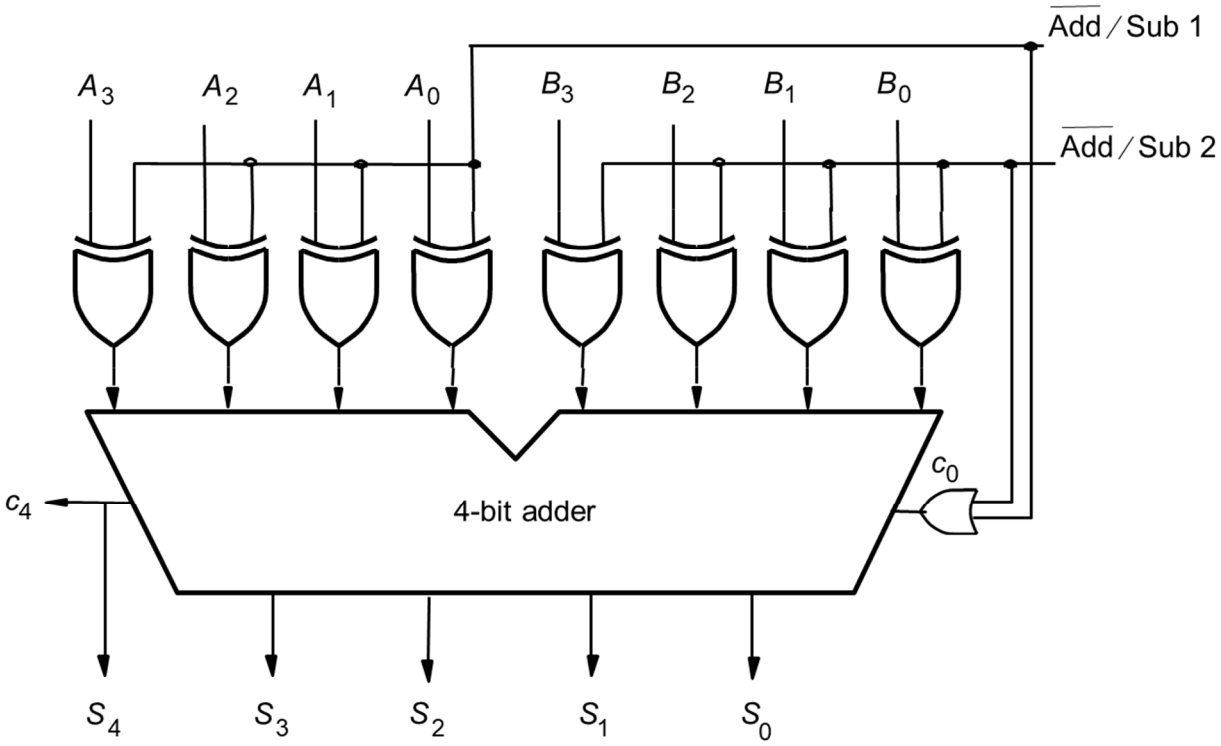
A = 1001.1000_2
A = - 8 + 1 + ½ = -7 + 0.5 = -6.5

15 Full Adder

Swedish: Vad blir resultatet från heladderarkretsen nedan?
Svara med 5 bitar (S4 S3 S2 S1 S0)

English: What is the result for the full adder circuit below?
Answer with 5 bits (S4 S3 S2 S1 S0)

A = 0001 B = 1100 $\overline{\text{Add}}/\text{Sub}\ \ 1 = 0$ $\overline{\text{Add}}/\text{Sub}\ \ 2 = 1$



B will be subtracted since $\overline{\text{Add}}/\text{Sub}\ \ 2 = 1$

A is not affected since $\overline{\text{Add}}/\text{Sub}\ \ 1 = 0$

S = A - B = 0001 – 1100 = 0001 + 0011 + 1 = 00101 (no carry out)

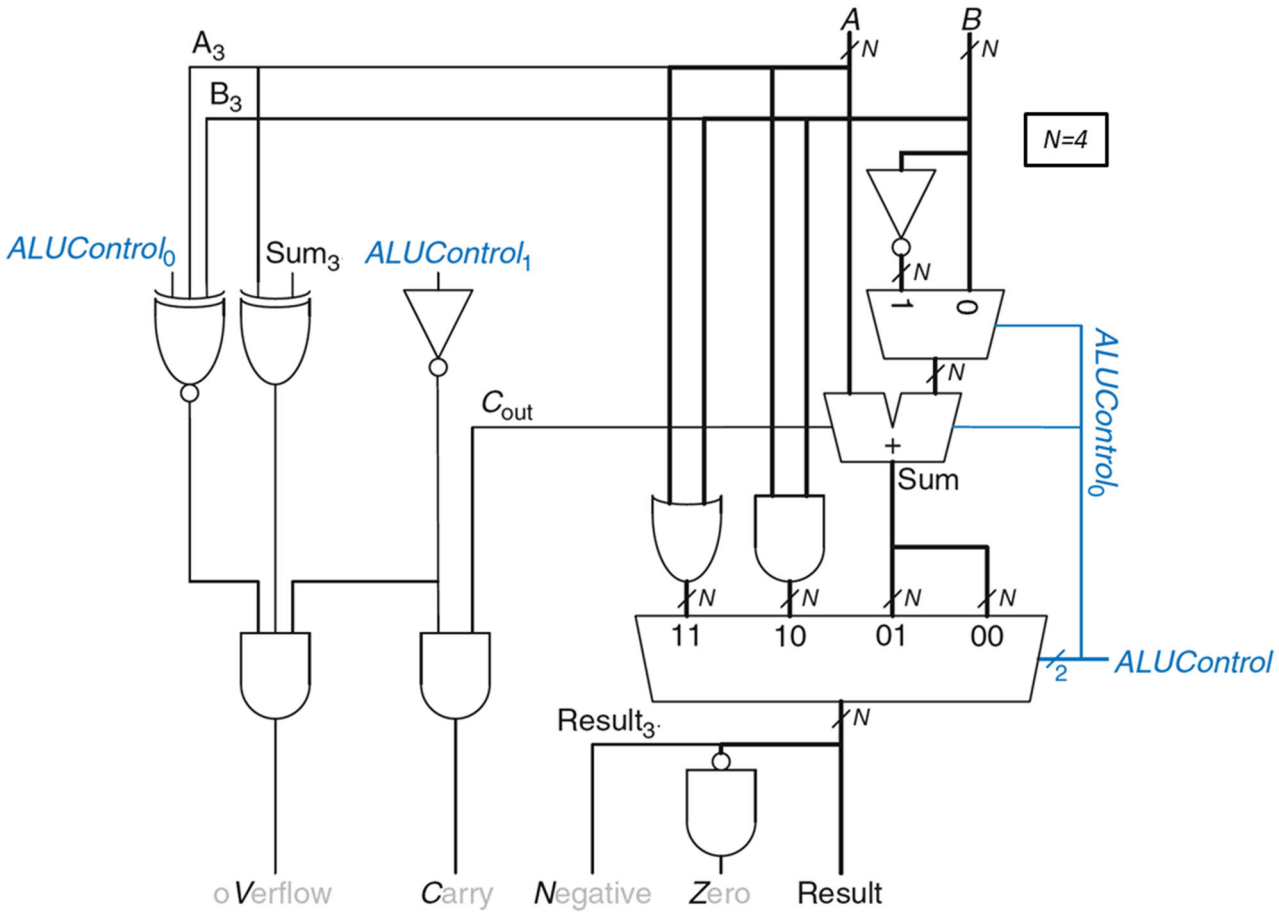
Check: A = 1, B = -4, S = 1 – (-4) = 5

16 ALU

Swedish: Med A och B enligt nedan blev flaggorna i ALU som visas.
Vilken instruktion genomfördes? Svara med 2 bitar för ALUControl.

English: Using A and B below, the flags gave the result shown.
Which instruction was executed? Answer with 2 bits for ALUControl.

A = 0110 B = 0011 → V C N Z = 1010



$ALUControl_{1:0}$	Function
0 0	Add
0 1	Subtract
1 0	AND
1 1	OR

Since N = 1 it was not a logic operation (A AND B = 0010, A OR B = 0111)

A + B = 0110 + 0011 = 1001 does not generate a carry (C = 0) but N= 1

A - B = 0110 – 0011 = 0110 + 1101 = 10011 generates a carry (C= 1, N=0), **Answer: 00**

Del 2/Part 2, 4 points per exercise, answer on separate paper

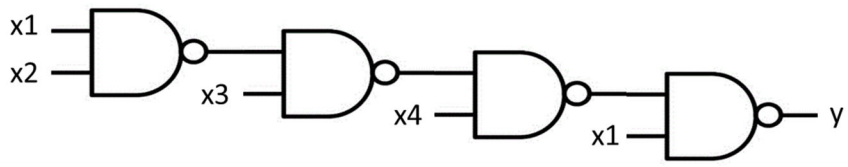
17 Analysis of Combinational Circuit

Swedish:

1. Ta fram booleskt uttryck för kretsen nedan.
2. Rita K-map för kretsen med variabelordning som i figuren.
3. Förenkla uttrycket med hjälp av K-map.
4. Rita ny krets med enbart NOR-grindar.

English:

1. Derive the Boolean expression for the circuit below.
2. Draw a K-map for the circuit with variables as in the figure.
3. Simplify the expression using the K-map.
4. Draw a new circuit using only NOR gates.

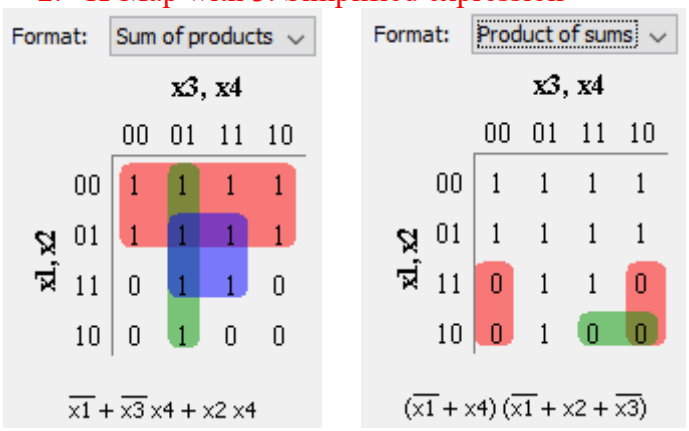


1. Boolean expression:

$$y = \overline{x1 \cdot \overline{x4 \cdot \overline{x3 \cdot \overline{x2 \cdot x1}}}} = \overline{x1} + \overline{x4 \cdot \overline{x3 \cdot \overline{x2 \cdot x1}}} = \overline{x1} + x4 \cdot \overline{\left(x3 \cdot \overline{x2 \cdot x1}\right)}$$
$$= \overline{x1} + x4 \cdot \left(\overline{x3} + x2 \cdot x1\right) = \overline{x1} + \overline{x3} \cdot x4 + x1 \cdot x2 \cdot x4 = \overline{x1} + \overline{x3} \cdot x4 + x2 \cdot x4$$

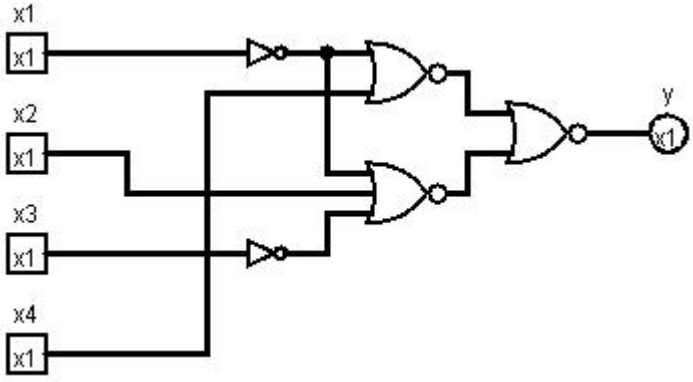

```
~(x1 ~(x4 ~(x3 ~(x2 x1))))
```

2. K-Map with 3. Simplified expression



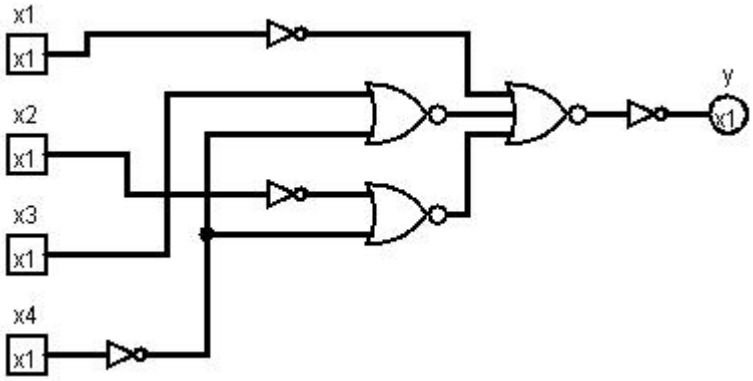
Use POS for NOR only (inverters are ok if you note that they can be made with a NOR)
No deductions if not simplest possible.

$$y = \overline{\overline{(\overline{x1} + x4)(\overline{x1} + x2 + \overline{x3})}} = \overline{\overline{\overline{x1} + x4} + \overline{\overline{x1} + x2 + \overline{x3}}}$$



For SoP you need double double inversion, and an extra NOR/Inverter at the output

$$y = \overline{\overline{\overline{x1} + \overline{\overline{x3} \cdot x4} + \overline{x2 \cdot x4}}} = \overline{\overline{x1} + \overline{x3} + \overline{x4} + \overline{x2} + \overline{x4}}$$



18 Design of Combinational Circuit

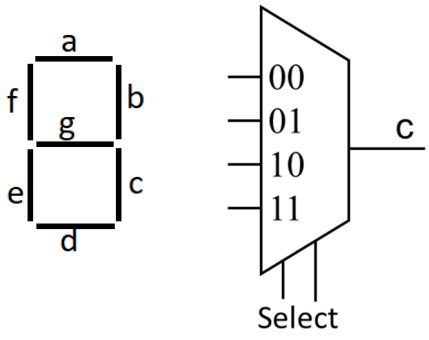
Swedish:
Konstruera kretsen för **c-segmentet** för en hexadecimal 7-segmentsdekoder.
Sanningstabellen är given nedan.

1. Rita K-map för sanningstabellen med variabelordning som i figuren.
2. Ta fram enklast möjliga booleska uttryck från K-map.
3. Rita en krets för uttrycket med enbart NAND-grindar.
4. Rita en krets för K-map som använder en 4:1 Mux, grindar och 0 och 1.

English:
Design the circuit for the **c-segment** of a hexadecimal to 7-segment decoder.
The truth table is given below.

1. Draw a K-map for the truth table with variables as in the figure.
2. Derive simplest possible Boolean expression from the K-map.
3. Draw a circuit for the expression using only NAND-gates.
4. Draw a circuit for the K-Map using a 4:1 Mux, gates and 0 and 1.

c	CD 00	CD 01	CD 11	CD 10
AB 00				
AB 01				
AB 11				
AB 10				



Inputs				Segments						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

↑

Rita om K-map i dina inlämnade svar.

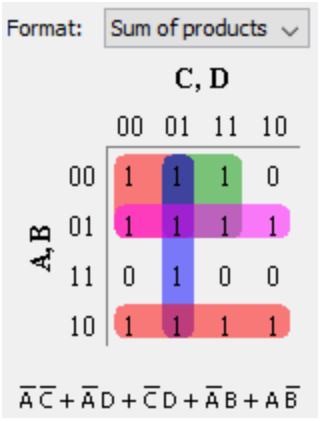
Redraw the K-map in your answer sheets.

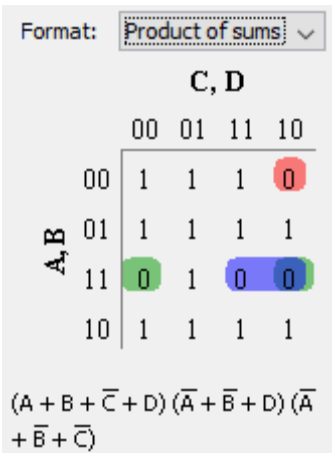
(Answer on next page)

0. Truth Table

A	B	C	D	c
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

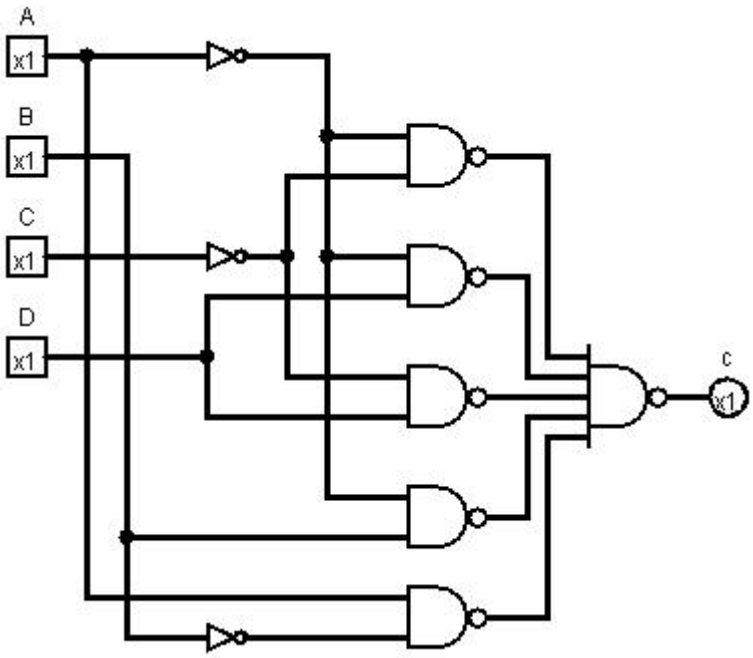
1. K-Map and 2. Boolean expressions





3. Use SOP for NAND only (inverters are ok if you note that they can be made with a NAND) No deductions if not simplest possible.

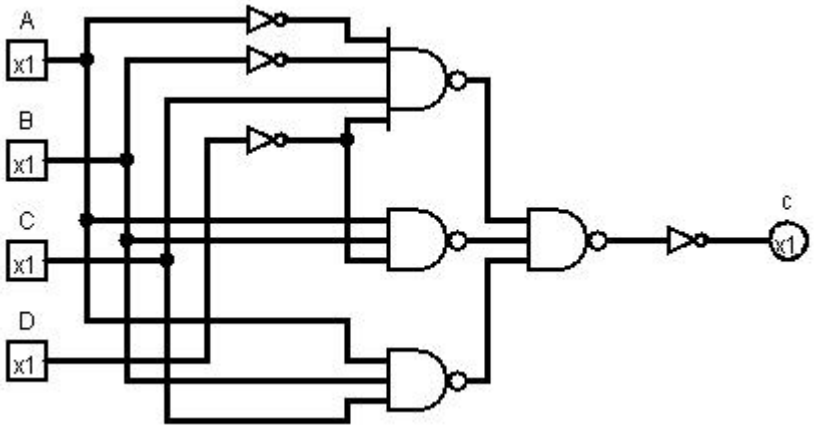
For SOP draw $Y = \overline{\overline{\overline{A} \cdot \overline{C} + \overline{A} \cdot D + \overline{C} \cdot D + \overline{A} \cdot B + A \cdot \overline{B}}} = \overline{\overline{\overline{A} \cdot \overline{C}} \cdot \overline{\overline{A} \cdot D} \cdot \overline{\overline{C} \cdot D} \cdot \overline{\overline{A} \cdot B} \cdot \overline{A \cdot \overline{B}}}$



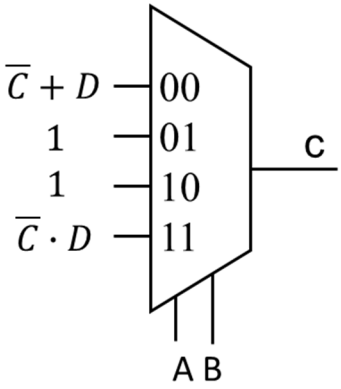
For POS draw

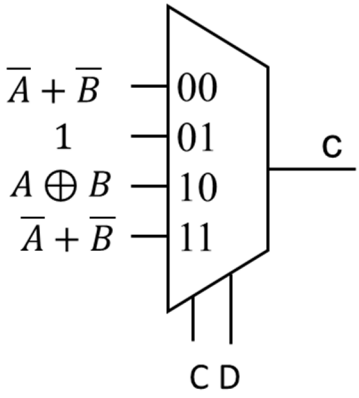
$$Y = \overline{\overline{(A + B + \overline{C} + D)}} \cdot \overline{\overline{(\overline{A} + \overline{B} + D)}} \cdot \overline{\overline{(\overline{A} + \overline{B} + \overline{C})}} = \overline{\overline{A} \cdot \overline{B} \cdot C \cdot \overline{D}} \cdot \overline{A \cdot B \cdot \overline{D}} \cdot \overline{A \cdot B \cdot C}$$

(note the double inversion bars, extra inverters/NANDs are needed)



4. The 4:1 Mux can be connected several ways, for instance:





19 Analysis of FSM

Swedish: Analysera vad nedanstående tillståndsmaskin (FSM) utför.

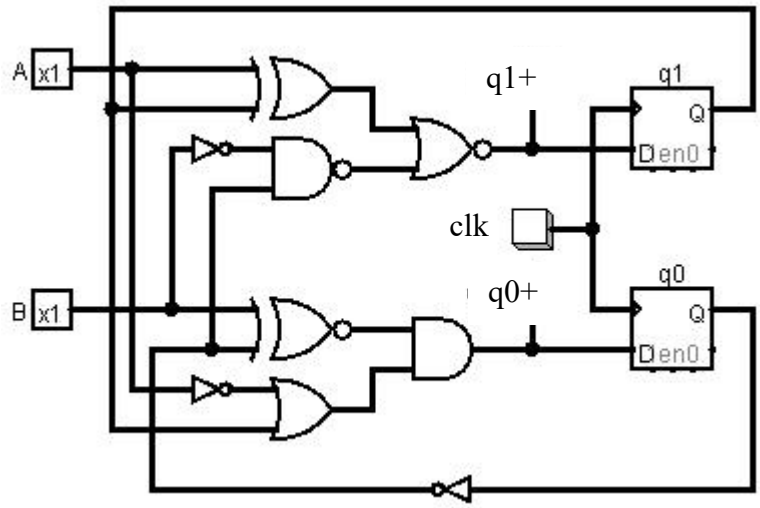
1. Ta fram Boolska uttryck för nästa tillstånd.
2. Rita K-Maps för q1+ och q0+.
3. Rita tillståndstabell.
4. Rita tillståndsdiagram.

Använd ordningen q1 q0 B A (det finns inga utsignaler förutom tillståndsvariablerna)

English: Analyze the state machine (FSM) below.

1. Derive Boolean expressions for next state.
2. Draw K-Maps for q1+ and q0+.
3. Draw a state table.
4. Draw a state diagram.

Use the order q1 q0 B A (there are no outputs except for the state variables)



1. Boolean expressions for next state q1+ and q0+

$$q_1^+ = \overline{A \oplus q_1 + \overline{B} \cdot \overline{q_0}} = \left(\overline{A \oplus q_1}\right)\left(\overline{\overline{B} \cdot \overline{q_0}}\right) = \left(\overline{A} \cdot \overline{q_1} + A \cdot q_1\right)\left(\overline{B} \cdot \overline{q_0}\right)$$
$$= \overline{A} \cdot \overline{B} \cdot \overline{q_1} \cdot \overline{q_0} + A \cdot \overline{B} \cdot q_1 \cdot \overline{q_0}$$

$$q_0^+ = \left(\overline{B \oplus \overline{q_0}}\right) \cdot \left(\overline{A} + q_1\right) = \left(B \oplus q_0\right) \cdot \left(\overline{A} + q_1\right)$$
$$= \left(B \cdot \overline{q_0} + \overline{B} \cdot q_0\right) \cdot \left(\overline{A} + q_1\right)$$
$$= \overline{A} \cdot B \cdot \overline{q_0} + \overline{A} \cdot \overline{B} \cdot q_0 + B \cdot q_1 \cdot \overline{q_0} + \overline{B} \cdot q_1 \cdot q_0$$

2. K-Maps for q1+ and q0+

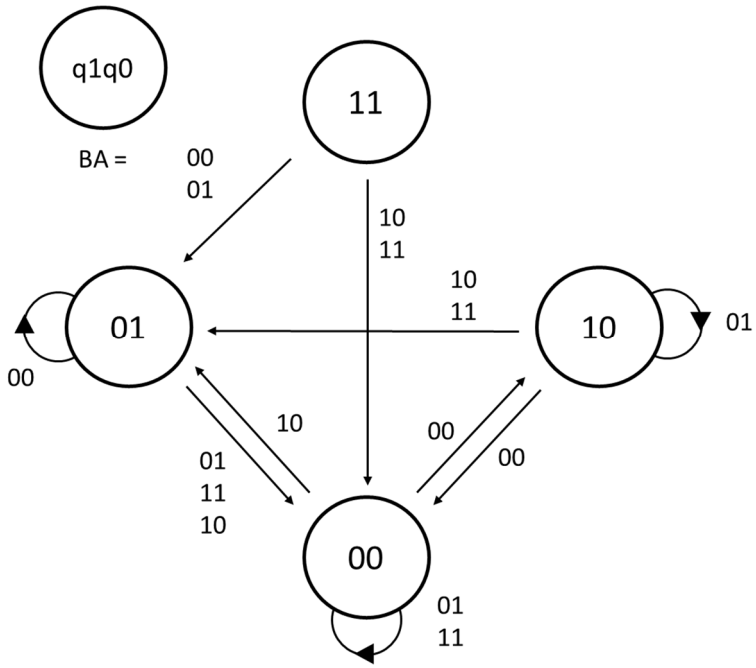
q1+	BA=			
q1q0	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	1	0	0

q0+	BA=			
q1q0	00	01	11	10
00	0	0	0	1
01	1	0	0	0
11	1	1	0	0
10	0	0	1	1

3. State table

		Next state							
Present state		BA = 00		BA = 01		BA = 11		BA = 10	
q1	q0	q1+	q0+	q1+	q0+	q1+	q0+	q1+	q0+
0	0	1	0	0	0	0	0	0	1
0	1	0	1	0	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0
1	0	0	0	1	0	0	1	0	1

4. State diagram



Other notations on the arrows are also possible

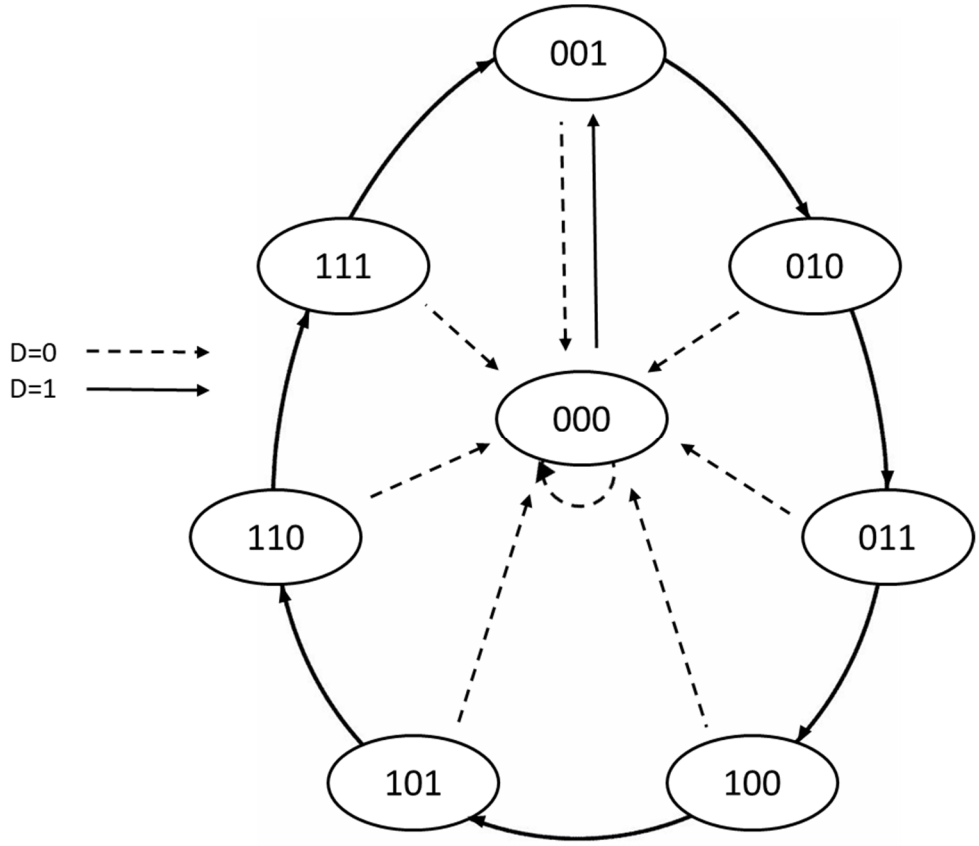
20 Design of FSM

Swedish: Konstruera en tillståndsmaskin (FSM) enligt tillståndsdiagrammet nedan.

1. Rita tillståndstabell.
2. Ta fram K-map för nästa tillstånd.
3. Ta fram minimerade uttryck för nästa tillstånd.
4. Rita kretsschema för en FSM med DFFs och vilka grindar som helst utom MUX.

English: Design a state machine (FSM) according to the state diagram below.

1. Draw a state table.
2. Derive K-maps for next state.
3. Derive minimized expressions for next state.
4. Draw the FSM circuit diagram with DFFs and any gates except MUX.



	Q_1Q_0 = 00	01	11	10
D Q_2 = 00				
01				
11				
10				

Rita om K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

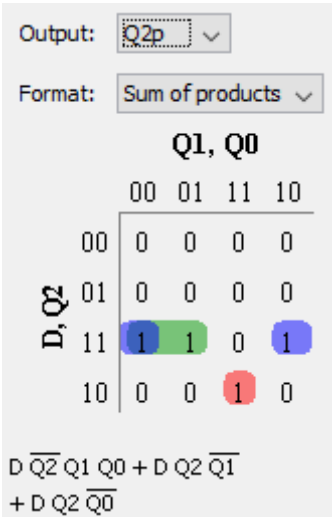
(Answer on next page)

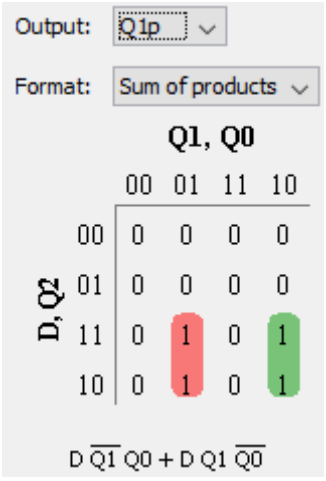
1. State Table

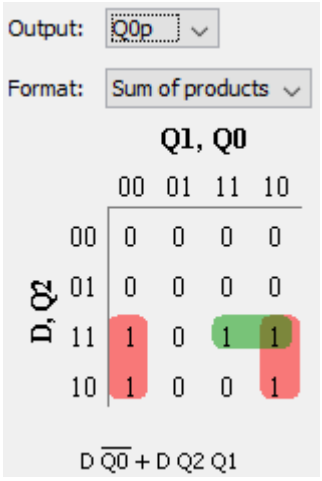
Present state			Next state D = 0			Next state D = 1		
Q2	Q1	Q0	Q2+	Q1+	Q0+	Q2+	Q1+	Q0+
0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	1	0
0	1	0	0	0	0	0	1	1
0	1	1	0	0	0	1	0	0
1	0	0	0	0	0	1	0	1
1	0	1	0	0	0	1	1	0
1	1	0	0	0	0	1	1	1
1	1	1	0	0	0	0	0	1

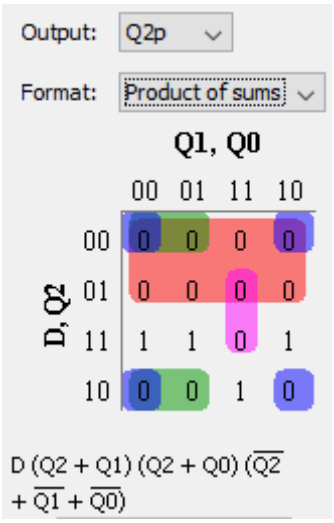
2. K-Maps for next state Q2+, Q1+, and Q0+

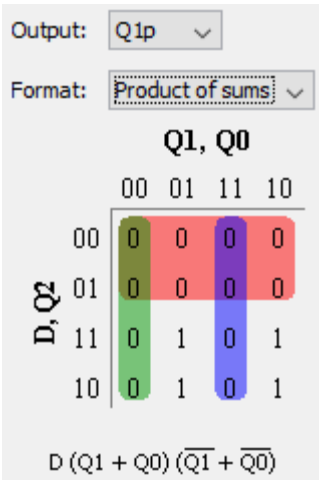
3. Minimized Boolean expressions for next state (select SoP or PoS)

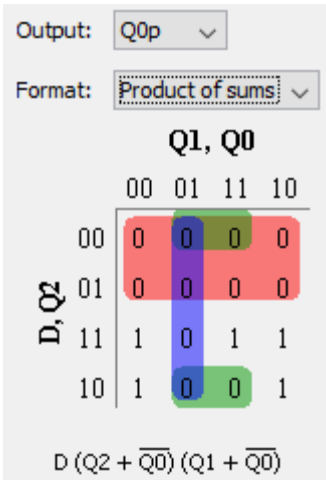












4. Schematic for FSM with DFFs (and SoP)