



Skriftlig Tentamen

IE1204 Digital Design

2023-04-12 **Med Lösningar**

Examiner/Examinator: Carl-Mikael Zetterling

Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

Swedish/Svenska:

Tentamenstexten ska lämnas in när lösningarna lämnas in.

Inga tillåtna hjälpmedel utom linjal.

Examen består av två delar:

Del 1 har 16 uppgifter med max 1 poäng per uppgift som ska besvaras på ”Answer Form”.

Del 2 har 4 uppgifter med max 4 poäng per uppgift som ska besvaras på separat papper.

Lämna in båda delar samtidigt. Disponera tiden själv mellan delarna.

Uppgifterna är inte ordnade efter svårighetsgrad.

Om slutsumman av tentan har halvpöäng avrundas det uppåt.

Totalt max 32 poäng på tentamen.

För godkänt krävs

(minst 8 poäng på del 1) OCH (minst 16 poäng totalt)

Fx om något villkor ej är uppfyllt med en poängs marginal.

Det betyder att

För E krävs minst 16 poäng totalt och minst 8 på del 1.

För Fx krävs 16 poäng totalt och minst 7 på del 1

eller 15 poäng totalt och minst 8 på del 1.

Betygskalan för tentamen förutsatt att studenten har minst 8 poäng från del 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

Resultat meddelas inom tre veckor.

Written Exam

IE1204 Digital Design

2023-04-12 **With Solutions**

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English:

The exam text should be handed in after the exam.

No aids allowed except ruler.

The exam consists of two parts:

Part 1 has 16 exercises for max 1 point per exercise to be answered on the “Answer Form”.

Part 2 has 4 exercises for max 4 points per exercise, to be answered on a separate paper.

Hand in both parts at the same time. Plan the time yourself between the parts.

The exercises are not in order of difficulty.

If the total sum of the exam has half points this will be rounded up.

Total max of 32 points on the exam.

To pass the exam requires

(at least 8 points from part 1) AND (at least 16 points in total)

Fx if any condition is not fulfilled by one point’s margin.

This means

For E, a minimum of 16 points in total and at least 8 in part 1 is required.

For Fx, 16 points are required in total and at least 7 on part 1

or 15 points in total and at least 8 in part 1.

Grades are given as follows provided the student has at least 8 points from part 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

The result will be announced within three weeks.

Del 1/Part 1, 1 point per exercise, fill in on “Answer Form”

1 Number Conversion

Swedish: Konvertera de positiva talen och utför beräkningen.
Svara med ett decimalt tal.

English: Convert the unsigned numbers and perform the calculation.
Answer with a decimal number.

$$Y = 100001_2 + 16_8 + 16_{10} + 16_{16} \\ = 33 + 14 + 16 + 22 = 85$$

2 Addition

Swedish: Konvertera A och B från hexadecimala till 8 bitars två-komplement kodade tal.
Beräkna A + B (binärt) och svara med ett 8 bitars två-komplement kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: Convert A and B from hexadecimal to 8-bit binary (two’s complement) numbers.
Calculate A + B (binary) and answer with an 8-bit binary (two’s complement) number.
You can check your calculations using decimal numbers.

$$\begin{array}{r} A = 0x53 = 53_{16} \quad 01010011 \\ B = 0x2B = 2B_{16} \quad + 00101011 \\ \hline A + B \quad \quad \quad = 01111110 = 0x7E \end{array}$$

3 Subtraction

Swedish: Konvertera A och B från hexadecimala till 8 bitars två-komplement kodade tal.
Beräkna A - B (binärt) och svara med ett 8 bitars två-komplement kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: Convert A and B from hexadecimal to 8-bit binary (two’s complement) numbers.
Calculate A - B (binary) and answer with an 8-bit binary (two’s complement) number.
You can check your calculations using decimal numbers.

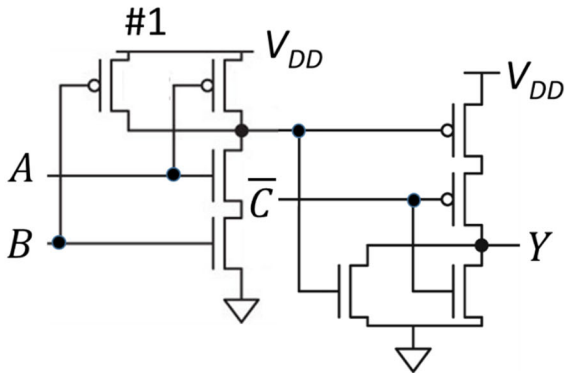
$$\begin{array}{r} A = 0x35 = 35_{16} \quad \quad \quad 00110101 \\ B = 0x79 = 79_{16} \quad \quad = 01111001 \\ - B = \quad \quad \quad \quad \quad + 10000111 \\ \hline A - B \quad \quad \quad \quad \quad = 10111100 = 0xBC \end{array}$$

4 CMOS circuits

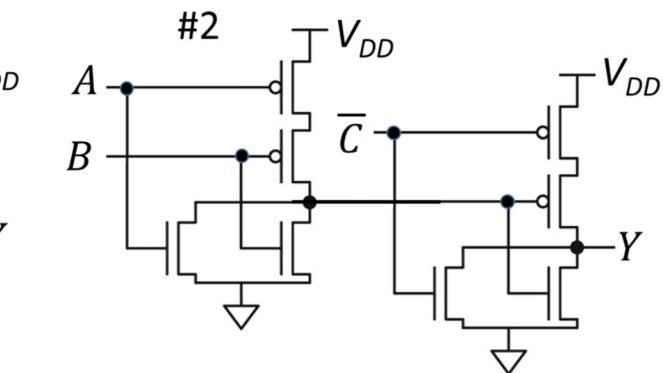
Swedish: Bestäm vilken/vilka av CMOS-grindnäten nedan som har den logiska funktionen Y. Det kan finnas mer än ett korrekt svar.

English: Determine which of the CMOS-circuits below have the logic function Y. There may be more than one correct answer.

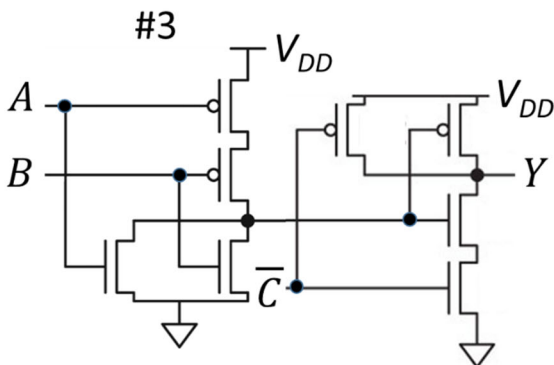
$$Y = A \cdot B + C$$



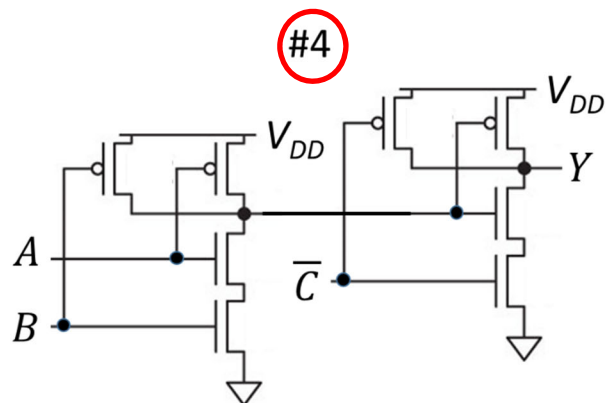
$$Y = \overline{\overline{A \cdot B} + \overline{C}} = \overline{\overline{A \cdot B} \cdot \overline{C}} = A \cdot B \cdot C$$



$$Y = \overline{\overline{A + B} + \overline{C}} = (A + B)C = A \cdot C + B \cdot C$$



$$Y = \overline{\overline{A + B} \cdot \overline{C}} = \overline{\overline{A + B} + C} = A + B + C$$



$$Y = \overline{\overline{A \cdot B} \cdot \overline{C}} = A \cdot B + C$$

5 Boolean Algebra

Swedish: Ta fram enklast möjliga booleska uttryck.

English: Derive the simplest possible Boolean expression.

$$Y = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot B \cdot \bar{C} \cdot \bar{D} + A \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot B \cdot \bar{C} \cdot D + A \cdot B \cdot C \cdot \bar{D} + \bar{A} \cdot B \cdot C \cdot D + \bar{A} \cdot B \cdot C \cdot \bar{D} + A \cdot B \cdot \bar{C} \cdot \bar{D} + A \cdot B \cdot \bar{C} \cdot D + A \cdot B \cdot C \cdot D$$

$$= A \cdot C \cdot D + \bar{A} \cdot \bar{C} \cdot D + B$$

$$Y = A \cdot C \cdot D + \bar{A} \cdot \bar{C} \cdot D + B$$

Y	CD 00	CD 01	CD 11	CD 10
AB 00		1		
AB 01	1	1	1	1
AB 11	1	1	1	1
AB 10			1	

6 MUX to K-map

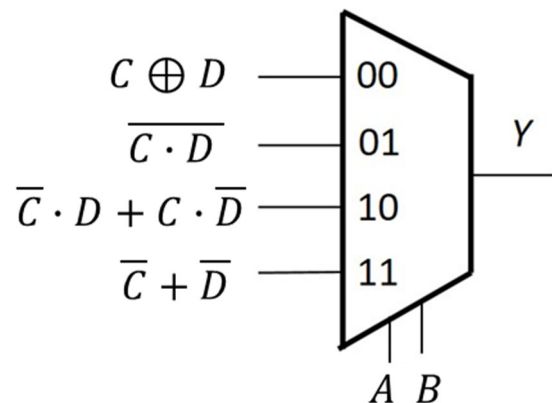
Swedish: Fyll i K-Map från MUX-kopplingen.

Ta fram enklast möjliga booleska uttryck för Y från K-map. Välj PoS eller SoP.

English: Fill in the K-Map from the MUX circuit.

Derive simplest possible Boolean expression from the K-map. Select PoS or SoP.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	0	1	0	1
AB 01	1	1	0	1
AB 11	1	1	0	1
AB 10	0	1	0	1



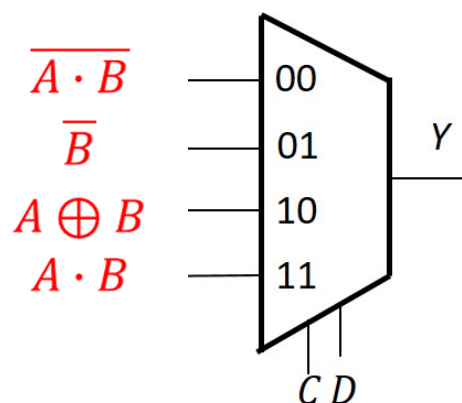
$$B \cdot \bar{C} + \bar{C} \cdot D + C \cdot \bar{D} = B \cdot \bar{C} + C \oplus D = (B + C + D)(\bar{C} + \bar{D})$$

7 K-Map to MUX

Swedish: Använd en 4:1 MUX och valfria grindar eller 0 och 1 och gör en krets för K-map med CD som select-signaler.

English: Use a 4:1 MUX and any logic gates or 0 or 1 to draw a circuit for the K-map with CD as select signals.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	1	0	0
AB 01	1	0	0	1
AB 11	0	0	1	0
AB 10	1	1	0	1



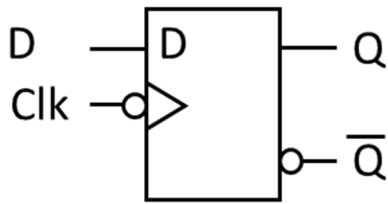
$\bar{A} + \bar{B}$ was also accepted for the first term.

0.5 point deducted if third and fourth expressions were interchanged.

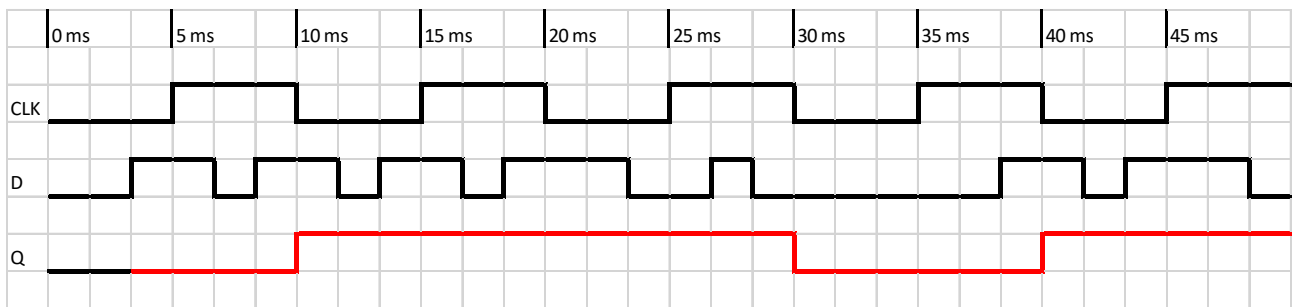
8 Timing diagram

Swedish: Rita tidsdiagram för D-vippan (D flip-flop) i "Answer Form".

English: Draw the timing diagram for the D flip-flop in the "Answer Form".



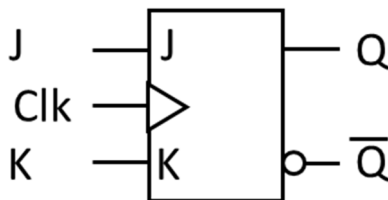
NOTE: negative edge



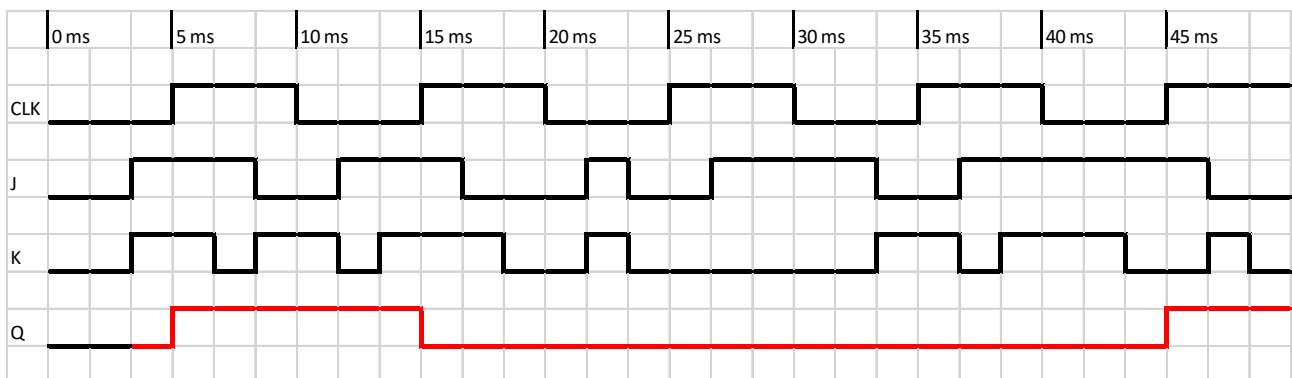
9 Timing diagram

Swedish: Rita tidsdiagram för JK-vippan (JK flip-flop) i "Answer Form".

English: Draw the timing diagram for the JK flip-flop in the "Answer Form".



NOTE: positive edge

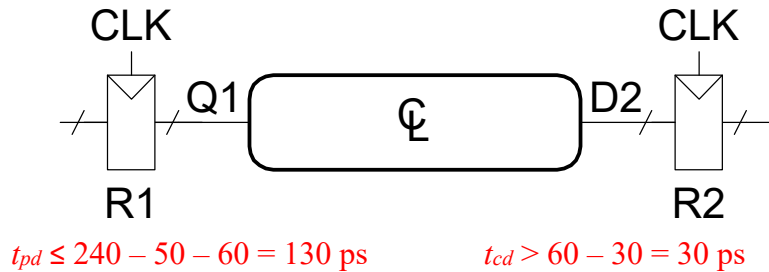


10 Timing calculation

Swedish: Beräkna fördröjningstiderna t_{pd} och t_{cd} för kretsen.

English: Calculate the delay times t_{pd} and t_{cd} for the circuit.

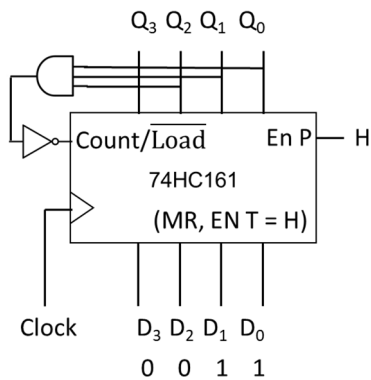
$t_{pcq} = 50 \text{ ps}$
 $t_{ccq} = 30 \text{ ps}$
 $t_{setup} = 60 \text{ ps}$
 $t_{hold} = 60 \text{ ps}$
 $T_c = 240 \text{ ps}$



11 Counter analysis

Swedish: Räknaren nedan har kommit till tillstånd $Q_3Q_2Q_1Q_0 = 0111$. Vad blir nästa tillstånd?

English: The counter below has counted to state $Q_3Q_2Q_1Q_0 = 0111$. What is the next state?

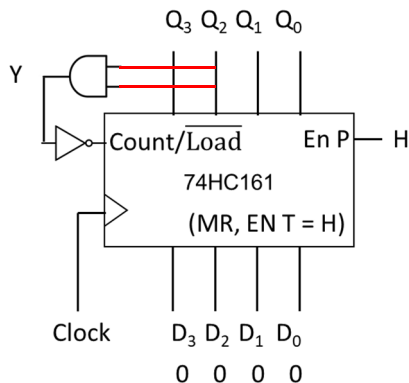


In the next state a load operation will be performed, and it is 0011 that is loaded

12 Counter design

Swedish: Hur ska AND-grunden kopplas för att få en räknare med 5 states? (dela med 5)

English: How should the AND-gate be connected to get a counter with 5 states? (divide-by-5)



The AND gate should detect 5, 0100, so $Y = Q_2$

13 Multiplication

Swedish: A och B är 8 bitars två-komplement kodade tal.

Beräkna $A \times B$ (binärt) och svara med ett 16 bitars två-komplement **hexadecimalt kodat tal**.

Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.

Calculate $A \times B$ (binary) and answer with a 16-bit binary (two's complement) **hexadecimal number**.

You can check your calculations using decimal numbers.

$$A = 00110100_2$$

$$B = 01111111_2$$

$A \times B = B \times A$ (both are positive) put B above since it has more '1's

$$\begin{array}{r} 01111111 \\ \times 00110100 \\ \hline 01111111 \quad \text{1st multiplication} \\ + 01111111 \quad \text{2nd multiplication} \\ \hline 100111101100 \\ + 01111111 \quad \text{3rd multiplication} \\ \hline 1100111001100 = 19CC_{16} \end{array}$$

14 Division

Swedish: A och B är 8 bitars två-komplement kodade tal.

Beräkna A / B (binärt) och svara med kvot och rest

(8 bitars två-komplement hexadecimalt kodade tal).

Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.

Calculate A / B (binary) and answer with quotient and remainder

(8-bit binary two's complement hexadecimal numbers).

You can check your calculations using decimal numbers.

$$A = 01111111_2$$

$$B = 00001110_2$$

A and B are both positive

$$\begin{array}{r} 1001 \quad \text{Quotient} = 9 \\ 1110 \overline{) 01111111} \\ - 1110 \\ 1111 \\ - 1110 \\ 1 \quad \text{Remainder} = 1 \end{array}$$

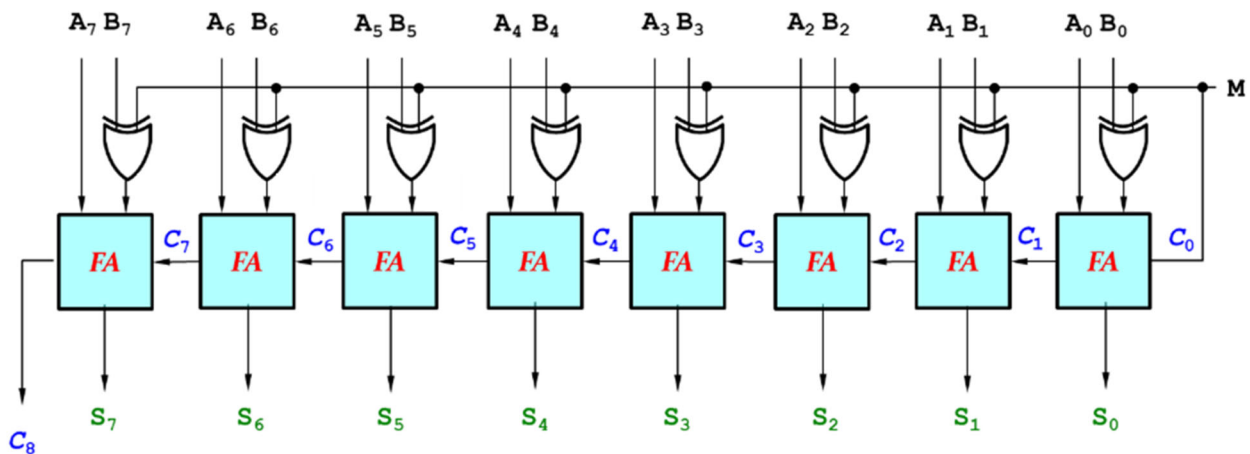
15 Full Addder

Swedish: Vad blir resultatet från kretsen nedan om $M = 1$?
Svara med 8 bitar ($S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0$). Ignorera carry out (C_8).

English: What is the result for the circuit below if $M = 1$?
Answer with 8 bits ($S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0$). Ignore carry out (C_8).

Use these A and B. 1 (with $M = 1$, B is inverted and a carry in is added)

A = 0011 1000	0011 1000	
B = 0111 1001	1000 0110	
	1011 1111	



16 Shift register

Swedish: Ett skiftregister har laddats med det binära talet Q.
Vad blir talet efter N klockpulser?
Svara med 8 bitar.

English: A shift register has been loaded with the binary number Q.
What is the result after N clock pulses?
Answer with 8 bits.

Operation = logic shift left (LSL)

Q = 00100110₂ 10011000 (zeroes are shifted in for LSL)

N = 2

Del 2/Part 2, 4 points per exercise, answer on separate paper

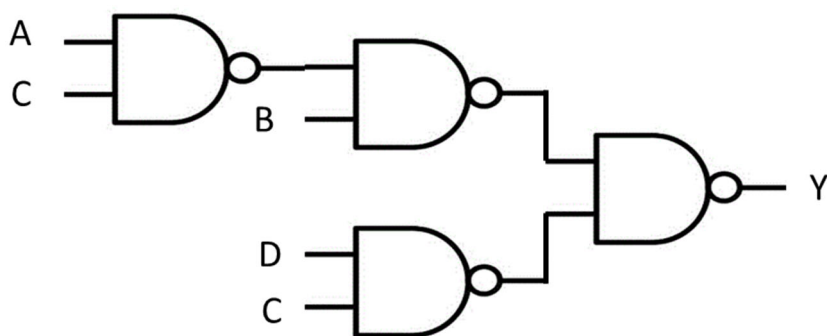
17 Analysis of Combinational Circuit

Swedish:

1. Ta fram booleskt uttryck för kretsen nedan.
2. Rita K-map för kretsen med variabelordning som i figuren.
3. Förenkla uttrycket med hjälp av K-map.
4. Rita ny krets med enbart NOR-grindar.

English:

1. Derive the Boolean expression for the circuit below.
2. Draw a K-map for the circuit with variables as in the figure.
3. Simplify the expression using the K-map.
4. Draw a new circuit using only NOR gates.



Y	CD 00	CD 01	CD 11	CD 10
AB 00	0	0	1	0
AB 01	1	1	1	1
AB 11	1	1	1	0
AB 10	0	0	1	0

Rita om K-map i dina
inlämnade svar.

Redraw the K-map in
your answer sheets.

Boolean expression and truth table

$$Y = B \cdot \overline{A} \cdot \overline{C} \cdot \overline{D} \cdot C$$

Output: Y

\overline{BACDC}

$\sim(\sim(B \sim(A C)) \sim(D C))$

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

K-Map and simplified expressions

Output: Y

Format: Sum of products

		C, D			
		00	01	11	10
A, B	00	0	0	1	0
	01	1	1	1	1
	11	1	1	1	0
	10	0	0	1	0

$CD + \overline{A}B + B\overline{C}$

Output: Y

Format: Product of sums

		C, D			
		00	01	11	10
A, B	00	0	0	1	0
	01	1	1	1	1
	11	1	1	1	0
	10	0	0	1	0

$(B + C)(B + D)(\overline{A} + \overline{C} + D)$

Can be simplified with Boolean Algebra (not necessary for full points) or from SOP:

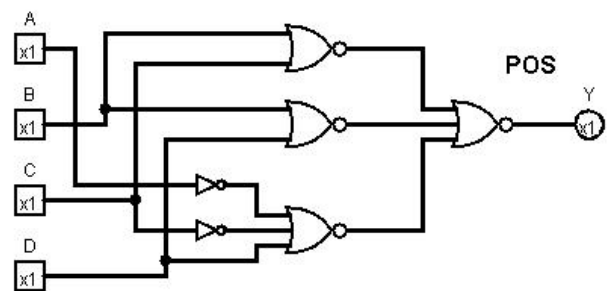
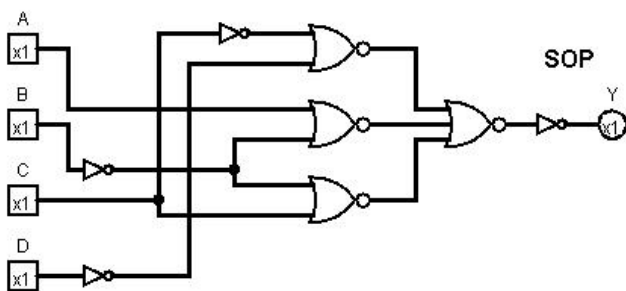
$$Y = B \cdot \overline{A} \cdot \overline{C} \cdot \overline{D} \cdot C = B \cdot \overline{A} \cdot \overline{C} + \overline{D} \cdot C = B(\overline{A} \cdot \overline{C}) + D \cdot C = B(\overline{A} + \overline{C}) + D \cdot C$$

$$= \overline{A} \cdot B + B \cdot \overline{C} + C \cdot D = \overline{\overline{A} \cdot B} + \overline{B \cdot \overline{C}} + \overline{C \cdot D} = \overline{\overline{A} + \overline{B}} + \overline{\overline{B} + C} + \overline{\overline{C} + D}$$

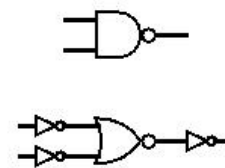
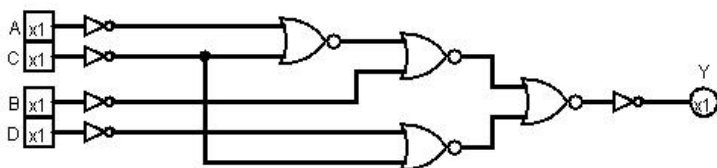
Or better from starting from POS since it is NOR (inverters can be made with NOR gates):

$$Y = (B + C)(B + D)(\overline{A} + \overline{C} + D) = \overline{\overline{B + C}} \overline{\overline{B + D}} \overline{\overline{\overline{A} + \overline{C} + D}}$$

$$= \overline{\overline{B} + \overline{C}} + \overline{\overline{B} + \overline{D}} + \overline{\overline{A} + \overline{C} + D}$$



From original circuit using Equivalence:



18 Design of Combinational Circuit

Swedish:

Konstruera kretsen för **c-segmentet** för en decimal 7-segmentsdekoder.
Sanningstabellen är given nedan.

1. Rita K-map för sanningstabellen med variabelordning som i figuren.
2. Uttnyttja $x = \text{don't care}$. Ta fram enklast möjliga booleska uttryck från K-map.
3. Rita en krets för uttrycket med enbart NAND-grindar.
4. Rita en krets för K-map som använder en 4:1 Mux, grindar och 0 och 1.

English:

Design the circuit for the **c-segment** of a decimal to 7-segment decoder.
The truth table is given below.

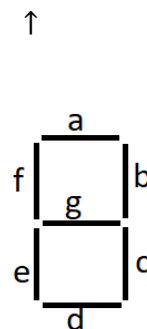
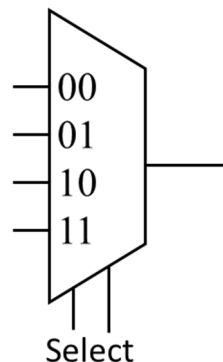
1. Draw a K-map for the truth table with variables as in the figure.
2. Use $x = \text{don't care}$. Derive simplest possible Boolean expression from the K-map.
3. Draw a circuit for the expression using only NAND-gates.
4. Draw a circuit for the K-Map using a 4:1 Mux, gates and 0 and 1.

C	CD 00	CD 01	CD 11	CD 10
AB 00	1	1	1	0
AB 01	1	1	1	1
AB 11	x	x	x	x
AB 10	1	1	x	x

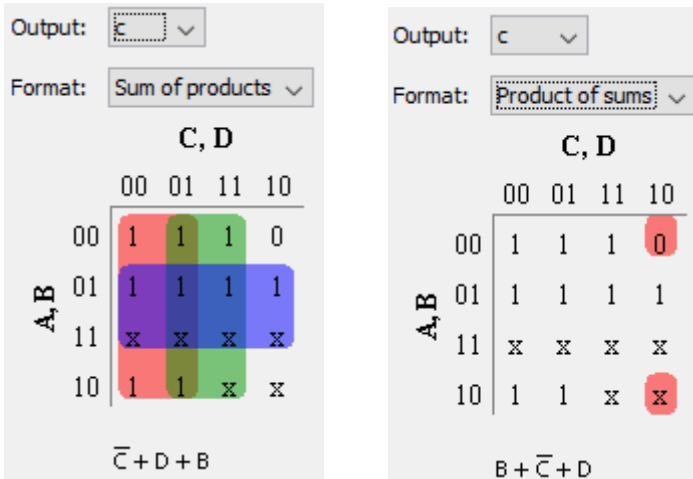
Inputs				Segments						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x

Rita om K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

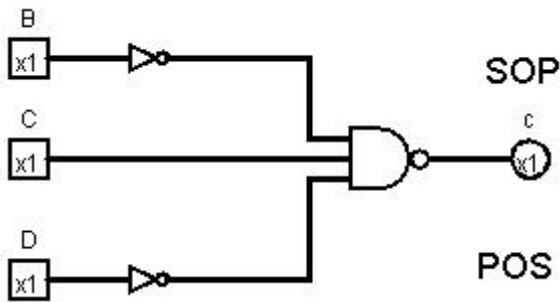


K-Map and simplified expressions

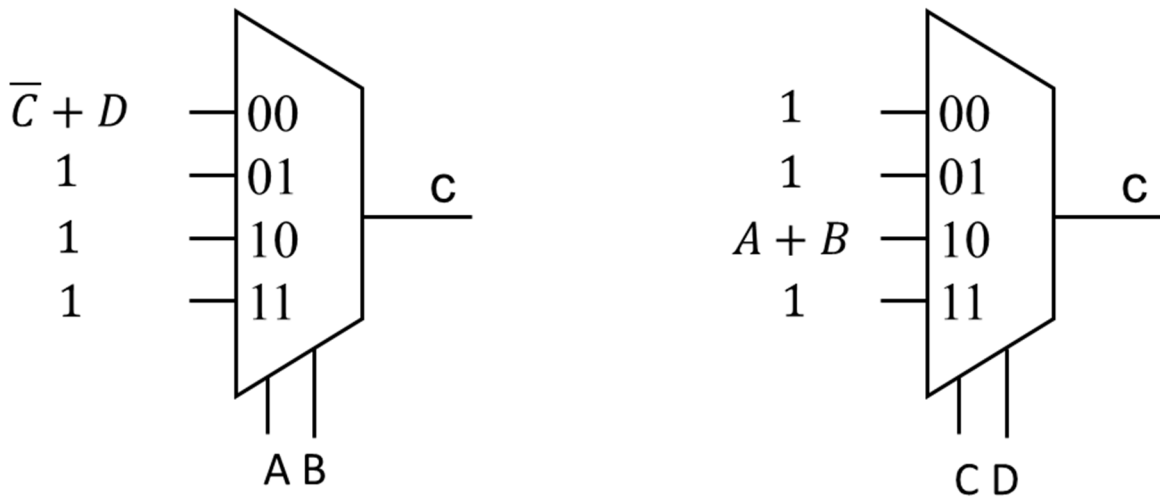


Normally use SOP for NAND only, however for this circuit the result is the same. (inverters are ok if you note that they can be made with a NAND)
 No deductions if not simplest possible, for instance if “A” was included in expression.

$$Y_{SOP} = Y_{POS} = B + \bar{C} + D = \overline{\overline{B + \bar{C} + D}} = \overline{\bar{B} \cdot C \cdot \bar{D}}$$



MUX (2 out of several possibilities due to the don't cares)



19 Analysis of FSM

Swedish: Analysera vad nedanstående tillståndsmaskin (FSM) utför.

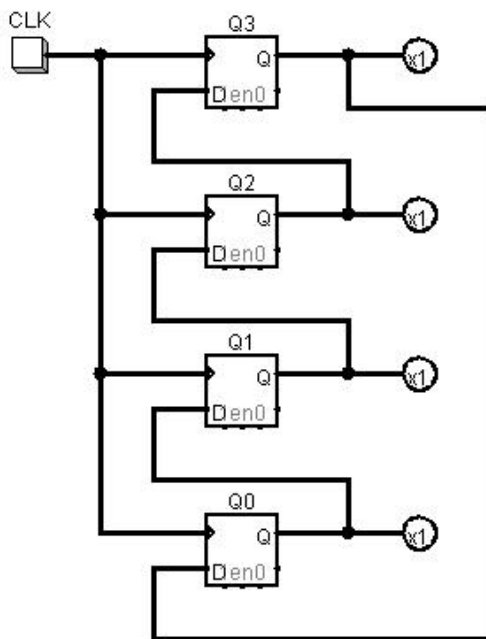
1. Ta fram Boolska uttryck för nästa tillstånd Q_3+ Q_2+ Q_1+ Q_0+ .
2. Rita K-Maps för Q_3+ Q_2+ Q_1+ Q_0+ .
3. Rita tillståndstabell.
4. Rita tillståndsdigram.

Använd ordningen Q_3 Q_2 Q_1 Q_0 (det finns inga utsignaler förutom tillståndsvariablerna)

English: Analyze the state machine (FSM) below.

1. Derive Boolean expressions for next state Q_3+ Q_2+ Q_1+ Q_0+ .
2. Draw K-Maps for Q_3+ Q_2+ Q_1+ Q_0+ .
3. Draw a state table.
4. Draw a state diagram.

Use the order Q_3 Q_2 Q_1 Q_0 (there are no outputs except for the state variables)



	$Q_1Q_0 =$			
	00	01	11	10
$Q_3Q_2 =$				
00				
01				
11				
10				

Rita om K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

Boolean expressions

$$Q_0^+ = Q_3$$

$$Q_1^+ = Q_0$$

$$Q_2^+ = Q_1$$

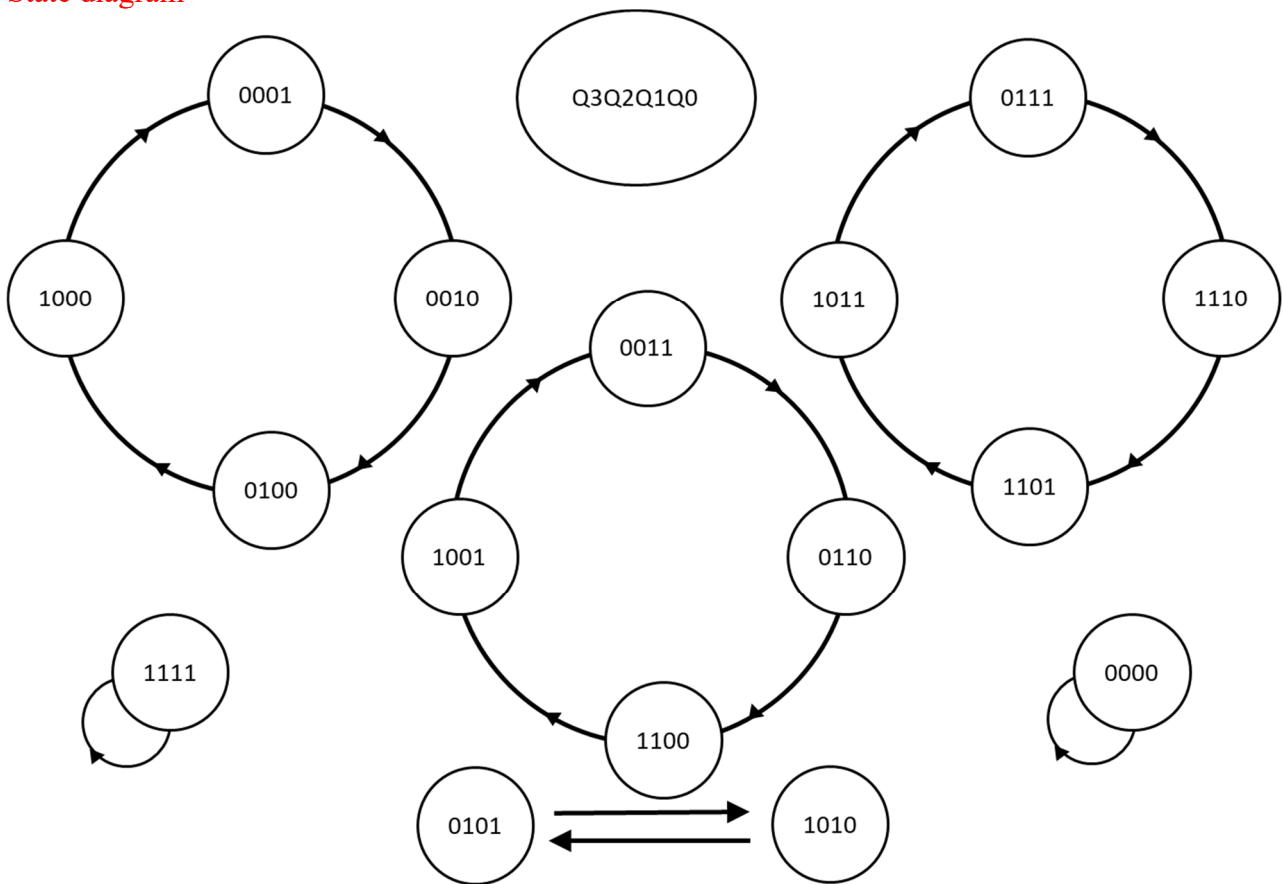
$$Q_3^+ = Q_2$$

K-Maps and/or state table

Q3+	Q ₁ Q ₀					Q2+	Q ₁ Q ₀			
	00	01	11	10			00	01	11	10
Q ₃ Q ₂						Q ₃ Q ₂				
00	0	0	0	0		00	0	0	1	1
01	1	1	1	1		01	0	0	1	1
11	1	1	1	1		11	0	0	1	1
10	0	0	0	0		10	0	0	1	1
Q1+	Q ₁ Q ₀					Q0+	Q ₁ Q ₀			
	00	01	11	10			00	01	11	10
Q ₃ Q ₂						Q ₃ Q ₂				
00	0	1	1	0		00	0	0	0	0
01	0	1	1	0		01	0	0	0	0
11	0	1	1	0		11	1	1	1	1
10	0	1	1	0		10	1	1	1	1

Present state				Next state			
Q3	Q2	Q1	Q0	Q3+	Q2+	Q1+	Q0+
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	0
0	1	0	1	1	0	1	0
0	1	1	0	1	1	0	0
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	1	1
1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1

State diagram



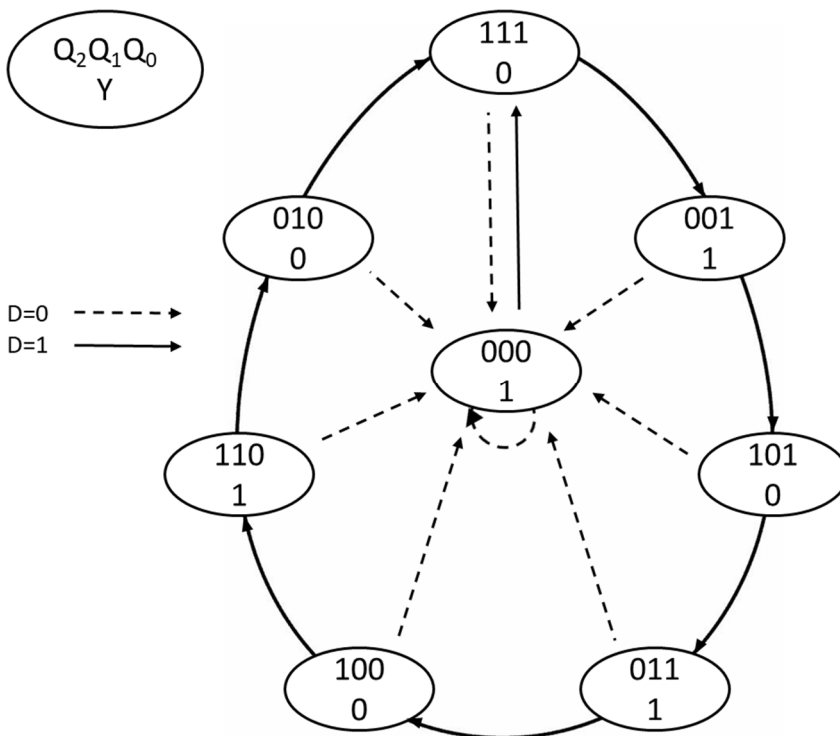
20 Design of FSM

Swedish: Konstruera en tillståndsmaskin (FSM) enligt tillståndsdigrammet nedan.

1. Rita tillståndstabell.
2. Ta fram K-map för nästa tillstånd och utsignalen Y.
3. Ta fram minimerade uttryck för nästa tillstånd och utsignal.
4. Rita kretsschema för en FSM med DFFs och vilka grindar som helst utom MUX.

English: Design a state machine (FSM) according to the state diagram below.

1. Draw a state table.
2. Derive K-maps for next state and output Y.
3. Derive minimized expressions for next state and output.
4. Draw the FSM circuit diagram with DFFs and any gates except MUX.



	$Q_1Q_0 =$			
	00	01	11	10
$DQ_2 =$				
00				
01				
11				
10				

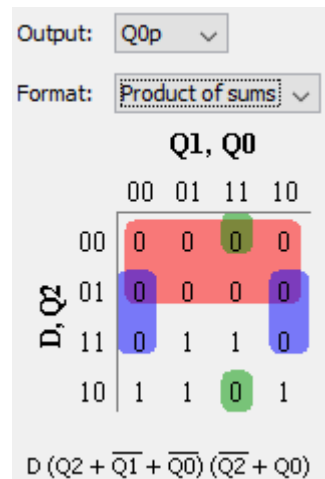
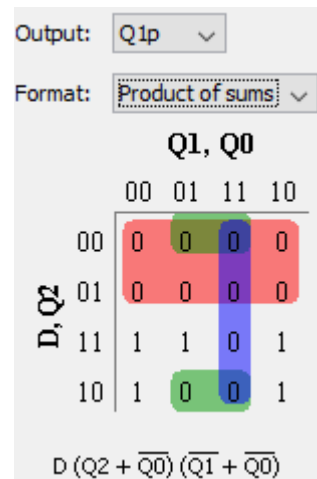
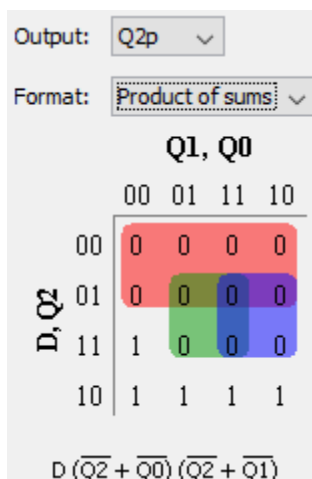
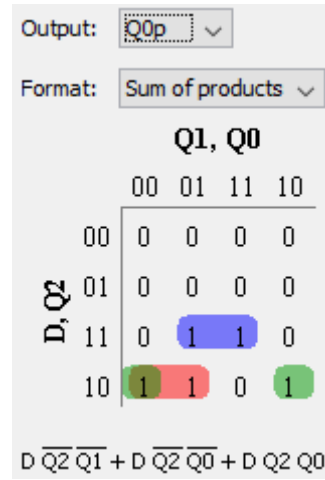
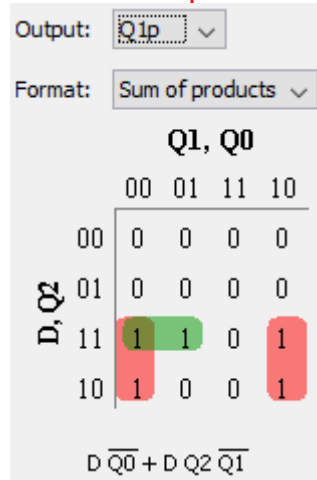
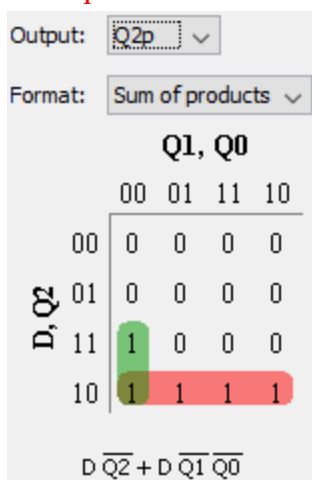
Rita om K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

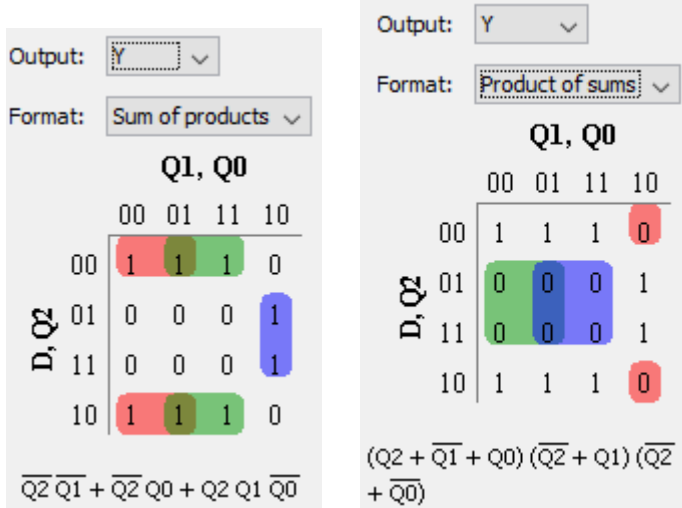
State table for the Easter Egg

Present state			Next state D = 0			Next state D = 1			Output
Q2	Q1	Q0	Q2+	Q1+	Q0+	Q2+	Q1+	Q0+	Y
0	0	0	0	0	0	1	1	1	1
0	0	1	0	0	0	1	0	1	1
0	1	0	0	0	0	1	1	1	0
0	1	1	0	0	0	1	0	0	1
1	0	0	0	0	0	1	1	0	0
1	0	1	0	0	0	0	1	1	0
1	1	0	0	0	0	0	1	0	1
1	1	1	0	0	0	0	0	1	0

K-Maps for next state with minimized expressions



K-Maps for output with minimized expressions (can be drawn without D!)



FSM circuit diagram (SoP version)

