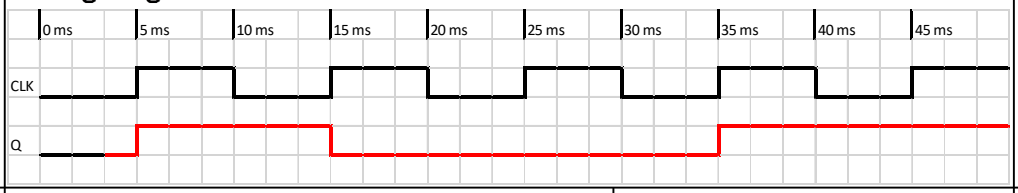
IE1204 Digital Design Answer Form 2024-04-05

Anonymized Code			
ABC-123		Exam 2024-04-05	
#	Answer with	Answer	Points
1	Decimal number	117	1
2	8 bit two's complement hexadecimal number	0xF5	1
3	8 bit two's complement hexadecimal number	0x21	1
4	Boolean expression, Y =	$Y = \overline{B} + A \cdot C$	1
5	Circuit number	#3	1
6	Boolean expression, Y =	$\overline{B} \cdot \overline{D} + B \cdot D = \overline{B \oplus D}$	1
7	MUX connections, Boolean expression or Gate		1
	Row CD = 00	$A + B$	
	Row CD = 01	$A \cdot \overline{B}$	
	Row CD = 10	$A \oplus B$	
	Row CD = 11	$\overline{A \oplus B}$	
8	Timing diagram		1
9	Flip-Flop or Latch #	#2	1
10	Maximum clock frequency =	5 GHz	1
	Is the Hold time constraint ok?	[X] Yes [ ] No	
11	Number of states =	7	1
	Final state $Q_3Q_2Q_1Q_0$ =	0 1 1 1	
12	Boolean expression Y =	$Y = Q_3 \cdot Q_1$	1
	Input $D_3D_2D_1D_0$ =	0 1 0 0	
13	16 bit two's complement hexadecimal Product A x B	P 0x29D6	1
14	8 bit two's complement hexadecimal Quotient (A / B) and Remainder	Q 0x09 R 0x01	1
15	8 result bits (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0)	1 0 0 1 0 0 0 0	1
16	Memory contents, 8 decimal digits	2 7 1 8 2 8 1 8	1
TOTAL POINTS		Examiner sign	16