Skriftlig Tentamen
IE1204 Digital Design
2024-04-05 Med Lösningar

Examiner/Examinator: Carl-Mikael Zetterling
Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

Swedish/Svenska:
Tentamenstexten ska lämnas in när lösningarna lämnas in.
Inga tillåtna hjälpmedel utom linjal.
Examen består av två delar:
Del 1 har 16 uppgifter med max 1 poäng per uppgift som ska besvaras på ”Answer Form”.
Del 2 har 4 uppgifter med max 4 poäng per uppgift som ska besvaras på separat papper.
Lämna in båda delar samtidigt. Disponera tiden själv mellan delarna.
Uppgifterna är inte ordnade efter svårighetsgrad.
Om slutsumman av tentan har halvpoäng avrundas det uppåt.

Totalt max 32 poäng på tentamen.
För godkänt krävs
(minst 8 poäng på del 1) OCH (minst 16 poäng totalt)
Fx om något villkor ej är uppfyllt med en poängs marginal.

Det betyder att
För E krävs minst 16 poäng totalt och minst 8 på del 1.
För Fx krävs 16 poäng totalt och minst 7 på del 1
eller 15 poäng totalt och minst 8 på del 1.

Betygskalan för tentamen förutsatt att studenten har minst 8 poäng från del 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

Resultat meddelas inom tre veckor.

Written Exam
IE1204 Digital Design
2024-04-05 With Solutions

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English:
The exam text should be handed in after the exam.
No aids allowed except ruler.
The exam consists of two parts:
Part 1 has 16 exercises for max 1 point per exercise to be answered on the "Answer Form".
Part 2 has 4 exercises for max 4 points per exercise, to be answered on a separate paper.
Hand in both parts at the same time. Plan the time yourself between the parts.
The exercises are not in order of difficulty.
If the total sum of the exam has half points this will be rounded up.

Total max of 32 points on the exam.
To pass the exam requires
(at least 8 points from part 1) AND (at least 16 points in total)
Fx if any condition is not fulfilled by one point's margin.

This means
For E, a minimum of 16 points in total and at least 8 in part 1 is required.
For Fx, 16 points are required in total and at least 7 on part 1
or 15 points in total and at least 8 in part 1.

Grades are given as follows provided the student has at least 8 points from part 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

The result will be announced within three weeks.

Del 1/Part 1, 1 point per exercise, fill in on "Answer Form"

1 Number Conversion

Swedish: Konvertera de positiva talen och utför beräkningen.
Svara med ett decimalt tal.

English: Convert the unsigned numbers and perform the calculation.
Answer with a decimal number.

$Y = 101010_2 + 20_8 + 20_{10} + 27_{16}$
$= 42 + 16 + 20 + 39 = 117$

2 Addition

Swedish: A och B är hexadecimala 8 bitars två-komplement kodade tal.
Beräkna A + B och svara med ett 8 bitars två-komplement hexadecimalt kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are hexadecimal 8-bit binary (two's complement) numbers.
Calculate A + B and answer with an 8-bit binary (two's complement) hexadecimal number.
You can check your calculations using decimal numbers.

$A = 0x43 = 43_{16}$ 01000011
$B = 0xB2 = B2_{16}$ + 10110010
A + B = 11110101 = 0xF5

or calculate directly from 0x43 + 0xB2

3 Subtraction

Swedish: A och B är hexadecimala 8 bitars två-komplement kodade tal.
Beräkna A - B och svara med ett 8 bitars två-komplement hexadecimalt kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are hexadecimal 8-bit binary (two's complement) numbers.
Calculate A - B and answer with an 8-bit binary (two's complement) hexadecimal number.
You can check your calculations using decimal numbers.

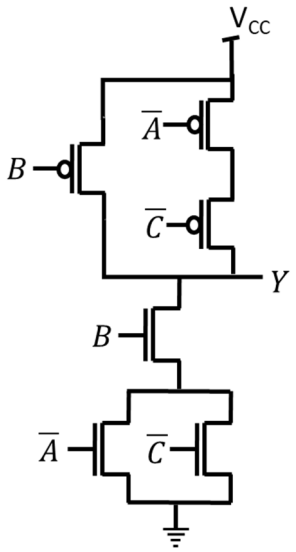
$A = 0x3D = 3D_{16}$ 00111101
$B = 0x1C = 1C_{16}$ = 00011100
- B = + 11100100
A – B = 00100001 = 0x21

or calculate directly from 0x3D – 0x1C

4 Analysis of CMOS circuits

Swedish: Ta fram enklast möjliga booleska uttryck för CMOS-kretsen.

English: Derive the simplest possible Boolean expression for the CMOS circuit.



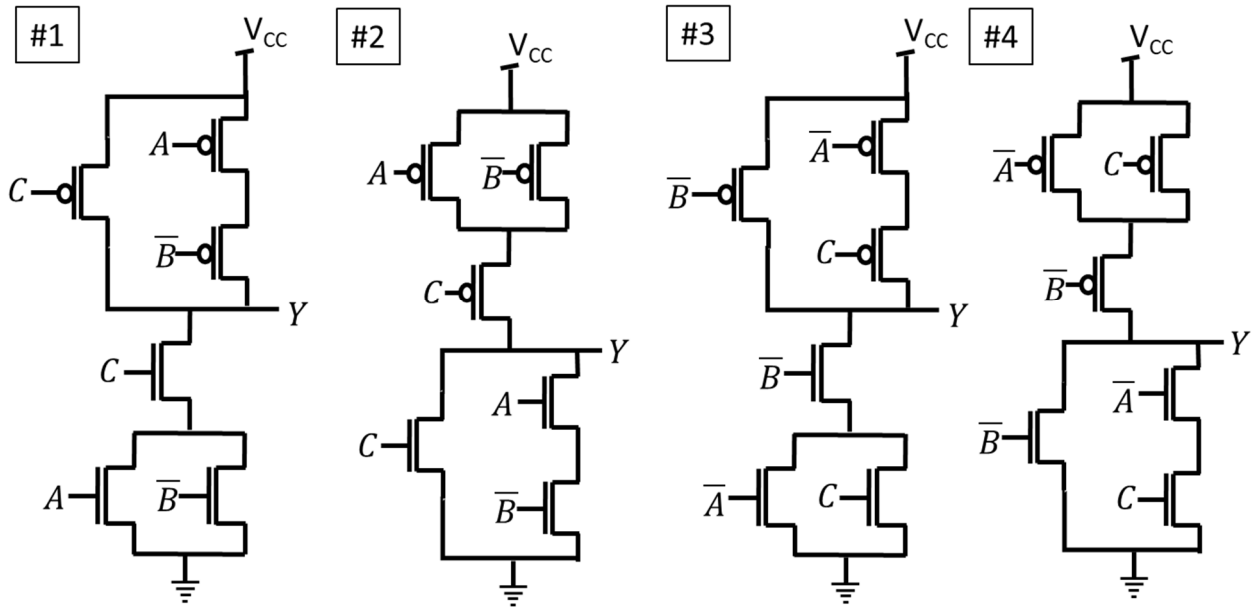
$$Y = \overline{B} + A \cdot C$$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

5 Design of CMOS circuits

Swedish: Bestäm vilken av CMOS-kretsarna som passar med sanningstabellen.

English: Determine which one of the CMOS circuits that matches the truth table.



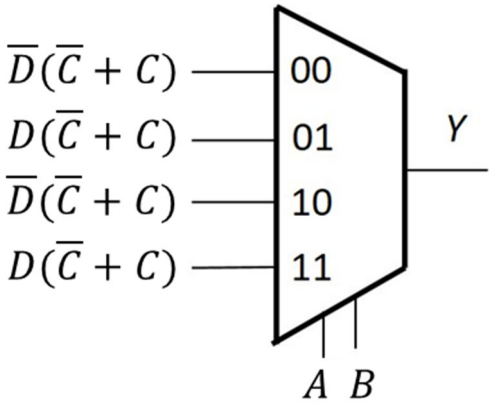
$$\#3 \; Y = B + A \cdot \overline{C}$$

6 Analysis: MUX to K-map

Swedish: Fyll i K-Map från MUX-kopplingen.
Ta fram enklast möjliga booleska uttryck för Y från K-map. Välj PoS eller SoP.

English: Fill in the K-Map from the MUX circuit.
Derive simplest possible Boolean expression from the K-map. Select PoS or SoP.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	0	1
AB 01	0	1	1	0
AB 11	0	1	1	0
AB 10	1	0	0	1



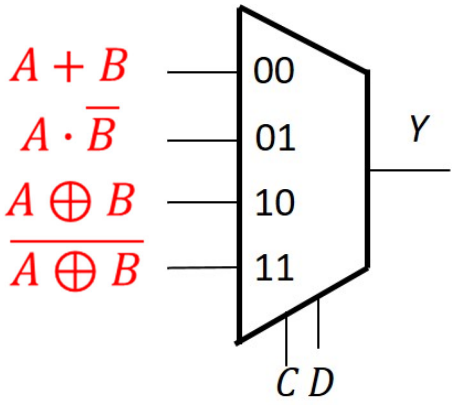
$$\overline{B}\cdot\overline{D}+B\cdot D=\overline{B\oplus D}$$

7 Design: K-Map to MUX

Swedish: Använd en 4:1 MUX och valfria grindar eller 0 och 1 och gör en krets för K-map med CD som select-signaler.

English: Use a 4:1 MUX and any logic gates or 0 or 1 to draw a circuit for the K-map with CD as select signals.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	0	0	1	0
AB 01	1	0	0	1
AB 11	1	0	1	0
AB 10	1	1	0	1

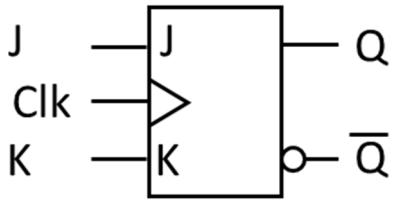


0.5 point deducted if third and fourth expressions are interchanged.

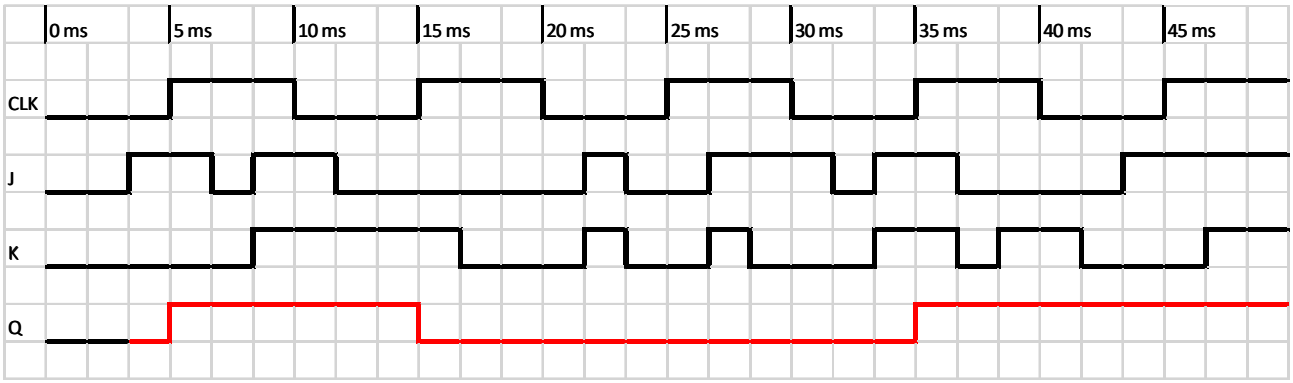
8 Timing diagram (Analysis)

Swedish: Rita tidsdiagram för kretsen i ”Answer Form”.

English: Draw the timing diagram for the circuit in the “Answer Form”.



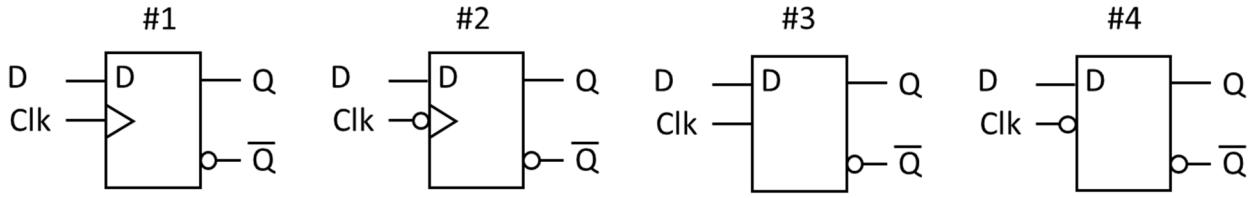
NOTE: positive edge

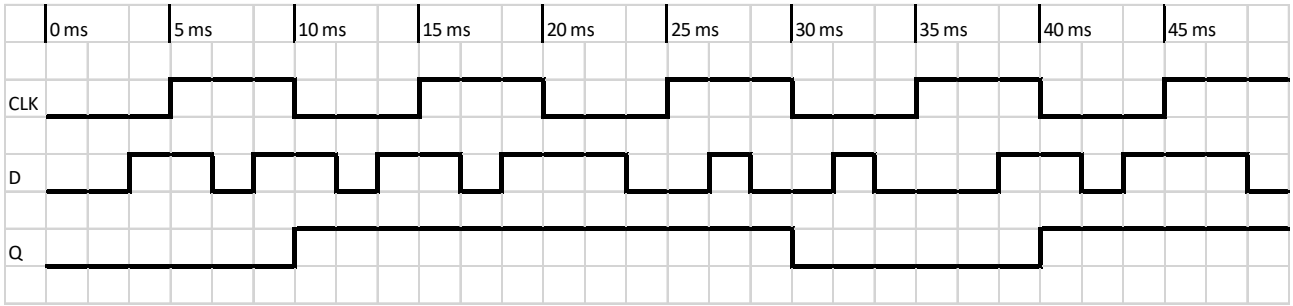


9 Timing diagram (Design)

Swedish: Vilken vippa eller latch ger tidsdiagrammet nedan?

English: Which flip-flop or latch has the timing diagram below?





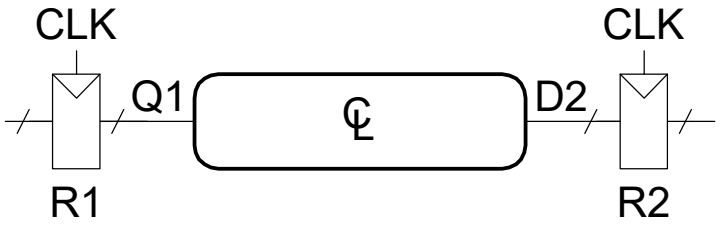
Answer: #2, negative edge DFF

10 Timing calculation

Swedish: Beräkna maximal klockfrekvens för kretsen. Är Hold-villkoret uppfyllt?

English: Calculate the maximum clock frequency for the circuit. Is the Hold time constraint ok?

t_{pcq} = 30 ps
t_{ccq} = 20 ps
t_{setup} = 50 ps
t_{hold} = 45 ps
t_{pd} = 120 ps
t_{cd} = 30 ps

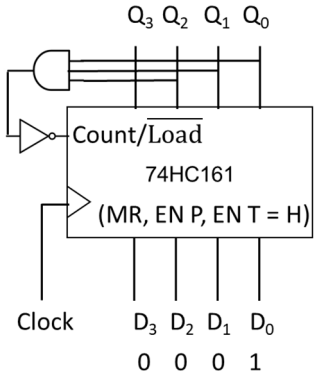


Tc = 30 + 50 + 120 = 200 ps fc = 1 / Tc = 5 GHz 45 - 20 - 30 = -5 ps, OK

11 Counter analysis

Swedish: Räknaren nedan har laddat in tillståndet $Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$.
Hur många tillstånd innan den upprepar sig? Vad är sista tillståndet?

English: The counter below has loaded state $Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$.
How many states until it repeats? What is the end state?

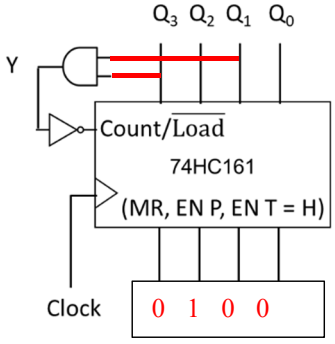


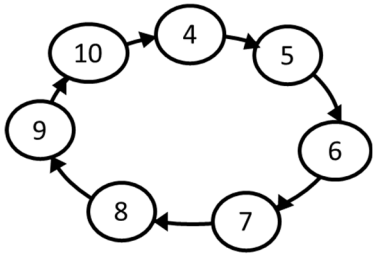
N = 7 Sequence: 0001 – 0111, Last state is 0111
The last state will cause the load operation next clk.
Count the number of states including the loaded state.

12 Counter design

Swedish: Hur ska AND-grinden (2 – 4 ingångar) och D_3 – D_0 kopplas för att få en räknare med tillståndsdiagrammet nedan?

English: How should the AND-gate (2 – 4 inputs) and D_3 – D_0 be connected to get a counter with the state diagram below?





The AND gate should detect the last state, $Y = Q_3 \cdot Q_1$
$D_3D_2D_1D_0$ should be connected to load the first state 0100

13 Multiplication

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A x B (binärt) och svara med ett 16 bitars två-komplement **hexadecimalt kodat tal**.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A x B (binary) and answer with a 16-bit binary (two's complement) **hexadecimal number**.
You can check your calculations using decimal numbers.

$A = 01011010_2$
$B = 01110111_2$

A x B = B x A (both are positive) put B above since it has more '1's
A = 90, B = 119, 90 x 119 = 10710

```
        01110111
      x 01011010
        01110111   1st multiplication
   +  01110111     2nd multiplication
      10010100110
   +  01110111     3rd multiplication
      110000010110
+  01110111        4th multiplication
0010100111010110 = 29D6₁₆
```

= 2x4096 + 9 x 256 + 13 x 16 + 6 = 10710

14 Division

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A / B (binärt) och svara med kvot och rest
(8 bitars två-komplement hexadecimalt kodade tal).
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A / B (binary) and answer with quotient and remainder
(8-bit binary two's complement hexadecimal numbers).
You can check your calculations using decimal numbers.

$A = 10000001_2$ $-A = 01111111_2$
$B = 11110010_2$ $-B = 00001110_2$

A and B are both negative, take 2's complement first, but results will be positive
-A = 127, -B = 14, 127 / 14 = 9, remainder 1

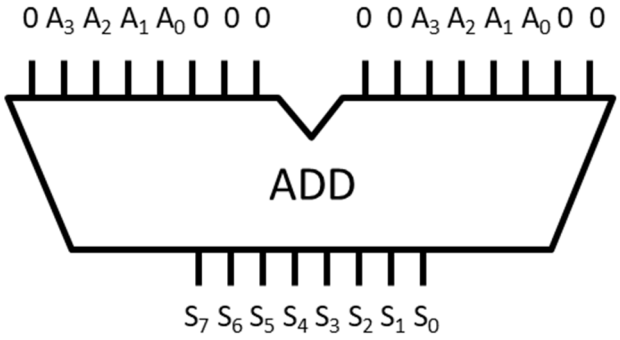
```
          1001  Quotient = 9
  1110/01111111
      - 1110
         1111
       - 1110
           01  Remainder = 1
```

15 Full Adder

Swedish: Vad blir resultatet från kretsen nedan?
Svara med 8 bitar (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0). Ignorera carry out (C_8).

English: What is the result for the circuit below?
Answer with 8 bits (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0). Ignore carry out (C_8).

A = 1100

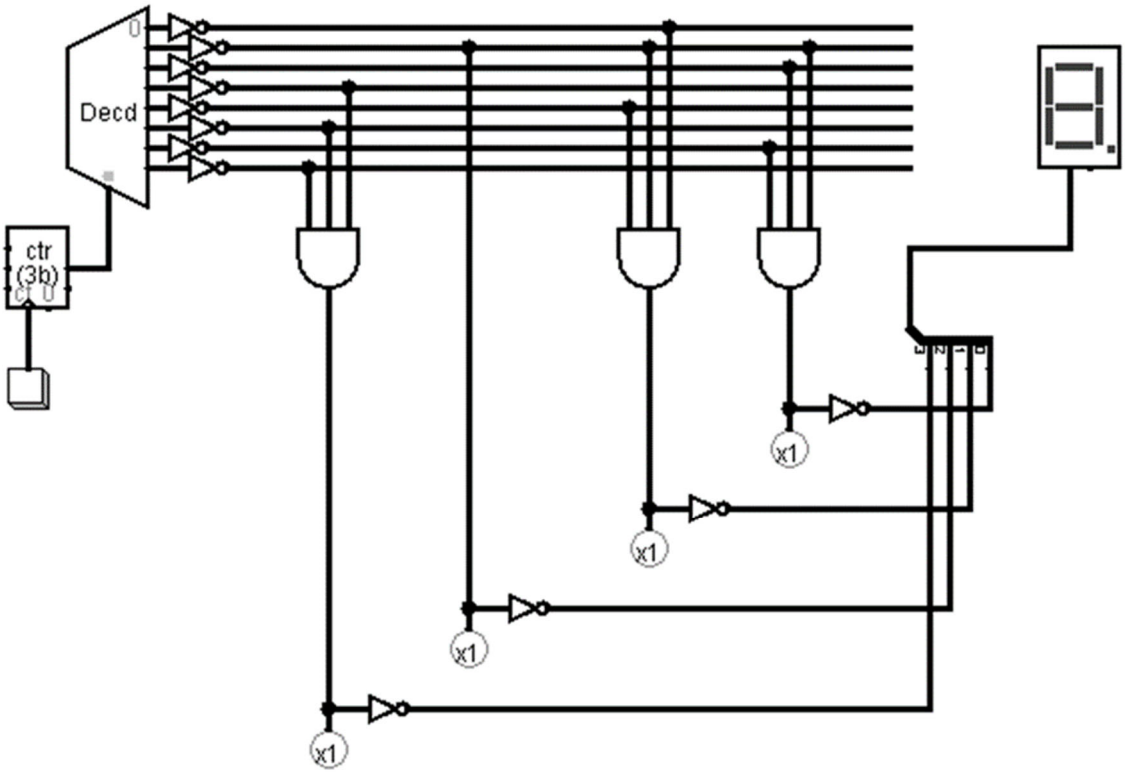



```
    110000   (12*4)
+   1100     (12*8)
  10010000   (12*12=144)
```

16 Memory

Swedish: Detta ROM har 8 st 4 bitars tal, vilka är talen?
Svara med 8 decimala siffror, från adress 000 till 111.

English: This ROM has 8 4-bit numbers stored, what are the numbers?
Answer with 8 decimal numbers, from address 000 to 111.



The number is 2 7 1 8 2 8 1 8 $(= e)$

Del 2/Part 2, 4 points per exercise, answer on separate paper

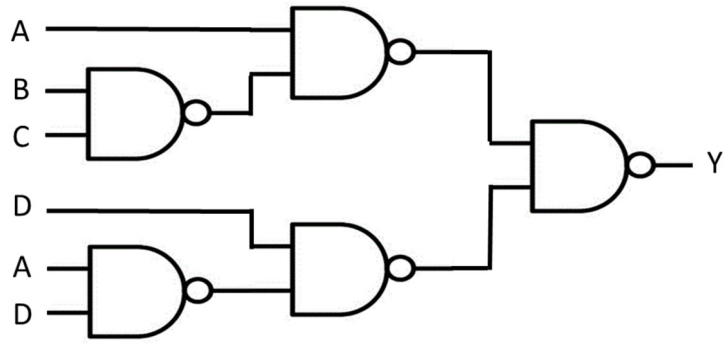
17 Analysis of Combinational Circuit

Swedish:

1. Ta fram booleskt uttryck för kretsen nedan.
2. Rita K-map för kretsen med variabelordning som i figuren.
3. Förenkla uttrycket med hjälp av K-map.
4. Rita ny krets med enbart NOR-grindar.

English:

1. Derive the Boolean expression for the circuit below.
2. Draw a K-map for the circuit with variables as in the figure.
3. Simplify the expression using the K-map.
4. Draw a new circuit using only NOR gates.



Y	CD 00	CD 01	CD 11	CD 10
AB 00	0	1	1	0
AB 01	0	1	1	0
AB 11	1	1	0	0
AB 10	1	1	1	1

Rita om K-map i dina inlämnade svar.

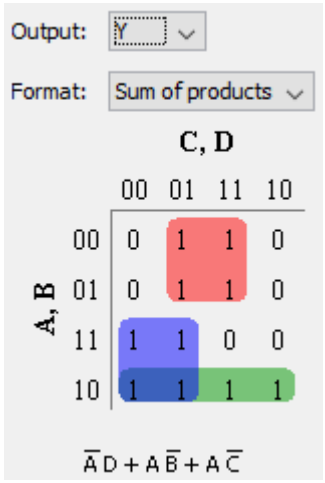
Redraw the K-map in your answer sheets.

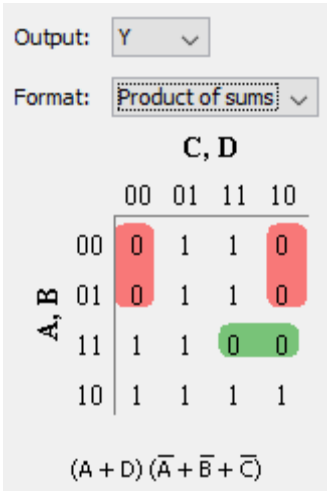
Boolean expression and truth table

$$Y = \overline{A \cdot \overline{B \cdot C} \cdot D \cdot \overline{A \cdot D}}$$

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

K-Map and simplified expressions



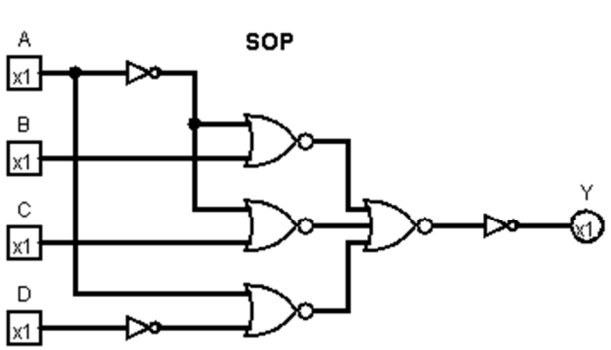


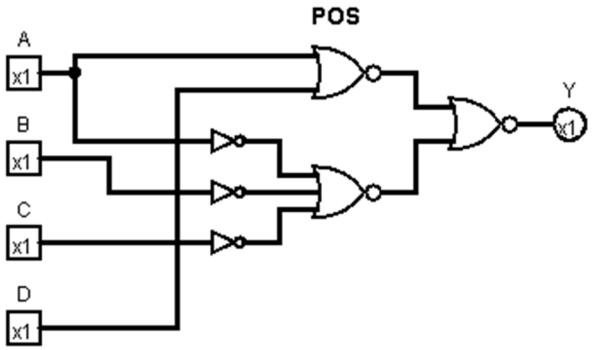
Can be simplified with Boolean Algebra (not necessary for full points) or from SOP:

$$Y = \overline{A \cdot \overline{B \cdot C} \cdot D \cdot \overline{A \cdot D}} = \overline{A \cdot \overline{B \cdot C}} + \overline{D \cdot \overline{A \cdot D}} = A \cdot \overline{B \cdot C} + D \cdot \overline{A \cdot D}$$
$$= A \cdot (\overline{B} + \overline{C}) + D \cdot (\overline{A} + \overline{D}) = A \cdot \overline{B} + A \cdot \overline{C} + D \cdot \overline{A} + D \cdot \overline{D}$$
$$= A \cdot \overline{B} + A \cdot \overline{C} + \overline{A} \cdot D = \overline{\overline{A \cdot \overline{B}}} + \overline{\overline{A \cdot \overline{C}}} + \overline{\overline{\overline{A} \cdot D}} = \overline{\overline{A} + B} + \overline{\overline{A} + C} + \overline{A + \overline{D}}$$
$$= \overline{\overline{\overline{A} + B + \overline{A} + C + A + \overline{D}}}$$

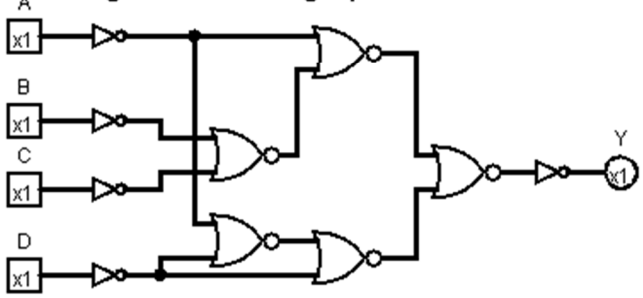
Or better from starting from POS since it is NOR (inverters can be made with NOR gates):

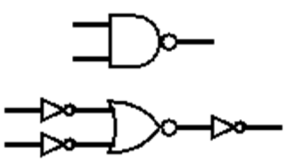
$$Y = (A + D)(\overline{A} + \overline{B} + \overline{C}) = \overline{\overline{(A + D)(\overline{A} + B + \overline{C})}} = \overline{\overline{A + D} + \overline{\overline{A} + \overline{B} + \overline{C}}}$$





From original circuit using equivalence:





18 Design of Combinational Circuit

Swedish:
Konstruera kretsen för en binär till BCD dekoder, som indikerar med y7y6y5y4 y3y2y1y0 hur siffrorna 0 - 15 i talet A B C D ska representeras i binary coded decimal med två siffror.
En del av sanningstabellen är given nedan. Bitarna y7, y6 och y5 är alltid 0.

1. Rita 5 st K-maps för sanningstabellen med variabelordning som i figuren.
2. Ta fram enklast möjliga booleska uttryck från 5 st K-maps.
3. Rita 5 st kretsar för uttrycken med enbart NAND-grindar.
4. Rita en krets som använder en 4 bitars adderare och grindar istället.
   Tips: BCD-talen genereras genom att addera 6 om talet är större än 9. Använd y4.

English:
Design the circuit for a binary to BCD decoder that indicates with y7y6y5y4 y3y2y1y0 how the numbers 0 - 15 represented by A B C D are represented in binary coded decimal with two digits.
The partial truth table is given below. The bits y7, y6 and y5 are always 0.

1. Draw 5 K-maps for the truth table with variables as in the figure.
2. Derive simplest possible Boolean expression from the 5 K-maps.
3. Draw 5 circuits for the expressions using only NAND-gates.
4. Draw a circuit that uses a 4 bit full adder and gates instead.
   Hint: BCD numbers add 6 to numbers greater than 9. Re-use y4.

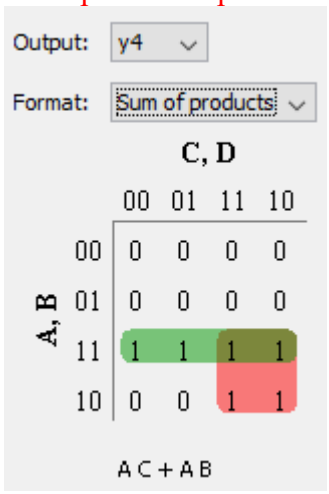
	CD 00	CD 01	CD 11	CD 10
AB 00				
AB 01				
AB 11				
AB 10				

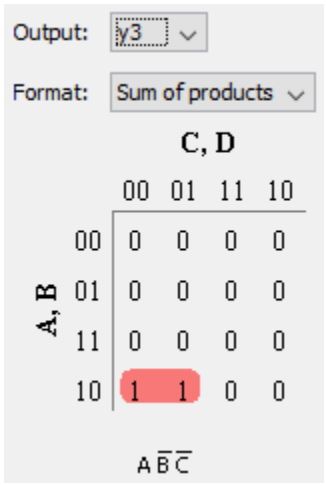
A	B	C	D	y4	y3	y2	y1	y0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0
0	0	1	1	0	0	0	1	1
0	1	0	0	0	0	1	0	0
0	1	0	1	0	0	1	0	1
0	1	1	0	0	0	1	1	0
0	1	1	1	0	0	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	1
1	0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	0	1
1	1	0	0	1	0	0	1	0
1	1	0	1	1	0	0	1	1
1	1	1	0	1	0	1	0	0
1	1	1	1	1	0	1	0	1

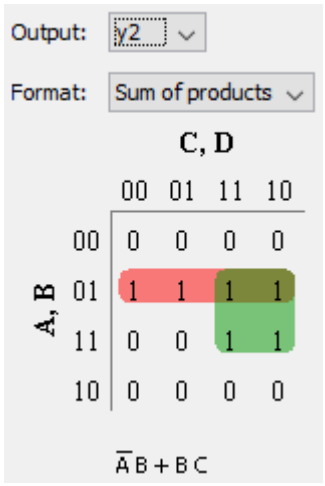
Rita om K-map i dina inlämnade svar.

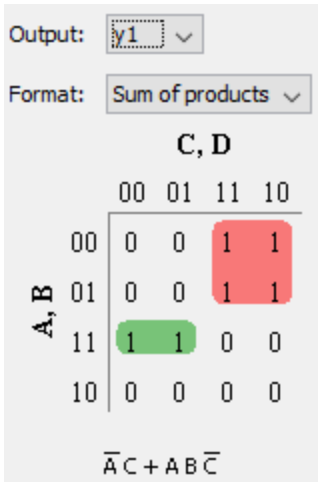
Redraw the K-map in your answer sheets.

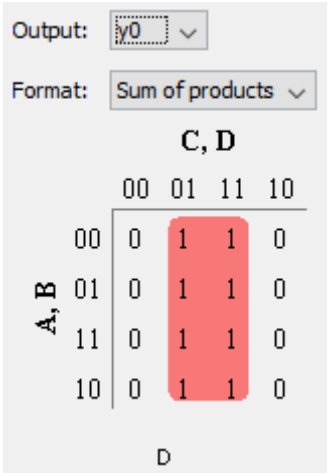
K-Maps and simplified expressions SOP:



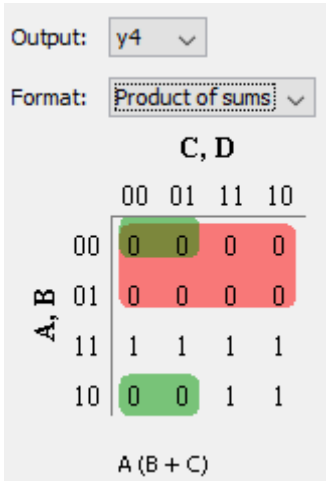


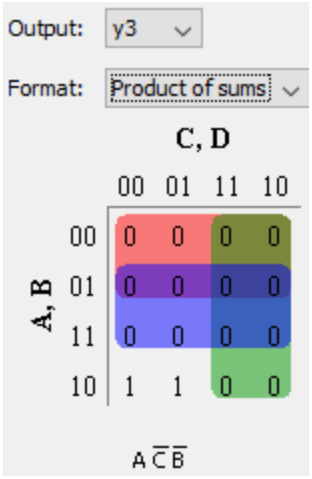


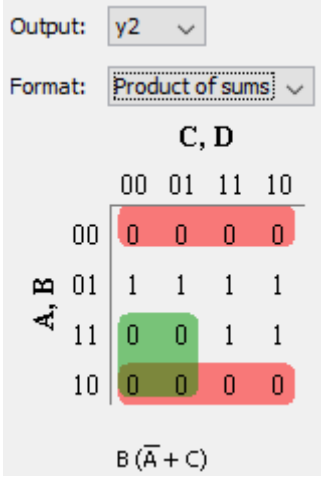


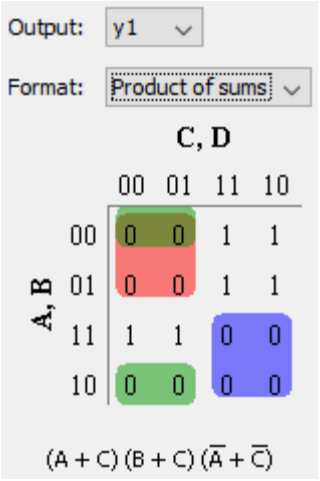


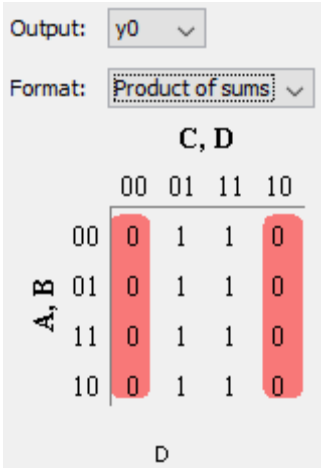
POS:



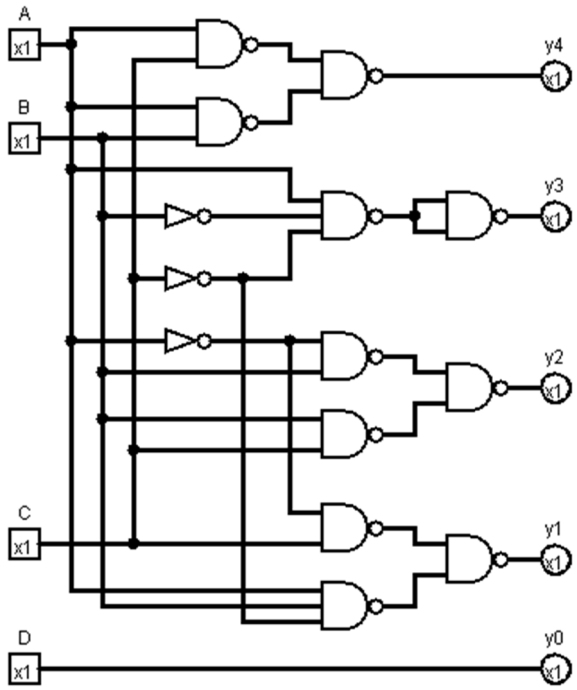




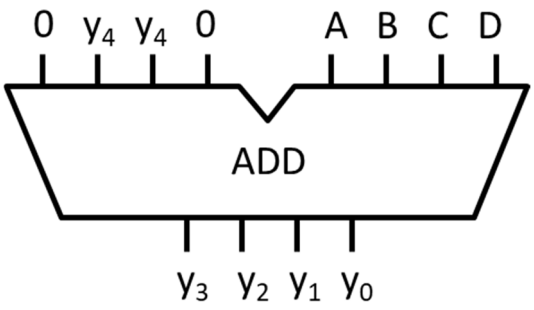




Normally use SOP for NAND only, and for this circuit the POS expressions are mostly longer. (inverters are ok if you note that they can be made with a NAND) See next page.



4 bit Full Adder version:



19 Analysis of FSM

Swedish: Analysera vad nedanstående tillståndsmaskin (FSM) utför.

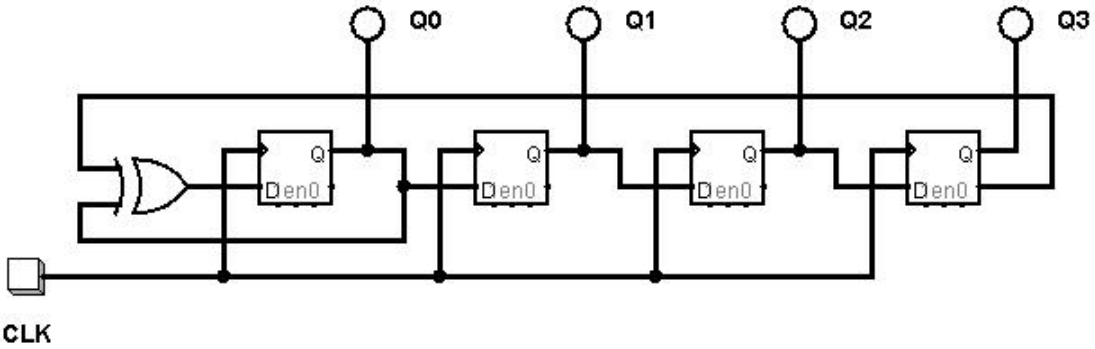
1. Ta fram Boolska uttryck för nästa tillstånd Q3+ Q2+ Q1+ Q0+.
2. Rita K-Maps för Q3+ Q2+ Q1+ Q0+.
3. Rita tillståndstabell.
4. Rita tillståndsdiagram.

Använd ordningen Q3 Q2 Q1 Q0

English: Analyze the state machine (FSM) below.

1. Derive Boolean expressions for next state Q3+ Q2+ Q1+ Q0+.
2. Draw K-Maps for Q3+ Q2+ Q1+ Q0+.
3. Draw a state table.
4. Draw a state diagram.

Use the order Q3 Q2 Q1 Q0



	Q_1Q_0 = 00	01	11	10
Q_3Q_2 = 00				
01				
11				
10				

Rita om K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

Boolean expressions

$Q3+= Q2$

$Q2+= Q1$

$Q1+= Q0$

$Q0+= \overline{Q3} \oplus Q0 = Q3 \cdot Q0 + \overline{Q3} \cdot \overline{Q0} = \overline{Q3 \oplus Q0}$

K-Maps and state table

Q3+	Q_1Q_0 00	01	11	10
Q_3Q_2 00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

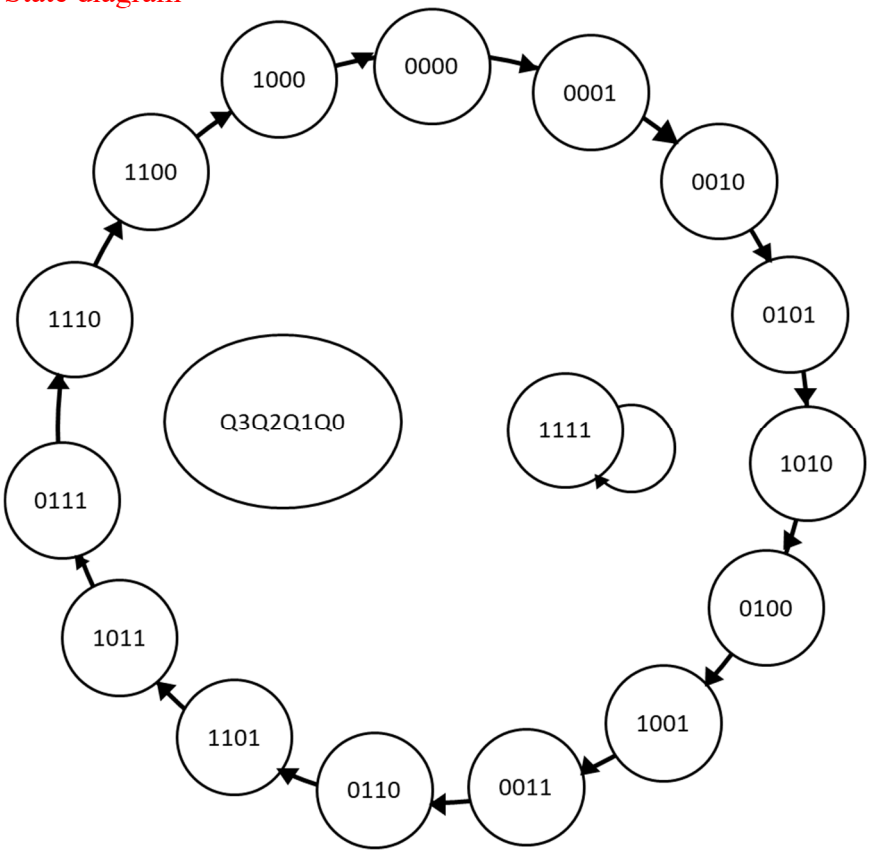
Q2+	Q_1Q_0 00	01	11	10
Q_3Q_2 00	0	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

Q1+	Q_1Q_0 00	01	11	10
Q_3Q_2 00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

Q0+	Q_1Q_0 00	01	11	10
Q_3Q_2 00	1	0	0	1
01	1	0	0	1
11	0	1	1	0
10	0	1	1	0

Present state				Next state			
Q3	Q2	Q1	Q0	Q3+	Q2+	Q1+	Q0+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	1	1
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1

State diagram



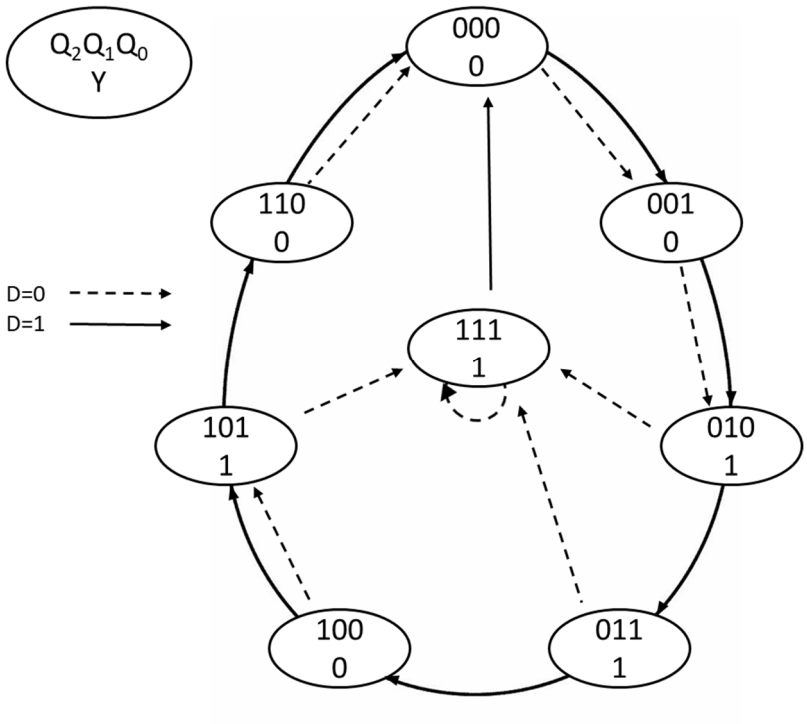
20 Design of FSM

Swedish: Konstruera en tillståndsmaskin (FSM) enligt tillståndsdiagrammet nedan.

1. Rita tillståndstabell.
2. Ta fram K-map för nästa tillstånd och utsignalen Y.
3. Ta fram minimerade uttryck för nästa tillstånd och utsignal.
4. Rita kretsschema för en FSM med DFFs och vilka grindar som helst utom MUX.

English: Design a state machine (FSM) according to the state diagram below.

1. Draw a state table.
2. Derive K-maps for next state and output Y.
3. Derive minimized expressions for next state and output.
4. Draw the FSM circuit diagram with DFFs and any gates except MUX.



	Q_1Q_0 = 00	01	11	10
D Q_2 = 00				
01				
11				
10				

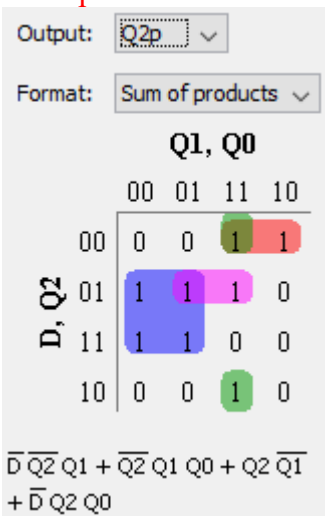
Rita om K-map i dina inlämnade svar.

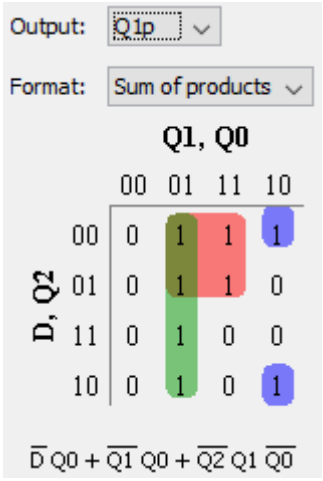
Redraw the K-map in your answer sheets.

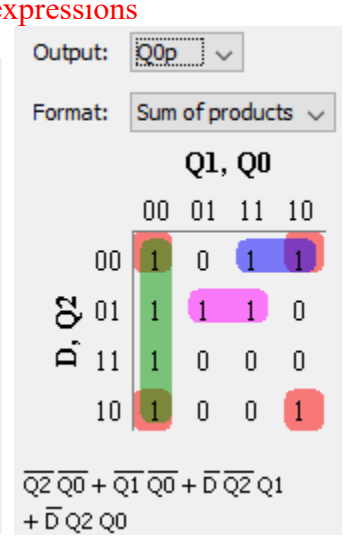
State table

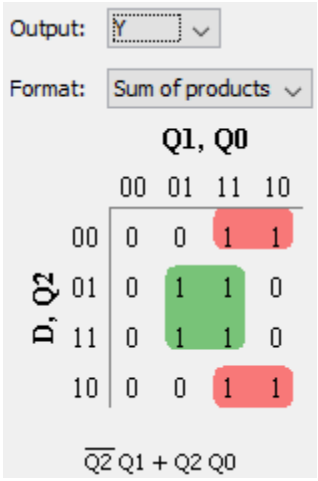
Present state			Next state D = 0			Next state D = 1			Output
Q2	Q1	Q0	Q2+	Q1+	Q0+	Q2+	Q1+	Q0+	Y
0	0	0	0	0	1	0	0	1	0
0	0	1	0	1	0	0	1	0	0
0	1	0	1	1	1	0	1	1	1
0	1	1	1	1	1	1	0	0	1
1	0	0	1	0	1	1	0	1	0
1	0	1	1	1	1	1	1	0	1
1	1	0	0	0	0	0	0	0	0
1	1	1	1	1	1	0	0	0	1

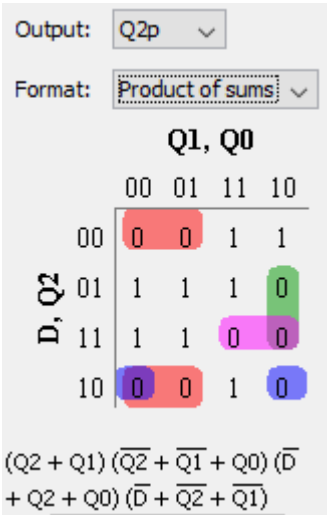
K-Maps for next state and output with minimized expressions

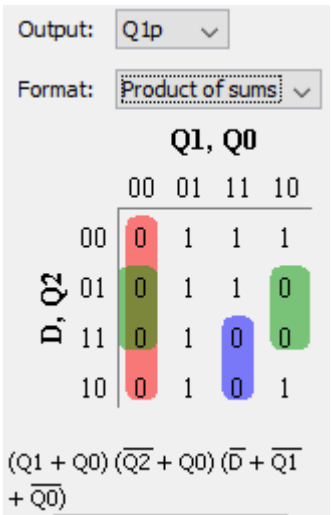


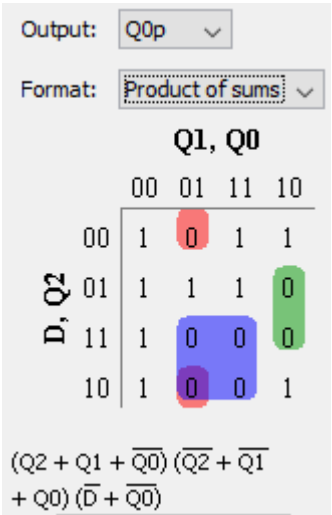


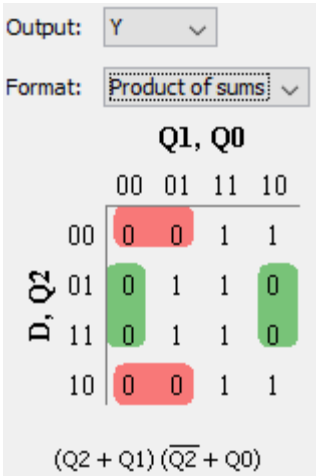












FSM circuit diagram (SoP version)