IE1204 Digital Design Answer Form 2025-01-09

Anonymized Code			
#	Answer with	Answer	Points
1	**Decimal** number		
2	8 bit two's complement **hexadecimal** number	0x	
3	8 bit two's complement **hexadecimal** number	0x	
4	Boolean expression, Y =		
5	Circuit number		
6	Boolean expression, Y =		
7	MUX connections, Boolean expression or Gate		
	Row CD = 00		
	Row CD = 01		
	Row CD = 10		
	Row CD = 11		
8	Timing diagrams		
9	Flip-Flop #		
10	Maximum circuit delay t_{pd} =	ps	
	Is the Hold time constraint ok?	[ ] Yes [ ] No	
11	Number of states =		
	Final state $Q_3Q_2Q_1Q_0$ =		
12	Boolean expression Y =		
	Input $D_3D_2D_1D_0$ =		
13	16 bit two's complement **hexadecimal**	P	
	Product A x B	0x	
14	8 bit two's complement **hexadecimal**	Q 0x	R 0x
	Quotient (A / B) and Remainder		
15	8 result bits (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0)		
16	Memory contents, 8 hexadecimal digits		
TOTAL POINTS		Examiner sign