



# Skriftlig Tentamen

## IE1204 Digital Design

### 2025-01-09 **Med Lösningar**

Examiner/Examinator: Carl-Mikael Zetterling

Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

#### **Swedish/Svenska:**

Tentamenstexten ska lämnas in när lösningarna lämnas in.

Inga tillåtna hjälpmedel utom linjal.

Examen består av två delar:

Del 1 har 16 uppgifter med max 1 poäng per uppgift som ska besvaras på "Answer Form".

Del 2 har 4 uppgifter med max 4 poäng per uppgift som ska besvaras på separat papper.

Lämna in båda delar samtidigt. Disponera tiden själv mellan delarna.

Uppgifterna är inte ordnade efter svårighetsgrad.

Om slutsumman av tentan har halvpöäng avrundas det uppåt.

Totalt max 32 poäng på tentamen.

För godkänt krävs

**(minst 8 poäng på del 1) OCH (minst 16 poäng totalt)**

Fx om något villkor ej är uppfyllt med en poängs marginal.

Det betyder att

För E krävs minst 16 poäng totalt och minst 8 på del 1.

För Fx krävs 16 poäng totalt och minst 7 på del 1

eller 15 poäng totalt och minst 8 på del 1.

**Betygskalan** för tentamen förutsatt att studenten har minst 8 poäng från del 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

Resultat meddelas inom tre veckor.

# Written Exam

## IE1204 Digital Design

### 2025-01-09 **With Solutions**

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Examiner/Examinator: Carl-Mikael Zetterling

Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

#### **English:**

The exam text should be handed in after the exam.

No aids allowed except ruler.

The exam consists of two parts:

Part 1 has 16 exercises for max 1 point per exercise to be answered on the “Answer Form”.

Part 2 has 4 exercises for max 4 points per exercise, to be answered on a separate paper.

Hand in both parts at the same time. Plan the time yourself between the parts.

The exercises are not in order of difficulty.

If the total sum of the exam has half points this will be rounded up.

Total max of 32 points on the exam.

To pass the exam requires

**(at least 8 points from part 1) AND (at least 16 points in total)**

Fx if any condition is not fulfilled by one point's margin.

This means

For E, a minimum of 16 points in total and at least 8 in part 1 is required.

For Fx, 16 points are required in total and at least 7 on part 1

or 15 points in total and at least 8 in part 1.

**Grades** are given as follows provided the student has at least 8 points from part 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

The result will be announced within three weeks.

# Del 1/Part 1, 1 point per exercise, fill in on "Answer Form"

## 1 Number Conversion

**Swedish:** Konvertera de positiva talen och utför beräkningen.  
Svara med ett decimalt tal.

**English:** Convert the unsigned numbers and perform the calculation.  
Answer with a decimal number.

$$Y = 101010_2 + 24_8 - 26_{10} + 28_{16} \\ = 42 + 20 - 26 + 40 = 76$$

## 2 Addition

**Swedish:** A och B är hexadecimala 8 bitars två-komplement kodade tal.  
Beräkna A + B och svara med ett 8 bitars två-komplement hexadecimalt kodat tal.  
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

**English:** A and B are hexadecimal 8-bit binary (two's complement) numbers.  
Calculate A + B and answer with an 8-bit binary (two's complement) hexadecimal number.  
You can check your calculations using decimal numbers.

$$\begin{array}{r} A = 0xC7 = C_{16} \quad 11000111 \\ B = 0x12 = 12_{16} \quad + 00010010 \\ \hline A + B \quad \quad \quad = 11011001 = 0xD9 \end{array}$$

or calculate directly from  $0xC7 + 0x12$

## 3 Subtraction

**Swedish:** A och B är hexadecimala 8 bitars två-komplement kodade tal.  
Beräkna A - B och svara med ett 8 bitars två-komplement hexadecimalt kodat tal.  
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

**English:** A and B are hexadecimal 8-bit binary (two's complement) numbers.  
Calculate A - B and answer with an 8-bit binary (two's complement) hexadecimal number.  
You can check your calculations using decimal numbers.

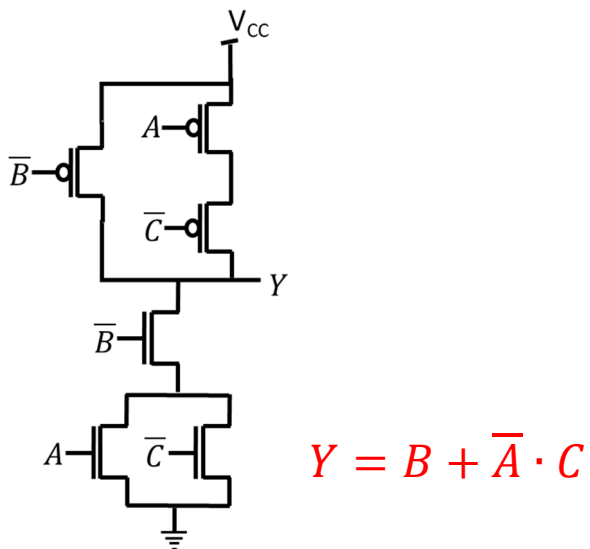
$$\begin{array}{r} A = 0xD9 = D_{16} \quad \quad \quad 11011001 \\ B = 0x53 = 53_{16} \quad = 01010011 \\ - B = \quad \quad \quad + \underline{10101101} \\ \hline A - B \quad \quad \quad = 10000110 = 0x86 \end{array}$$

or calculate directly from  $0xD9 - 0x53$

## 4 Analysis of CMOS circuits

**Swedish:** Ta fram enklast möjliga booleska uttryck för CMOS-kretsen.

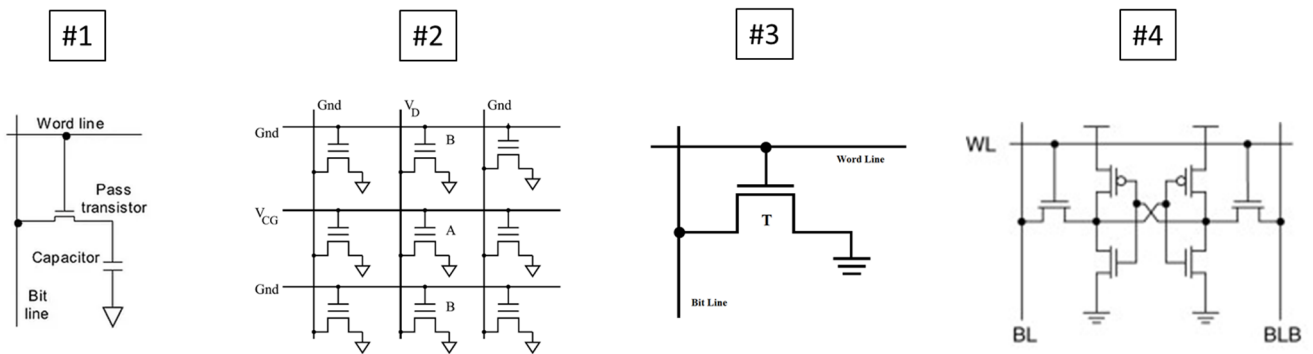
**English:** Derive the simplest possible Boolean expression for the CMOS circuit.



## 5 Memory circuits

**Swedish:** Vilken av kretsarna är en ROM?

**English:** Which circuit is a ROM?



#3

## 6 Analysis: MUX to K-map

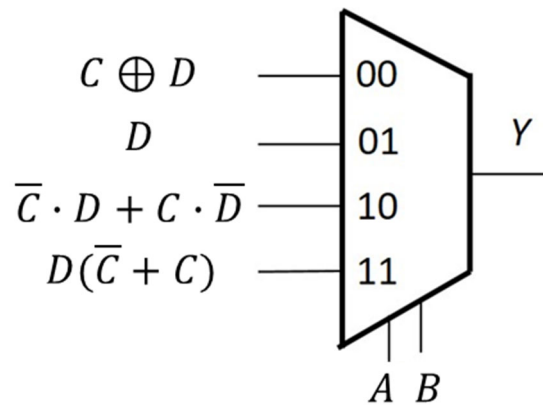
**Swedish:** Fyll i K-Map från MUX-kopplingen.

Ta fram enklast möjliga booleska uttryck för Y från K-map. Välj PoS eller SoP.

**English:** Fill in the K-Map from the MUX circuit.

Derive simplest possible Boolean expression from the K-map. Select PoS or SoP.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	0	1	0	1
AB 01	0	1	1	0
AB 11	0	1	1	0
AB 10	0	1	0	1



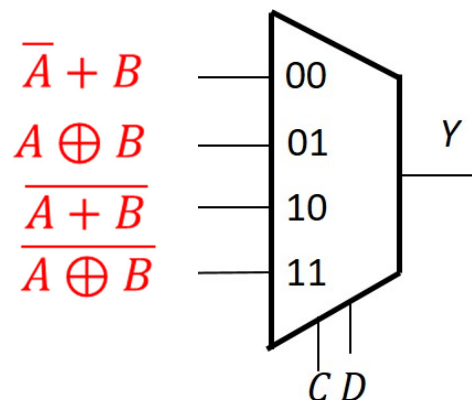
$$\bar{C} \cdot D + B \cdot D + \bar{B} \cdot C \cdot \bar{D} = (\bar{B} + D)(C + D)(B + \bar{C} + \bar{D})$$

## 7 Design: K-Map to MUX

**Swedish:** Använd en 4:1 MUX och valfria grindar eller 0 och 1 och gör en krets för K-map med CD som select-signaler.

**English:** Use a 4:1 MUX and any logic gates or 0 or 1 to draw a circuit for the K-map with CD as select signals.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	1	1
AB 01	1	1	0	0
AB 11	1	0	1	0
AB 10	0	1	0	0

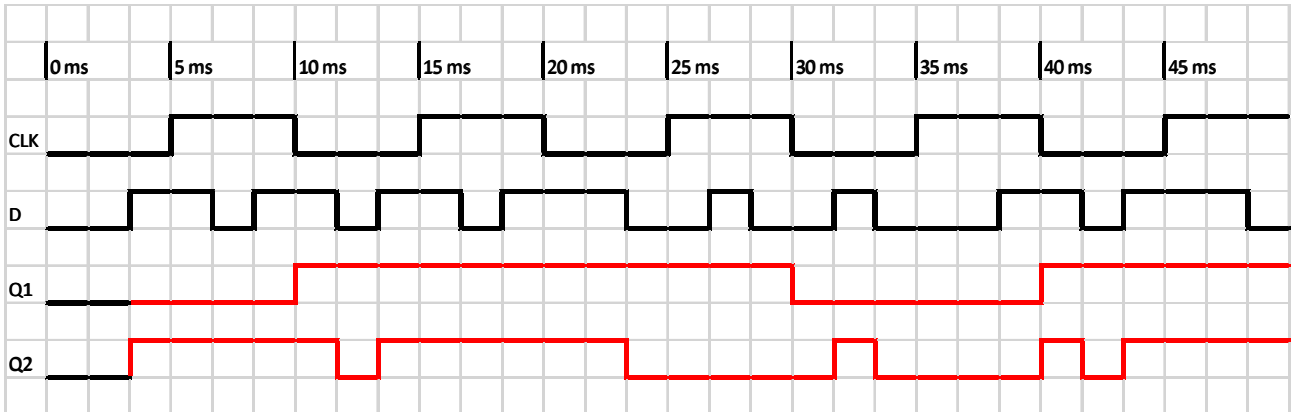
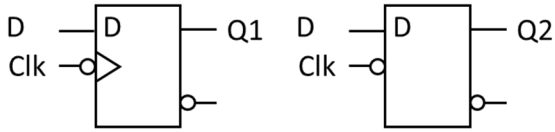


0.5 point deducted if third and fourth expressions are interchanged.

## 8 Timing diagram (Analysis)

**Swedish:** Rita tidsdiagram för kretsen i "Answer Form".

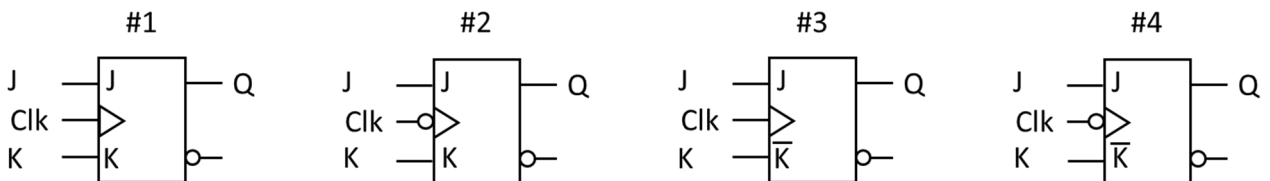
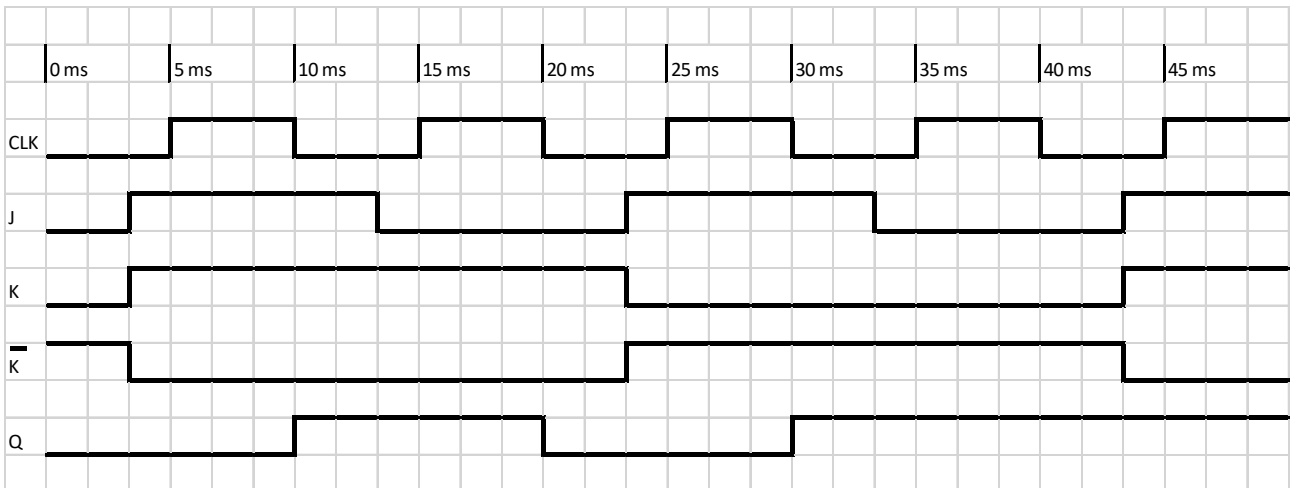
**English:** Draw the timing diagrams for the circuit in the "Answer Form".



## 9 Timing diagram (Design)

**Swedish:** Vilken vippa ger tidsdiagrammet nedan? OBS att alla fyra är olika.

**English:** Which flip-flop has the timing diagram below? NOTE that all four are different.



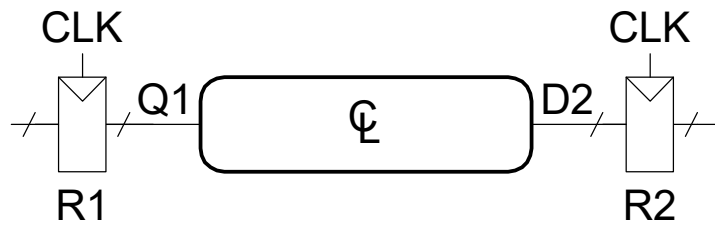
**Answer:** #2 negative edge triggered JK Flip-flop

## 10 Timing calculation

**Swedish:** Beräkna maximala fördröjningstiden  $t_{pd}$  för kretsen. Är Hold-villkoret uppfyllt?

**English:** Calculate the maximum delay time  $t_{pd}$  for the circuit. Is the Hold time constraint ok?

$t_{pcq} = 40 \text{ ps}$   
 $t_{ccq} = 20 \text{ ps}$   
 $t_{setup} = 50 \text{ ps}$   
 $t_{hold} = 45 \text{ ps}$   
 $t_{cd} = 30 \text{ ps}$   
 $T_c = 270 \text{ ps}$



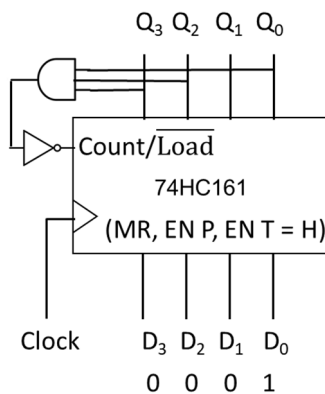
$$t_{pd} \leq 270 - 40 - 50 = 180 \text{ ps}$$

$$20 + 30 > 45 \text{ OK}$$

## 11 Counter analysis

**Swedish:** Räknaren nedan har laddat in tillståndet  $Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$ . Hur många klockpulser innan den upprepar sig? Vad är sista tillståndet?

**English:** The counter below has loaded state  $Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$ . How many clock pulses until it repeats? What is the end state?

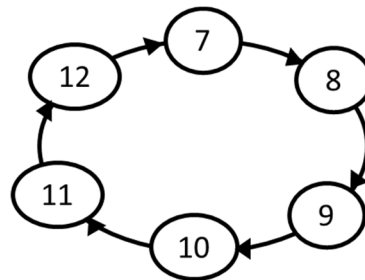
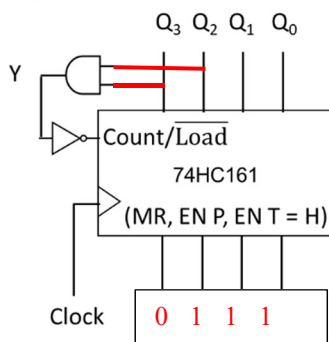


$N = 13$  Sequence: 0001 – 1101, Last state is 1101  
 The last state will cause a load operation on the next clk.  
 Count the number of states including the loaded state:  
 Last – Loaded (first) + 1

## 12 Counter design

**Swedish:** Hur ska AND-grunden och  $D_3 - D_0$  kopplas för att få en räknare med tillståndsdigrammet nedan?

**English:** How should the AND-gate and  $D_3 - D_0$  be connected to get a counter with the state diagram below?



The AND gate should detect the last state,  $Y = Q_3 \cdot Q_2$   
 $D_3D_2D_1D_0$  should be connected to load the first state 0111

### 13 Multiplication

**Swedish:** A och B är 8 bitars två-komplement kodade tal.  
Beräkna A x B (binärt) och svara med ett 16 bitars två-komplement **hexadecimalt kodat tal**.  
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

**English:** A and B are 8-bit binary (two's complement) numbers.  
Calculate A x B (binary) and answer with a 16-bit binary (two's complement) **hexadecimal number**.  
You can check your calculations using decimal numbers.

A = 01100101<sub>2</sub>  
B = 01111110<sub>2</sub>

A x B = B x A (both are positive) put B above since it has more '1's

```

      01111110
    x 01100101
    +-----
      01111110  1st multiplication
    + 01111110  2nd multiplication
      1001110110
    + 01111110  3rd multiplication
      1001000110110
    + 01111110  4th multiplication
    0011000110110110 = 31B616
```

### 14 Division

**Swedish:** A och B är 8 bitars två-komplement kodade tal.  
Beräkna A / B (binärt) och svara med kvot och rest  
(8 bitars två-komplement **hexadecimalt kodade tal**).  
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

**English:** A and B are 8-bit binary (two's complement) numbers.  
Calculate A / B (binary) and answer with quotient and remainder  
(8-bit binary two's complement **hexadecimal numbers**).  
You can check your calculations using decimal numbers.

A = 01111110<sub>2</sub>  
B = 00110000<sub>2</sub>

A and B are both positive

```

      10  Quotient = 2
110000/01111110
  - 110000
  -----
    11110  Remainder = 1E
```



## 15 Full Subtractor

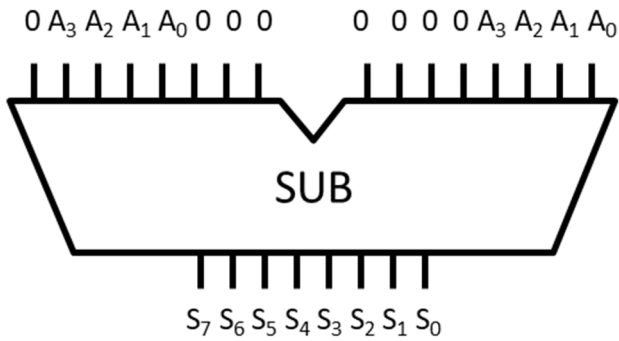
**Swedish:** Vad blir resultatet från kretsen nedan?

Svara med 8 bitar ( $S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0$ ). Ignorera carry out ( $C_8$ ).

**English:** What is the result for the circuit below?

Answer with 8 bits ( $S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0$ ). Ignore carry out ( $C_8$ ).

A = 1101



```

11110011 (-13)
+ 1101    (13*8)
(1)01011011 (13*7=91)
Ignore leading 1 for
subtraction
    
```

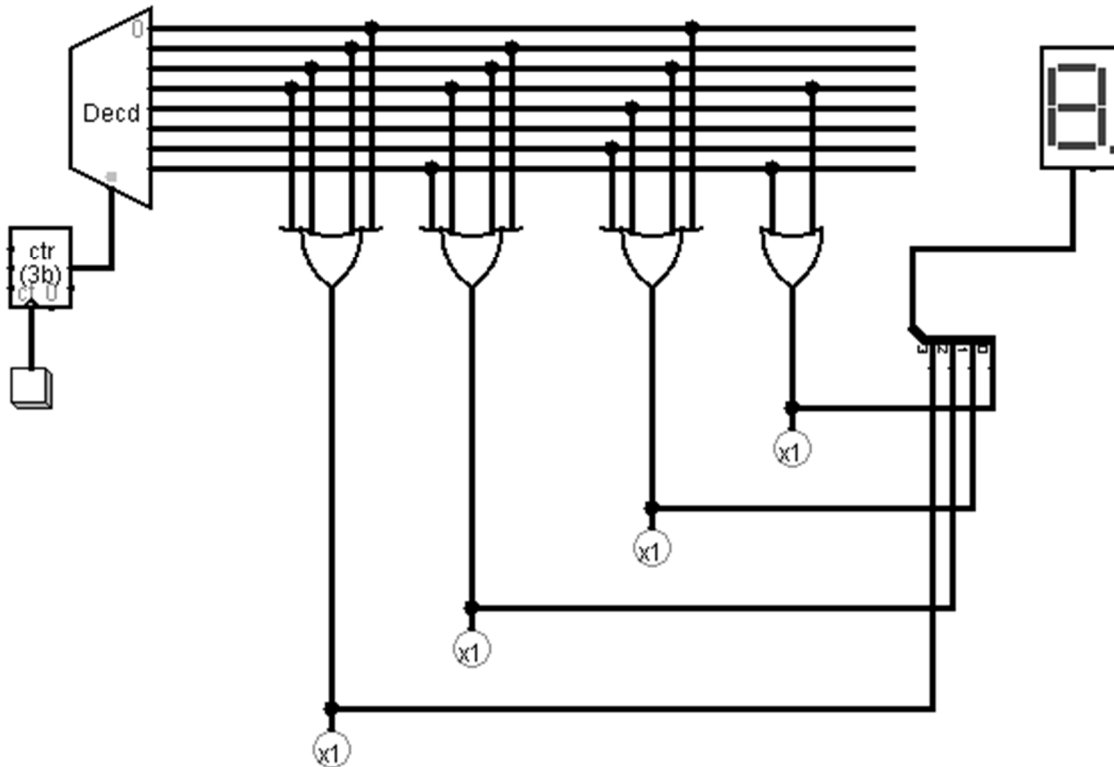
## 16 Memory

**Swedish:** Detta ROM har åtta 4 bitars tal, vilka är talen?

Svara med 8 **hexadecimala siffror**, från adress 000 till 111.

**English:** This ROM has eight 4-bit numbers stored, what are the numbers?

Answer with 8 **hexadecimal digits**, from address 000 to 111.



The hexadecimal number is A C E D 2 0 2 5

## Del 2/Part 2, 4 points per exercise, answer on separate paper

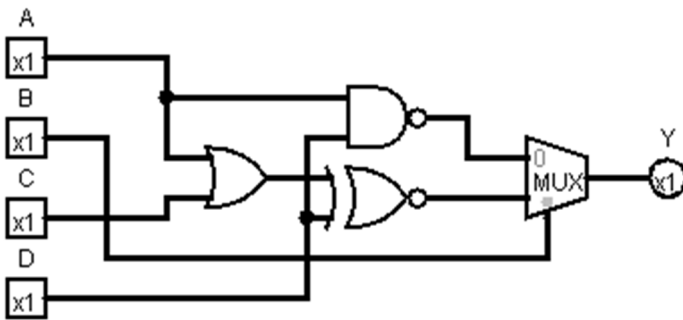
### 17 Analysis of Combinational Circuit

#### Swedish:

1. Ta fram booleskt uttryck för kretsen nedan.
2. Rita K-map för kretsen med variabelordning som i figuren.
3. Förenkla uttrycket med hjälp av K-map.
4. Rita ny krets med enbart NOR-grindar.

#### English:

1. Derive the Boolean expression for the circuit below.
2. Draw a K-map for the circuit with variables as in the figure.
3. Simplify the expression using the K-map.
4. Draw a new circuit using only NOR gates.



Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	1	1	1
AB 01	1	0	1	0
AB 11	0	1	1	0
AB 10	1	0	0	1

Rita av K-map i dina inlämnade svar.

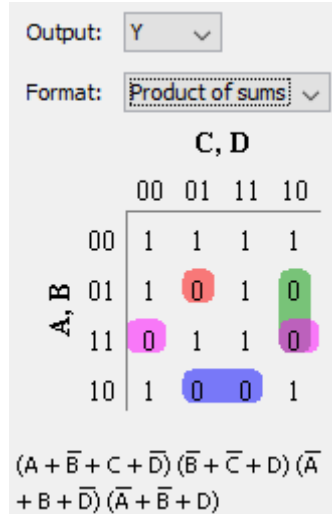
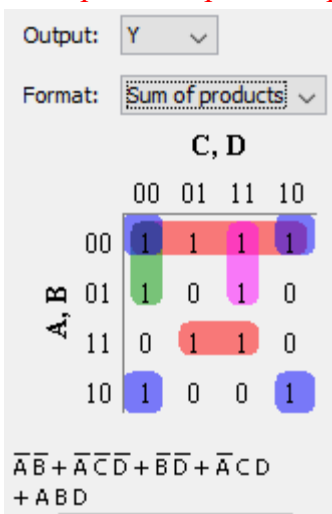
Redraw the K-map in your answer sheets.

Boolean expression and truth table

$$Y = \overline{B} \cdot \overline{A} \cdot \overline{D} + B \cdot ((A + C) \oplus D) = \overline{B} \cdot (\overline{A} + \overline{D}) + B \cdot ((A + C) \cdot \overline{D} + (A + C) \cdot D) = \overline{A} \cdot \overline{B} + \overline{B} \cdot \overline{D} + B \cdot (\overline{A} \cdot \overline{C} \cdot \overline{D} + A \cdot D + C \cdot D) = \overline{A} \cdot \overline{B} + \overline{B} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + A \cdot B \cdot D + B \cdot C \cdot D$$

(Equivalent to SoP below if  $B \cdot C \cdot D$  is exchanged for  $\overline{A} \cdot C \cdot D$ )

K-Map and simplified expressions



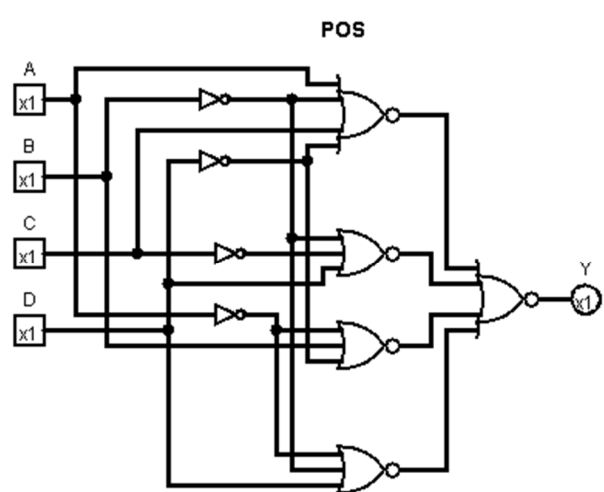
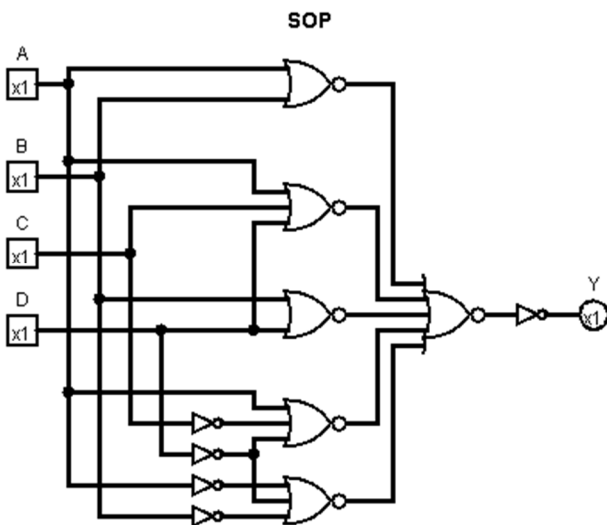
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Can be built from SOP:

$$\begin{aligned} Y &= \overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{C} \cdot \overline{D} + \overline{B} \cdot \overline{D} + \overline{A} \cdot C \cdot D + A \cdot B \cdot D \\ &= \overline{\overline{\overline{A} \cdot \overline{B}}} + \overline{\overline{\overline{A} \cdot \overline{C} \cdot \overline{D}}} + \overline{\overline{\overline{B} \cdot \overline{D}}} + \overline{\overline{\overline{A} \cdot C \cdot D}} + \overline{\overline{\overline{A} \cdot B \cdot D}} \\ &= \overline{\overline{A + B} + \overline{A + C + D} + \overline{B + D} + \overline{A + C} + \overline{D} + \overline{A + B} + \overline{D}} \\ &= \overline{\overline{A + B} + \overline{A + C + D} + \overline{B + D} + \overline{A + C} + \overline{D} + \overline{A + B} + \overline{D}} \end{aligned}$$

Or better from starting from POS since it is NOR (inverters can be made with NOR gates):

$$\begin{aligned} Y &= (A + \overline{B} + C + \overline{D})(\overline{B} + \overline{C} + D)(\overline{A} + B + \overline{D})(\overline{A} + \overline{B} + D) \\ &= \overline{\overline{A + \overline{B} + C + \overline{D}} + \overline{\overline{B} + \overline{C} + D} + \overline{\overline{A} + B + \overline{D}} + \overline{\overline{A} + \overline{B} + D}} \\ &= \overline{(A + \overline{B} + C + \overline{D}) + (\overline{B} + \overline{C} + D) + (\overline{A} + B + \overline{D}) + (\overline{A} + \overline{B} + D)} \end{aligned}$$



## 18 Design of Combinational Circuit

### Swedish:

Decimaltal kan konverteras till binära tal med fixnotation. Tex så blir  $e \approx 2,718281828$  på detta sätt 10.10110111111000. Vi kan använda det som funktion för en sanningstabell, se nedan.

1. Rita en K-map för sanningstabellen med variabelordning som i figuren.
2. Ta fram enklast möjliga booleska uttryck.
3. Rita en krets för uttrycket med enbart NAND-grindar.
4. Rita en krets för K-map som använder en 4:1 Mux och grindar.

### English:

Decimal numbers can be converted to binary with fix notation. For instance  $e \approx 2,718281828$  can be written as 10.10110111111000. We can use it as the truth table function, see below.

1. Draw a K-map for the truth table with variables as in the figure.
2. Derive the simplest possible Boolean expression from the K-map.
3. Draw the circuit for the expression using only NAND-gates.
4. Draw a circuit for the K-Map using a 4:1 Mux and gates.

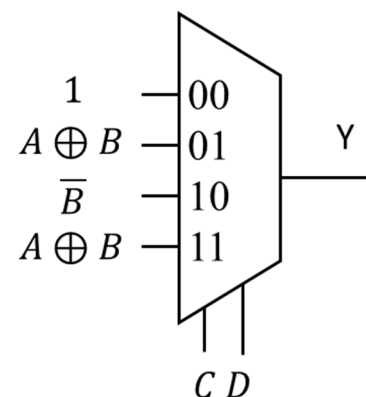
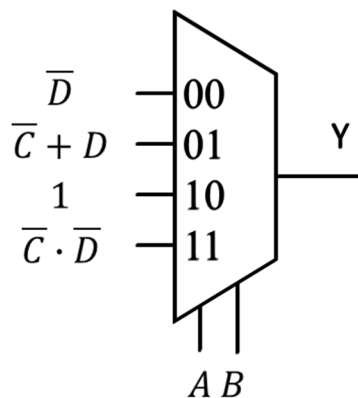
Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	0	1
AB 01	1	1	1	0
AB 11	1	0	0	0
AB 10	1	1	1	1

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

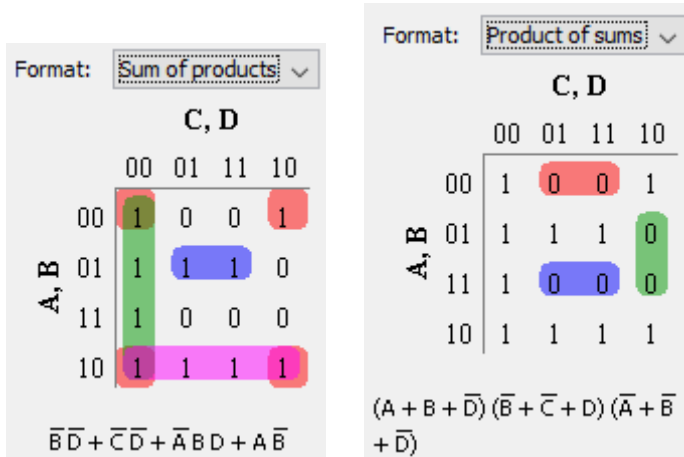
Rita av K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

Two possible Mux solutions:

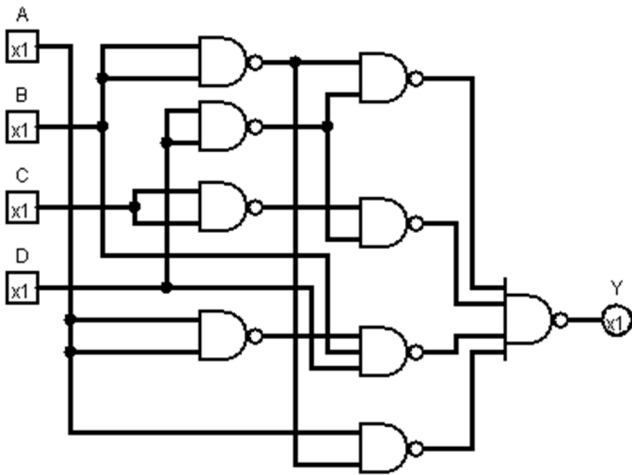


## K-Maps and simplified expressions

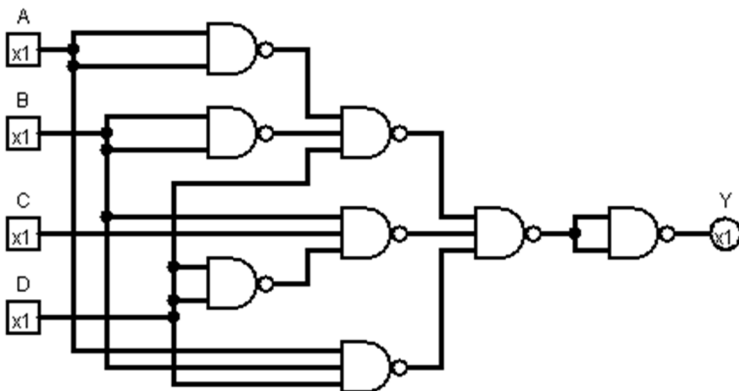


Normally use SOP for NAND only (inverters are ok if you note that they can be made with NAND).

$$\begin{aligned}
 Y &= \overline{B} \cdot \overline{D} + \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot D + A \cdot \overline{B} = \overline{\overline{\overline{B} \cdot \overline{D} + \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot D + A \cdot \overline{B}}} \\
 &= \overline{\overline{\overline{B} \cdot \overline{D}} \cdot \overline{\overline{C} \cdot \overline{D}} \cdot \overline{\overline{A} \cdot B \cdot D}} \cdot \overline{\overline{A \cdot \overline{B}}}
 \end{aligned}$$



$$\begin{aligned}
 \text{For POS } Y &= (A + B + \overline{D})(\overline{B} + \overline{C} + D)(\overline{A} + \overline{B} + D) = \overline{\overline{\overline{A + B + \overline{D}}}} \cdot \overline{\overline{\overline{\overline{B} + \overline{C} + D}}} \cdot \overline{\overline{\overline{\overline{\overline{A} + \overline{B} + D}}}} \\
 &= \overline{\overline{\overline{A} \cdot \overline{B} \cdot D}} \cdot \overline{\overline{\overline{B} \cdot C \cdot \overline{D}}} \cdot \overline{\overline{\overline{A} \cdot B \cdot D}} = \overline{\overline{\overline{\overline{\overline{A} \cdot \overline{B} \cdot D}} \cdot \overline{\overline{B} \cdot C \cdot \overline{D}} \cdot \overline{\overline{A} \cdot B \cdot D}}}
 \end{aligned}$$



## 19 Analysis of FSM

**Swedish:** Analysera vad tillståndsmaskinen (FSM) på nästa sida utför.

1. Ta fram Boolska uttryck för nästa tillstånd  $Q_3+$   $Q_2+$   $Q_1+$   $Q_0+$  och utsignal  $Y$ .
2. Rita K-Maps för  $Q_3+$   $Q_2+$   $Q_1+$   $Q_0+$  och utsignal  $Y$ .
3. Rita tillståndstabell.
4. Rita tillståndsdigram.

Använd ordningen  $Q_3$   $Q_2$   $Q_1$   $Q_0$

**English:** Analyze the state machine (FSM) on the next page.

1. Derive Boolean expressions for next state  $Q_3+$   $Q_2+$   $Q_1+$   $Q_0+$  and output  $Y$ .
2. Draw K-Maps for  $Q_3+$   $Q_2+$   $Q_1+$   $Q_0+$  and output  $Y$ .
3. Draw a state table.
4. Draw a state diagram.

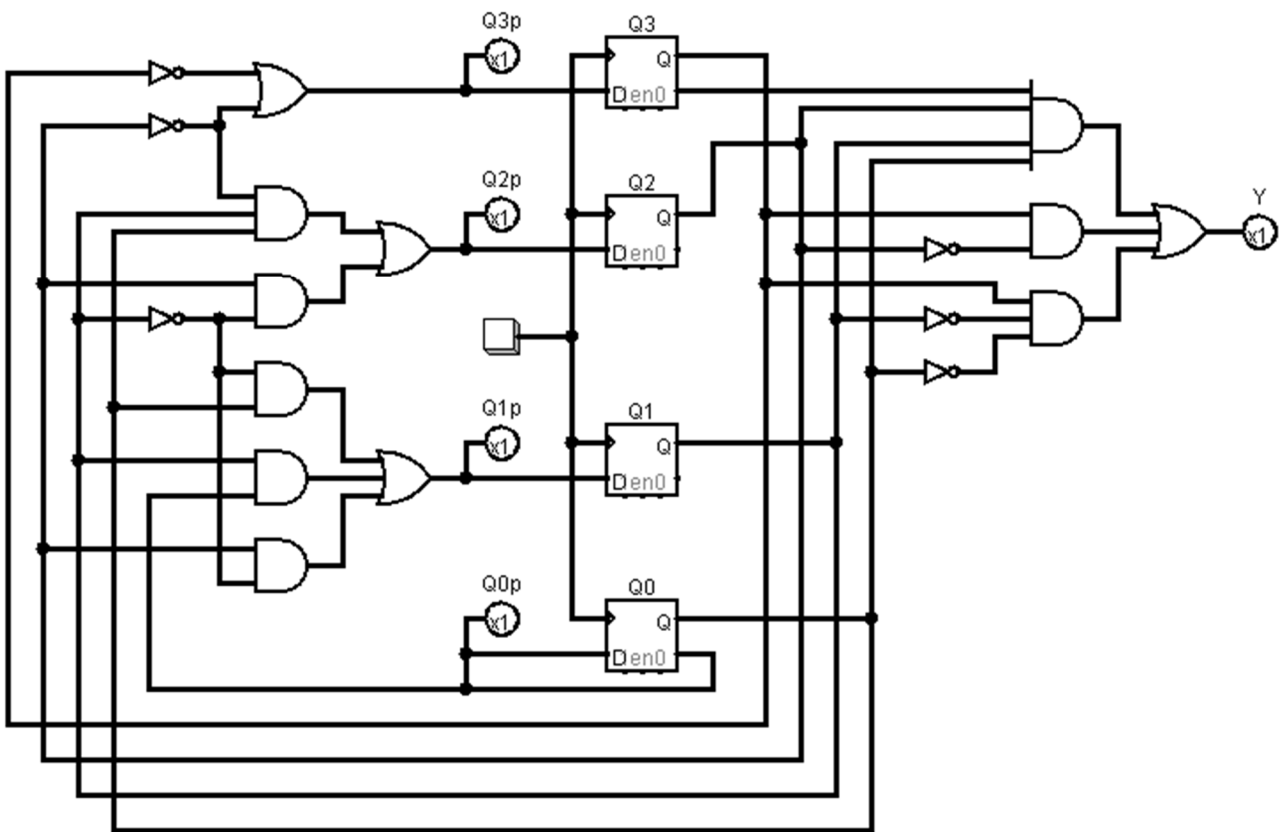
Use the order  $Q_3$   $Q_2$   $Q_1$   $Q_0$

	$Q_1Q_0 =$ 00	01	11	10
$Q_3Q_2 =$ 00				
01				
11				
10				

Rita av K-map i dina  
inlämnade svar.

Redraw the K-map in  
your answer sheets.

19 Analysis of FSM cont.



Boolean expressions:

$$Q_3^+ = \overline{Q_3} + \overline{Q_2}$$

$$Q_2^+ = \overline{Q_2} \cdot Q_1 \cdot Q_0 + Q_2 \cdot \overline{Q_1}$$

$$Q_1^+ = \overline{Q_1} \cdot Q_0 + Q_1 \cdot \overline{Q_0} + Q_2 \cdot \overline{Q_1}$$

$$Q_0^+ = \overline{Q_0}$$

$$Y = \overline{Q_3} \cdot Q_2 \cdot Q_1 \cdot Q_0 + Q_3 \cdot \overline{Q_2} + Q_3 \cdot \overline{Q_1} \cdot \overline{Q_0}$$

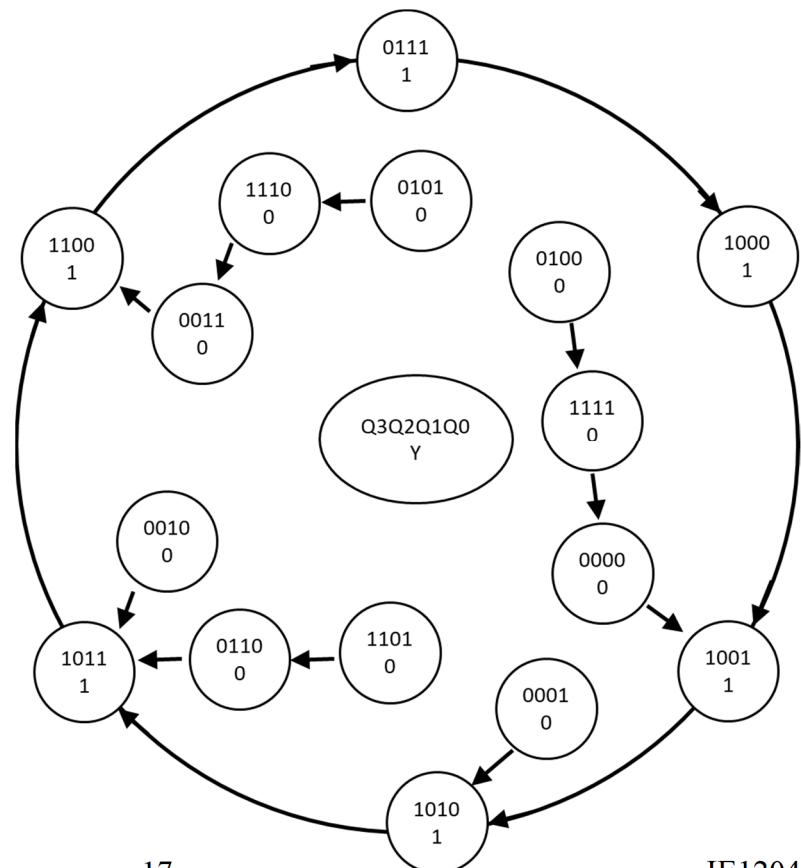
Y	Q <sub>1</sub> Q <sub>0</sub>			
	00	01	11	10
Q <sub>3</sub> Q <sub>2</sub>	00	0	0	0
	01	0	0	1
11	1	0	0	0
10	1	1	1	1

K-Maps and state table

Q <sub>3</sub> <sup>+</sup>	Q <sub>1</sub> Q <sub>0</sub>				Q <sub>2</sub> <sup>+</sup>	Q <sub>1</sub> Q <sub>0</sub>				
	00	01	11	10		00	01	11	10	
	00	1	1	1		1	0	0	1	0
	01	1	1	1		1	1	1	0	0
	11	0	0	0		0	1	1	0	0
10	1	1	1	1	0	0	1	0		
Q <sub>1</sub> <sup>+</sup>	Q <sub>1</sub> Q <sub>0</sub>				Q <sub>0</sub> <sup>+</sup>	Q <sub>1</sub> Q <sub>0</sub>				
	00	01	11	10		00	01	11	10	
	00	0	1	0		1	1	0	0	1
	01	1	1	0		1	1	0	0	1
	11	1	1	0		1	1	0	0	1
10	0	1	0	1	1	0	0	1		

Present state				Next state				Output
Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	Q <sub>3</sub> <sup>+</sup>	Q <sub>2</sub> <sup>+</sup>	Q <sub>1</sub> <sup>+</sup>	Q <sub>0</sub> <sup>+</sup>	Y
0	0	0	0	1	0	0	1	0
0	0	0	1	1	0	1	0	0
0	0	1	0	1	0	1	1	0
0	0	1	1	1	1	0	0	0
0	1	0	0	1	1	1	1	0
0	1	0	1	1	1	1	0	0
0	1	1	0	1	0	1	1	0
0	1	1	1	1	0	0	0	1
1	0	0	0	1	0	0	1	1
1	0	0	1	1	0	1	0	1
1	0	1	0	1	1	0	1	1
1	0	1	1	1	1	1	0	0
1	1	0	0	0	1	1	1	1
1	1	0	1	0	1	1	0	0
1	1	1	0	0	0	1	1	0
1	1	1	1	0	0	0	0	0

State diagram; a counter for 0111 – 1100 reversed, Y = 0 if outside the sequence. Similar to Exercise 12.





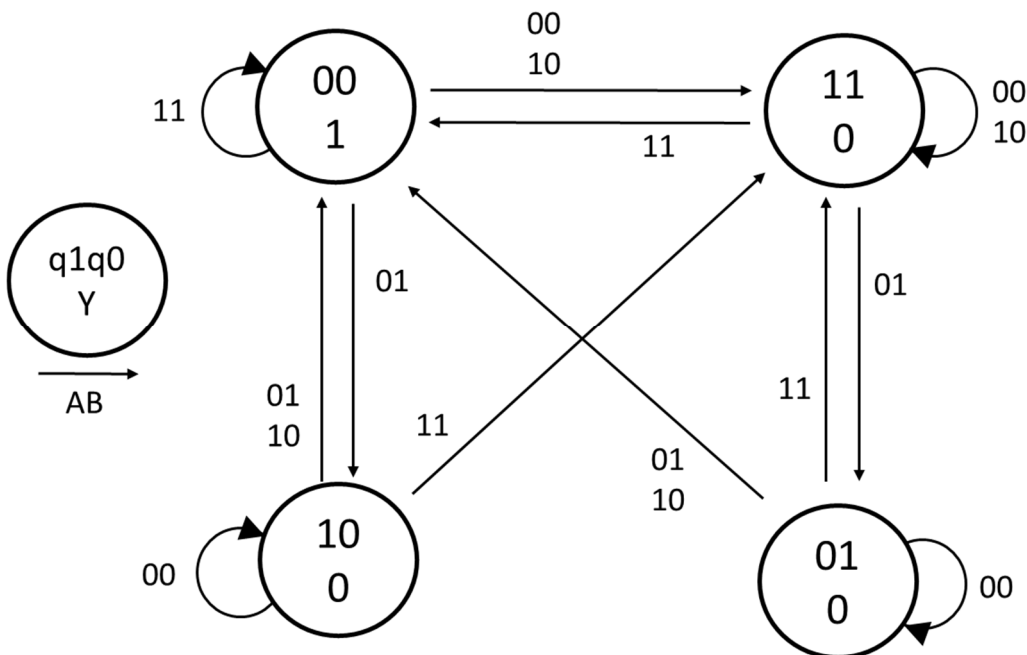
## 20 Design of FSM

**Swedish:** Konstruera en tillståndsmaskin (FSM) enligt tillståndsdigrammet nedan.

1. Rita tillståndstabell.
2. Ta fram K-map för nästa tillstånd.
3. Ta fram minimerade uttryck för nästa tillstånd.
4. Rita kretsschema för en FSM med DFFs och MUX eller vilka grindar som helst.

**English:** Design a state machine (FSM) according to the state diagram below.

1. Draw a state table.
2. Derive K-maps for next state.
3. Derive minimized expressions for next state.
4. Draw the FSM circuit diagram with DFFs and MUX or any gates.



	AB 00	AB 01	AB 11	AB 10
q1q0 00				
q1q0 01				
q1q0 11				
q1q0 10				

Rita av K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

State table

Present state		Next state								
		AB = 00		AB = 01		AB = 11		AB = 10		Out Y
q1	q0	q1+	q0+	q1+	q0+	q1+	q0+	q1+	q0+	
0	0	1	1	1	0	0	0	1	1	1
0	1	0	1	0	0	1	1	0	0	0
1	1	1	1	0	1	0	0	1	1	0
1	0	1	0	0	0	1	1	0	0	0

K-Maps for next state with minimized expressions (not necessary for  $Y = \overline{q1 + q0} = \overline{q1} \cdot \overline{q0}$ )

Output:

Format:

A, B

	00	01	11	10
00	1	1	0	1
01	0	0	1	0
11	1	0	0	1
10	1	0	1	0

$\overline{q1} \overline{q0} \overline{A} + \overline{q1} \overline{q0} B + \overline{q0} A \overline{B}$   
 $+ \overline{q1} q0 A B + q1 \overline{q0} A B$   
 $+ q1 q0 \overline{B}$

Output:

Format:

A, B

	00	01	11	10
00	1	0	0	1
01	1	0	1	0
11	1	1	0	1
10	0	0	1	0

$\overline{q1} \overline{q0} \overline{B} + \overline{q1} A \overline{B} + \overline{q1} q0 A B$   
 $+ q1 \overline{q0} A B + q1 q0 \overline{A} + q1 q0 \overline{B}$

Output:

Format:

A, B

	00	01	11	10
00	1	1	0	1
01	0	0	1	0
11	1	0	0	1
10	1	0	1	0

$(q1 + q0 + \overline{A} + \overline{B})(q1 + \overline{q0} + A)(q1 + \overline{q0} + B)(\overline{q1} + A + \overline{B})(\overline{q1} + q0 + \overline{A} + B)(\overline{q1} + \overline{q0} + \overline{B})$

Output:

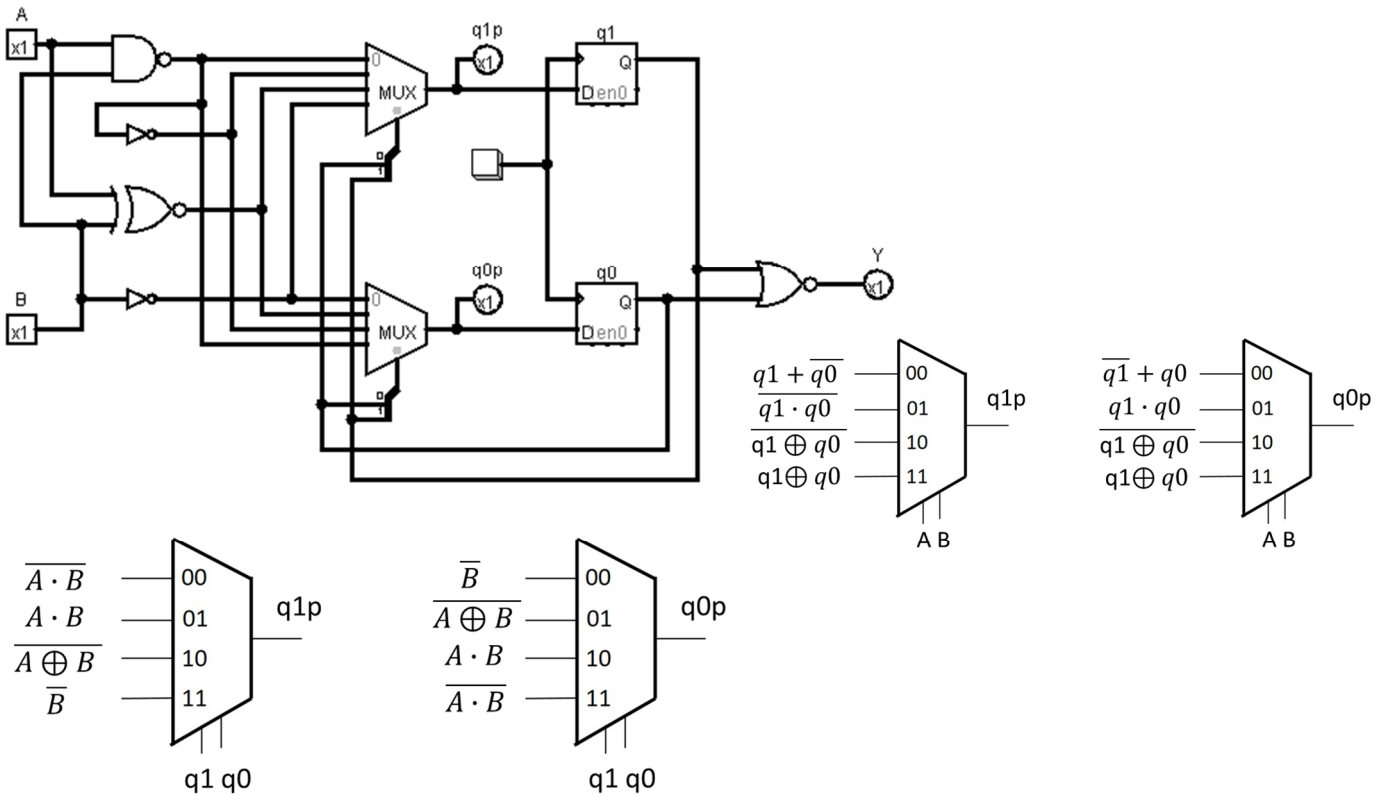
Format:

A, B

	00	01	11	10
00	1	0	0	1
01	1	0	1	0
11	1	1	0	1
10	0	0	1	0

$\overline{q1} \overline{q0} \overline{B} + \overline{q1} A \overline{B} + \overline{q1} q0 A B$   
 $+ q1 \overline{q0} A B + q1 q0 \overline{A} + q1 q0 \overline{B}$

FSM circuit diagram (MUX version)



FSM Diagram SOP version

