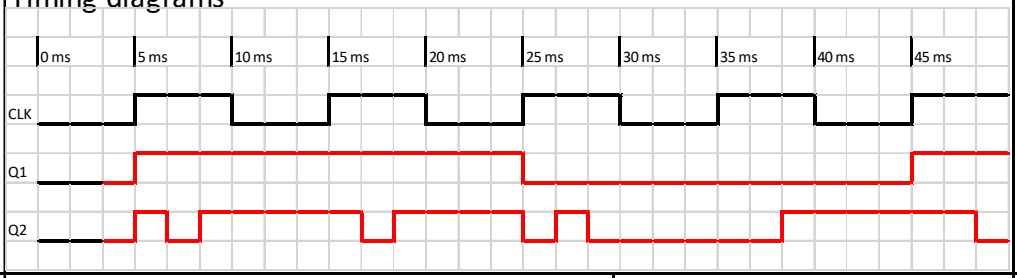
IE1204 Digital Design Answer Form 2025-04-25

Anonymized Code			
2025-04-25			
#	Answer with	Answer	Points
1	**Decimal** number	75	
2	8 bit two's complement **hexadecimal** number	0xDC	
3	8 bit two's complement **hexadecimal** number	0x88	
4	Boolean expression, Y =	$Y = \overline{C} + A \cdot B$	
5	Circuit number	#1	
6	Boolean expression, Y =	$\overline{B} \cdot D + B \cdot \overline{D} = B \oplus D$	
7	MUX connections, Boolean expression or Gate		
	Row CD = 00	$A \oplus B$	
	Row CD = 01	$A \cdot B$	
	Row CD = 10	$\overline{A \oplus B}$	
	Row CD = 11	$\overline{A} + B$	
8	Timing diagrams		
9	Flip-Flop #	#1	
10	Maximum circuit delay t_{pd} =	170 ps	
	Is the Hold time constraint ok?	[ ] Yes [X] No	
11	Number of states =	15	
	Final state $Q_3Q_2Q_1Q_0$ =	1 1 1 0	
12	Boolean expression Y =	$Y = Q_3 \cdot Q_1$	
	Input $D_3D_2D_1D_0$ =	0 1 0 1	
13	16 bit two's complement **hexadecimal** Product A x B	P 0x30CF	
14	8 bit two's complement **hexadecimal** Quotient (A / B) and Remainder	Q 0x02	R 0x1B
15	8 result bits (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0)	0 1 0 0 1 0 0 0	
16	Memory contents, 8 hexadecimal digits	B E A D 2 0 2 3	
TOTAL POINTS		Examiner sign	