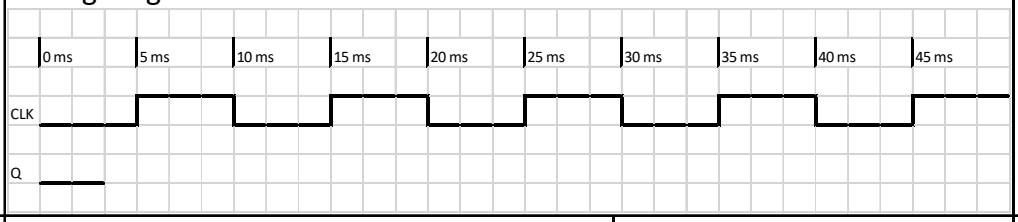
IE1204 Digital Design Answer Form 2025-2026

Anonymized Code		

#	Answer with	Answer	Points
1	**Decimal** number		
2	8 bit two's complement **hexadecimal** number	0x	
3	8 bit two's complement **hexadecimal** number	0x	
4	Boolean expression, Y =		
5	Circuit number		
6	Boolean expression, Y =		
7	MUX connections, Boolean expression or Gate		
	Row CD = 00		
	Row CD = 01		
	Row CD = 10		
	Row CD = 11		
8	Timing diagram		
9	Timing diagram		
10	Maximum clock frequency =	GHz	
	Is the Hold time constraint ok?	[ ] Yes [ ] No	
11	Number of states =		
	Final state $Q_3Q_2Q_1Q_0$ =		
12	Boolean expression Y =		
	Input $D_3D_2D_1D_0$ =		
13	16 bit two's complement **hexadecimal** Product A x B	P 0x	
14	8 bit two's complement **hexadecimal** Quotient (A / B) and Remainder	Q 0x R 0x	
15	8 result bits (Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0)		
16	Memory contents, 8 hexadecimal digits		
TOTAL POINTS		Examiner sign	