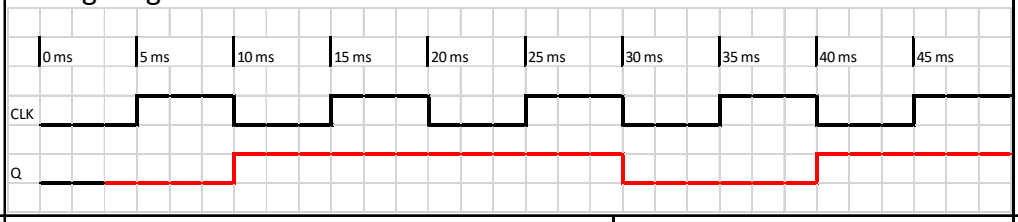
IE1204 Digital Design Answer Form 2025-2026

Anonymized Code		
JB-007		

#	Answer with	Answer	Points
1	**Decimal** number	36	
2	8 bit two's complement **hexadecimal** number	0x36	
3	8 bit two's complement **hexadecimal** number	0x36	
4	Boolean expression, Y =	$Y = A(\overline{B} + C)$	
5	Circuit number	#4	
6	Boolean expression, Y =	$Y = \overline{A} \cdot \overline{C} + B \cdot C \cdot \overline{D}$	
7	MUX connections, Boolean expression or Gate Row CD = 00	$\overline{A \oplus B}$	
	Row CD = 01	$\overline{A \cdot B}$	
	Row CD = 10	A	
	Row CD = 11	$A \cdot \overline{B}$	
8	Timing diagram		
9	Timing diagram	#1	
10	Maximum clock frequency = Is the Hold time constraint ok?	2.5 GHz [X] Yes [ ] No	
11	Number of states = Final state $Q_3Q_2Q_1Q_0$ =	10 1 1 0 0	
12	Boolean expression Y = Input $D_3D_2D_1D_0$ =	$Y = Q_3 \cdot Q_1$ 0 1 0 0	
13	16 bit two's complement **hexadecimal** Product A x B	P 0x34BC	
14	8 bit two's complement **hexadecimal** Quotient (A / B) and Remainder	Q 0x03 R 0x01	
15	8 result bits (Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0)	1 1 1 1 0 0 0 0	
16	Memory contents, 8 hexadecimal digits	B A B A 1 3 3 7	
TOTAL POINTS		Examiner sign	