Skriftlig Tentamen
IE1204 Digital Design
2025-2026 Med Lösningar

Examiner/Examinator: Carl-Mikael Zetterling
Responsible teacher/Ansvarig lärare: Carl-Mikael Zetterling, 08-790 4344

Swedish/Svenska:
Tentamenstexten ska lämnas in när lösningarna lämnas in.
Inga tillåtna hjälpmedel utom linjal.
Examen består av två delar:
Del 1 har 16 uppgifter med max 1 poäng per uppgift som ska besvaras på ”Answer Form”.
Del 2 har 4 uppgifter med max 3 till 5 poäng per uppgift som ska besvaras på separat papper.
Lämna in båda delar samtidigt. Disponera tiden själv mellan delarna.
Uppgifterna är inte ordnade efter svårighetsgrad.
Om slutsumman av tentan har halvpoäng avrundas det uppåt.

Totalt max 32 poäng på tentamen.
För godkänt krävs
(minst 8 poäng på del 1) OCH (minst 16 poäng totalt)
Fx om något villkor ej är uppfyllt med en poängs marginal.

Det betyder att
För E krävs minst 16 poäng totalt och minst 8 på del 1.
För Fx krävs 16 poäng totalt och minst 7 på del 1
eller 15 poäng totalt och minst 8 på del 1.

Betygskalan för tentamen förutsatt att studenten har minst 8 poäng från del 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

Resultat meddelas inom tre veckor.

Written Exam
IE1204 Digital Design
2025-2026 With Solutions

Examiner/Examinator: Carl-Mikael Zetterling
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English:
The exam text should be handed in after the exam.
No aids allowed except ruler.
The exam consists of two parts:
Part 1 has 16 exercises for max 1 point per exercise to be answered on the "Answer Form".
Part 2 has 4 exercises for max 3 to 5 points per exercise, to be answered on a separate paper.
Hand in both parts at the same time. Plan the time yourself between the parts.
The exercises are not in order of difficulty.
If the total sum of the exam has half points this will be rounded up.

Total max of 32 points on the exam.
To pass the exam requires
(at least 8 points from part 1) AND (at least 16 points in total)
Fx if any condition is not fulfilled by one point's margin.

This means
For E, a minimum of 16 points in total and at least 8 in part 1 is required.
For Fx, 16 points are required in total and at least 7 on part 1
or 15 points in total and at least 8 in part 1.

Grades are given as follows provided the student has at least 8 points from part 1.

0-15	16-18	19-21	22-24	25-27	28-31	32
F	E	D	C	B	A	A+

The result will be announced within three weeks.

Del 1/Part 1, 1 point per exercise, fill in on "Answer Form"

1 Number Conversion

Swedish: Konvertera de positiva talen och utför beräkningen.
Svara med ett decimalt tal.

English: Convert the unsigned numbers and perform the calculation.
Answer with a decimal number.

$Y = 1000110_2 - 25_8 + 10_{10} - 17_{16}$
$= 70 - 21 + 10 - 23 = 36$

2 Addition

Swedish: A och B är hexadecimala 8 bitars två-komplement kodade tal.
Beräkna A + B och svara med ett 8 bitars två-komplement hexadecimalt kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are hexadecimal 8-bit binary (two's complement) numbers.
Calculate A + B and answer with an 8-bit binary (two's complement) hexadecimal number.
You can check your calculations using decimal numbers.

$A = 0x11 = 11_{16}$ 00010001
$B = 0x25 = 25_{16}$ + 00100101
A + B = 00110110 = 0x36

or calculate directly from 0x11 + 0x25

3 Subtraction

Swedish: A och B är hexadecimala 8 bitars två-komplement kodade tal.
Beräkna A - B och svara med ett 8 bitars två-komplement hexadecimalt kodat tal.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are hexadecimal 8-bit binary (two's complement) numbers.
Calculate A - B and answer with an 8-bit binary (two's complement) hexadecimal number.
You can check your calculations using decimal numbers.

$A = 0xA9 = A9_{16}$ 10101001
$B = 0x73 = 73_{16}$ = 01110011
- B = + 10001100
A – B = 00110101 = 0x36

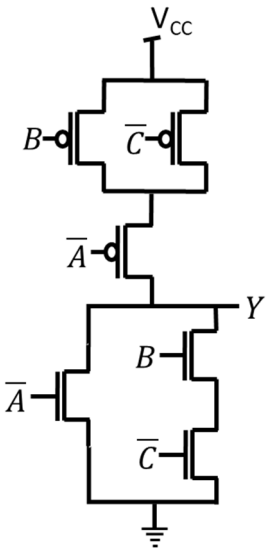
or calculate directly from 0xA9 – 0x73

There is an overflow in this calculation but but 0x36 would be accepted as the correct 8-bit result of the addition. No question was made about overflow in this exercise.

4 Analysis of CMOS circuits

Swedish: Ta fram enklast möjliga booleska uttryck för CMOS-kretsen.

English: Derive the simplest possible Boolean expression for the CMOS circuit.

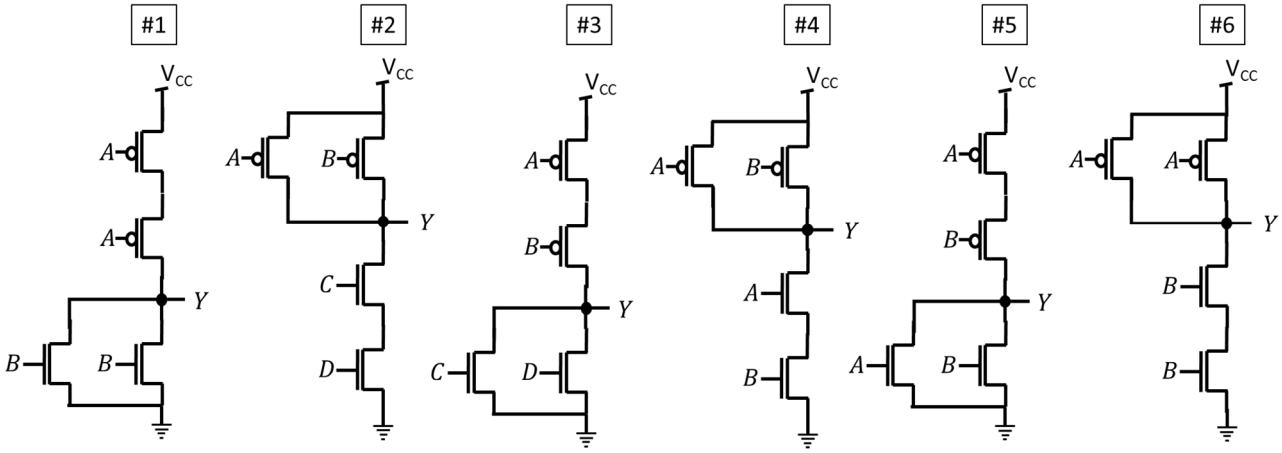


$$Y = A(\overline{B} + C)$$

5 Memory circuits

Swedish: Vilken av kretsarna är en CMOS NAND?

English: Which circuit is a CMOS NAND?



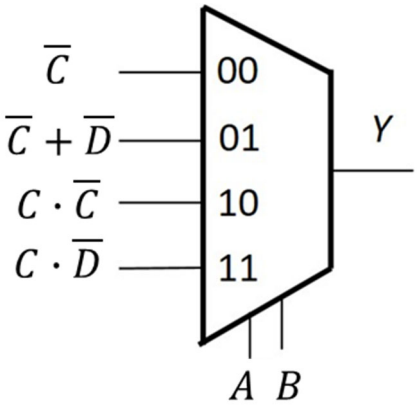
#4

6 Analysis: MUX to K-map

Swedish: Fyll i K-Map från MUX-kopplingen.
Ta fram enklast möjliga booleska uttryck för Y från K-map. Välj PoS eller SoP.

English: Fill in the K-Map from the MUX circuit.
Derive simplest possible Boolean expression from the K-map. Select PoS or SoP.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	1	0	0
AB 01	1	1	0	1
AB 11	0	0	0	1
AB 10	0	0	0	0



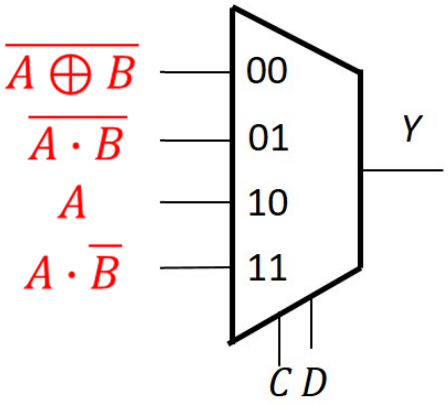
$$Y = \overline{A} \cdot \overline{C} + B \cdot C \cdot \overline{D}$$

7 Design: K-Map to MUX

Swedish: Använd en 4:1 MUX och valfria grindar eller 0 och 1 och gör en krets för K-map med CD som select-signaler.

English: Use a 4:1 MUX and any logic gates or 0 or 1 to draw a circuit for the K-map with CD as select signals.

Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	1	0	0
AB 01	0	1	0	0
AB 11	1	0	0	1
AB 10	0	1	1	1

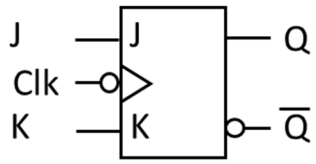


0.5 point deducted if third and fourth expressions are interchanged.

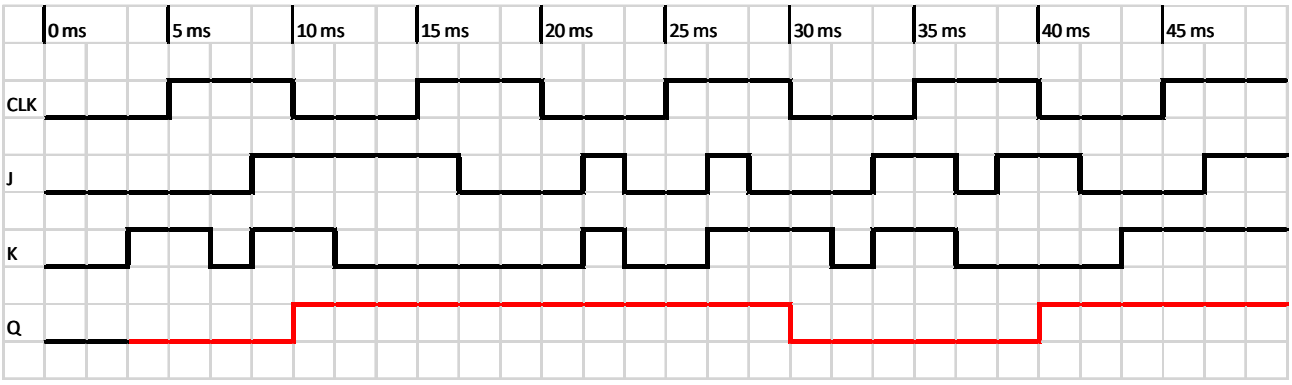
8 Timing diagram (Analysis)

Swedish: Rita tidsdiagram för kretsen i ”Answer Form”.

English: Draw the timing diagram for the circuit in the “Answer Form”.



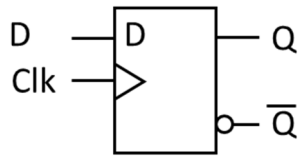
NOTE: negative edge

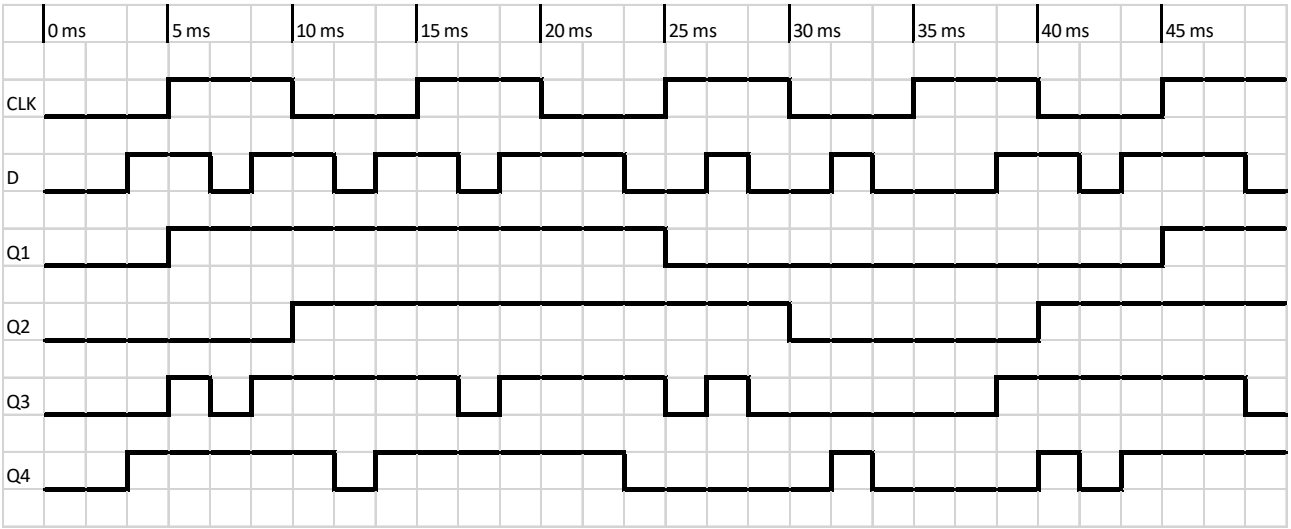


9 Timing diagram (Design)

Swedish: Vilket tidsdiagram Q1 – Q4 nedan stämmer?

English: Which timing diagram Q1 – Q4 below is correct?





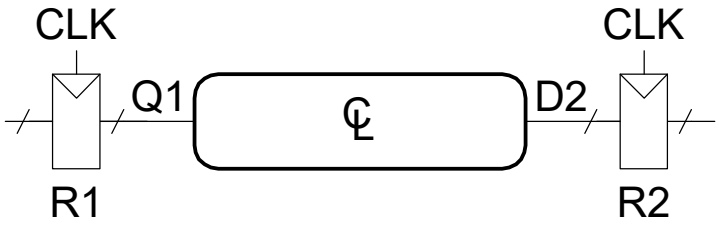
Answer: Q1

10 Timing calculation

Swedish: Beräkna maximal klockfrekvens för kretsen. Är Hold-villkoret uppfyllt?

English: Calculate the maximum clock frequency for the circuit. Is the Hold time constraint ok?

t_{pcq} = 50 ps
t_{ccq} = 20 ps
t_{setup} = 50 ps
t_{hold} = 25 ps
t_{pd} = 300 ps
t_{cd} = 20 ps

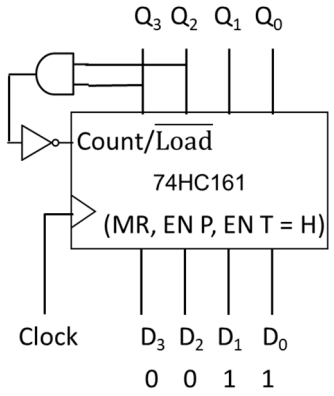


Tc = 50 + 50 + 300 = 400 ps fc = 1 / Tc = 2.5 GHz 25 - 20 - 20 = -15 ps, OK

11 Counter analysis

Swedish: Räknaren nedan har laddat in tillståndet $Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$.
Hur många klockpulser innan den upprepar sig? Vad är sista tillståndet?

English: The counter below has loaded state $Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$.
How many clock pulses until it repeats? What is the end state?

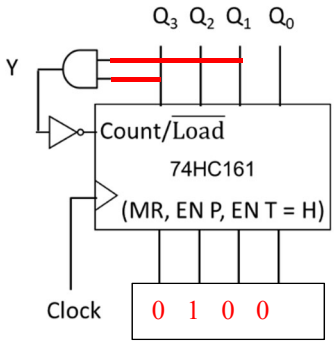


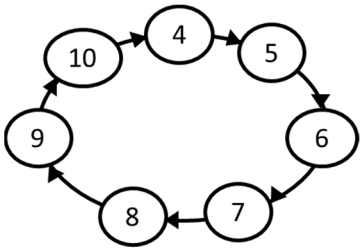
N = 10 Sequence: 0011 – 1100, Last state is 1100
The last state will cause a load operation on the next clk.
Count the number of states including the loaded state:
Last – Loaded (first) + 1

12 Counter design

Swedish: Hur ska AND-grinden och D_3 – D_0 kopplas för att få en räknare med tillståndsdiagrammet nedan?

English: How should the AND-gate and D_3 – D_0 be connected to get a counter with the state diagram below?





The AND gate should detect the last state, $Y = Q_3 \cdot Q_1$
$D_3D_2D_1D_0$ should be connected to load the first state 0100

13 Multiplication

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A x B (binärt) och svara med ett 16 bitars två-komplement **hexadecimalt kodat tal**.
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A x B (binary) and answer with a 16-bit binary (two's complement) **hexadecimal number**.
You can check your calculations using decimal numbers.

$A = 01101100_2$
$B = 01111101_2$

A x B = B x A (both are positive) put B above since it has more '1's

```
        01111101
      x 01101100
        01111101   1st multiplication
   +  01111101     2nd multiplication
      10111011100
 +    01111101     3rd multiplication
     1010101111100
+    01111101     4th multiplication
0011010010111100 = 34BC16
```

14 Division

Swedish: A och B är 8 bitars två-komplement kodade tal.
Beräkna A / B (binärt) och svara med kvot och rest
(8 bitars två-komplement **hexadecimalt kodade tal**).
Tänk på att du kan kontrollera dina beräkningar med decimala tal.

English: A and B are 8-bit binary (two's complement) numbers.
Calculate A / B (binary) and answer with quotient and remainder
(8-bit binary two's complement **hexadecimal numbers**).
You can check your calculations using decimal numbers.

$A = 01111111_2$
$B = 00101010_2$

A and B are both positive

```
          11  Quotient = 3
101010/01111111
      - 101010
        101011
      -  101010
            1  Remainder = 1
```

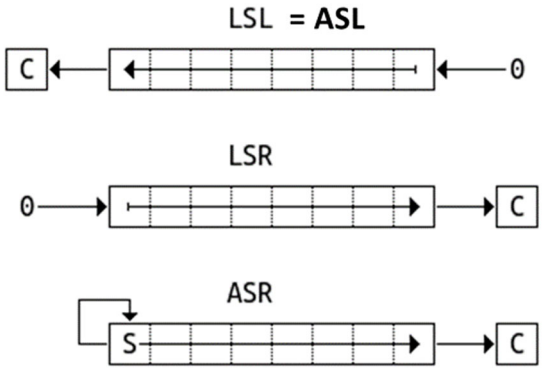
15 Shift Registers

Swedish: Ett skiftregister har laddats med 8 bitar med värdet D.
Vad blir resultatet efter de uppräknade operationerna?
Svara med 8 bitar (Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0).

English: A shift register has been preloaded with 8 bita of data D.
What is the result after the listed operations?
Answer with 8 bits (Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0).

D = 11110001 Q = 11110000

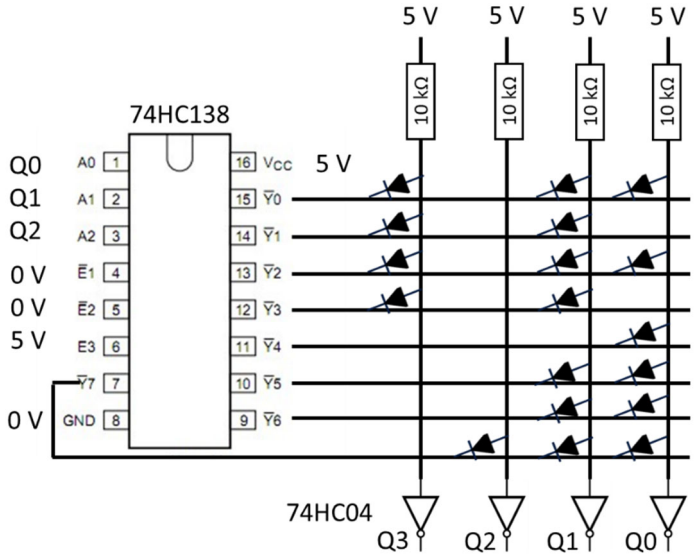
Operations: LSR 1, ASL 1, LSL 1, ASR 1 (earlier version had the "1" implied)



16 Memory circuit from Lab 4

Swedish: Detta diod-ROM har åtta 4 bitars tal lagrade, vilka är talen?
Svara med 8 **hexadecimala siffror**, från adress 000 till 111.

English: This diode ROM has eight 4-bit numbers stored, what are the numbers?
Answer with 8 **hexadecimal digits**, from address 000 to 111.



The hexadecimal number is B A B A 1 3 3 7

Del 2/Part 2, 4 points per exercise, answer on separate paper

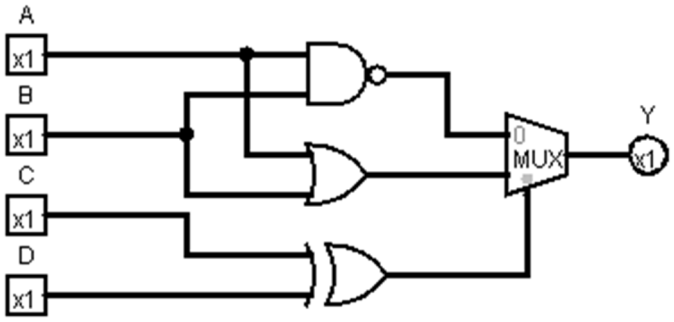
17 Analysis of Combinational Circuit (4 p)

Swedish:

1. Ta fram booleskt uttryck för kretsen nedan.
2. Rita K-map för kretsen med variabelordning som i figuren.
3. Förenkla uttrycket med hjälp av K-map.
4. Rita ny krets med valfria grindar (men inte MUX).

English:

1. Derive the Boolean expression for the circuit below.
2. Draw a K-map for the circuit with variables as in the figure.
3. Simplify the expression using the K-map.
4. Draw a new circuit using any gates (but not MUX).



Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	1	0
AB 01	1	1	1	1
AB 11	0	1	0	1
AB 10	1	1	1	1

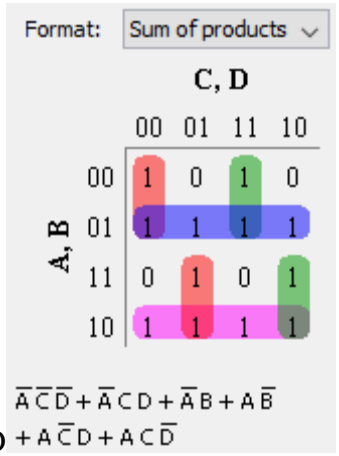
Rita av K-map i dina inlämnade svar.

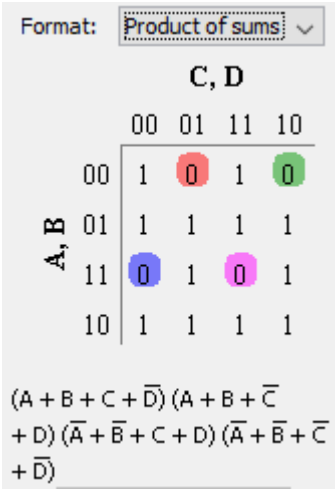
Redraw the K-map in your answer sheets.

Boolean expression and truth table

$$Y = \overline{S} \cdot \overline{A \cdot B} + S \cdot (A + B) = \{S = C \oplus D\} = \overline{C \oplus D} \cdot \overline{A \cdot B} + (C \oplus D) \cdot (A + B)$$

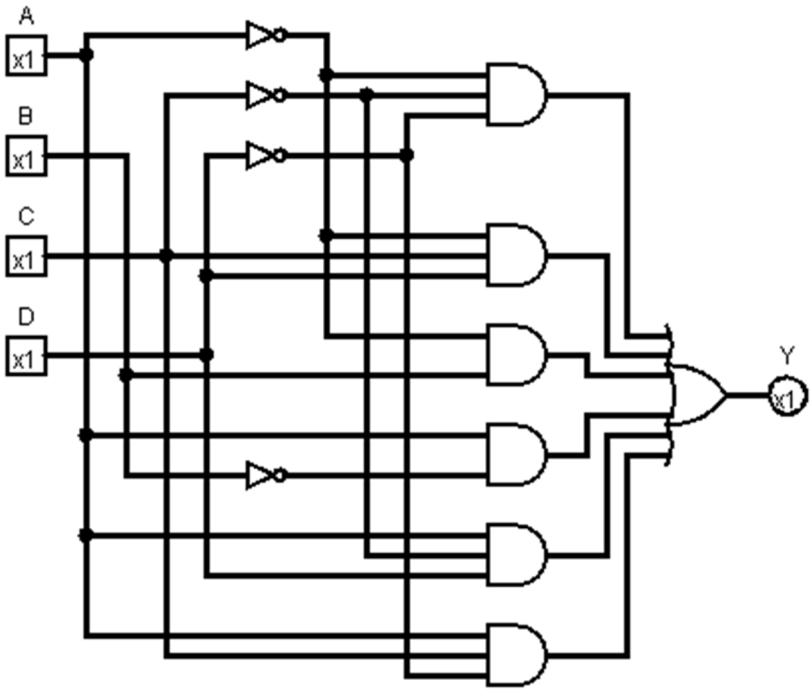
K-Map and simplified expressions





A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Circuit can be built from SOP:



Interestingly, Logisim does not generate the simplest Boolean expression from the K-Map!

One of the two row min-terms can be removed if the other groups are adjusted, so for instance

$$Y = \overline{A} \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot C \cdot D + B \cdot \overline{C} \cdot D + B \cdot C \cdot \overline{D} + A \cdot \overline{B}$$

is simpler and requires one less two-input AND gate.

18 Design of Combinational Circuit (4 p)

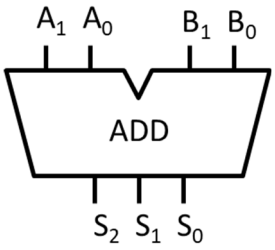
Swedish:
En tvåbitars heladderare utan carry in kan konstrueras från sanningstabell och K-maps.

1. Rita hela sanningstabellen med hjälp av den som är påbörjad nedan.
2. Rita K-maps för sanningstabellen med variabelordning som i figuren.
3. Ta fram enklast möjliga booleska uttryck.
4. Rita kretsar för uttrycken med valfria grindar eller MUX.

English:
A two bit full adder without carry in can be designed from truth table and K-maps.

1. Draw a complete truth table with help from the one that has been started below.
2. Draw K-maps for the truth table with variables as in the figure.
3. Derive the simplest possible Boolean expression.
4. Draw the circuit for the expression using any gates or MUX.

A1	A0	B1	B0	S2	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
I	I	I	I	I	I	I
1	1	1	1	1	1	0



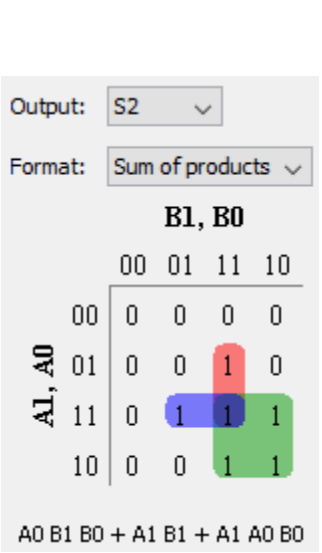
A1	A0	B1	B0	S2	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

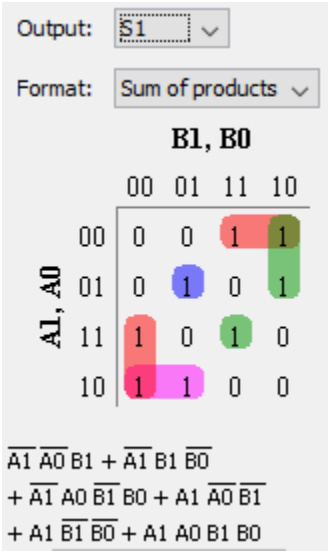
Sx	B 00	B 01	B 11	B 10
A 00				
A 01				
A 11				
A 10				

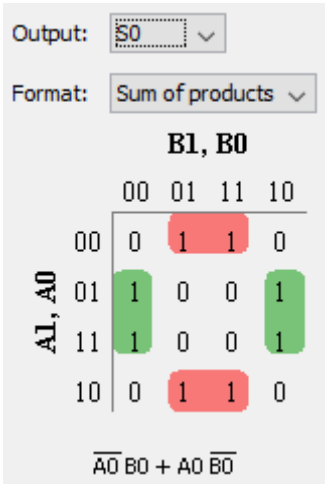
Rita av K-map i dina inlämnade svar.

Redraw the K-map in your answer sheets.

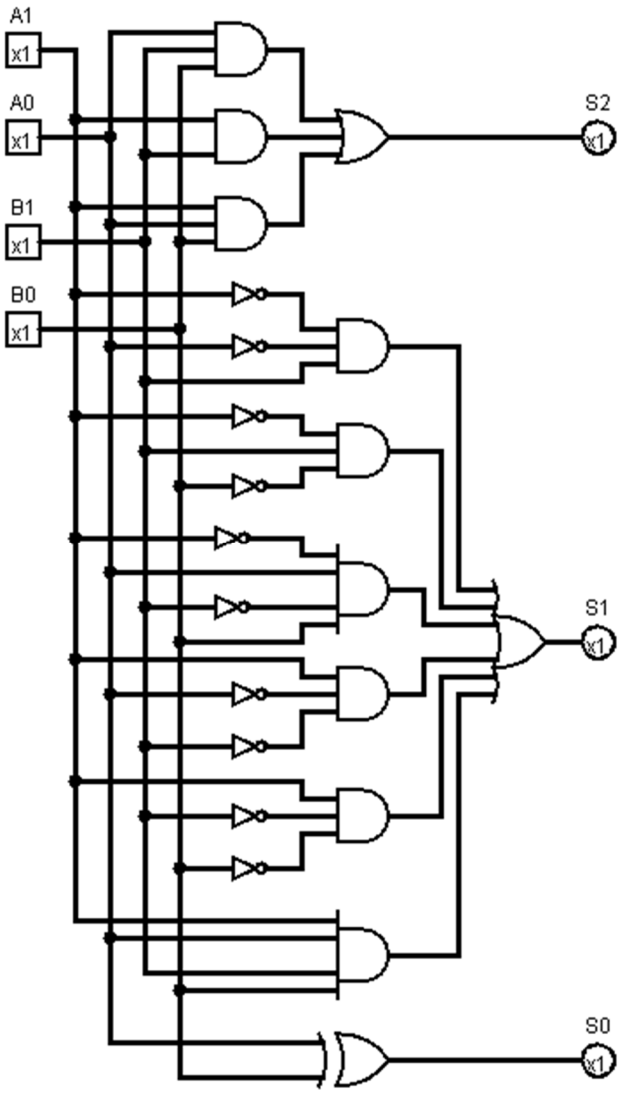
K-Maps and simplified expressions

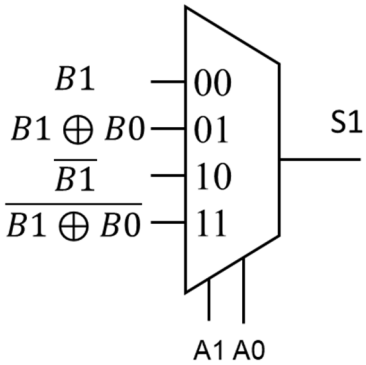






Circuit solution can be simplified if XOR is used for S0, and a MUX can be used for S1:





19 Analysis of FSM (3 p)

Swedish: Analysera vad tillståndsmaskinen (FSM) utför.

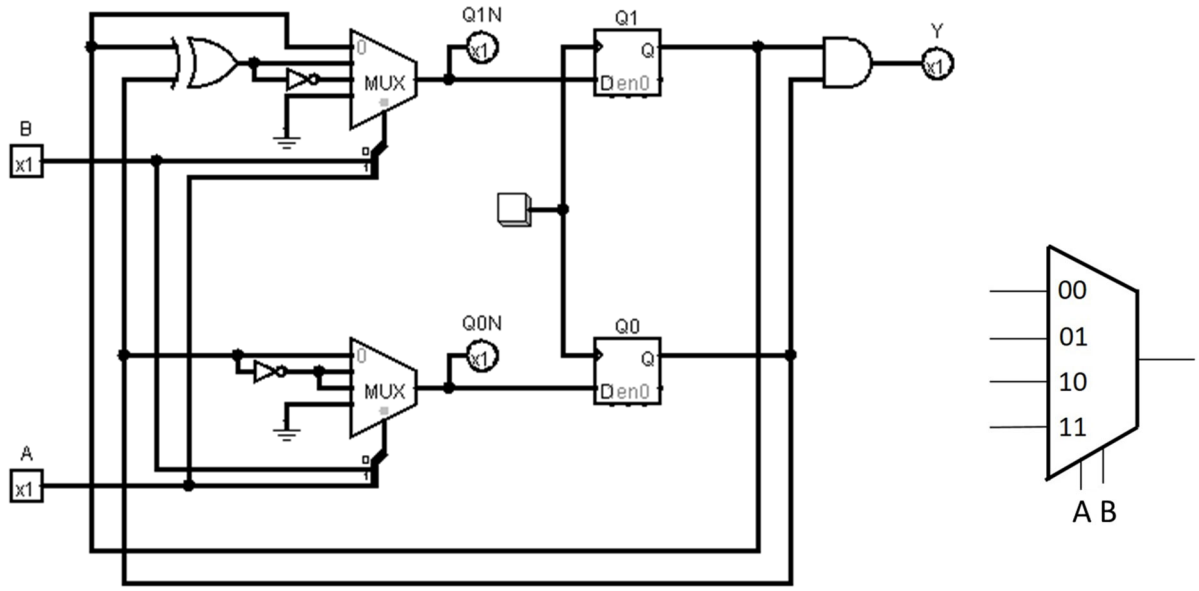
1. Rita K-Maps för Q1N och Q0N.
2. Rita tillståndstabell.
3. Rita tillståndsdiagram.

Använd ordningen Q1 Q0 A B

English: Analyze the state machine (FSM).

1. Draw K-Maps for Q1N and Q0N.
2. Draw a state table.
3. Draw a state diagram.

Use the order Q1 Q0 A B



Q1N	AB=			
Q1Q0	00	01	11	10
00				
01				
11				
10				

Q0N	AB=			
Q1=	00	01	11	10
00				
01				
11				
10				

Rita av K-map och state tabell i dina inlämnade svar.

Redraw the K-map and state table in your answer sheets.

		Next state								
Present state		AB = 00		AB = 01		AB = 11		AB = 10		Output
Q1	Q0	Q1N	Q0N	Q1N	Q0N	Q1N	Q0N	Q1N	Q0N	Y
0	0									
0	1									
1	1									
1	0									

K-Maps

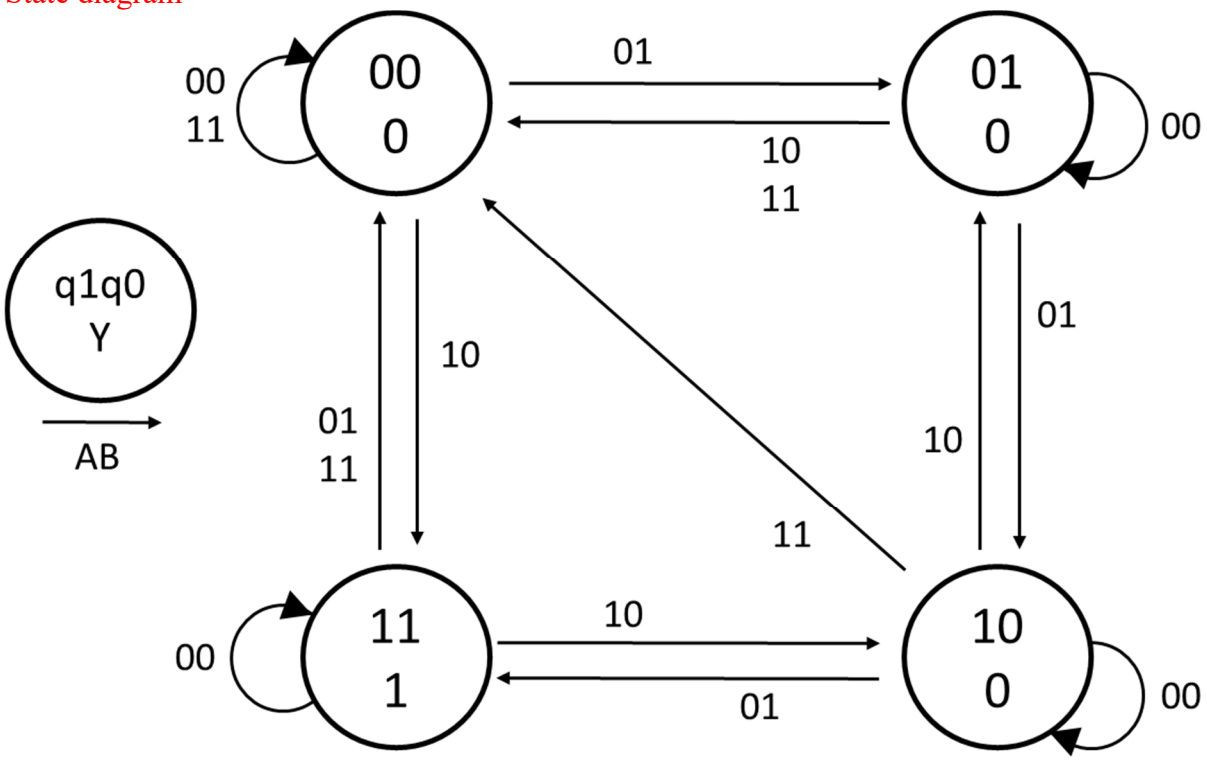
Q1N	AB=			
Q1Q0	00	01	11	10
00	0	0	0	1
01	0	1	0	0
11	1	0	0	1
10	1	1	0	0

Q0N	AB=			
Q1Q0	00	01	11	10
00	0	1	0	1
01	1	0	0	0
11	1	0	0	0
10	0	1	0	1

State Table

		Next state								
Present state		AB = 00		AB = 01		AB = 11		AB = 10		Output
Q1	Q0	Q1N	Q0N	Q1N	Q0N	Q1N	Q0N	Q1N	Q0N	Y
0	0	0	0	0	1	0	0	1	1	0
0	1	0	1	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	1	0	1
1	0	1	0	1	1	0	0	0	1	0

State diagram



Function (not required)

AB	Function
00	Idle
01	Forward
10	Reverse
11	Reset

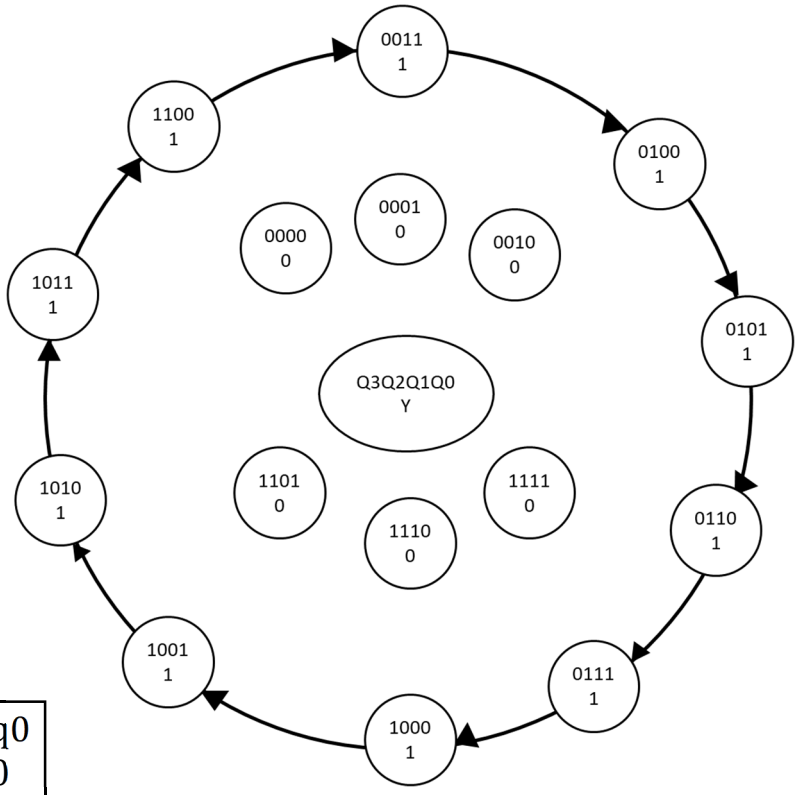
20 Design of FSM (5 p)

Swedish: Konstruera en tillståndsmaskin (FSM) enligt tillståndsdiagrammet nedan.

1. Rita tillståndstabell. Sätt don't care för de sex oanvända tillstånden.
2. Ta fram K-map för nästa tillstånd.
3. Ta fram minimerade uttryck för nästa tillstånd. Använd don't cares.
4. Rita kretsschema för en FSM med DFFs och MUX eller vilka grindar som helst.
5. Fyll i don't cares i tillståndstabellen och rita det kompletta tillståndsdiagrammet.

English: Design a state machine (FSM) according to the state diagram below.

1. Draw a state table. Put don't care for the six unused states.
2. Derive K-maps for next state.
3. Derive minimized expressions for next state. Use don't cares.
4. Draw the FSM circuit diagram with DFFs and MUX or any gates.
5. Fill in the don't cares in the state table and draw the complete state diagram.



	q1q0 00	q1q0 01	q1q0 11	q1q0 10
q3q2 00				
q3q2 01				
q3q2 11				
q3q2 10				

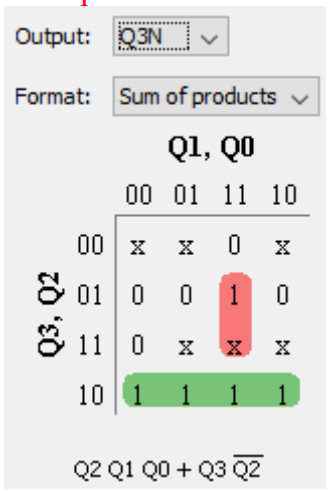
Rita av K-map i dina inlämnade svar.

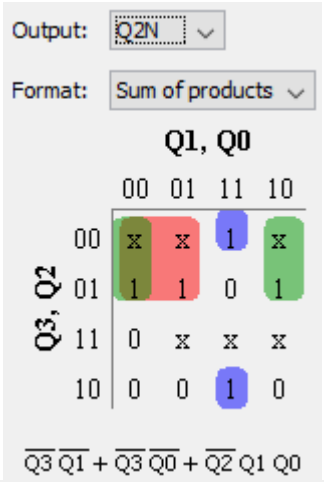
Redraw the K-map in your answer sheets.

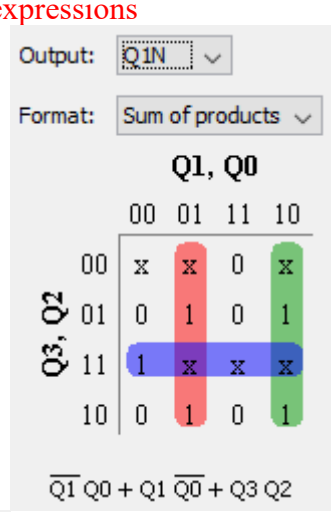
State table (fixed in v3)

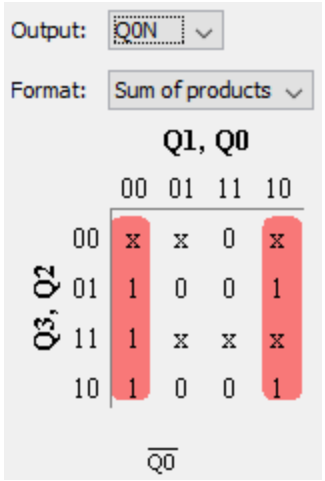
Present state				Next state				Output
Q3	Q2	Q1	Q0	Q3+	Q2+	Q1+	Q0+	Y
0	0	0	0	x	x	x	x	0
0	0	0	1	x	x	x	x	0
0	0	1	0	x	x	x	x	0
0	0	1	1	0	1	0	0	1
0	1	0	0	0	1	0	1	1
0	1	0	1	0	1	1	0	1
0	1	1	0	0	1	1	1	1
0	1	1	1	1	0	0	0	1
1	0	0	0	1	0	0	1	1
1	0	0	1	1	0	1	0	1
1	0	1	0	1	0	1	1	1
1	0	1	1	1	1	0	0	1
1	1	0	0	0	0	1	1	1
1	1	0	1	x	x	x	x	0
1	1	1	0	x	x	x	x	0
1	1	1	1	x	x	x	x	0

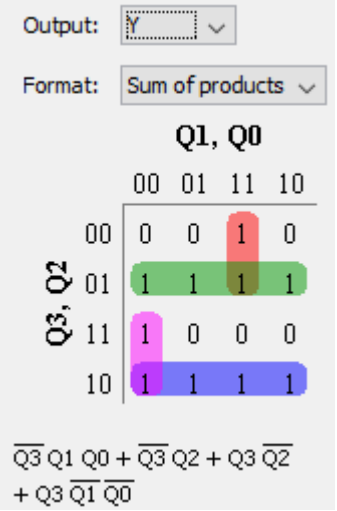
K-Maps for next state and output with minimized expressions



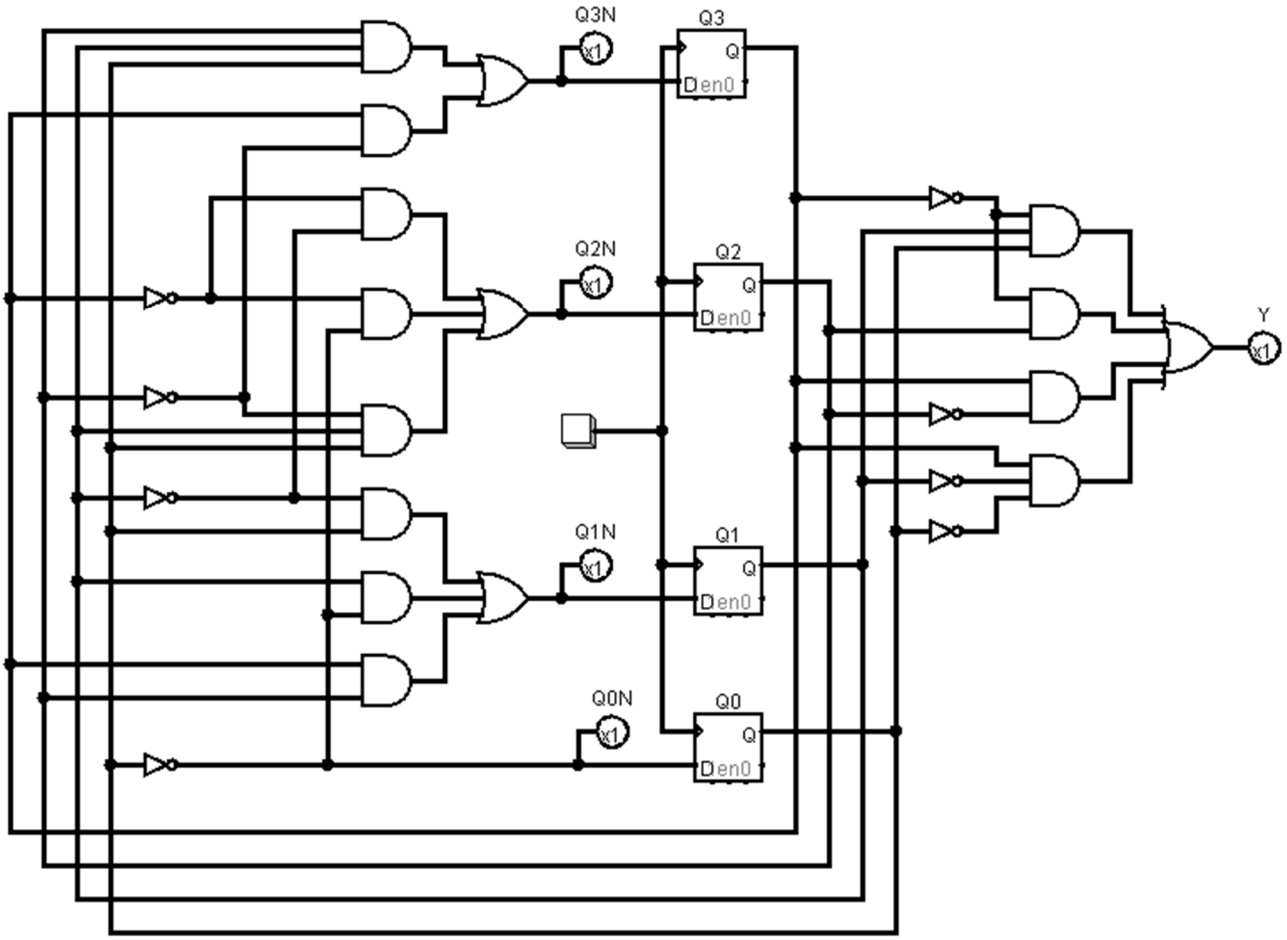








FSM circuit diagram



Final state table and state diagram, a counter for 0011 – 1100. Similar to Exercise 11.

Present state				Next state				Output
Q3	Q2	Q1	Q0	Q3+	Q2+	Q1+	Q0+	Y
0	0	0	0	0	1	0	1	0
0	0	0	1	0	1	1	0	0
0	0	1	0	0	1	1	1	0
0	0	1	1	0	1	0	0	1
0	1	0	0	0	1	0	1	1
0	1	0	1	0	1	1	0	1
0	1	1	0	0	1	1	1	1
0	1	1	1	1	0	0	0	1
1	0	0	0	1	0	0	1	1
1	0	0	1	1	0	1	0	1
1	0	1	0	1	0	1	1	1
1	0	1	1	1	1	0	0	1
1	1	0	0	0	0	1	1	1
1	1	0	1	0	0	1	0	0
1	1	1	0	0	0	1	1	0
1	1	1	1	1	0	1	0	0