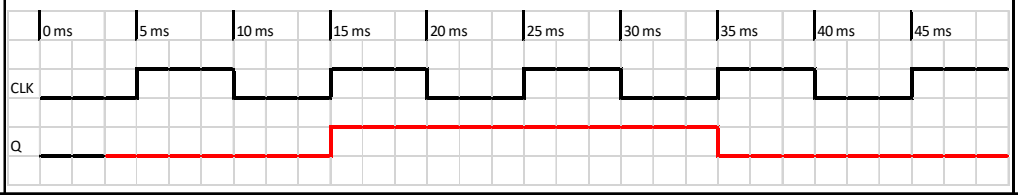
IE1204 Digital Design Answer Form 2025-10-23

Anonymized Code			

#	Answer with	Answer	Points
1	**Decimal** number	30	
2	8 bit two's complement **hexadecimal** number	0x40	
3	8 bit two's complement **hexadecimal** number	0xC0	
4	Boolean expression, Y =	$Y = \overline{B}(A + C)$	
5	Circuit number	#3	
6	Boolean expression, Y =	$Y = \overline{B} \cdot \overline{C} + \overline{A} \cdot C \cdot \overline{D}$	
7	MUX connections, Boolean expression or Gate		
	Row CD = 00	$A \oplus B$	
	Row CD = 01	$\overline{A}$	
	Row CD = 10	$A \cdot \overline{B}$	
	Row CD = 11	$\overline{A \cdot B}$	
8	Timing diagram		
9	Timing diagram	#3	
10	Maximum clock frequency =	3.3 GHz	
	Is the Hold time constraint ok?	[X] Yes [ ] No	
11	Number of states =	8	
	Final state $Q_3Q_2Q_1Q_0$ =	1 1 0 0	
12	Boolean expression Y =	Y= $Q_3 \cdot Q_0$	
	Input $D_3D_2D_1D_0$ =	0 0 1 1	
13	16 bit two's complement **hexadecimal** Product A x B	P 0x35EC	
14	8 bit two's complement **hexadecimal** Quotient (A / B) and Remainder	Q 0x09 R 0x0A	
15	8 result bits (Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0)	0 0 0 0 0 0 1 1	
16	Memory contents, 8 hexadecimal digits	D E 1 3 3 7 D E	
TOTAL POINTS		Examiner sign	