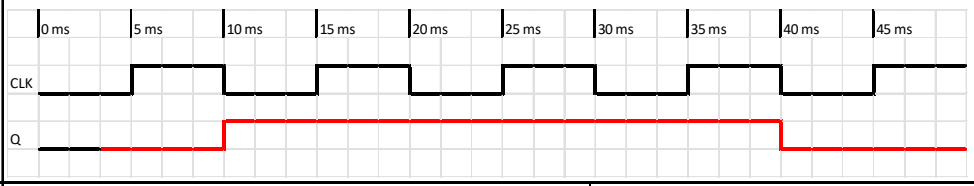
IE1204 Digital Design Answer Form 2026-01-12

Anonymized Code			

#	Answer with	Answer	Points
1	**Decimal** number	49	
2	8 bit two's complement **hexadecimal** number	0x50	
3	8 bit two's complement **hexadecimal** number	0xC1	
4	Boolean expression, Y =	$Y = C(\overline{A} + B)$	
5	Circuit number	#5	
6	Boolean expression, Y =	$Y = \overline{C} \cdot D + A \cdot \overline{B} \cdot C$	
7	MUX connections, Boolean expression or Gate Row CD = 00	$\overline{A} + B$	
	Row CD = 01	A	
	Row CD = 10	$\overline{A + B}$	
	Row CD = 11	$\overline{A \oplus B}$	
8	Timing diagram		
9	Timing diagram	#4	
10	Maximum clock frequency = Is the Hold time constraint ok?	4 GHz [X] Yes [ ] No	
11	Number of states = Final state $Q_3Q_2Q_1Q_0$ =	12 1 1 0 0	
12	Boolean expression Y = Input $D_3D_2D_1D_0$ =	$Y = Q_3 \cdot Q_2$ 0 1 1 0	
13	16 bit two's complement **hexadecimal** Product A x B	P 0x39A8	
14	8 bit two's complement **hexadecimal** Quotient (A / B) and Remainder	Q 0x04 R 0x13	
15	8 result bits (Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0)	0 1 1 0 1 0 1 0	
16	Memory contents, 8 hexadecimal digits	1 9 A C D C 6 7	
TOTAL POINTS		Examiner sign	