

IE1204 Digital Design Answer Form 2026-04-10

Anonymized Code			
#	Answer with	Answer	Points
1	Decimal number	78	
2	8 bit two's complement hexadecimal number	0x78	
3	8 bit two's complement hexadecimal number	0xE8	
4	Boolean expression, Y =	$A(B + C)$	
5	Circuit number	#2	
6	Boolean expression, Y =	$\overline{B} \cdot D + B \cdot \overline{D} = B \oplus D$	
7	MUX connections, Boolean expression or Gate	$A \oplus B$	
	Row CD = 00	$A \cdot B$	
	Row CD = 01	B	
	Row CD = 10	$\overline{A} + B$	
8	Timing diagram		
9	Timing diagram	#2	
10	Maximum clock frequency =	5 GHz	
	Is the Hold time constraint ok?	☒ Yes ☐ No	
11	Number of states =	14	
	Final state $Q_3Q_2Q_1Q_0 =$	1 1 1 0	
12	Boolean expression Y =	$Y = Q_2 \cdot Q_1$	
	Input $D_3D_2D_1D_0 =$	0 0 0 0	
13	16 bit two's complement hexadecimal Product A x B	P 0x381C	
14	8 bit two's complement hexadecimal Quotient (A / B) and Remainder	Q 0x01 R 0x3A	
15	8 result bits ($Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0$)	0 0 0 1 1 1 0 0	
16	Memory contents, 8 hexadecimal digits	1 3 3 7 F E E D	
TOTAL POINTS		Examiner sign	