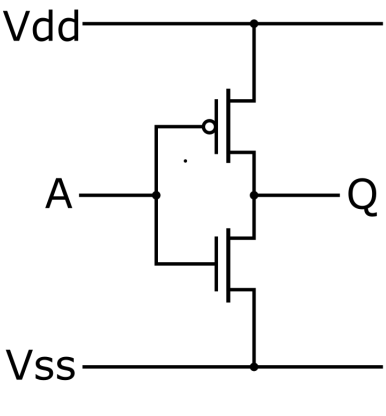
CMOS

Complementary metal-oxide-semiconductor (**CMOS**) (pronounced /ˈsiːmɒs/) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1967 (US patent 3,356,858).



CMOS inverter (NOT logic gate)

CMOS is also sometimes referred to as **complementary-symmetry metal-oxide-semiconductor** (or COS-MOS[1]). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. CMOS also allows a high density of logic functions on a chip. It was primarily this reason why CMOS won the race in the eighties and became the most used technology to be implemented in VLSI chips.

The phrase "metal-oxide-semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.[2]

Technical details

"CMOS" refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes.[3] As of 2010, the CPUs with the best performance per watt each year have been CMOS static logic since 1976.

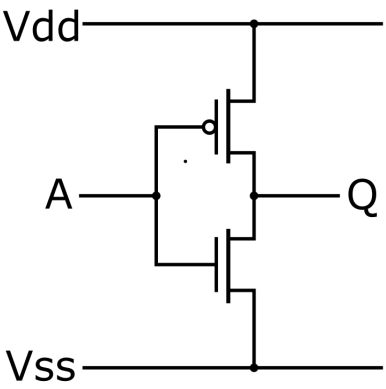
CMOS circuits use a combination of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits found in computers, telecommunications equipment, and signal processing equipment. Although CMOS logic can be implemented with discrete devices (for instance, in an introductory circuits class), typical commercial CMOS products are integrated circuits composed of millions (or hundreds of millions) of transistors of both types on a rectangular piece of silicon of between 10 to 400mm^2. These devices are commonly called "chips", although within the industry they are also referred to as "die" (singular) or "dice", "dies", or "die" (plural).

Composition

The main principle behind CMOS circuits that allows them to implement logic gates is the use of p-type and n-type metal-oxide-semiconductor field-effect transistors to create paths to the output from either the voltage source or ground. When a path to output is created from the voltage source, the circuit is said to be pulled up. The other circuit state occurs when a path to output is created from ground and the output pulled down to the ground potential.

Inversion

CMOS circuits are constructed so that all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied.



Static CMOS Inverter

The image on the right shows what happens when an input is connected to both a PMOS transistor (top of diagram) and an NMOS transistor (bottom of diagram). When the voltage of input A is low, the NMOS transistor's channel is in a high resistance state. This limits the current that can flow from Q to ground. The PMOS transistor's channel is in a low resistance state and much more current can flow from the supply to the output. Because the resistance between the supply voltage and Q is low, the voltage drop between the supply voltage and Q due to a current drawn from Q is small. The output therefore registers a high voltage.

On the other hand, when the voltage of input A is high, the PMOS transistor is in an off (high resistance) state so it would limit the current flowing from the positive supply to the output, while the NMOS transistor is in an on (low resistance) state, allowing the output to drain to ground. Because the resistance between Q and ground is low, the voltage drop due to a current drawn into Q placing Q above ground is small. This low drop results in the output registering a low voltage.

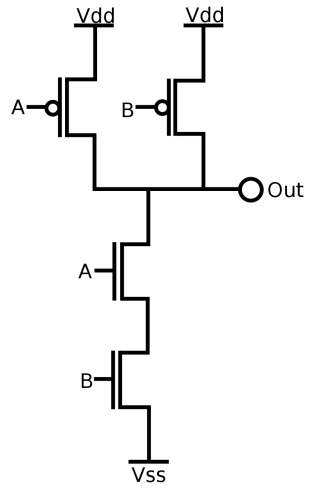
In short, the outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this opposite behavior of input and output, the CMOS circuits' output is the inversion of the input.

Duality

An important characteristic of a CMOS circuit is the duality that exists between its PMOS transistors and NMOS transistors. A CMOS circuit is created to allow a path always to exist from the output to either the power source or ground. To accomplish this, the set of all paths to the voltage source must be the complement of the set of all paths to ground. This can be easily accomplished by defining one in terms of the NOT of the other. Due to the De Morgan's laws based logic, the PMOS transistors in parallel have corresponding NMOS transistors in series while the PMOS transistors in series have corresponding NMOS transistors in parallel.

Logic

More complex logic functions such as those involving AND and OR gates require manipulating the paths between gates to represent the logic. When a path consists of two transistors in series, then both transistors must have low resistance to the corresponding supply voltage, modeling an AND. When a path consists of two transistors in parallel, then either one or both of the transistors must have low resistance to connect the supply voltage to the output, modeling an OR.



NAND gate in CMOS logic

Shown on the right is a circuit diagram of a NAND gate in CMOS logic. If both of the A and B inputs are high, then both the NMOS transistors (bottom half of the diagram) will conduct, neither of the PMOS transistors (top half) will conduct, and a conductive path will be established between the output and V_{ss} (ground), bringing the output low. If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and V_{dd} (voltage source), bringing the output high.

An advantage of CMOS over NMOS is that *both* low-to-high and high-to-low output transitions are fast since the pull-up transistors have low resistance when switched on, unlike the load resistors in NMOS logic. In addition, the output signal swings the full voltage between the low and high rails. This strong, more nearly symmetric response also makes CMOS more resistant to noise.

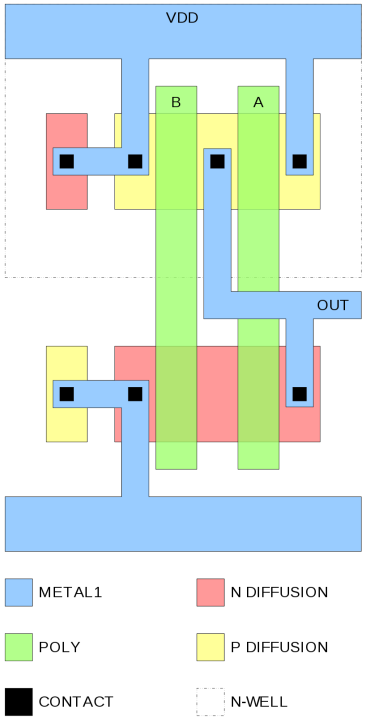
See Logical effort for a method of calculating delay in a CMOS circuit.

Example: NAND gate in physical layout

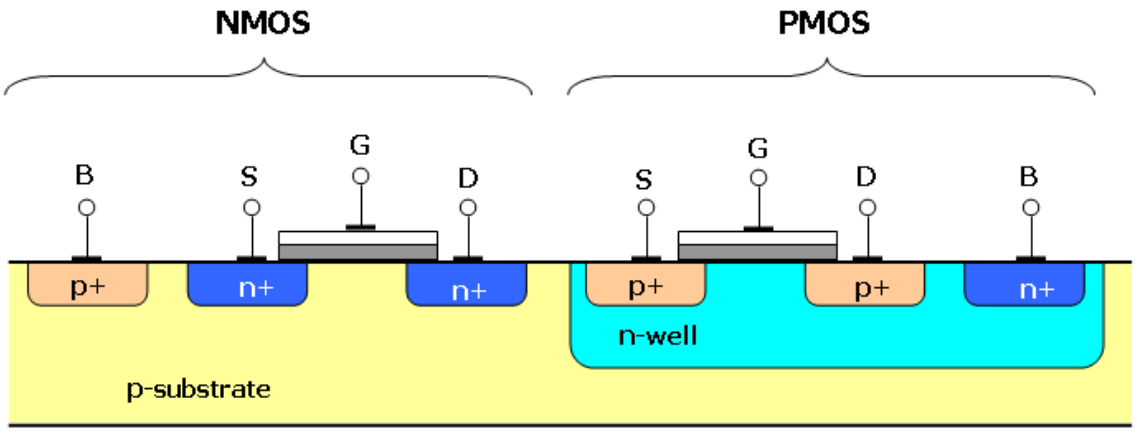
This example shows a NAND logic device drawn as a physical representation as it would be manufactured. The physical layout perspective is a "bird's eye view" of a stack of layers. The circuit is constructed on a P-type substrate. The polysilicon, diffusion, and n-well are referred to as "base layers" and are actually inserted into trenches of the P-type substrate. The contacts penetrate an insulating layer between the base layers and the first layer of metal (metal1) making a connection.

The inputs to the NAND (illustrated in green coloring) are in polysilicon. The CMOS transistors (devices) are formed by the intersection of the polysilicon and diffusion: N diffusion for the N device; P diffusion for the P device (illustrated in salmon and yellow coloring respectively). The output ("out") is connected together in metal (illustrated in cyan coloring). Connections between metal and polysilicon or diffusion are made through contacts (illustrated as black squares). The physical layout example matches the NAND logic circuit given in the previous example.

The N device is manufactured on a P-type substrate. The P device is manufactured in an N-type well (n-well). A P-type substrate "tap" is connected to V_{SS} and an N-type n-well tap is connected to V_{DD} to prevent latchup.



The physical layout of a NAND circuit. The larger regions of N-type diffusion and P-type diffusion are part of the transistors. The two smaller regions on the left are taps to prevent latchup.



Cross section of two transistors in a CMOS gate, in an N-well CMOS process

Power: switching and leakage

CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ("dynamic power"). On a typical ASIC in a modern 90 nanometer process, switching the output might take 120 picoseconds, and happen once every ten nanoseconds. NMOS logic dissipates power whenever the output is low ("static power"), because there is a current path from V_{dd} to V_{ss} through the load resistor and the n-type network.

CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. The charge moved is the capacitance multiplied by the voltage change. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOS device: $P = CV^2f$.

An additional form of power consumption became significant in the 1990s as wires on chip became narrower and the long wires became more resistive. CMOS gates at the end of those resistive wires see slow input transitions. During the middle of these transitions, both the NMOS and PMOS networks are partially conductive, and current flows directly from V_{dd} to V_{ss}. The power thus used is called *crowbar* power. Careful design which avoids weakly driven long skinny wires has ameliorated this effect, and crowbar power is nearly always substantially smaller than switching power.

Both NMOS and PMOS transistors have a gate–source threshold voltage, below which the current (called *subthreshold* current) through the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages (V_{dd} might have been 5 V, and V_{th} for both NMOS and PMOS might have been 700 mV). A special type of the CMOS transistor with near zero threshold voltage is the native transistor.

To speed up designs, manufacturers have switched to constructions that have lower voltage thresholds; but because of this a modern NMOS transistor with a V_{th} of 200 mV has a significant subthreshold leakage current. Designs (e.g. desktop processors) which include vast numbers of circuits which are not actively switching still consume power because of this leakage current. Leakage power is a significant portion of the total power consumed by such designs. Further technology advances that use even thinner gate dielectrics have an additional leakage component because of current tunnelling through the extremely thin gate dielectric. Using high-k dielectrics instead of silicon dioxide that is the conventional gate dielectric allows similar device performance, but with a thicker gate insulator, thus avoiding this current. Leakage power reduction using new material and system design is critical to sustaining scaling of CMOS. A good overview of leakage and reduction methods are explained in the book Leakage in Nanometer CMOS Technologies [4] ISBN 0-387-25737-3.

Analog CMOS

Besides digital applications, CMOS technology is also used in analog applications. For example, there are CMOS operational amplifier ICs available in the market. Transmission gates may be used instead of signal relays. CMOS technology is also widely used for RF circuits all the way to microwave frequencies, in mixed-signal (analog+digital) applications.

Temperature range

Conventional CMOS devices work over a range of −55 °C to +125 °C. There were theoretical indications as early as August 2008 that silicon CMOS will work down to 40 K, or −233 °C.[5] Functioning temperatures near 40 K have since been achieved using overclocked AMD Phenom II processors with a combination of liquid nitrogen and liquid helium cooling. [6]

See also

- Active pixel sensor
- MOSFET
- HCMOS
- Gate equivalent (GE)
- Electric and Magic are open-source software often used to lay out CMOS circuits.

Further reading

- Baker, R. Jacob (2010). *CMOS: Circuit Design, Layout, and Simulation, Third Edition*. Wiley-IEEE. p. 1174. ISBN 978-0-470-88132-3.
- Weste, Neil H. E. and Harris, David M. (2010). *CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Edition*. Boston: Pearson/Addison-Wesley. p. 840. ISBN 978-0-321-54774-3. http://CMOSVLSI.com/
- Veendrick, Harry J. M. (2008). *Nanometer CMOS ICs, from Basics to ASICs*. New York: Springer. p. 770. ISBN 978-1-4020-8332-7.
- Mead, Carver A. and Conway, Lynn (1980). *Introduction to VLSI systems*. Boston: Addison-Wesley. ISBN 0-201-04358-0.

External links

- CMOS gate description and interactive illustrations [7]
- LASI [8] is a "general purpose" IC layout CAD tool. It is a free download and can be used as a layout tool for CMOS circuits.

References

[1] *COS-MOS* was an RCA trademark, which forced other manufacturers to find another name —CMOS

[2] Intel 45nm Hi-k Silicon Technology (http://www.intel.com/technology/45nm/index.htm)

[3] Baker, R. Jacob (2008). *CMOS: circuit design, layout, and simulation* (Second ed.). Wiley-IEEE. p. xxix. ISBN 978-0-470-22941-5.

[4] http://www.springer.com/engineering/circuits+%26+systems/book/978-0-387-25737-2

[5] Edwards C, "Temperature control", *Engineering & Technology Magazine* 26 July - 8 August 2008, IET

[6] Patrick Moorhead (January 15th, 2009). "Breaking Records with Dragons and Helium in the Las Vegas Desert" (http://blogs.amd.com/home/2009/01/15/breaking-records-with-dragons-and-helium-in-the-las-vegas-desert/). blogs.amd.com/patmoorhead. . Retrieved 2009-09-18.

[7] http://tams-www.informatik.uni-hamburg.de/applets/cmos/

[8] http://lasihomesite.com/

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