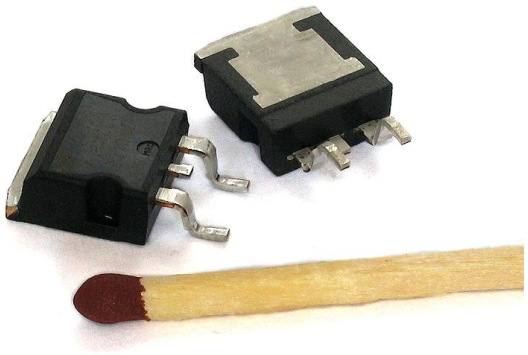
MOSFET

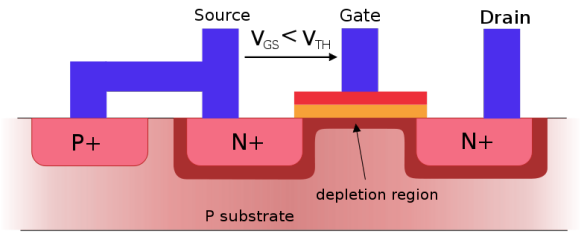
The **metal–oxide–semiconductor field-effect transistor** (**MOSFET**, **MOS-FET**, or **MOS FET**) is a device used for amplifying or switching electronic signals. The basic principle of the device was first proposed by Julius Edgar Lilienfeld in 1925. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type (see article on semiconductor devices), and is accordingly called an nMOSFET or a pMOSFET (also commonly nMOS, pMOS). It is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common.

The 'metal' in the name is now often a misnomer because the previously metal gate material is now often a layer of polysilicon (polycrystalline silicon). Aluminium had been the gate material until the mid 1970s, when polysilicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity, since it is difficult to increase the speed of operation of transistors without metal gates.

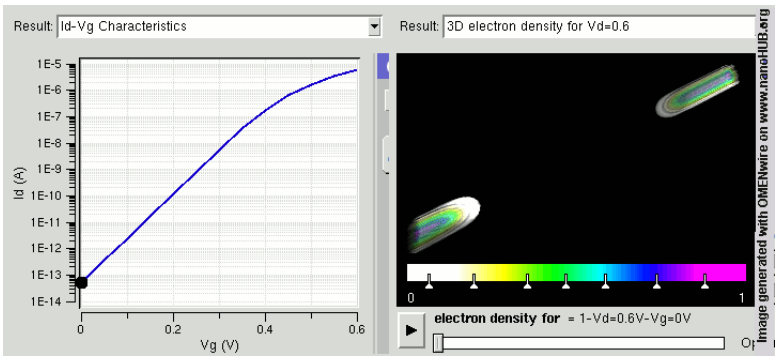
IGFET is a related term meaning insulated-gate field-effect transistor, and is almost synonymous with MOSFET, though it can refer to FETs with a gate insulator that is not oxide. Another synonym is MISFET for metal–insulator–semiconductor FET.



Two power MOSFETs in the surface-mount package D2PAK. Operating as switches, each of these components can sustain a blocking voltage of 120 volts in the *OFF* state, and can conduct a continuous current of 30 amperes in the *ON* state, dissipating up to about 100 watts and controlling a load of over 2000 watts. A matchstick is pictured for scale.

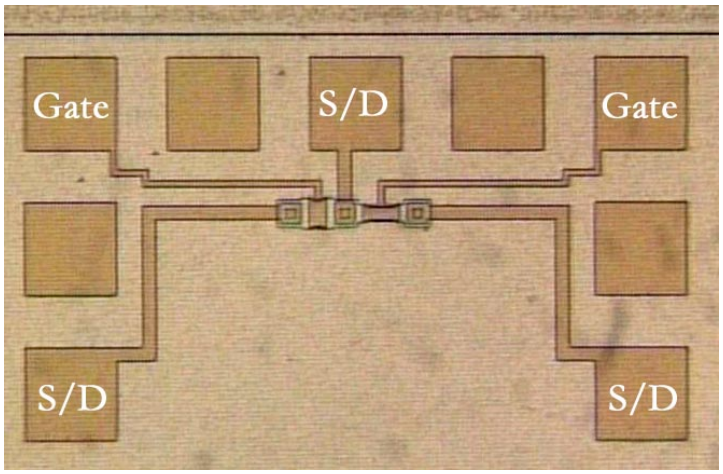


A cross section through an nMOSFET when the gate voltage V_{GS} is below the threshold for making a conductive channel; there is little or no conduction between the terminals source and drain; the switch is off. When the gate is more positive, it attracts electrons, inducing an *n*-type conductive channel in the substrate below the oxide, which allows electrons to flow between the *n*-doped terminals; the switch is on.



Simulation result for formation of inversion channel (electron density) and attainment of threshold voltage (IV) in a nanowire MOSFET. Note that the threshold voltage for this device lies around 0.45V.

Composition



Photomicrograph of two metal-gate MOSFETs in a test pattern. Probe pads for two gates and three source/drain nodes are labeled.

Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM, recently started using a chemical compound of silicon and germanium (SiGe) in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces, thus are not suitable for MOSFETs. Research continues on creating insulators with acceptable electrical characteristics on other semiconductor material.

In order to overcome power consumption increase due to gate current leakage, high-κ dielectric replaces silicon dioxide for the gate insulator, while metal gates return by replacing polysilicon (see Intel announcement[1]).

The gate is separated from the channel by a thin insulating layer, traditionally of silicon dioxide and later of silicon oxynitride. Some companies have started to introduce a high-κ dielectric + metal gate combination in the 45 nanometer node.

When a voltage is applied between the gate and body terminals, the electric field generated penetrates through the oxide and creates an alleged "inversion layer" or "channel" at the semiconductor-insulator interface. The inversion channel is of the same type, P-type or N-type, as the source and drain, thus it provides a channel through which current can pass. Varying the voltage between the gate and body modulates the conductivity of this layer and allows to control the current flow between drain and source.

Circuit symbols

A variety of symbols are used for the MOSFET. The basic design is generally a line for the channel with the source and drain leaving it at right angles and then bending back at right angles into the same direction as the channel. Sometimes three line segments are used for enhancement mode and a solid line for depletion mode. Another line is drawn parallel to the channel for the gate.

The bulk connection, if shown, is shown connected to the back of the channel with an arrow indicating PMOS or NMOS. Arrows always point from P to N, so an NMOS (N-channel in P-well or P-substrate) has the arrow pointing in (from the bulk to the channel). If the bulk is connected to the source (as is generally the case with discrete devices) it is sometimes angled to meet up with the source leaving the transistor. If the bulk is not shown (as is often the case in IC design as they are generally common bulk) an inversion symbol is sometimes used to indicate PMOS, alternatively an arrow on the source may be used in the same way as for bipolar transistors (out for nMOS, in for pMOS).

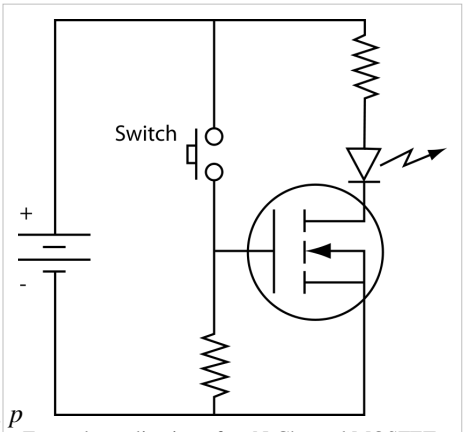
Comparison of enhancement-mode and depletion-mode MOSFET symbols, along with JFET symbols (drawn with source and drain ordered such that higher voltages appear higher on the page than lower voltages):

					P-channel
					N-channel
JFET	MOSFET enh	MOSFET enh (no bulk)		MOSFET dep	

For the symbols in which the bulk, or body, terminal is shown, it is here shown internally connected to the source. This is a typical configuration, but by no means the only important configuration. In general, the MOSFET is a four-terminal device, and in integrated circuits many of the MOSFETs share a body connection, not necessarily connected to the source terminals of all the transistors.

MOSFET operation

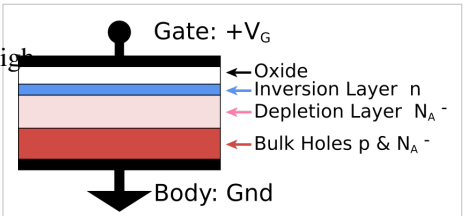
Metal–oxide–semiconductor structure



Example application of an N-Channel MOSFET. When the switch is pushed the LED lights up.[2]

A traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.

When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a P-type semiconductor (with N_A the density of acceptors, p the density of holes; $p = N_A$ in neutral bulk), a positive voltage, V_{GB}, from gate to body (see figure) creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface,



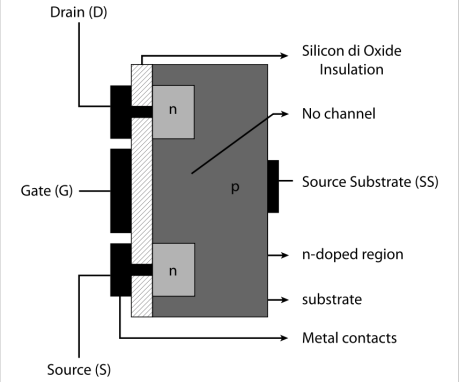
Metal–oxide–semiconductor structure on P-type silicon

leaving exposed a carrier-free region of immobile, negatively charged acceptor ions (see doping (semiconductor)). If V_{GB} is high enough, a high concentration of negative charge carriers forms in an **inversion layer** located in a thin layer next to the interface between the semiconductor and the insulator. Unlike the MOSFET, where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region. Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage.

This structure with P-type body is the basis of the N-type MOSFET, which requires the addition of an N-type source and drain regions.

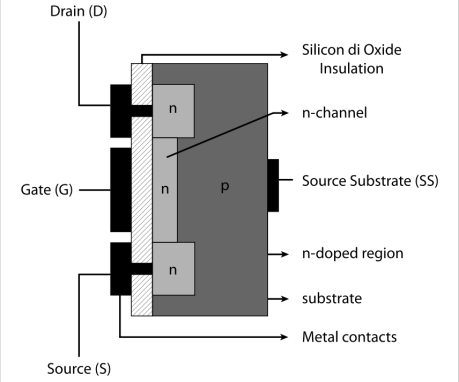
MOSFET structure and channel formation

A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a **body** electrode and a **gate** electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. If dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). Compared to the MOS capacitor, the MOSFET includes two additional terminals (**source** and **drain**), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a '+' sign after the type of doping.



Cross section of an NMOS without channel formed: OFF state

If the MOSFET is an n-channel or nMOS FET, then the source and drain are 'n+' regions and the body is a 'p' region. As described above, with sufficient gate voltage, holes from the body are driven away from the gate, forming an inversion layer or *n-channel* at the interface between the p region and the oxide. This conducting channel extends between the source and the drain, and current is conducted through it when a voltage is applied between source and drain.



Cross section of an NMOS with channel formed: ON state

For gate voltages below the threshold value, the channel is lightly populated, and only a very small subthreshold leakage current can flow between the source and the drain.

If the MOSFET is a p-channel or pMOS FET, then the source and drain are 'p+' regions and the body is a 'n' region. When a negative gate-source voltage (positive source-gate) is applied, it creates a *p-channel* at the surface of the n region, analogous to the n-channel case, but with opposite polarities of charges and voltages. When a voltage less negative than the threshold value (a negative voltage for p-channel) is applied between gate and source, the channel disappears and only a very small subthreshold current can flow between the source and the drain.

The source is so named because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel.

The device may comprise a Silicon On Insulator (SOI) device in which a Buried OXide (BOX) is formed below a thin semiconductor layer. If the channel region between the gate dielectric and a Buried Oxide (BOX) region is very thin, the very thin channel region is referred to as an Ultra Thin Channel (UTC) region with the source and drain regions formed on either side thereof in and/or above the thin semiconductor layer. Alternatively, the device may comprise a SEMiconductor On Insulator (SEMOI) device in which semiconductors other than silicon are employed. Many alternative semicondutor materials may be employed.

When the source and drain regions are formed above the channel in whole or in part, they are referred to as Raised Source/Drain (RSD) regions.

Modes of operation

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. In the following discussion, a simplified algebraic model is used that is accurate only for old technology. Modern MOSFET characteristics require computer models that have rather more complex behavior.

For an **enhancement-mode, n-channel MOSFET**, the three operational modes are:

Cutoff, subthreshold, or weak-inversion mode

When $V_{GS} < V_{th}$:

where V_{th} is the threshold voltage of the device.

According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gate–source voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage.

In weak inversion the current varies exponentially with gate-to-source bias V_{GS} as given approximately by:[3] [4]

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}},$$

where I_{D0}= current at $V_{GS} = V_{th}$ and the slope factor *n* is given by

$$n = 1 + C_D/C_{OX},$$

with C_D = capacitance of the depletion layer and C_{OX} = capacitance of the oxide layer. In a long-channel device, there is no drain voltage dependence of the current once $V_{DS} >> V_T$, but as channel length is reduced drain-induced barrier lowering introduces drain voltage dependence that depends in a complex way upon the device geometry (for example, the channel doping, the junction doping and so on). Frequently, threshold voltage V_{th} for this mode is defined as the gate voltage at which a selected value of current I_{D0} occurs, for example, I_{D0} = 1 μA, which may not be the same V_{th}-value used in the equations for the following modes.

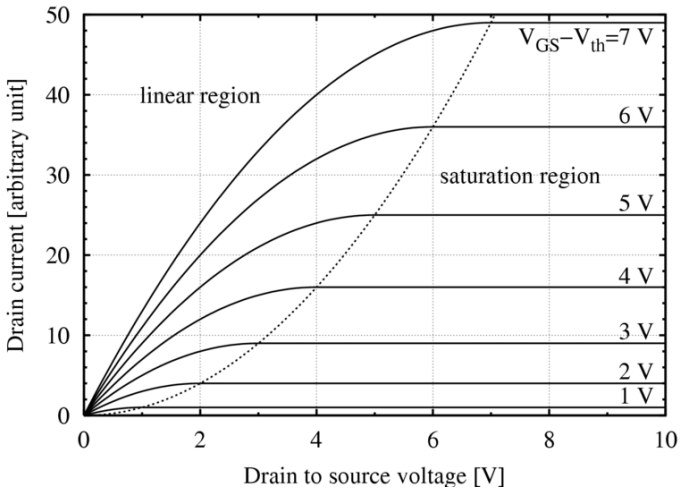
Some micropower analog circuits are designed to take advantage of subthreshold conduction.[5] [6] [7] By working in the weak-inversion region, the MOSFETs in these circuits deliver the highest possible transconductance-to-current ratio, namely: $g_m/I_D = 1/(nV_T)$, almost that of a bipolar transistor.[8]

The subthreshold *I–V curve* depends exponentially upon threshold voltage, introducing a strong dependence on any manufacturing variation that affects threshold voltage; for example: variations in oxide thickness, junction depth, or body doping that change the degree of drain-induced barrier lowering. The resulting sensitivity to fabricational variations complicates optimization for leakage and performance.[9] [10]

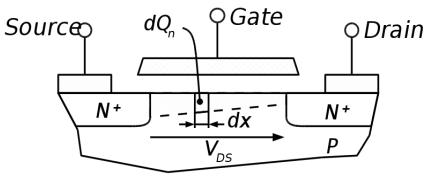
Triode mode or linear region (also known as the ohmic mode[11] [12])

When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$

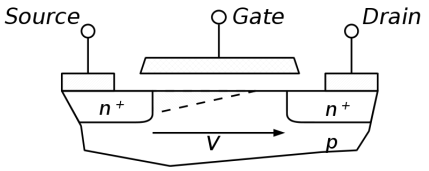
The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:



MOSFET drain current vs. drain-to-source voltage for several values of $V_{GS} - V_{th}$; the boundary between **linear** (**Ohmic**) and **saturation** (**active**) modes is indicated by the upward curving parabola.



Cross section of a MOSFET operating in the linear (Ohmic) region; strong inversion region present even near drain



Cross section of a MOSFET operating in the saturation (active) region; channel exhibits **pinch-off** near drain

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

where μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area. The transition from the exponential subthreshold region to the triode region is not as sharp as the equations suggest.

Saturation or active mode[3] [13]

When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not

through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as **pinch-off** to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled very approximately as:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) .$$

The additional factor involving λ, the channel-length modulation parameter, models current dependence on drain voltage due to the Early effect, or channel length modulation. According to this equation, a key design parameter, the MOSFET transconductance is:

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2I_D}{V_{ov}},$$

where the combination $V_{ov} = V_{GS} - V_{th}$ is called the **overdrive voltage**.[14] Another key design parameter is the MOSFET output resistance r_O given by:

$$r_{OUT} = \frac{1}{\lambda I_D}.$$

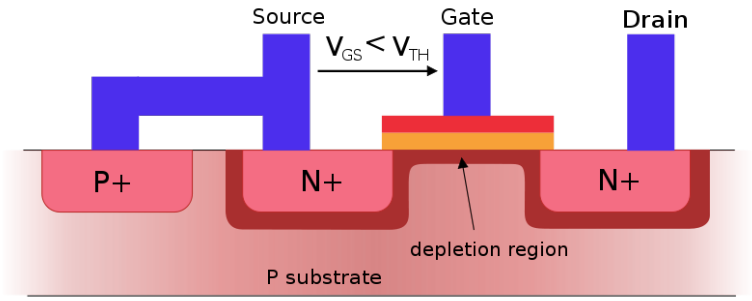
r_{out} is the inverse of g_{ds} where $g_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}}$. V_{DS} is the expression in saturation region.

If λ is taken as zero, an infinite output resistance of the device results that leads to unrealistic circuit predictions, particularly in analog circuits.

As the channel length becomes very short, these equations become quite inaccurate. New physical effects arise. For example, carrier transport in the active mode may become limited by velocity saturation. When velocity saturation dominates, the saturation drain current is more nearly linear than quadratic in V_{GS}. At even shorter lengths, carriers transport with near zero scattering, known as quasi-ballistic transport. In addition, the output current is affected by drain-induced barrier lowering of the threshold voltage.

Body effect

The body effect describes the changes in the threshold voltage by the change in the source-bulk voltage, approximated by the following equation:



Ohmic contact to body to ensure no body bias; top left:subthreshold, top right:Ohmic mode, bottom left:Active mode at onset of pinch-off, bottom right: Active mode well into pinch-off - channel length modulation evident

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\phi} - \sqrt{2\phi}\right),$$

where V_{TN} is the threshold voltage with substrate bias present, and V_{TO} is the zero- V_{SB} value of threshold voltage, γ is the body effect parameter, and 2ϕ is the surface potential parameter.

The body can be operated as a second gate, and is sometimes referred to as the "back gate"; the body effect is sometimes called the "back-gate effect".[15]

The primacy of MOSFETs

In 1959, Dawon Kahng and Martin M. (John) Atalla at Bell Labs invented the metal–oxide–semiconductor field-effect transistor (MOSFET).[16] Operationally and structurally different from the bipolar junction transistor,[17] the MOSFET was made by putting an insulating layer on the surface of the semiconductor and then placing a metallic gate electrode on that. It used crystalline silicon for the semiconductor and a thermally oxidized layer of silicon dioxide for the insulator. The silicon MOSFET did not generate localized electron traps at the interface between the silicon and its native oxide layer, and thus was inherently free from the trapping and scattering of carriers that had impeded the performance of earlier field-effect transistors. Following the (expensive) development of clean rooms to reduce contamination to levels never before thought necessary, and of photolithography[18] and the planar process to allow circuits to be made in very few steps, the Si–SiO_2 system possessed such technical attractions as low cost of production (on a per circuit basis) and ease of integration. Largely because of these two factors, the MOSFET has become the most widely used type of transistor in integrated circuits.

CMOS circuits

The MOSFET is used in digital CMOS logic,[19] which uses p- and n-channel MOSFETs as building blocks. Overheating is a major concern in integrated circuits since ever more transistors are packed into ever smaller chips. CMOS logic reduces power consumption because no current flows (ideally), and thus no power is consumed, except when the inputs to logic gates are being switched. CMOS accomplishes this current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET not to conduct and a low voltage on the gates causes the reverse. During the switching time as the voltage goes from one state to another, both MOSFETs will conduct briefly. This arrangement greatly reduces power consumption and heat generation. Digital and analog CMOS applications are described below.

Digital

The growth of digital technologies like the microprocessor has provided the motivation to advance MOSFET technology faster than any other type of silicon-based transistor. A timeline can be found at computerhistory.org.[20] A big advantage of MOSFETs for digital switching is that the oxide layer between the gate and the channel prevents DC current from flowing through the gate, further reducing power consumption and giving a very large input impedance. The insulating oxide between the gate and channel effectively isolates a MOSFET in one logic stage from earlier and later stages, which allows a single MOSFET output to drive a considerable number of MOSFET inputs. Bipolar transistor-based logic (such as TTL) does not have such a high fanout capacity. This isolation also makes it easier for the designers to ignore to some extent loading effects between logic stages independently. That extent is defined by the operating frequency: as frequencies increase, the input impedance of the MOSFETs decreases.

Analog

The MOSFET's advantages in most digital circuits do not translate into supremacy in all analog circuits. The two types of circuit draw upon different features of transistor behavior. Digital circuits switch, spending most of their time outside the switching region, while analog circuits depend on MOSFET behavior held precisely in the switching region of operation. The bipolar junction transistor (BJT) has traditionally been the analog designer's transistor of choice, due largely to its higher transconductance and its higher output impedance (drain-voltage independence) in the switching region.

Nevertheless, MOSFETs are widely used in many types of analog circuits because of certain advantages. The characteristics and performance of many analog circuits can be designed by changing the sizes (length and width) of the MOSFETs used. By comparison, in most bipolar transistors the size of the device does not significantly affect the performance. MOSFETs' ideal characteristics regarding gate current (zero) and drain-source offset voltage (zero) also make them nearly ideal switch elements, and also make switched capacitor analog circuits practical. In their linear region, MOSFETs can be used as precision resistors, which can have a much higher controlled resistance than BJTs. In high power circuits, MOSFETs sometimes have the advantage of not suffering from thermal runaway as BJTs do. Also, they can be formed into capacitors and gyrator circuits which allow op-amps made from them to appear as inductors, thereby allowing all of the normal analog devices, except for diodes (which can be made smaller than a MOSFET anyway), to be built entirely out of MOSFETs. This allows for complete analog circuits to be made on a silicon chip in a much smaller space.

Some ICs combine analog and digital MOSFET circuitry on a single mixed-signal integrated circuit, making the needed board space even smaller. This creates a need to isolate the analog circuits from the digital circuits on a chip level, leading to the use of isolation rings and Silicon-On-Insulator (SOI). The main advantage of BJTs versus MOSFETs in the analog design process is the ability of BJTs to handle a larger current in a smaller space. Fabrication processes exist that incorporate BJTs and MOSFETs into a single device. Mixed-transistor devices are called Bi-FETs (Bipolar-FETs) if they contain just one BJT-FET and BiCMOS (bipolar-CMOS) if they contain complementary BJT-FETs. Such devices have the advantages of both insulated gates and higher current density.

BJTs have some advantages over MOSFETs for at least two digital applications. Firstly, in high speed switching, they do not have the "larger" capacitance from the gate, which when multiplied by the resistance of the channel gives the intrinsic time constant of the process. The intrinsic time constant places a limit on the speed a MOSFET can operate at because higher frequency signals are filtered out. Widening the channel reduces the resistance of the channel, but increases the capacitance by the exact same amount. Reducing the width of the channel increases the resistance, but reduces the capacitance by the same amount. R*C=Tc1, 0.5R*2C=Tc1, 2R*0.5C=Tc1. There is no way to minimize the intrinsic time constant for a certain process. Different processes using different channel lengths, channel heights, gate thicknesses and materials will have different intrinsic time constants. This problem is mostly avoided with a BJT because it does not have a gate.

The second application where BJTs have an advantage over MOSFETs stems from the first. When driving many other gates, called fanout, the resistance of the MOSFET is in series with the gate capacitances of the other FETs, creating a secondary time constant. Delay circuits use this fact to create a fixed signal delay by using a small CMOS device to send a signal to many other, many times larger CMOS devices. The secondary time constant can be minimized by increasing the driving FET's channel width to decrease its resistance and decreasing the channel widths of the FETs being driven, decreasing their capacitance. The drawback is that it increases the capacitance of the driving FET and increases the resistance of the FETs being driven, but usually these drawbacks are a minimal problem when compared to the timing problem. BJTs are better able to drive the other gates because they can output more current than MOSFETs, allowing for the FETs being driven to charge faster. Many chips use MOSFET inputs and BiCMOS outputs (see above).

MOSFET scaling

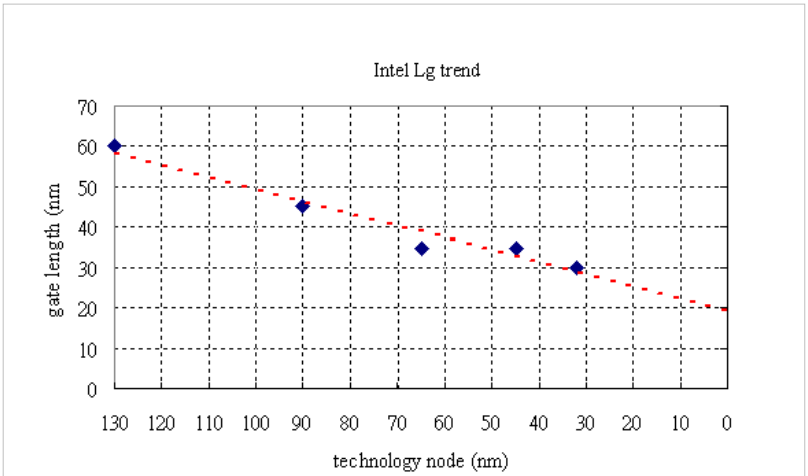
Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. Intel began production of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009. The semiconductor industry maintains a "roadmap", the ITRS [21] , which sets the pace for MOSFET development. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation (small MOSFETs exhibit higher leakage currents, and

lower output resistance, discussed below).

Reasons for MOSFET scaling

Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology is twice as many as in a 65 nm chip. This doubling of the transistor count was first observed by Gordon Moore in 1965 and is commonly referred to as Moore's law.[22]

It is also expected that smaller transistors switch faster. For example, one approach to size reduction is a scaling of the MOSFET that requires all device dimensions to reduce proportionally. The main device dimensions are the transistor length, width, and the oxide thickness, each (used to) scale with a factor of 0.7 per node. This way, the transistor channel resistance does not change with scaling, while gate capacitance is cut by a factor of 0.7. Hence, the RC delay of the transistor scales with a factor of 0.7.



Trend of Intel CPU transistor gate length

While this has been traditionally the case for the older technologies, for the state-of-the-art MOSFETs reduction of the transistor dimensions does not necessarily translate to higher chip speed because the delay due to interconnections is more significant.

Difficulties arising due to MOSFET size reduction

Producing MOSFETs with channel lengths much smaller than a micrometer is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. In recent years, the small size of the MOSFET, below a few tens of nanometers, has created operational problems.

Higher subthreshold conduction

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available; the circuit design is a compromise between strong current in the "on" case and low current in the "off" case, and the application determines whether to favor one over the other. Subthreshold leakage (including subthreshold conduction, gate-oxide leakage and reverse-biased junction leakage), which was ignored in the past, now can consume upwards of half of the total power consumption of modern high-performance VLSI chips.[23] [24] [25]

Increased gate-oxide leakage

The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance when the transistor is on and to reduce subthreshold leakage when the transistor is off. However, with current gate oxides with a thickness of around 1.2 nm (which in silicon is ~5 atoms thick) the quantum mechanical phenomenon of electron tunneling occurs between the gate and channel, leading to increased power consumption.

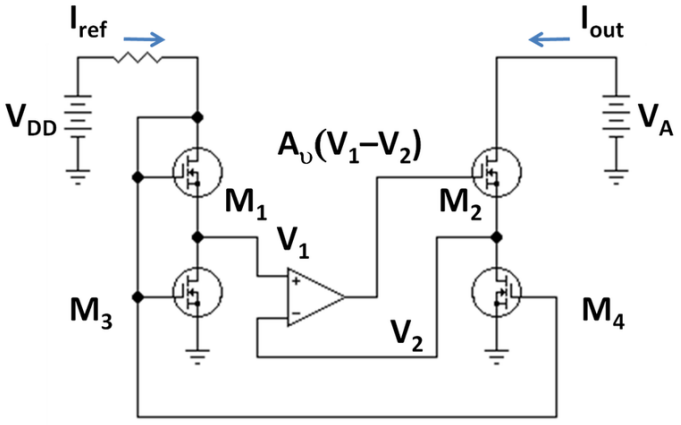
Insulators (referred to as high-k dielectrics) that have a larger dielectric constant than silicon dioxide, such as group IVb metal silicates e.g. hafnium and zirconium silicates and oxides are being used to reduce the gate leakage from the 45 nanometer technology node onwards. Increasing the dielectric constant of the gate dielectric allows a thicker layer while maintaining a high capacitance (capacitance is proportional to dielectric constant and inversely proportional to dielectric thickness). All else equal, a higher dielectric thickness reduces the quantum tunneling current through the dielectric between the gate and the channel. On the other hand, the barrier height of the new gate insulator is an important consideration; the difference in conduction band energy between the semiconductor and the dielectric (and the corresponding difference in valence band energy) also affects leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 8 eV. For many alternative dielectrics the value is significantly lower, tending to increase the tunneling current, somewhat negating the advantage of higher dielectric constant.

Increased junction leakage

To make devices smaller, junction design has become more complex, leading to higher doping levels, shallower junctions, "halo" doping and so forth,[26] [27] all to decrease drain-induced barrier lowering (see the section on junction design). To keep these complex junctions in place, the annealing steps formerly used to remove damage and electrically active defects must be curtailed[28] increasing junction leakage. Heavier doping is also associated with thinner depletion layers and more recombination centers that result in increased leakage current, even without lattice damage.

Lower output resistance

For analog operation, good gain requires a high MOSFET output impedance, which is to say, the MOSFET current should vary only slightly with the applied drain-to-source voltage. As devices are made smaller, the influence of the drain competes more successfully with that of the gate due to the growing proximity of these two electrodes, increasing the sensitivity of the MOSFET current to the drain voltage. To counteract the resulting decrease in output resistance, circuits are made more complex, either by requiring more devices, for example the cascode and cascade amplifiers, or by feedback circuitry using operational amplifiers, for example a circuit like that in the adjacent figure.



MOSFET version of gain-boosted current mirror; M_1 and M_2 are in active mode, while M_3 and M_4 are in Ohmic mode, and act like resistors. The operational amplifier provides feedback that maintains a high output resistance

Lower transconductance

The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility (depending on device type), at least for low drain voltages. As MOSFET size is reduced, the fields in the channel increase and the

dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths are reduced without proportional reduction in drain voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance.

Interconnect capacitance

Traditionally, switching time was roughly proportional to the gate capacitance of gates. However, with transistors becoming smaller and more transistors being placed on the chip, interconnect capacitance (the capacitance of the wires connecting different parts of the chip) is becoming a large percentage of capacitance.[29] [30] Signals have to travel through the interconnect, which leads to increased delay and lower performance.

Heat production

The ever-increasing density of MOSFETs on an integrated circuit creates problems of substantial localized heat generation that can impair circuit operation. Circuits operate slower at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling methods are now required for many integrated circuits including microprocessors.

Power MOSFETs are at risk of thermal runaway. As their on-state resistance rises with temperature, if the load is approximately a constant-current load then the power loss rises correspondingly, generating further heat. When the heatsink is not able to keep the temperature low enough, the junction temperature may rise quickly and uncontrollably, resulting in destruction of the device.

Large heatsinks to cool power transistors in a TRM-800 audio amplifier

In order to assist designers in the device selection process, a simulation tool such as ThermaSim™ can be used to simulate in-circuit performance[31] .

Process variations

With MOSFETS becoming smaller, the number of atoms in the silicon that produce many of the transistor's properties is becoming fewer, with the result that control of dopant numbers and placement is more erratic. During chip manufacturing, random process variations affect all transistor dimensions: length, width, junction depths, oxide thickness *etc.*, and become a greater percentage of overall transistor size as the transistor shrinks. The transistor characteristics become less certain, more statistical. The random nature of manufacture means we do not know which particular example MOSFETs actually will end up in a particular instance of the circuit. This uncertainty forces a less optimal design because the design must work for a great variety of possible component MOSFETs. See process variation, design for manufacturability, reliability engineering, and statistical process control.[32]

Modeling challenges

Modern ICs are computer-simulated with the goal of obtaining working circuits from the very first manufactured lot. As devices are miniaturized, the complexity of the processing makes it difficult to predict exactly what the final devices look like, and modeling of physical processes becomes more challenging as well. In addition, microscopic variations in structure due simply to the probabilistic nature of atomic processes require statistical (not just deterministic) predictions. These factors combine to make adequate simulation and "right the first time" manufacture difficult.

MOSFET construction

Gate material

The primary criterion for the gate material is that it is a good conductor. Highly-doped polycrystalline silicon is an acceptable but certainly not ideal conductor, and also suffers from some more technical deficiencies in its role as the standard gate material. Nevertheless, there are several reasons favoring use of polysilicon:

1. The threshold voltage (and consequently the drain to source on-current) is modified by the work function difference between the gate material and channel material. Because polysilicon is a semiconductor, its work function can be modulated by adjusting the type and level of doping. Furthermore, because polysilicon has the same bandgap as the underlying silicon channel, it is quite straightforward to tune the work function to achieve low threshold voltages for both NMOS and PMOS devices. By contrast, the work functions of metals are not easily modulated, so tuning the work function to obtain low threshold voltages becomes a significant challenge. Additionally, obtaining low-threshold devices on both PMOS and NMOS devices would likely require the use of different metals for each device type, introducing additional complexity to the fabrication process.
2. The Silicon-SiO_2 interface has been well studied and is known to have relatively few defects. By contrast many metal–insulator interfaces contain significant levels of defects which can lead to Fermi-level pinning, charging, or other phenomena that ultimately degrade device performance.
3. In the MOSFET IC fabrication process, it is preferable to deposit the gate material prior to certain high-temperature steps in order to make better-performing transistors. Such high temperature steps would melt some metals, limiting the types of metal that can be used in a metal-gate-based process.

While polysilicon gates have been the de facto standard for the last twenty years, they do have some disadvantages which have led to their likely future replacement by metal gates. These disadvantages include:

1. Polysilicon is not a great conductor (approximately 1000 times more resistive than metals) which reduces the signal propagation speed through the material. The resistivity can be lowered by increasing the level of doping, but even highly doped polysilicon is not as conductive as most metals. In order to improve conductivity further, sometimes a high-temperature metal such as tungsten, titanium, cobalt, and more recently nickel is alloyed with the top layers of the polysilicon. Such a blended material is called silicide. The silicide-polysilicon combination has better electrical properties than polysilicon alone and still does not melt in subsequent processing. Also the threshold voltage is not significantly higher than with polysilicon alone, because the silicide material is not near the channel. The process in which silicide is formed on both the gate electrode and the source and drain regions is sometimes called salicide, self-aligned silicide.
2. When the transistors are extremely scaled down, it is necessary to make the gate dielectric layer very thin, around 1 nm in state-of-the-art technologies. A phenomenon observed here is the so-called poly depletion, where a depletion layer is formed in the gate polysilicon layer next to the gate dielectric when the transistor is in the inversion. To avoid this problem, a metal gate is desired. A variety of metal gates such as tantalum, tungsten, tantalum nitride, and titanium nitride are used, usually in conjunction with high-k dielectrics. An alternative is to use fully-silicided polysilicon gates, a process known as FUSI.

Insulator

As devices are made smaller, insulating layers are made thinner, and at some point tunneling of carriers through the insulator from the channel to the gate electrode takes place. To reduce the resulting leakage current, the insulator can be made thicker by choosing a material with a higher dielectric constant. To see how thickness and dielectric constant are related, note that Gauss' law connects field to charge as:

$$Q = \kappa\epsilon_0 \ E\,,$$

with Q = charge density, κ = dielectric constant, ε_0 = permittivity of empty space and E = electric field. From this law it appears the same charge can be maintained in the channel at a lower field provided κ is increased. The voltage on the gate is given by:

$$V_G = V_{ch} + E\ t_{ins} = V_{ch} + \frac{Qt_{ins}}{\kappa\epsilon_0},$$

with V_G = gate voltage, V_{ch} = voltage at channel side of insulator, and t_{ins} = insulator thickness. This equation shows the gate voltage will not increase when the insulator thickness increases, provided κ increases to keep t_{ins}/κ = *constant* (see the article on high-κ dielectrics for more detail, and the section in this article on gate-oxide leakage).

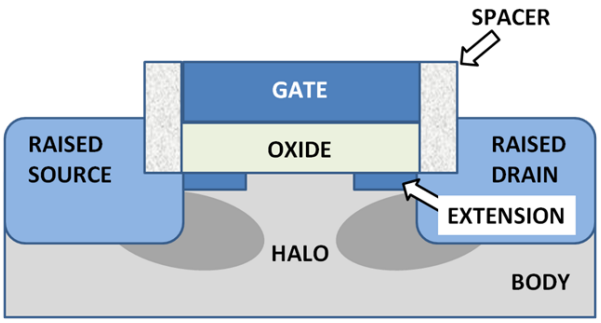
The insulator in a MOSFET is a dielectric which can in any event be silicon oxide, but many other dielectric materials are employed. The generic term for the dielectric is gate dielectric since the dielectric lies directly below the gate electrode and above the channel of the MOSFET.

Junction design

The source-to-body and drain-to-body junctions are the object of much attention because of three major factors: their design affects the current-voltage (*I-V*) characteristics of the device, lowering output resistance, and also the speed of the device through the loading effect of the junction capacitances, and finally, the component of stand-by power dissipation due to junction leakage.

The drain induced barrier lowering of the threshold voltage and channel length modulation effects upon *I-V* curves are reduced by using shallow junction extensions. In addition, *halo* doping can be used, that is, the addition of very thin heavily doped regions of the same doping type as the body tight against the junction walls to limit the extent of depletion regions.[33]

The capacitive effects are limited by using raised source and drain geometries that make most of the contact area border thick dielectric instead of silicon.[34]



MOSFET showing shallow junction extensions, raised source and drain and halo implant. Raised source and drain separated from gate by oxide spacers.

These various features of junction design are shown (with artistic license) in the figure.

Junction leakage is discussed further in the section increased junction leakage.

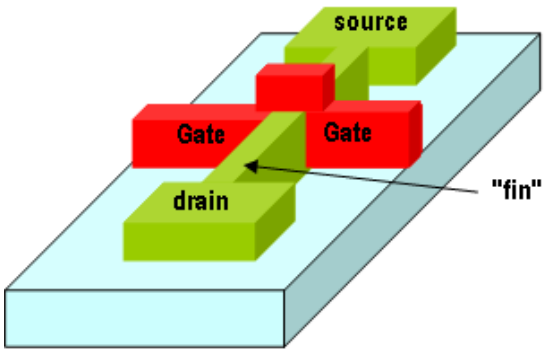
Other MOSFET types

Dual gate MOSFET

The dual gate MOSFET has a tetrode configuration, where both gates control the current in the device. It is commonly used for small signal devices in radio frequency applications where the second gate is normally used for gain control or mixing and frequency conversion.

FinFET

The Finfet, see figure to right, is a double gate device, one of a number of geometries being introduced to mitigate the effects of short channels and reduce drain-induced barrier lowering.



A double-gate FinFET device.

Depletion-mode MOSFETs

There are *depletion-mode* MOSFET devices, which are less commonly used than the standard *enhancement-mode* devices already described. These are MOSFET devices that are doped so that a channel exists even with zero voltage from gate to source. In order to control the channel, a negative voltage is applied to the gate (for an n-channel device), depleting the channel, which reduces the current flow through the device. In essence, the depletion-mode device is equivalent to a normally closed (on) switch, while the enhancement-mode device is equivalent to a normally open (off) switch.[35]

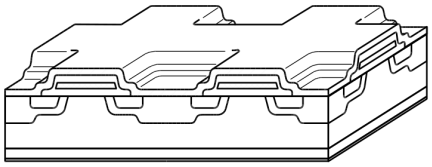
Due to their low noise figure in the RF region, and better gain, these devices are often preferred to bipolars in RF front-ends such as in TV sets. Depletion-mode MOSFET families include BF 960 by Siemens and BF 980 by Philips (dated 1980s), whose derivatives are still used in AGC and RF mixer front-ends.

NMOS logic

n-channel MOSFETs are smaller than p-channel MOSFETs and producing only one type of MOSFET on a silicon substrate is cheaper and technically simpler. These were the driving principles in the design of NMOS logic which uses n-channel MOSFETs exclusively. However, unlike CMOS logic, NMOS logic consumes power even when no switching is taking place. With advances in technology, CMOS logic displaced NMOS logic in the 1980s to become the preferred process for digital chips.

Power MOSFET

Power MOSFETs have a different structure than the one presented above.[36] As with all power devices, the structure is vertical and not planar. Using a vertical structure, it is possible for the transistor to sustain both high blocking voltage and high current. The voltage rating of the transistor is a function of the doping and thickness of the N-epitaxial layer (see cross section), while the current rating is a function of the channel width (the wider the channel, the higher the current). In a planar structure, the current and breakdown voltage ratings are both a function of the channel dimensions (respectively width and length of the channel), resulting in inefficient use of the "silicon estate". With the vertical structure, the component area is roughly proportional to the current it can sustain, and the component thickness (actually the N-epitaxial layer thickness) is proportional to the breakdown voltage[37] .



Cross section of a Power MOSFET, with square cells. A typical transistor is constituted of several thousand cells

It is worth noting that power MOSFETs with lateral structure are mainly used in high-end audio amplifiers and high-power PA systems. Their advantage is a better behaviour in the saturated region (corresponding to the linear region of a bipolar transistor) than the vertical MOSFETs. Vertical MOSFETs are designed for switching applications[38] .

DMOS

DMOS stands for double-diffused metal–oxide–semiconductor. Most power MOSFETs are made using this technology.

RHBD MOSFETs

Semiconductor sub-micron and nano-meter electronic circuits are the primary concern for operating within the normal tolerance in harsh radiation environments like space. One of the design approaches for making a radiation-hardened-by-design (RHBD) device is Enclosed-Layout-Transistor (ELT). Normally, the gate of the MOSFET surrounds the drain, which is placed in the center of the ELT. The source of the MOSFET surrounds the gate. Another RHBD MOSFET is called H-Gate. Both of these transistors have very low leakage current with respect to radiation. However, they are large in size and take more space on silicon than a standard MOSFET.

Newer technologies are emerging for smaller devices for cost saving, low power and increased operating speed. The standard MOSFET is also becoming extremely sensitive to radiation for the newer technologies. A lot more research works should be completed before space electronics can safely use RHBD MOSFET circuits of nanotechnology.

When radiation strikes near the silicon oxide region (STI) of the MOSFET, the channel inversion occurs at the corners of the standard MOSFET due to accumulation of radiation induced trapped charges. If the charges are large enough, the accumulated charges affect STI surface edges along the channel near the channel interface (gate) of the standard MOSFET. Thus the device channel inversion occurs along the channel edges and the device creates off-state leakage path, causing device to turn on. So the reliability of circuits degrades severely. The ELT offers many advantages. These advantages include improvement of reliability by reducing unwanted surface inversion at the gate edges that occurs in the standard MOSFET. Since the gate edges are enclosed in ELT, there is no gate oxide edge (STI at gate interface), and thus the transistor off-state leakage is reduced very much.

Low-power microelectronic circuits including computers, communication devices and monitoring systems in space shuttle and satellites are very different than what we use on earth. They are radiation (high-speed atomic particles like proton and neutron, solar flare magnetic energy dissipation in earth's space, energetic cosmic rays like X-ray,

Gamma-ray etc.) tolerant circuits. These special electronics are designed by applying very different techniques using RHBD MOSFETs to ensure the safe space journey and also space-walk of astronauts.

MOSFET analog switch

MOSFET analog switches use the MOSFET channel as a low–on-resistance switch to pass analog signals when on, and as a high impedance when off. Signals flow in both directions across a MOSFET switch. In this application the drain and source of a MOSFET exchange places depending on the voltages of each electrode compared to that of the gate. For a simple MOSFET without an integrated diode, the source is the more negative side for an N-MOS or the more positive side for a P-MOS. All of these switches are limited on what signals they can pass or stop by their gate-source, gate-drain and source-drain voltages, and source-to-drain currents; exceeding the voltage limits will potentially damage the switch.

Single-type MOSFET switch

This analog switch uses a four-terminal simple MOSFET of either P or N type. In the case of an N-type switch, the body is connected to the most negative supply (usually GND) and the gate is used as the switch control. Whenever the gate voltage exceeds the source voltage by at least a threshold voltage, the MOSFET conducts. The higher the voltage, the more the MOSFET can conduct. An N-MOS switch passes all voltages less than ($V_{gate}-V_{tn}$). When the switch is conducting, it typically operates in the linear (or Ohmic) mode of operation, since the source and drain voltages will typically be nearly equal.

In the case of a P-MOS, the body is connected to the most positive voltage, and the gate is brought to a lower potential to turn the switch on. The P-MOS switch passes all voltages higher than ($V_{gate}+|V_{tp}|$). Threshold voltage (V_{tp}) is typically negative in the case of P-MOS.

A P-MOS switch will have about three times the resistance of an N-MOS device of equal dimensions because electrons have about three times the mobility of holes in silicon.

Dual-type (CMOS) MOSFET switch

This "complementary" or CMOS type of switch uses one P-MOS and one N-MOS FET to counteract the limitations of the single-type switch. The FETs have their drains and sources connected in parallel, the body of the P-MOS is connected to the high potential (V_{DD}) and the body of the N-MOS is connected to the low potential (Gnd). To turn the switch on the gate of the P-MOS is driven to the low potential and the gate of the N-MOS is driven to the high potential. For voltages between ($V_{DD}-$Vtn) and (Gnd+Vtp) both FETs conduct the signal, for voltages less than (Gnd+Vtp) the N-MOS conducts alone and for voltages greater than ($V_{DD}-$Vtn) the P-MOS conducts alone.

The only limits for this switch are the gate-source, gate-drain and source-drain voltage limits for both FETs. Also, the P-MOS is typically three times the width of the N-MOS so the switch will be balanced.

Tri-state circuitry sometimes incorporates a CMOS MOSFET switch on its output to provide for a low ohmic, full range output when on and a high ohmic, mid level signal when off.

See also

- BSIM
- Transistor models

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External links

- An introduction to depletion-mode MOSFETs [40]
- Power MOSFETs [41]
- MOSFET Process Step by Step [42] A Flash slide showing the fabricating process of a MOSFET in detail step
- MOSFET Calculator [43] MOSFET Calculator
- Advanced MOSFET Issues [44]
- MOSFET applet [45] Very nice applet that helps to understand MOSFET.
- MIT OpenCourseWare courses:
  - MIT Open Courseware 6.002 - Spring 2007 [46] -- Link to the intro electrical engineering course at MIT on circuits and electronics.
  - MIT Open Courseware 6.012 - Fall 2005 [47] -- Link to a more advanced class taught at MIT all about microelectronics and MOSFETs
- Georgia Tech BJT and FET Slides [48] Slides from a Microelectronic Circuits class at Georgia Tech
- CircuitDesign: MOS Diffusion Parasitics [49] Crude illustrations of MOS diffusion structure and sample circuit layouts to minimize their parasitics
- Course on *Physics of Nanoscale Transistors* [50]
- Notes on Ballistic MOSFETs by Dr. Lundstrom [51] nice resource to understand theory of ballistic MOSFETs.

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