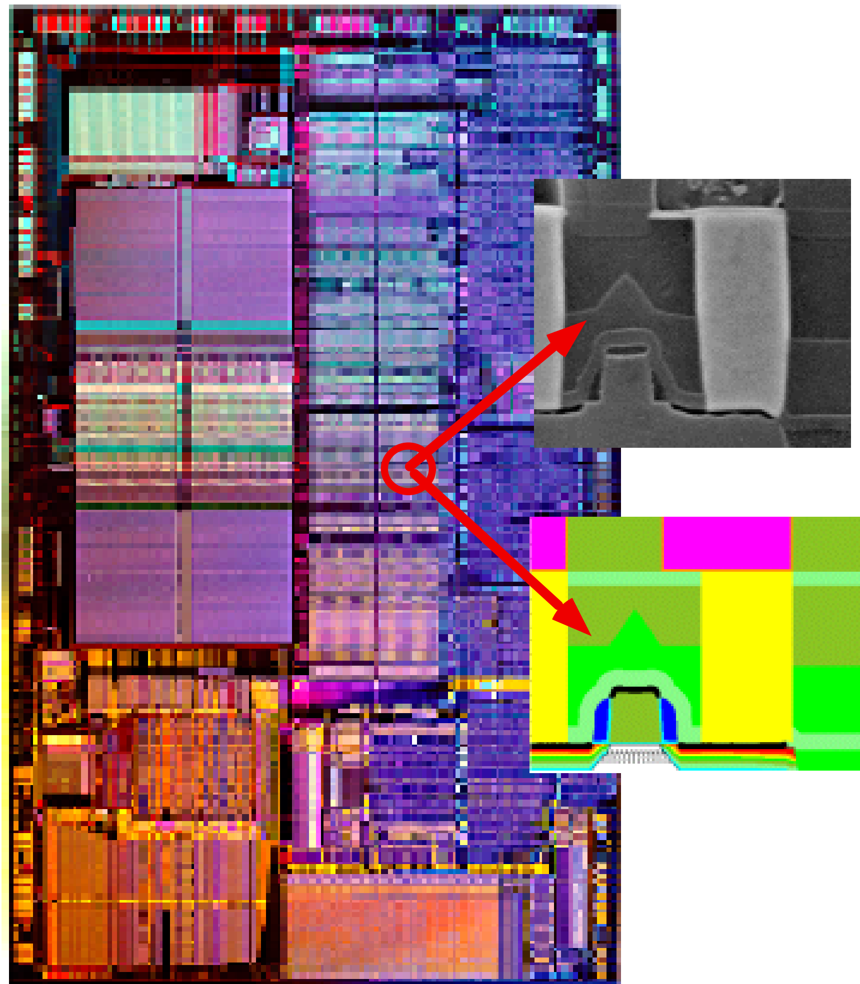
KTH VETENSKAP OCH KONST

Lecture 1
Introduction and technology roadmap



- Introduction to IH2655
- Brief historic overview
- Moore's Law and the ITRS Roadmap
- From Geometrical to Material-based scaling
- CMOS Process Flow

Course PM

Subject: Advanced course of the physical and technological concepts used in modern CMOS and bipolar/BiCMOS fabrication.

Prerequisites: Semiconductor Devices (IH1611) or Semiconductor Theory and Device Physics (IH2651) or equivalent knowledge in semiconductor device physics.

Course content: 24 h lectures week 3-10 (see Daisy schedule).

Approximately 8 h laboratory exercises (2 labs), to be scheduled in groups of 4-5.

Language: English

Course PM cont'd

Lecturer and Course Director: Prof. Mikael Östling, Division of Integrated Devices & Circuits (EKT), School of ICT, KTH.
E-mail: ostling@kth.se, phone: 08-790 4301

Lectures will also be given by: Dr Christop Henkel 08-790 4177, chenkel@kth.se and Assoc. prof Gunnar Malm, gunta@kth.se, 08-790 4332, same department

Laboratory asisstants are Ms Maryam Olyaei, olyaei@kth.se and Mr Sam Vaziri, vaziri@kth.se, same department.

Literature: Plummer, Deal and Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling*. Prentice-Hall 2000, ISBN 0-13-085037-3. (725 kr THS Bookstore in Kista)

Examples from other VLSI books and journal articles

Strong Suggestion: Read chapters before class – Concept Tests will help you much more

Examination: Two written lab reports on time and 1 h Oral examination.

Signup sheets for labs and exam through Daisy.

Course PM cont'd

NOTE: LAB REPORTS ARE DUE ONE WEEK AFTER THE LAB!

IF YOUR LAB REPORT IS LATE YOUR MAXIMUM GRADE IS E

Individual laboratory reports are required and please observe that any signs of plagiarism will directly be reported to the Disciplinary board

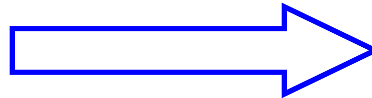
Schedule

#	Date	Time	Room	Subject
1	17-Jan	13-15	Ka431	Introduction. Technology roadmap. Overview of fabrication flow
2	18-Jan	10-12	Ka431	Wafer fabrication and silicon epitaxy.
3	23-Jan	13-15	Ka431	Wafer clean and wet processing, Screening of "Silicon Run" DVD: fabrication process,
	25-Jan	13-15		NO LECTURE
4	30-jan	13-15	Ka431	Electrical characterization. (G Malm)
5	1-Feb	10-12	Ka431	Oxidation of silicon (C Henkel)
6	8-Feb	10-12	Ka431	Annealing (FA & RTA) Diffusion and ion implantation, (C Henkel)
7	10-Feb	10-12	Ka431	Deposition of dielectrics and metal gate stacks (C Henkel)
8	15-Feb	10-12	Ka431	Dry etching (C Henkel)
9	17-Feb	13-15	Ka431	Microlithography
10	21-Feb	13-15	Ka431	Thin film deposition / Back-end processing
11	22-Feb	10-12	Ka431	Process integration: MOS and Bipolar (C Henkel)
12	28-Feb	13-15	Ka431	Nanostructures / nanophysics
	29-Feb	10-12		NO LECTURE
13	5-Mar	13-15	Ka431	Reserve time (prel no lecture)
13	7-Mar	13-15	Ka431	Reserve time (prel no lecture)

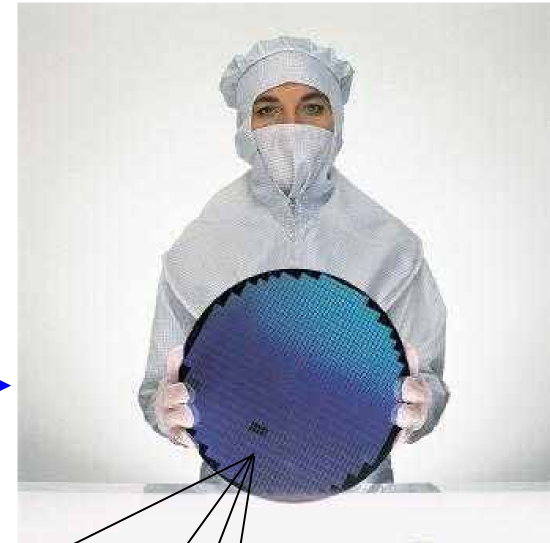
Microelectronic processing

Clean room environment

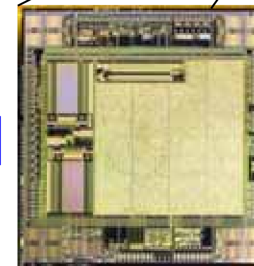
Source: Infineon



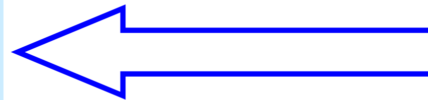
Wafer level

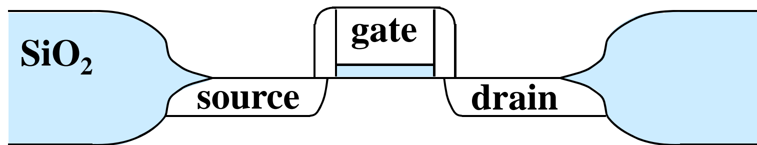


Source: Infineon



Chip level

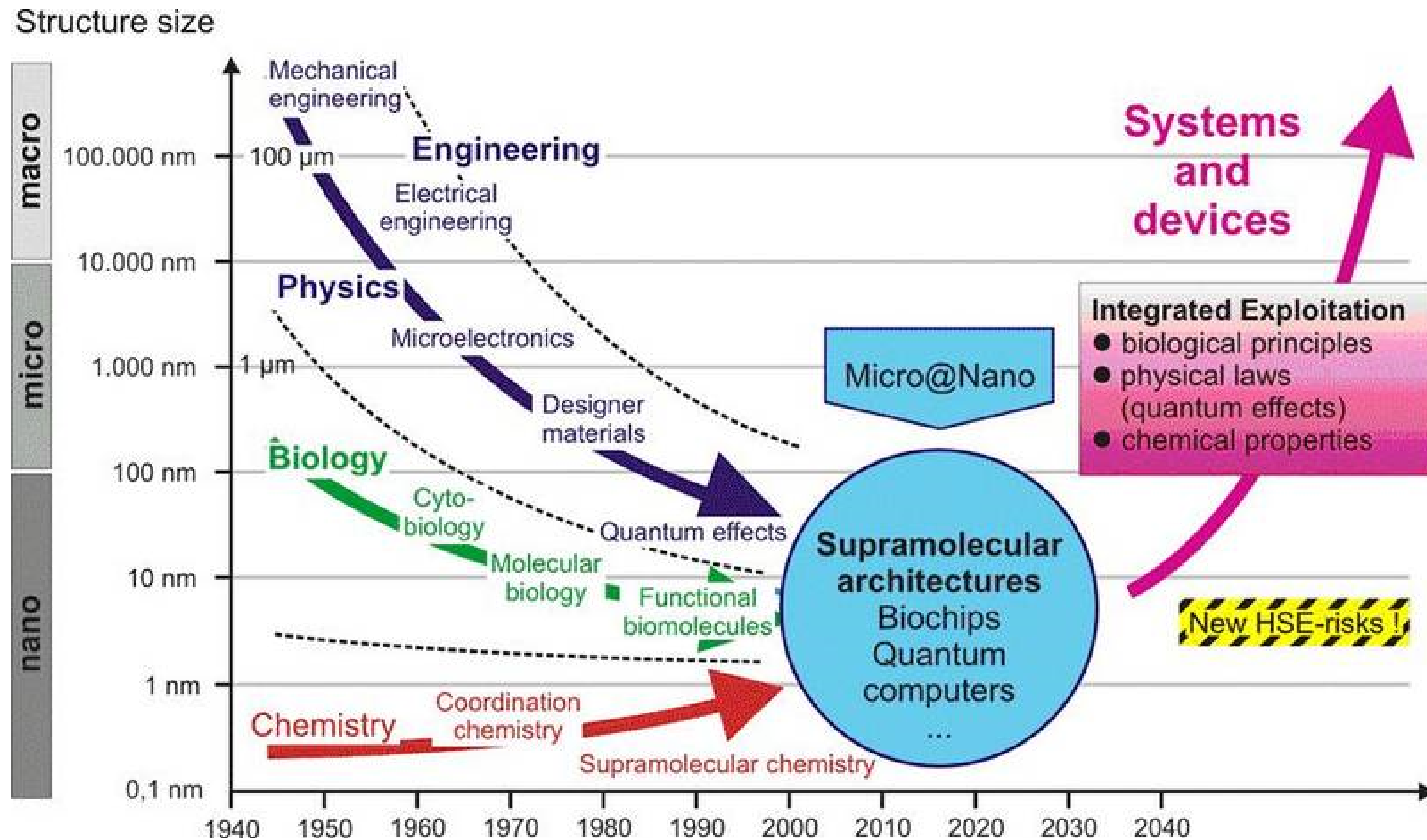




Transistor level

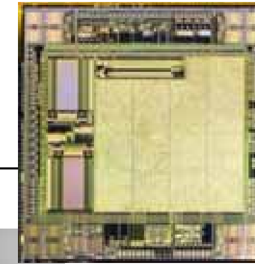
…so why should you care if you plan to work in Nanoscience, MEMS, PV or Photonics?

Top down AND Bottom Up

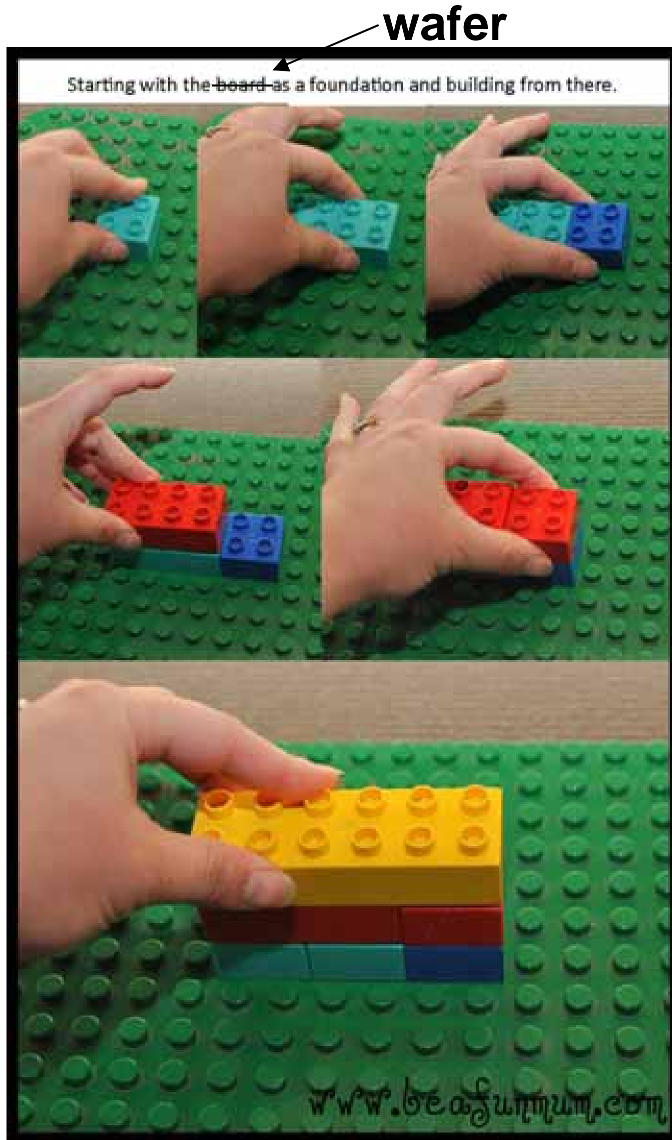


Source: website Univ. Wien

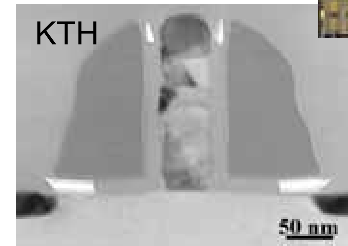
IH2655: Lego for grown-ups



wafer



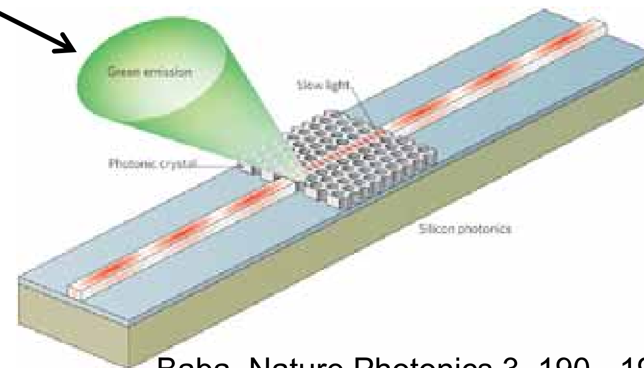
Silicon MOSFET



Graphene and CNTs

Photovoltaics

Photonics



Baba, Nature Photonics 3, 190 - 192 (2009)

IH2655 Aim

This course is about the process technology used to ***manufacture semiconductor devices***. It aims to familiarize with the related ***technical vocabulary*** and to provide the students with a ***tool kit of fabrication methods*** for a range of devices.

After the course the student should be able to

describe the technological processes involved in the fabrication of nano- and microelectronic devices and circuits

compare alternative fabrication methods

apply the knowledge to specific device requirements through careful ***selection*** among a number of choices

assess pros and cons of different fabrication methods

combine fabrication methods to ***develop*** complex process flows for functional devices and circuits in a range of applications (e.g. transistors, solar cells, optoelectronics...)

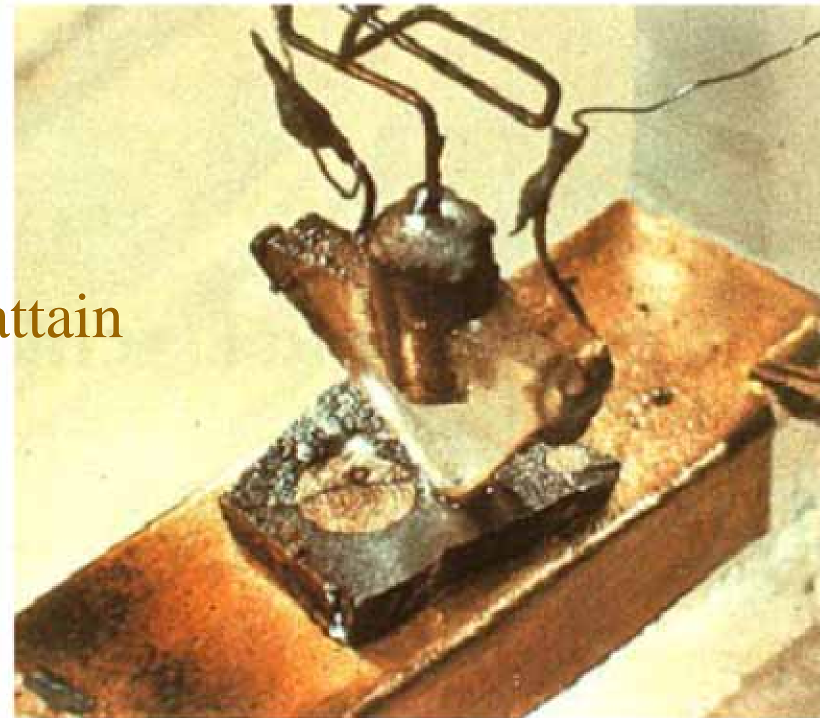
- Introduction to IH2655
- Brief historic overview
- Moore’s Law and the ITRS Roadmap
- From Geometrical to Material-based scaling
- CMOS Process Flow

Brief retrospect：A great invention based on Sciences

- **Bardeen, Brattain, Shockley**, First Ge-based bipolar transistor invented 1947, Bell Labs. **Nobel prize 1956**
- **Atalla**, First Si-based MOSFET invented 1958, Bell Labs.
- **Kilby** (TI) & **Noyce** (Fairchild), Invention of integrated circuits 1959, **Nobel prize**
- Planar technology, **Jean Hoerni**, Fairchild, 1960
- First CMOS invented early 1960's
- "**Moore**'s law" coined 1965, Fairchild
- **Dennard**, scaling rule presented 1974, IBM
- First Si technology roadmap published 1994, USA

Bardeen, Brattain, Shockley, First Ge-based bipolar transistor invented 1947, Bell Labs. **Nobel prize 1956**

1st point contact transistor -- by Bell Lab



(Reprinted with permission of Lucent Technologies).

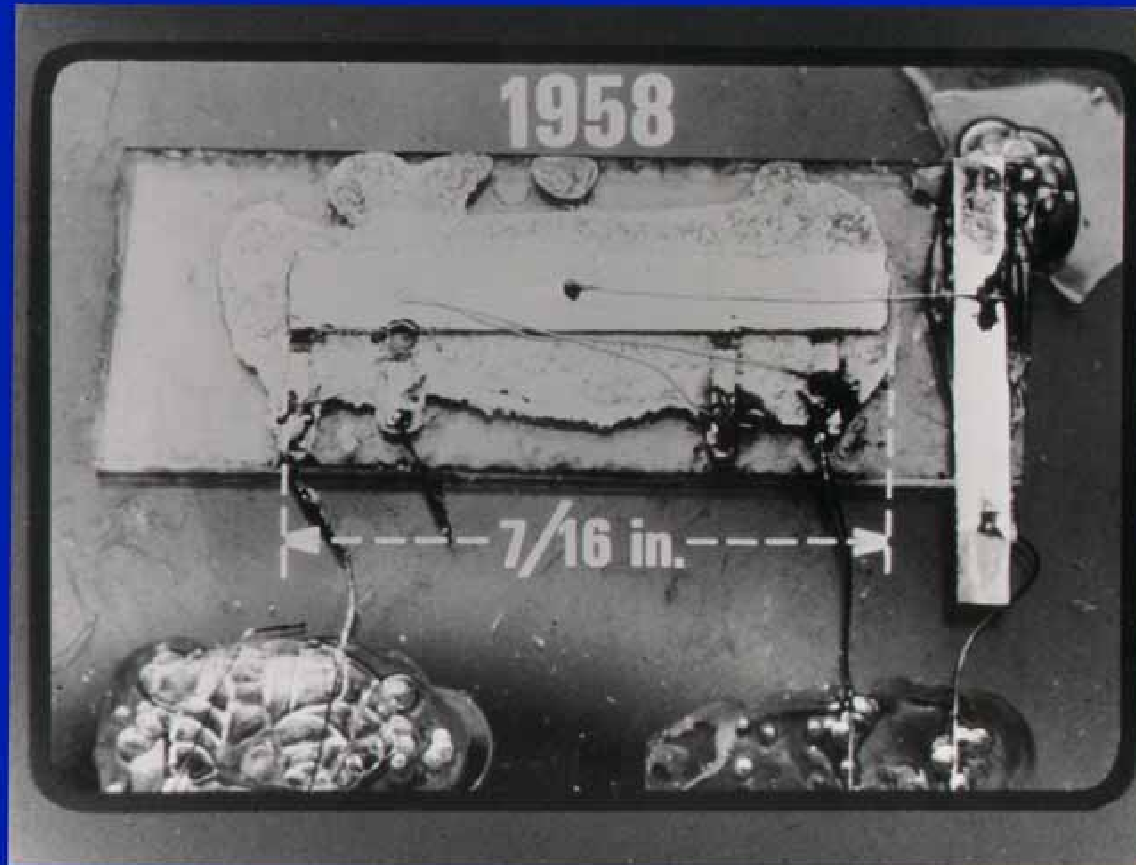
Polycrystalline Ge
1956 Nobel Physics Prize

Transistor=transfer + resistor
--Transferring electrical signal across a resistor

Kilby (TI) & **Noyce** (Fairchild), Invention of integrated circuits 1959, **Nobel prize**

FIRST INTEGRATED CIRCUIT BY J. S. KILBY

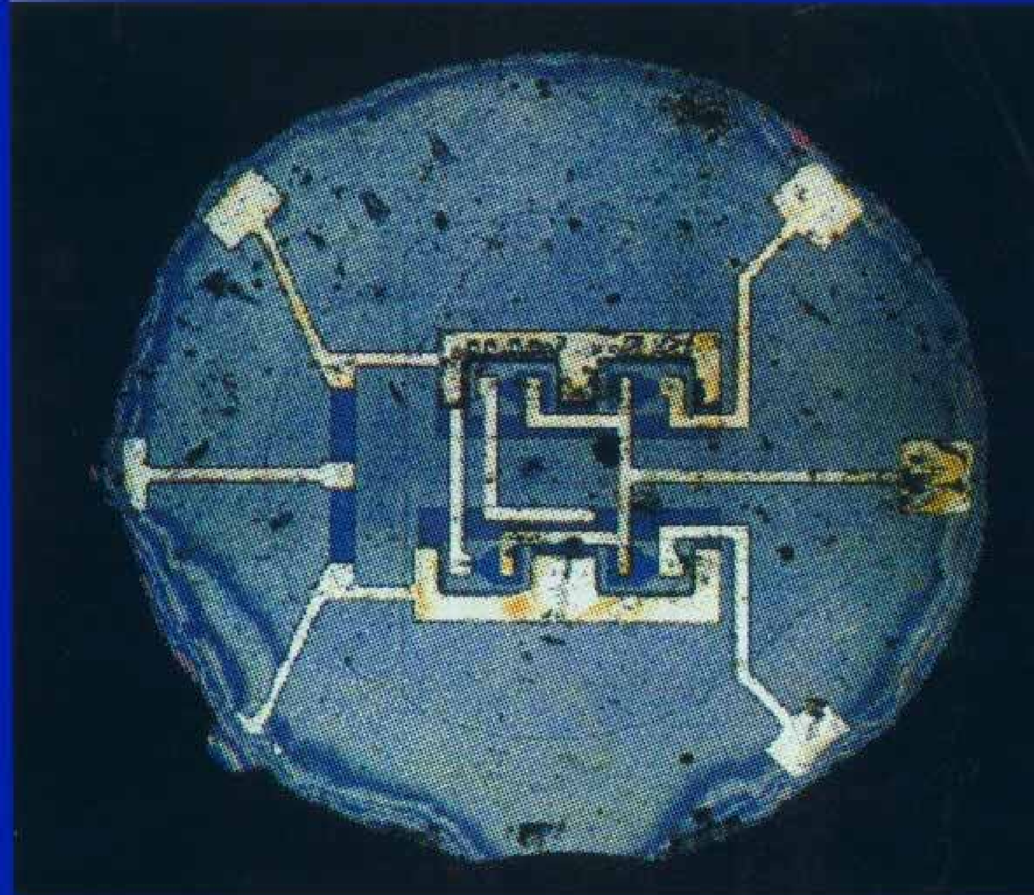
(US Patent 3,138,763 filed Feb. 1959, granted 1964)



Kilby (TI) & **Noyce** (Fairchild), Invention of integrated circuits 1959, **Nobel prize**

FIRST MONOLITHIC IC BY R. N. NOYCE

(US Patent 2,981,877 filed July 1959, granted 1961)



This marked the start of an amazing development -> Increasing integration of components

Planar technology, **Jean Hoerni**, Fairchild, 1960

Planar process

Invented by Jean Hoerni at Fairchild Semiconductor (late 50's)

April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 2

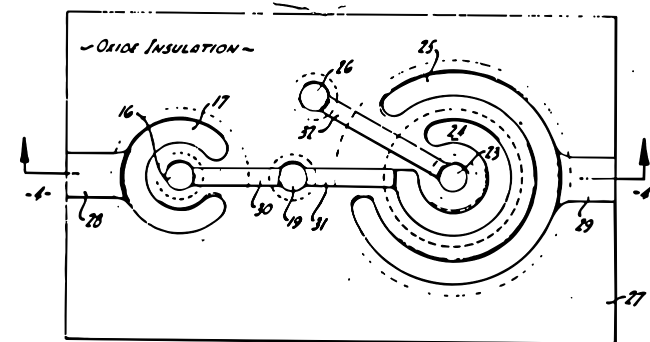


FIG. 3

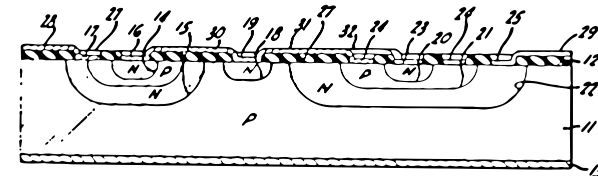


FIG. 4

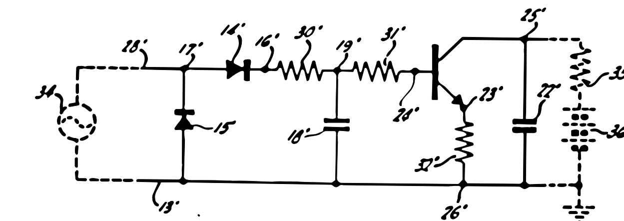


FIG. 5

INVENTOR.
ROBERT N. NOYCE
BY Lippincott & Ralls

((

Dennard, scaling rule presented 1974, IBM

NMOS technology

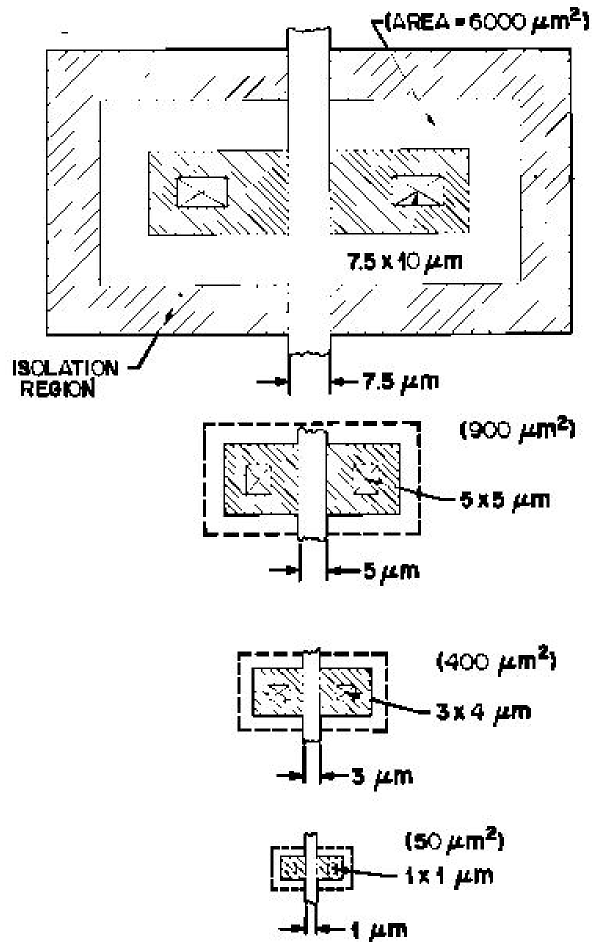


Fig. 13 Reduction in the area of MOSFET as the gate length (minimum feature length) is reduced.[8]

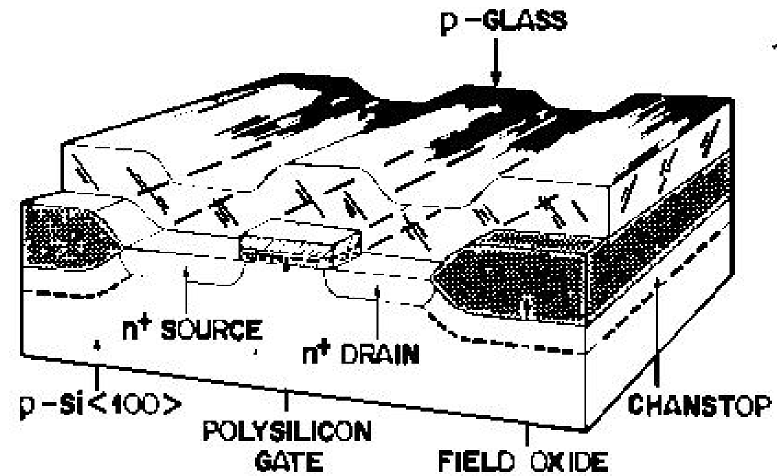


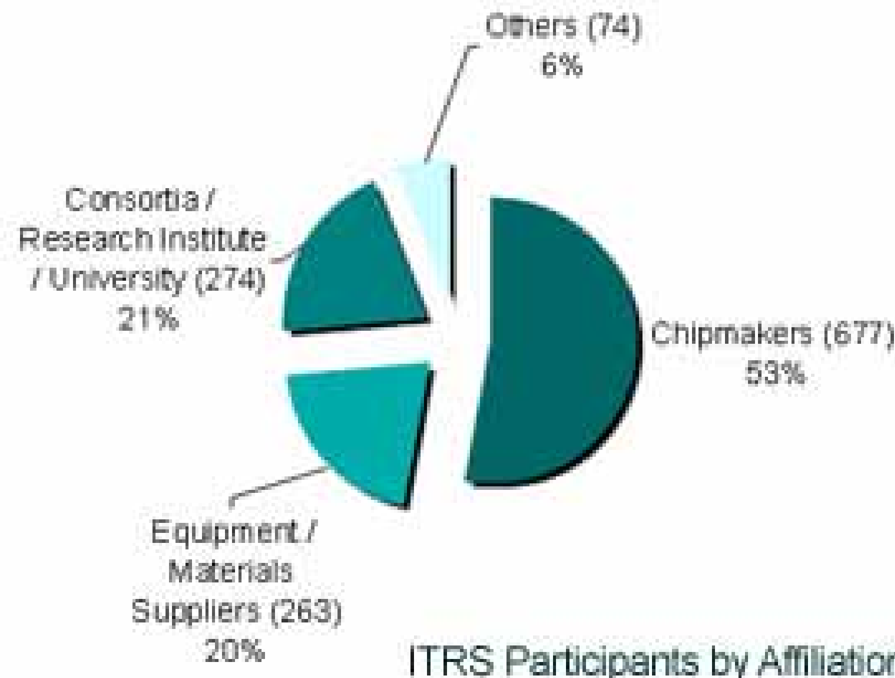
Fig. 14 Perspective view of an n-channel MOSFET.[9]

First Si technology roadmap published 1994, USA

Started by Semiconductor Industry Association (SIA) in USA
1994: creation of an American style roadmap
The National Technology Roadmap for Semiconductors (NTRS)

1998, the SIA became closer to its European, Japanese, Korean and Taiwanese counterparts by creating the first global roadmap
The International Technology Roadmap for Semiconductors (ITRS).

Today: Over 1000 companies and research institutions



ITRS Participants by Affiliation

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Teams for:

- System Drivers
- Design
- Test & Test Equipment
- Process Integration, Devices, & Structures
- RF and A/MS Technologies for Wireless Communications
- Emerging Research Devices
- Emerging Research Materials
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly & Packaging
- Environment, Safety, & Health
- Yield Enhancement
- Metrology
- Modeling & Simulation

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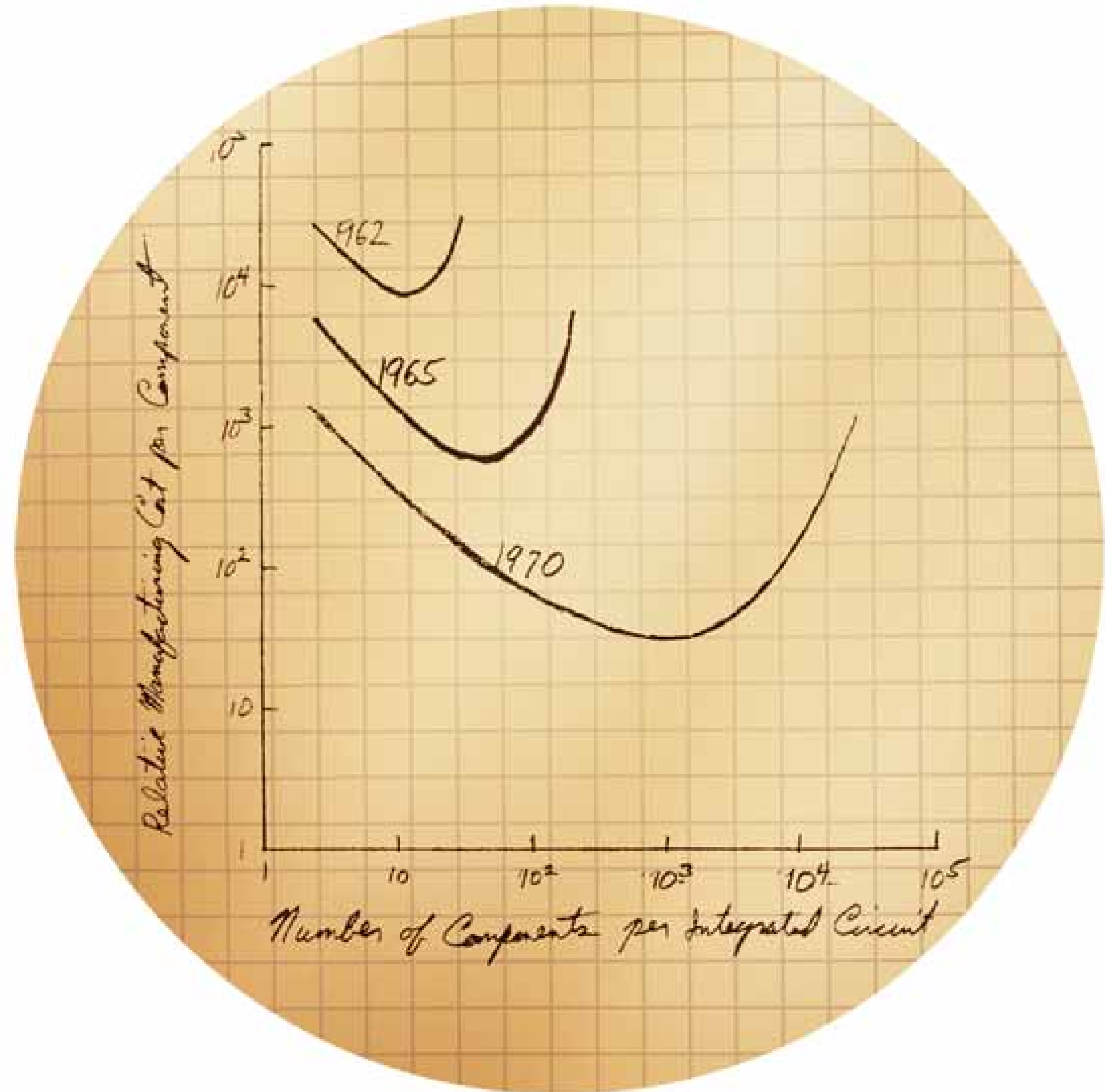
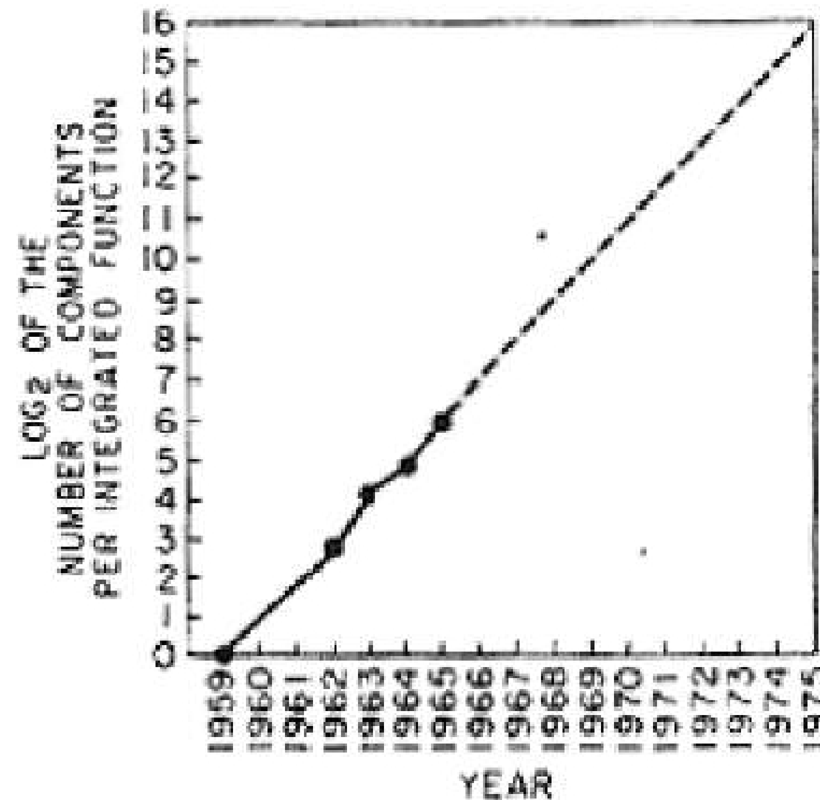
“**Moore**’s law”: coined 1965, Fairchild

Gordon Moore’s original
Ideas in 1965

Source; Intel



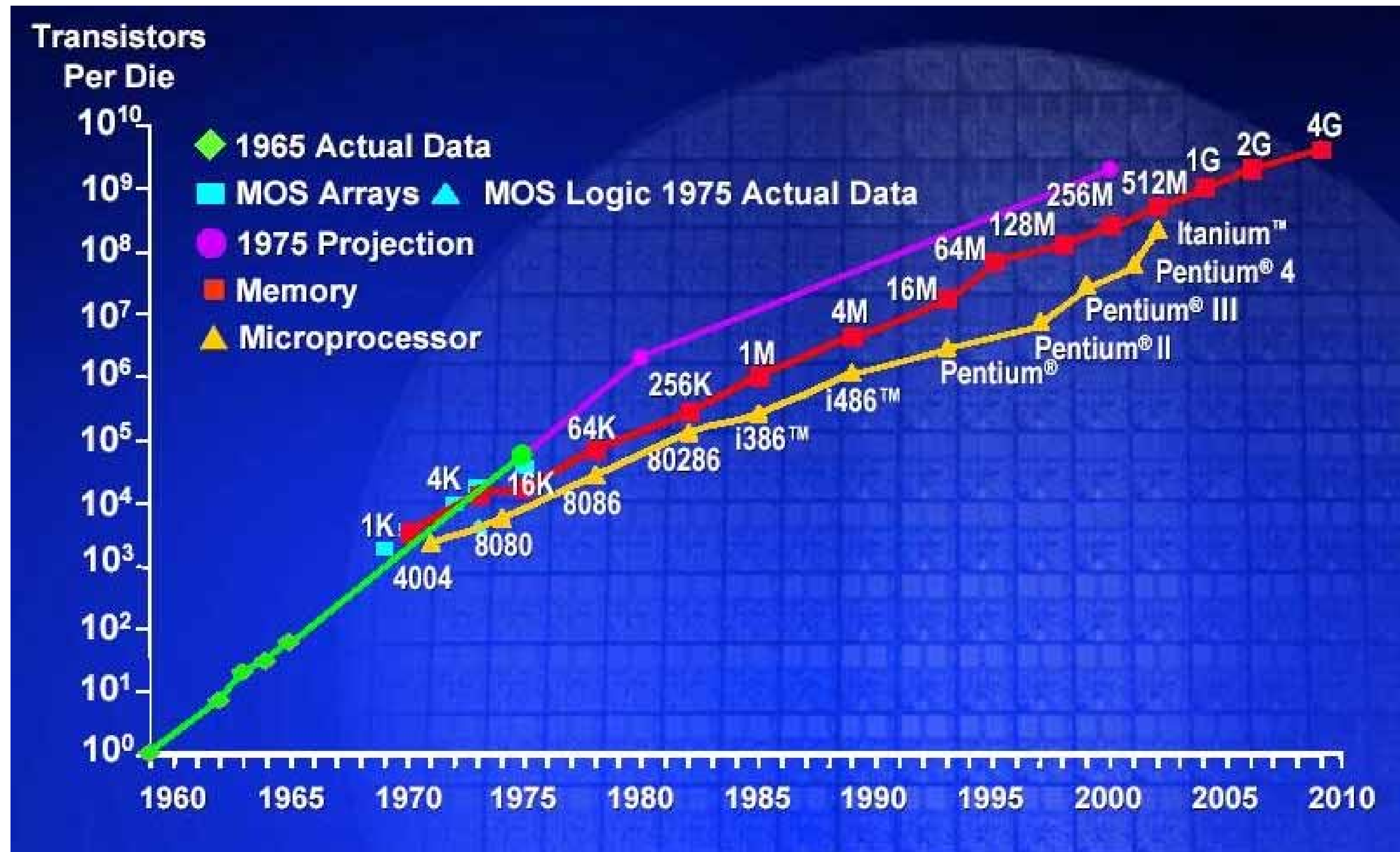
“**Moore**’s law”: coined 1965, Fairchild



1965: Components per „integrated function“

Source: G.E. Moore, Cramming more components onto integrated circuits, Electronics, Volume 38, Number 8, April 19, 1965

“**Moore**’s law”: rewritten in 1975, INtel



1975: Transistors per chip. Basis: Exponential behavior…

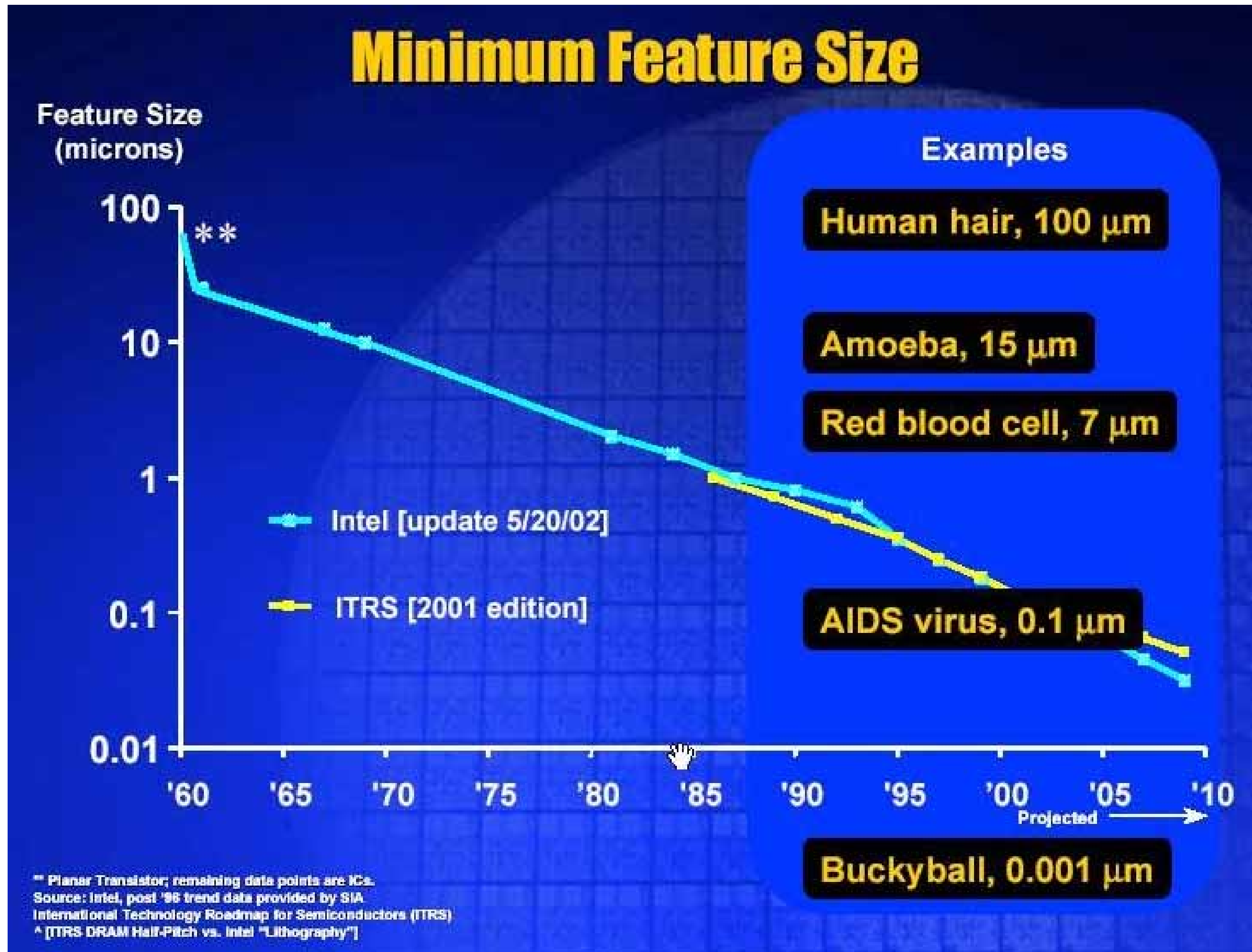
Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

“**Moore**’s law”: the real motivation

... Driven by $$$...

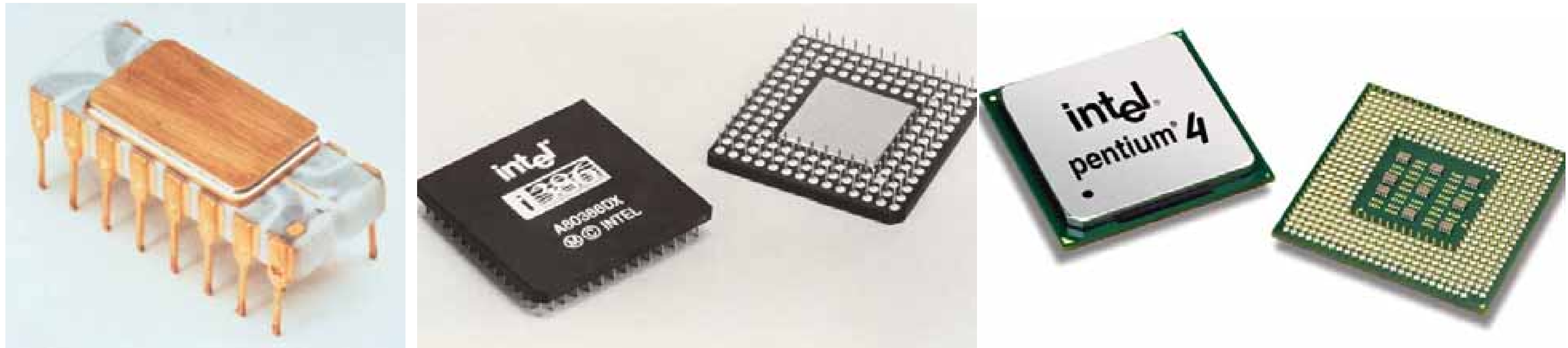
Source: G.E. Moore, No exponential is forever..., ISSCC, February 2003

“**Moore**’s law”: enabled by scaling



Source: G.E. Moore, No exponential is forever..., ISSCC, February 2003

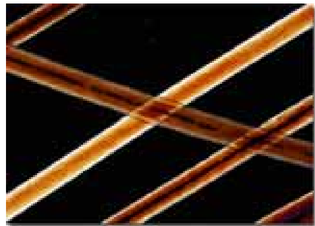
“**Moore**’s law”: enabled by scaling

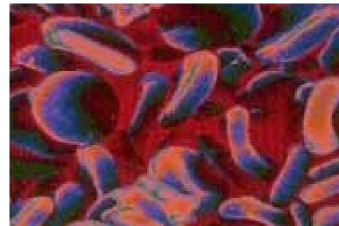


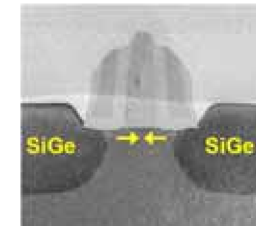
4004 386 Pentium 4

10 µm **1 µm** **0.1 µm**

Human hair **Red blood cell** **Bacteria** **Virus** **MOSFET**







“**Moore**’s law”: enabled by scaling

MOSFET metrics provide additional advantage

A simple model for I_{Don} is given by the MOSFET ***“Square-Law” Equation:***

$$\mathbf{I_{Don} = (W/L)\,(\mu\varepsilon_{ox}/t_{ox})\,(V_{GS} - V_T)^2}$$

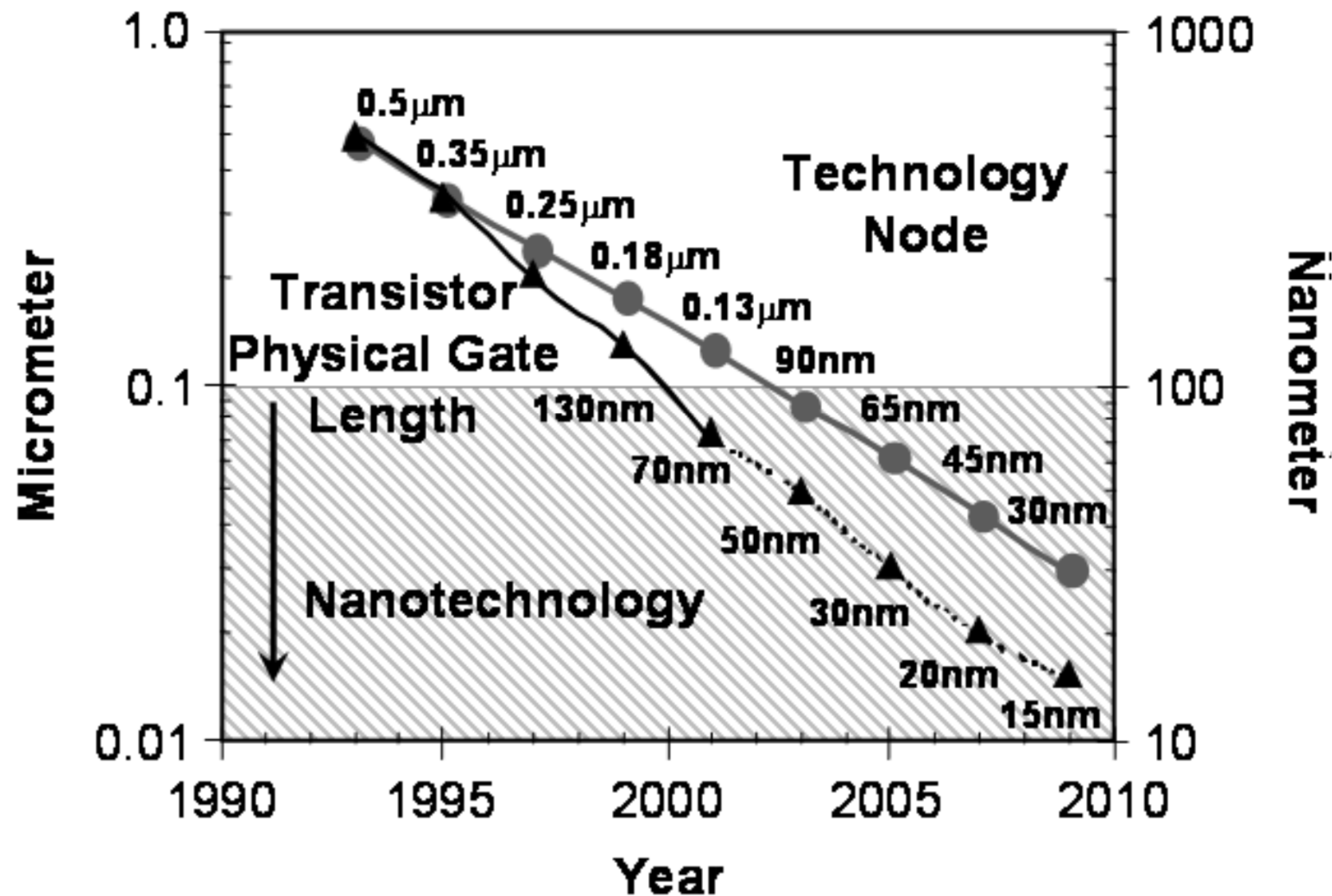
Chips are faster if the gate length L is reduced

“**Moore**’s law”: enabled by scaling

IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 4, NO. 2, MARCH 2005 , p153

Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications

Robert Chau *et al*

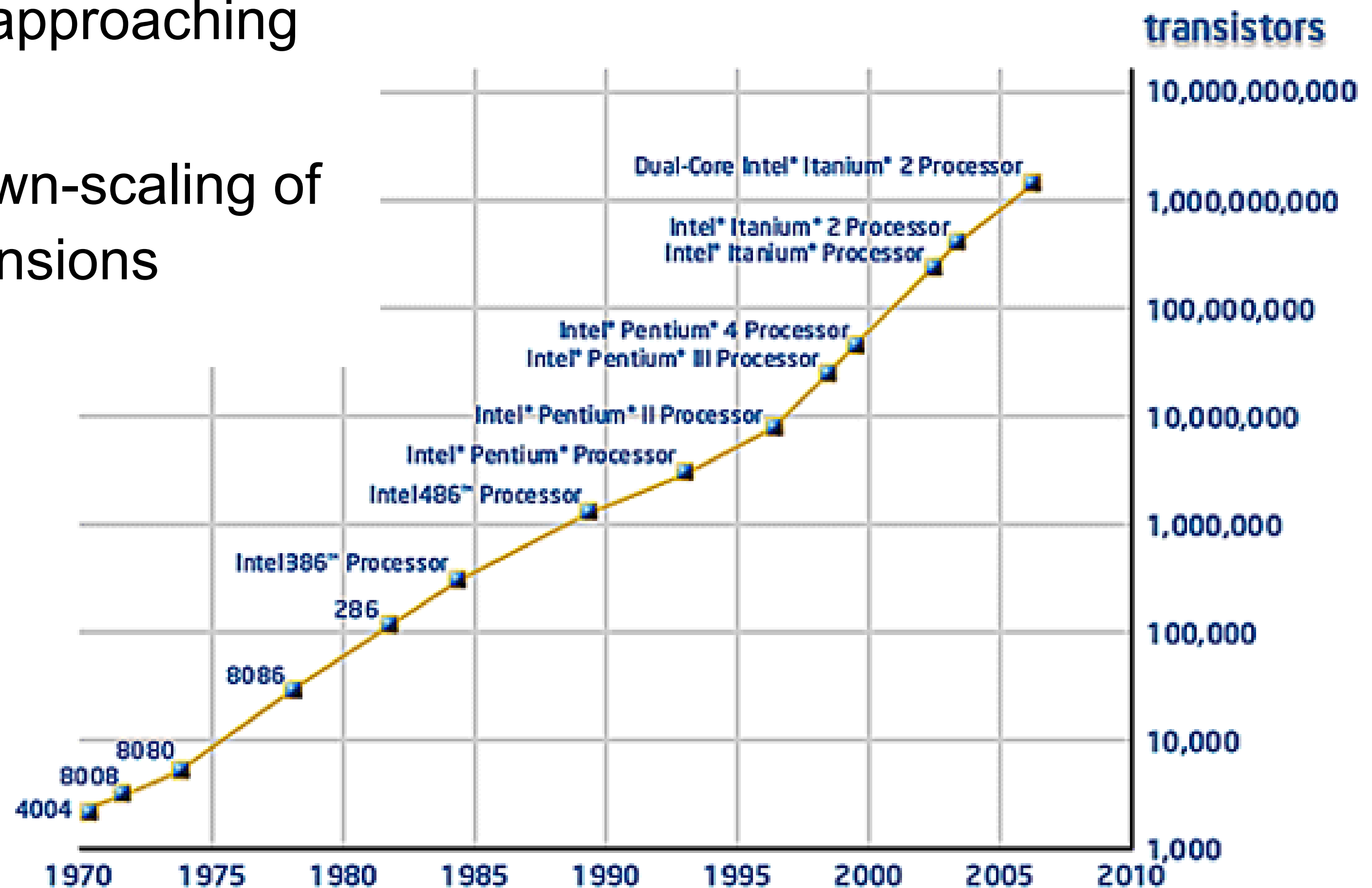


“**Moore**’s law”: still going strong in 2010

Transistors are found in processors, memories etc.

Number of transistors grows exponentially, approaching 1,000,000,000!

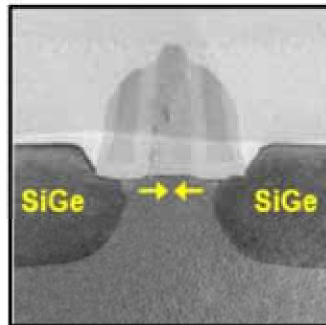
Continuous down-scaling of transistor dimensions

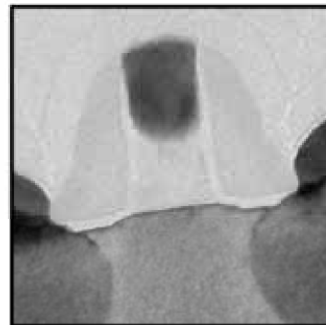


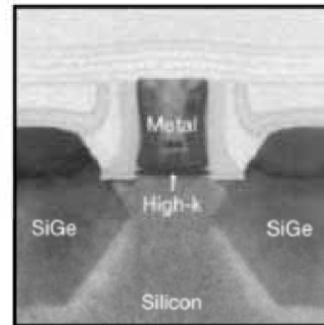
Source: Intel

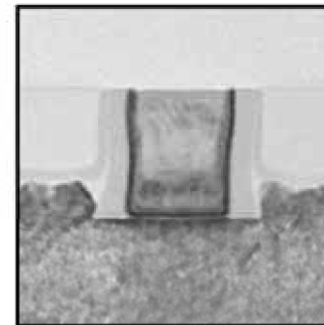
Intel Transistor Leadership

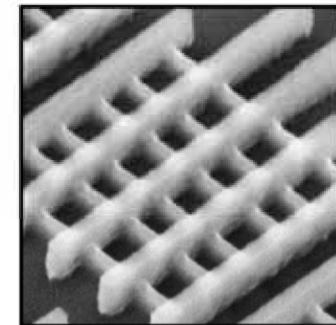
2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm











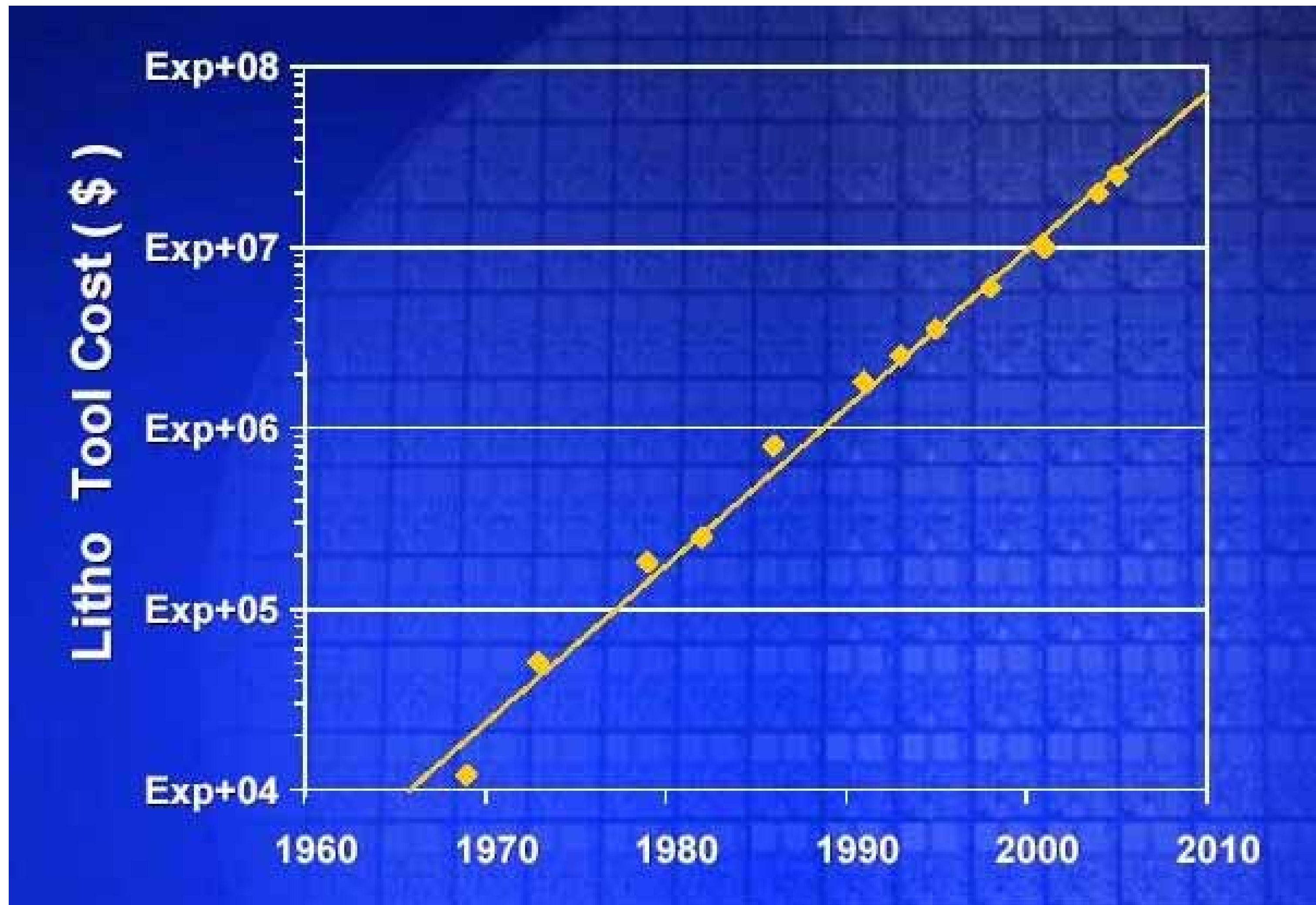
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon →

High-k Metal Gate →

Tri-Gate →

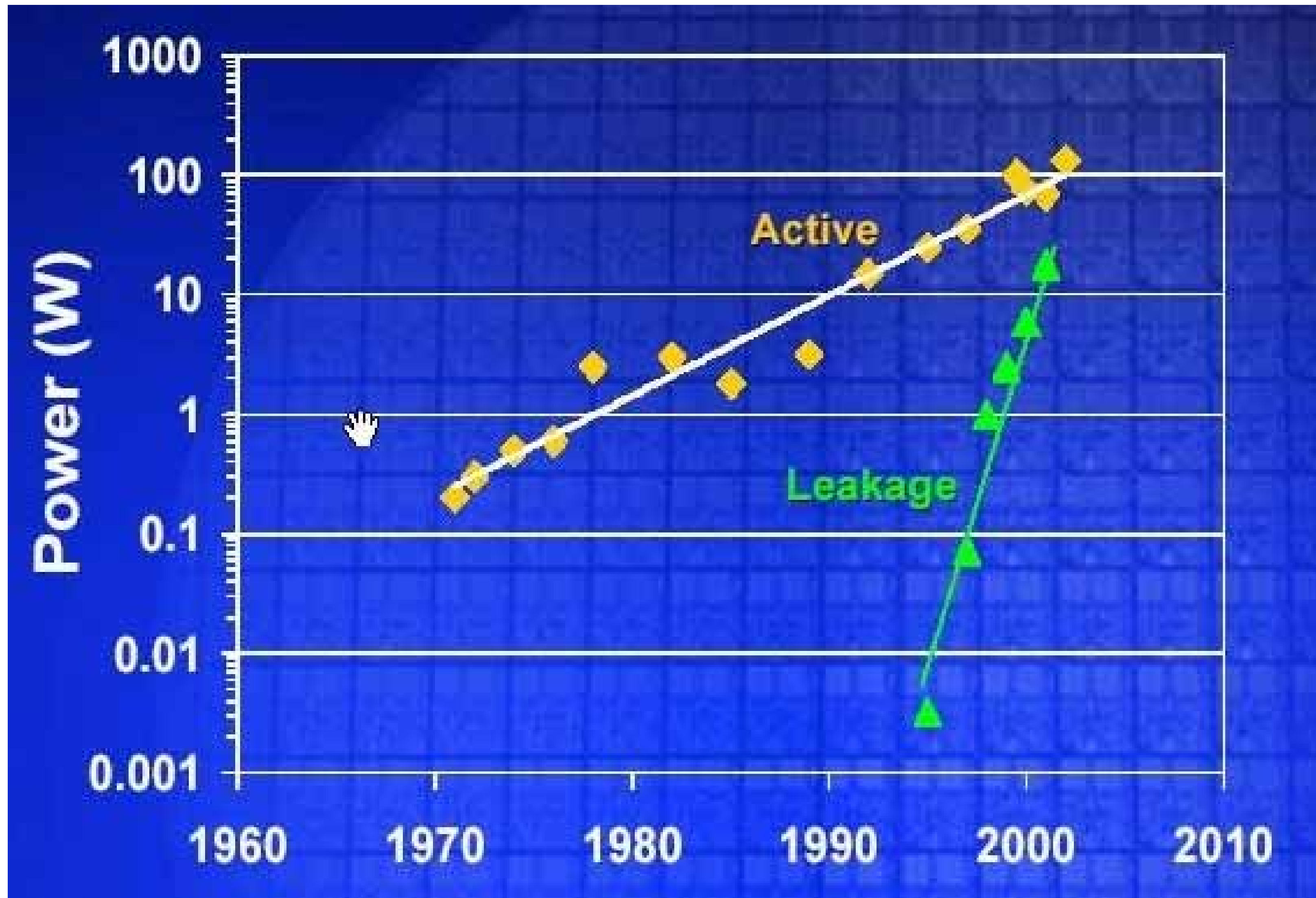
“**Moore**’s law”: However! (or: The notorious „e“)



Costs are rising exponentially, too!!!

Source: G.E. Moore, No exponential is forever..., ISSCC, February 2003

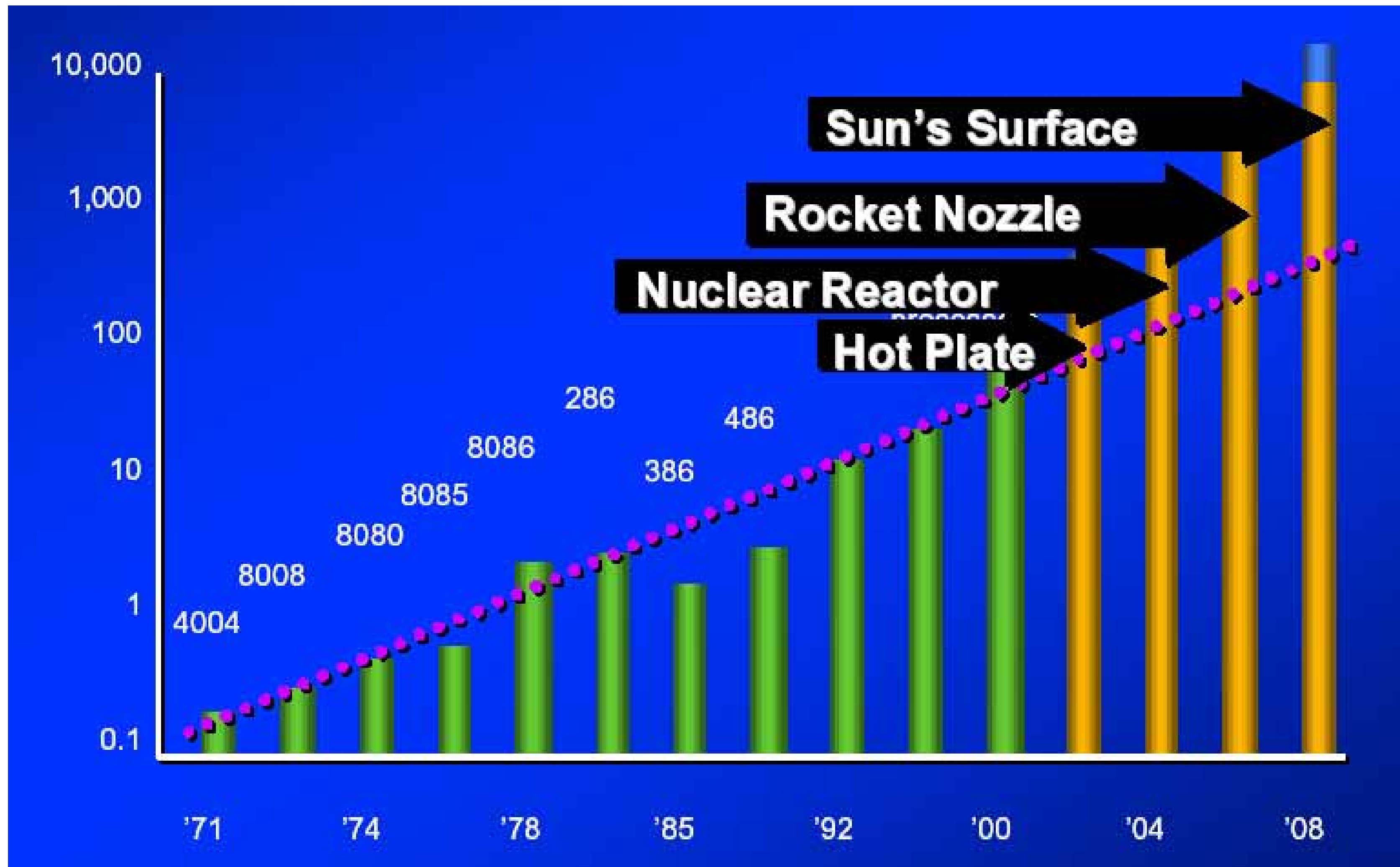
“**Moore**’s law”: …and its consequences



…limited by power dissipation ???

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

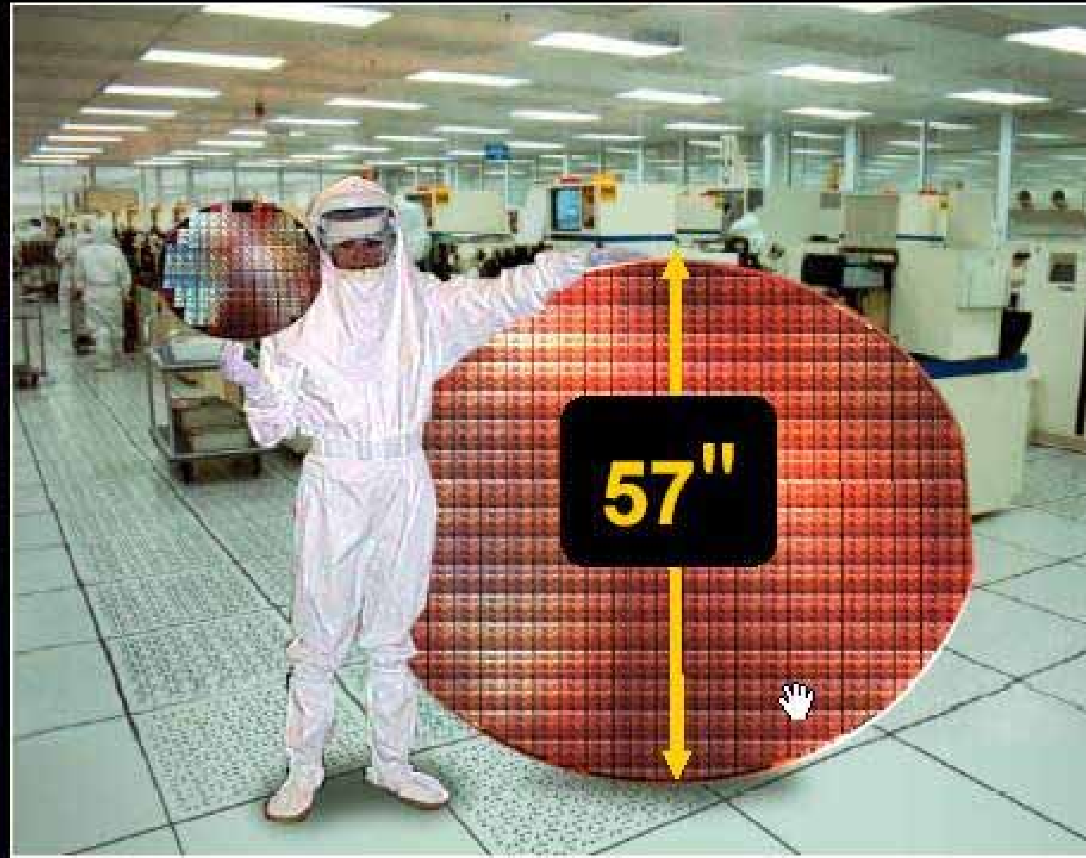
“**Moore**’s law”: …and its consequences



Yes, if $\dot{P}$ continues exponentially !

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

“**Moore**’s law”: …not



Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

ITRS Roadmap – Moore's Heirs

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- •Design
- •Test & Test Equipment
- •Process Integration, Devices, & Structures
- •RF and A/MS Technologies for Wireless Communications
- •Emerging Research Devices
- •Emerging Research Materials
- •Front End Processes
- •Lithography
- •Interconnect
- •Factory Integration
- •Assembly & Packaging
- •Environment, Safety, & Health
- •Yield Enhancement
- •Metrology
- •Modeling & Simulation

ITRS Roadmap

Moving Closer to the "Red Brick Wall"

2001 Results

Challenges/Opportunities for Semiconductor R&D

Year of Production:	2001	2003	2005	2007	2010	2016
DRAM Half-Pitch [nm]:	130	100	80	65	45	22
Overlay Accuracy [nm]:	46	35	28	23	18	9
MPU Gate Length [nm]:	90	65	45	35	25	13
CD Control [nm]:	8	5.5	3.9	3.1	2.2	1.1
T_{OX} (equivalent) [nm]:	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.5
Junction Depth [nm]:	48-95	33-66	24-47	18-37	13-26	7-13
Metal Cladding [nm]:	16	12	9	7	5	2.5
Inter-Metal Dielectric K:	3.0-3.6	3.0-3.6	2.6-3.1	2.3-2.7	2.1	1.8

2001 ITRS

IRC

- Introduction to IH2655
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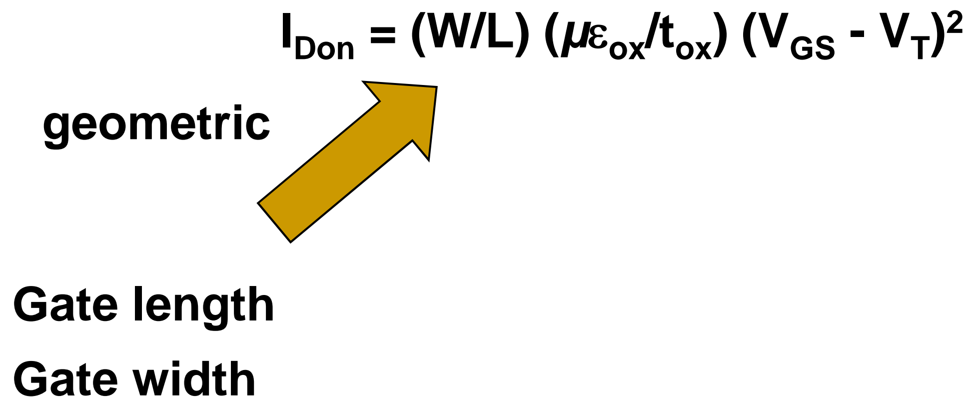
“**Moore**’s law”: scaling parameters

MOSFET metrics provide additional leverage: Materials

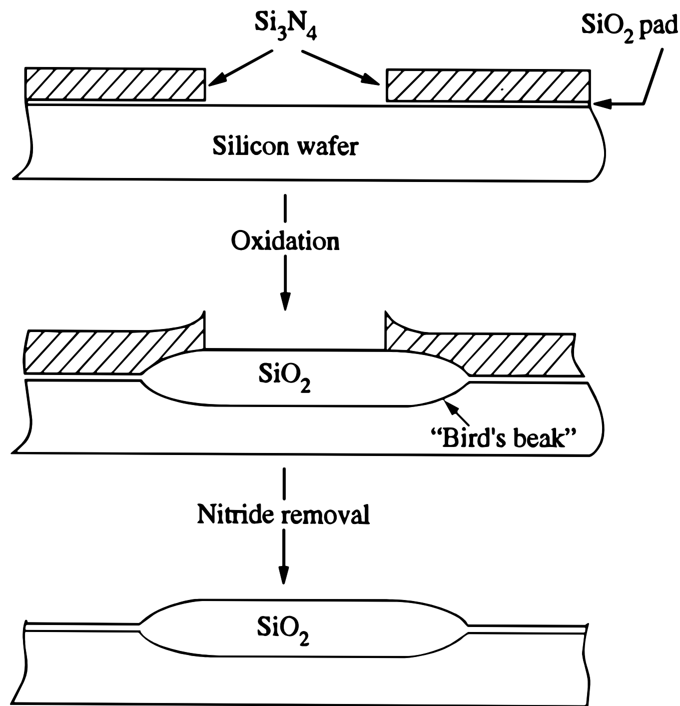
A simple model for I_{Don} is given by the MOSFET ***“Square-Law” Equation:***



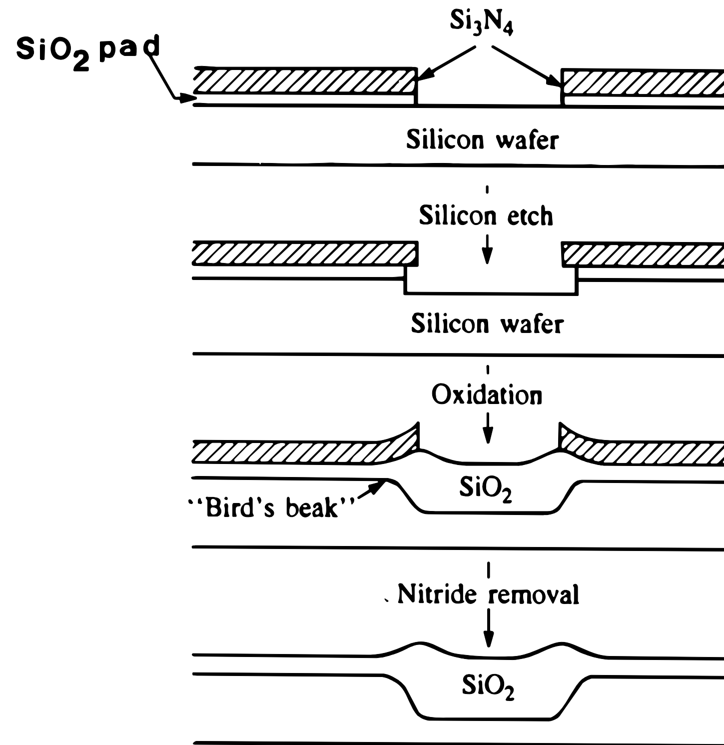
Geometric scaling is determined by improvements in process technology

Geometric Scaling: Isolation modules 1/2

LOCOS (semirecessed)



Recessed oxidation (ROX) (fully recessed)



Pros: **Improved geometric scalability**
Higher device density

Con: **Increased process complexity**

Geometric Scaling: Isolation modules 2/2

Bird's head and beak in LOCOS and ROX exhibit 0.6 –0.4 μm encroachment

Further process technology improvements

***Shallow Trench Isolation* (STI)**

- High-density plasma fills etched and liner-oxidixed trenches with SiO_2

Deep-trench isolation

- Trench isolation can be combined with silicon-on-insulator (SOI) wafers for nearly complete device isolation

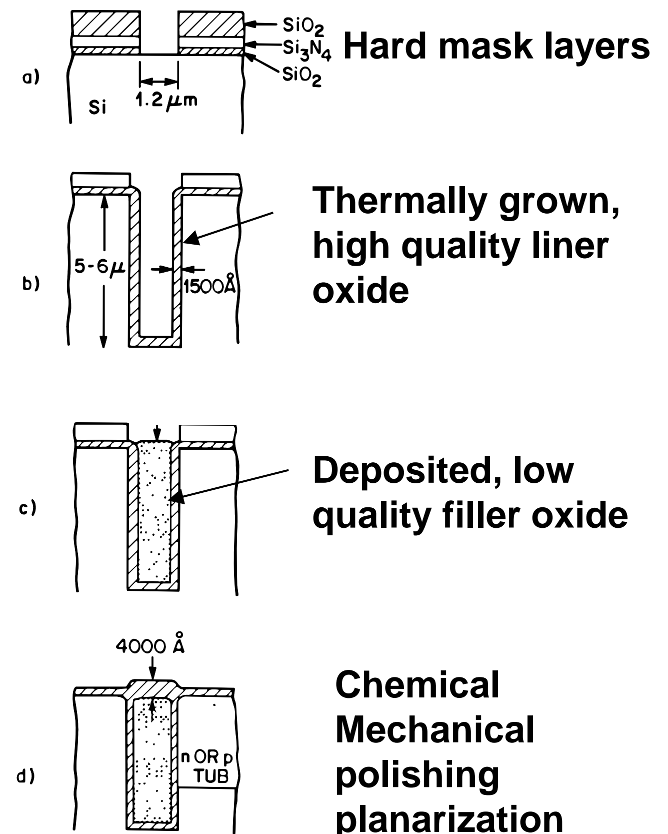
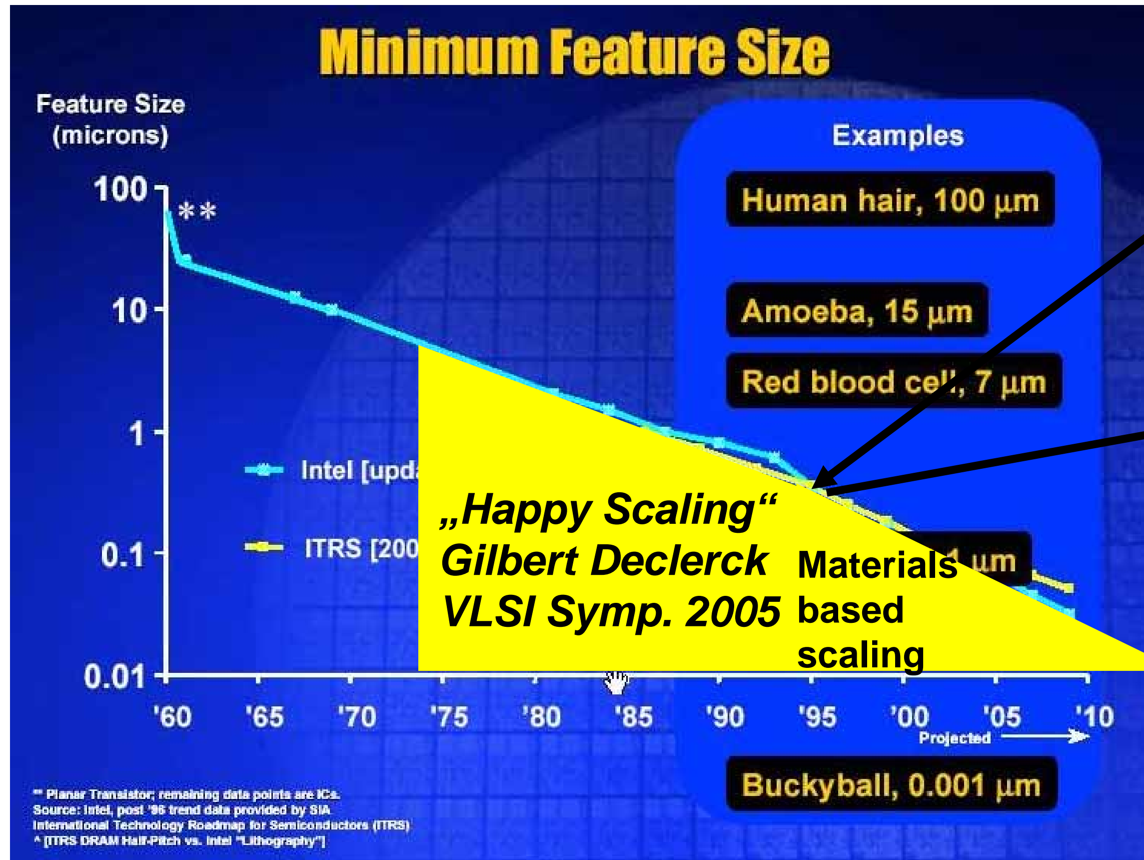


FIGURE 17
Process sequence for forming trench isolation structure for CMOS. (a) Trench mask patterning, (b) trench etching and oxide growth, (c) polysilicon deposition to fill trench, (d) oxide grown to cap trench. (*After Rung, Ref. 23.*)

“**Moore**’s law”: still going strong in 2010 – Why?

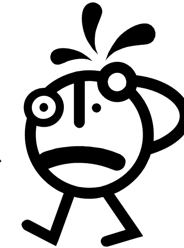


„Happy Scaling“
Gilbert Declerck
VLSI Symp. 2005

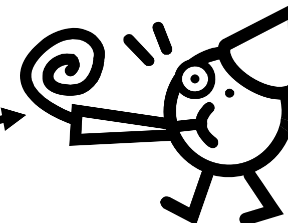
Materials based scaling

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

Industry guy



Researcher



- **SOI**
- **High-k**
- **Metal Gates**
- **Strained Silicon**
- **Germanium**
- **Carbon Nanotubes**
- **Graphene(!)**

“**Moore**’s law”: old & new scaling parameters

MOSFET metrics provide additional leverage: Materials

A simple model for I_{Don} is given by the MOSFET ***“Square-Law” Equation:***

$$I_{Don} = (W/L)\,(\mu\varepsilon_{ox}/t_{ox})\,(V_{GS} - V_T)^2$$

“old”

geometric

Gate length

Gate width

“new”

material

Mobility

Dielectric constant

Oxide thickness

All scaling parameters are determined by improvements in process technology

“**Moore**’s law”: still going strong in 2010 – Why?

Before 1990s

Since 1990s

Beyond 2005

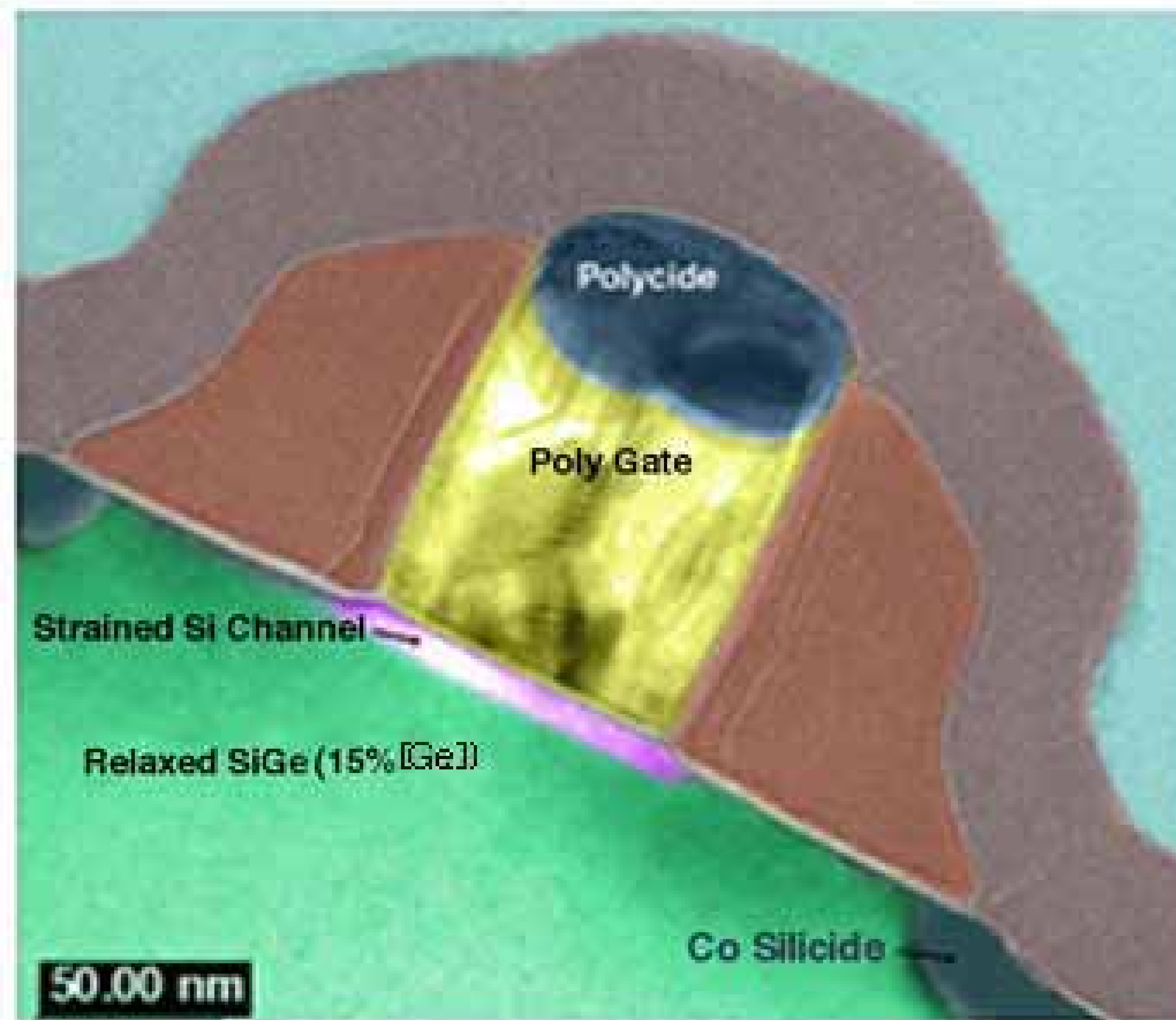
Period \ Group	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba	* 57 La	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra	** 89 Ac	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Uub	113 Uut	114 Uuq	115 Uup	116 Uuh	117 Uus	118 Uuo

* Lanthanides	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
** Actinides	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

Source: fabtech.org / Sigma Aldrich

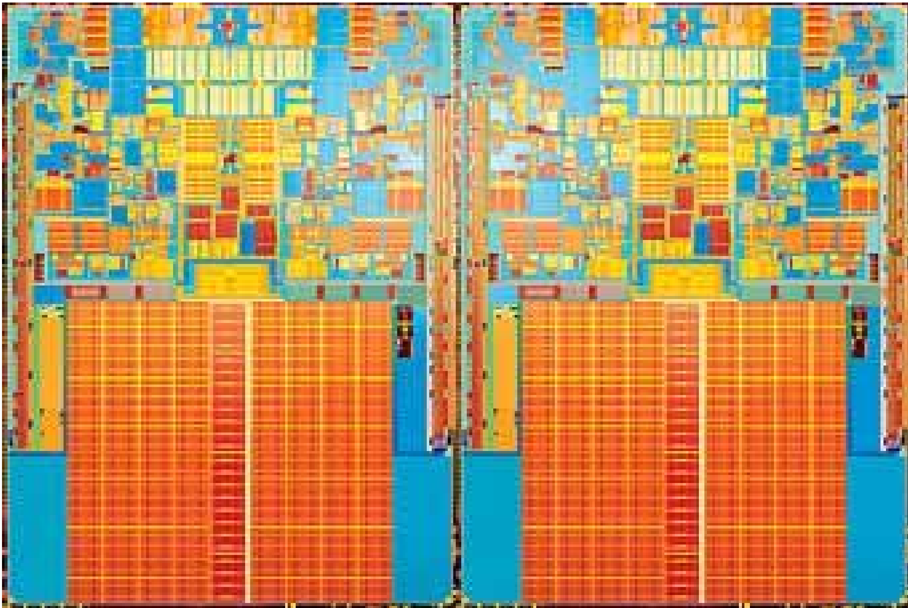
Today: New materials in connection with improvements in process technology

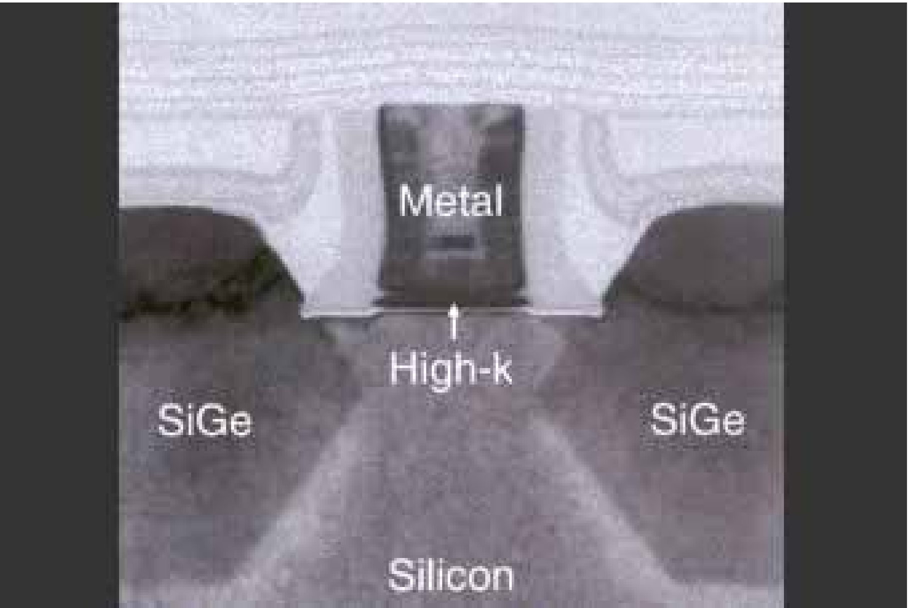
Strained silicon & SiGe



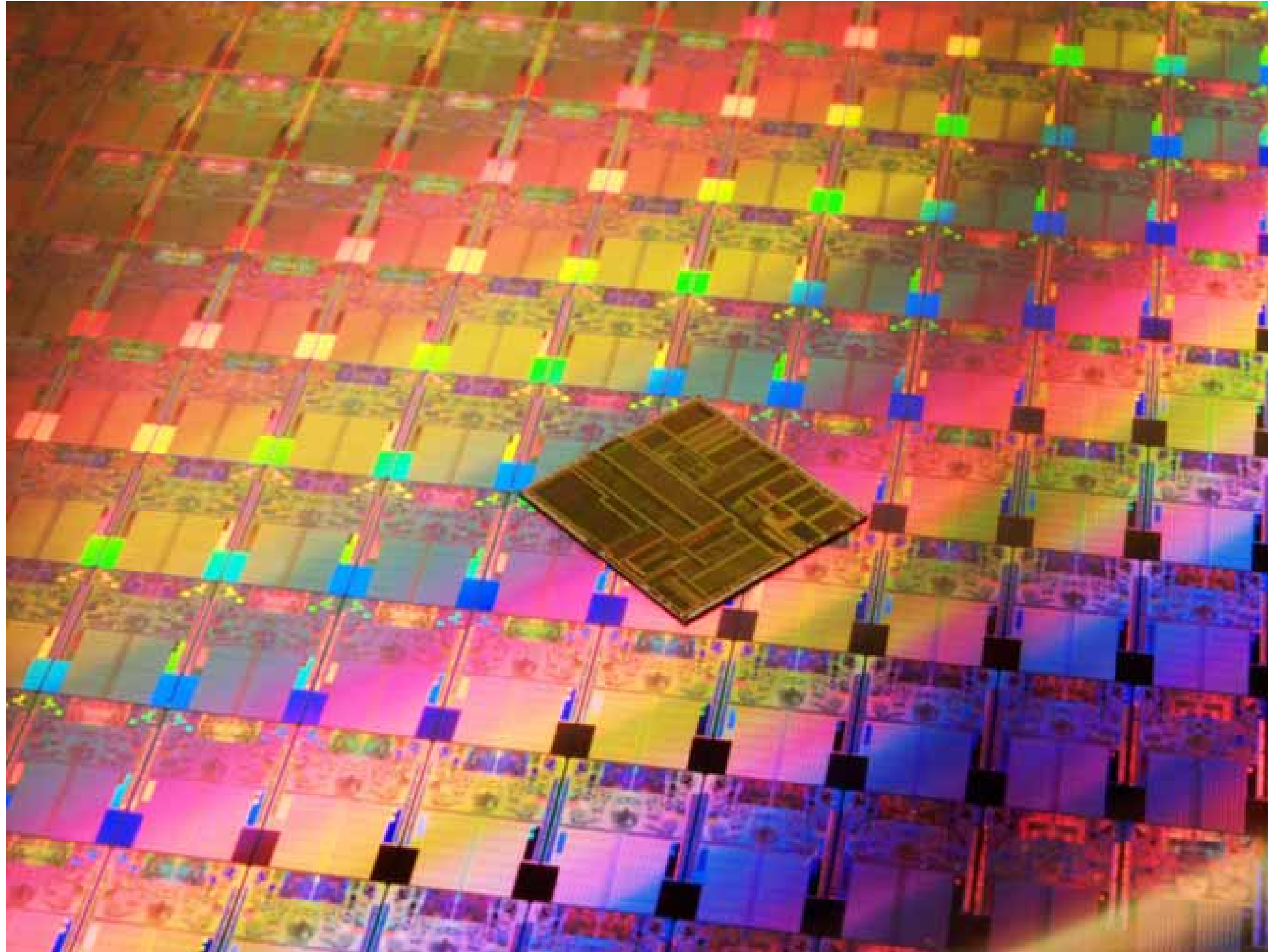
A transistor built with strained silicon. The silicon is “stretched out” because of the natural tendency for atoms inside compounds to align with one another. When is silicon is deposited on top of a substrate with atoms spaced farther apart, the atoms in silicon stretch to line up with the atoms beneath, stretching – “straining” – the silicon. In the strained silicon, electrons experience less resistance and flow up to 70 percent faster, which can lead to chips that are up to 35 percent faster – without having to shrink them. Image Reproduced with Permission of IBM Almaden Research Center, IBM.

Intel 45nm dual-core processor die





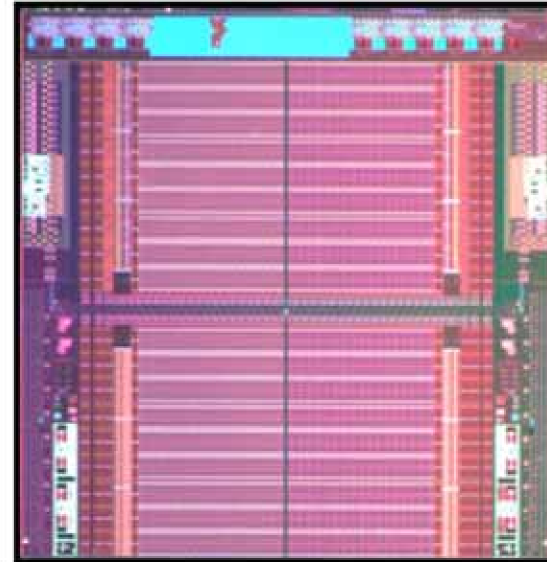
http://www.intel.com/pressroom/kits/45nm/photos.htm



Processors on an Intel 45nm Hafnium-based High-k Metal Gate "Penryn" Wafer photographed with an original Intel Pentium processor die. Using an entirely new transistor formula, the new processors incorporate 410 million transistors for each dual core chip, and 820 million for each quad core chip. The original Intel Pentium Processor only has 3.1 million transistors.

22 nm Tri-Gate Circuits

- 364 Mbit array size
- >2.9 billion transistors
- 3rd generation high-k + metal gate transistors
- Same transistor and interconnect features as on 22 nm CPUs



22 nm SRAM, Sept. '09

22 nm SRAMs using Tri-Gate transistors were first demonstrated in Sept. '09

Intel is now demonstrating the world's first 22 nm microprocessor (Ivy Bridge) and it uses revolutionary Tri-Gate transistors

- Introduction to IH2655
- Brief historic overview
- Moore’s Law and the ITRS Roadmap
- From Geometrical to Material-based scaling
- CMOS Process Flow

CMOS structures

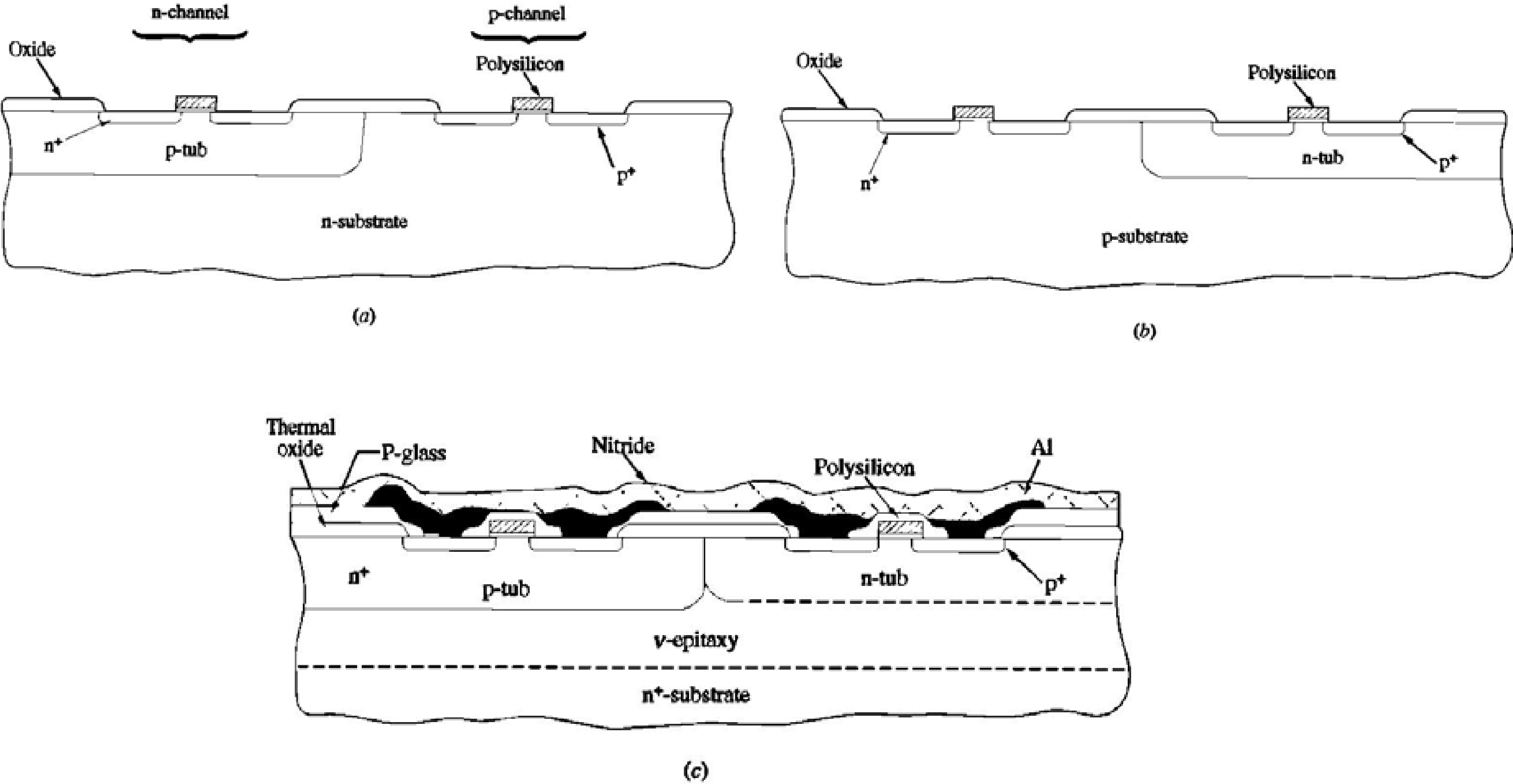
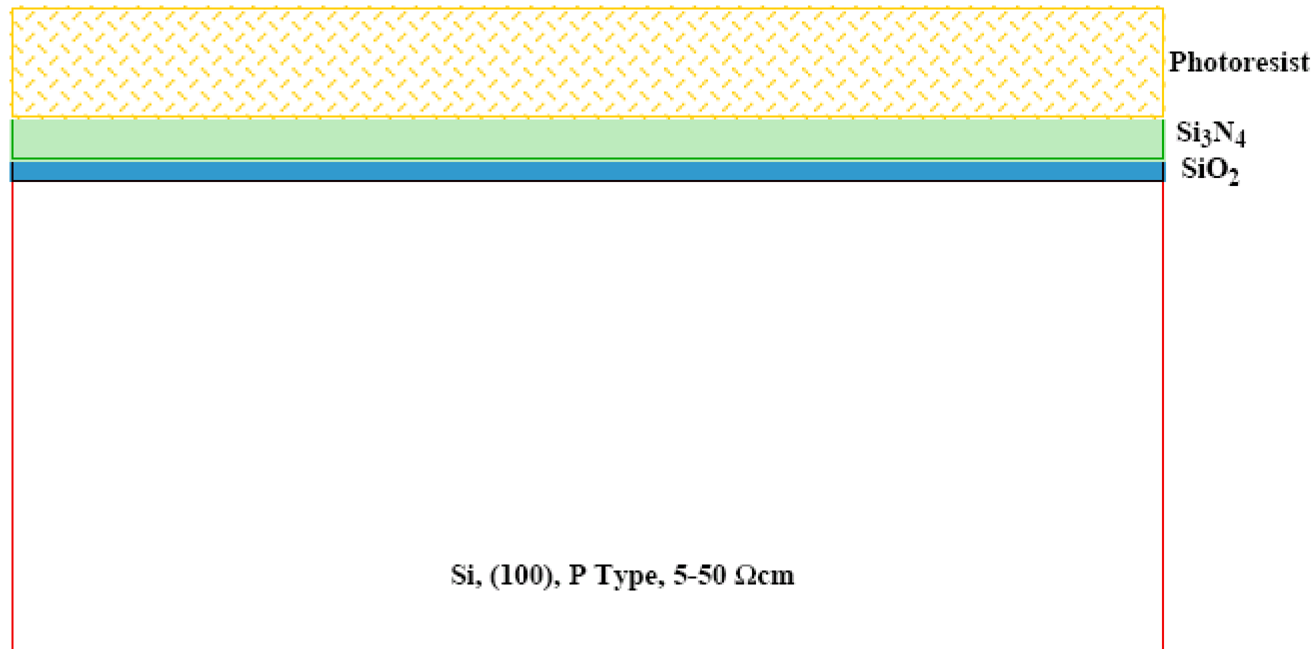


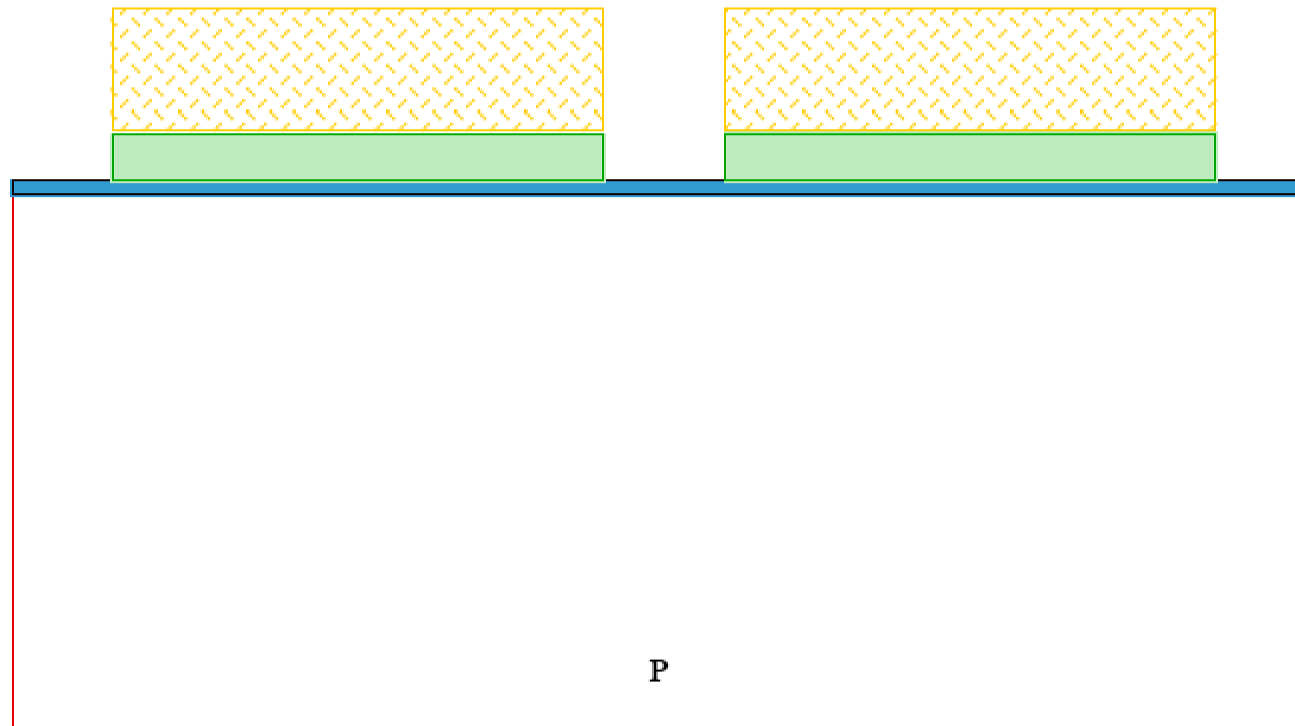
FIGURE 2
Various CMOS structures: (*a*) p-well, (*b*) n-well, (*c*) twin-well. (*After Parrillo et al., Ref. 4.* ©1980 IEEE.)

CMOS Process Flow



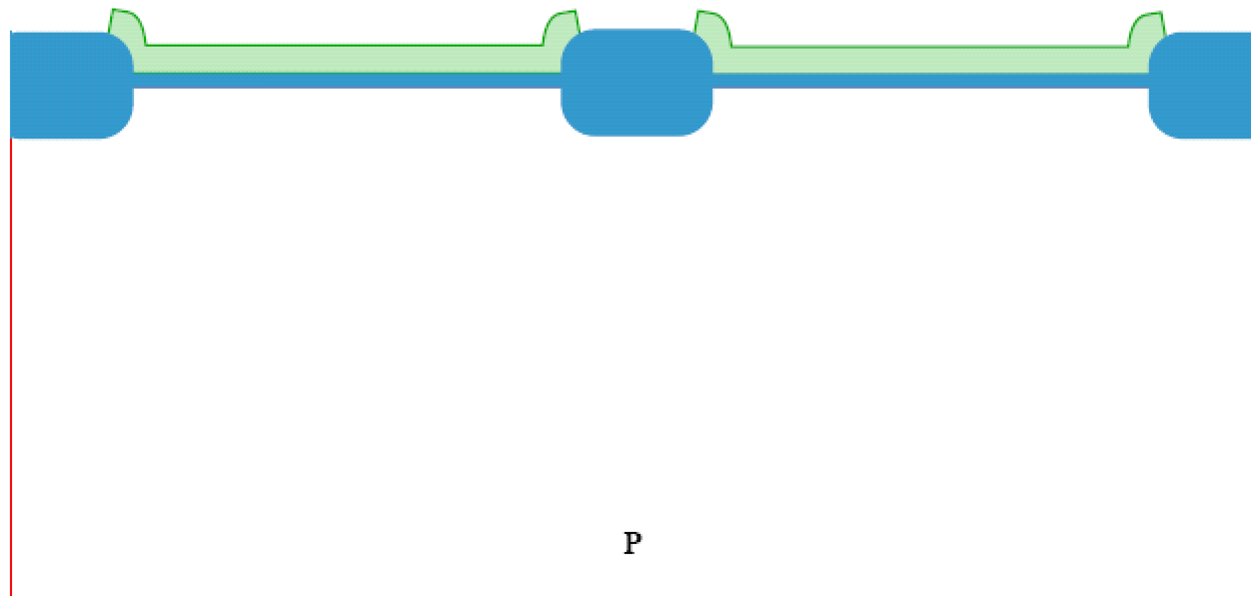
- Substrate selection: moderately high resistivity, (100) orientation, P type.
- Wafer cleaning
- Thermal oxidation (≈ 40 nm)
- Silicon Nitride LPCVD deposition (≈ 80 nm)
- Photoresist spinning and baking (≈ 0.5 - 1.0 μm)

CMOS Process Flow



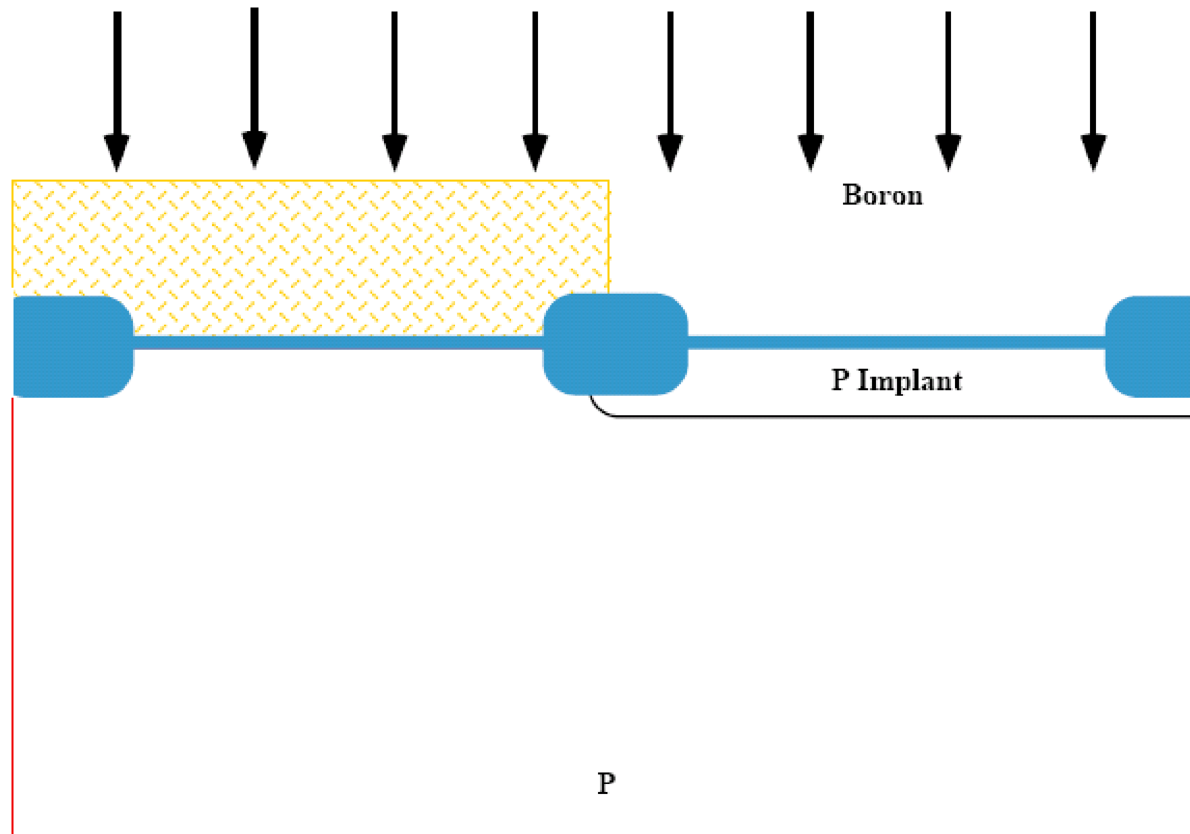
- Mask #1 patterns the active areas
- Silicon Nitride is dry etched
- Photoresist is stripped

CMOS Process Flow



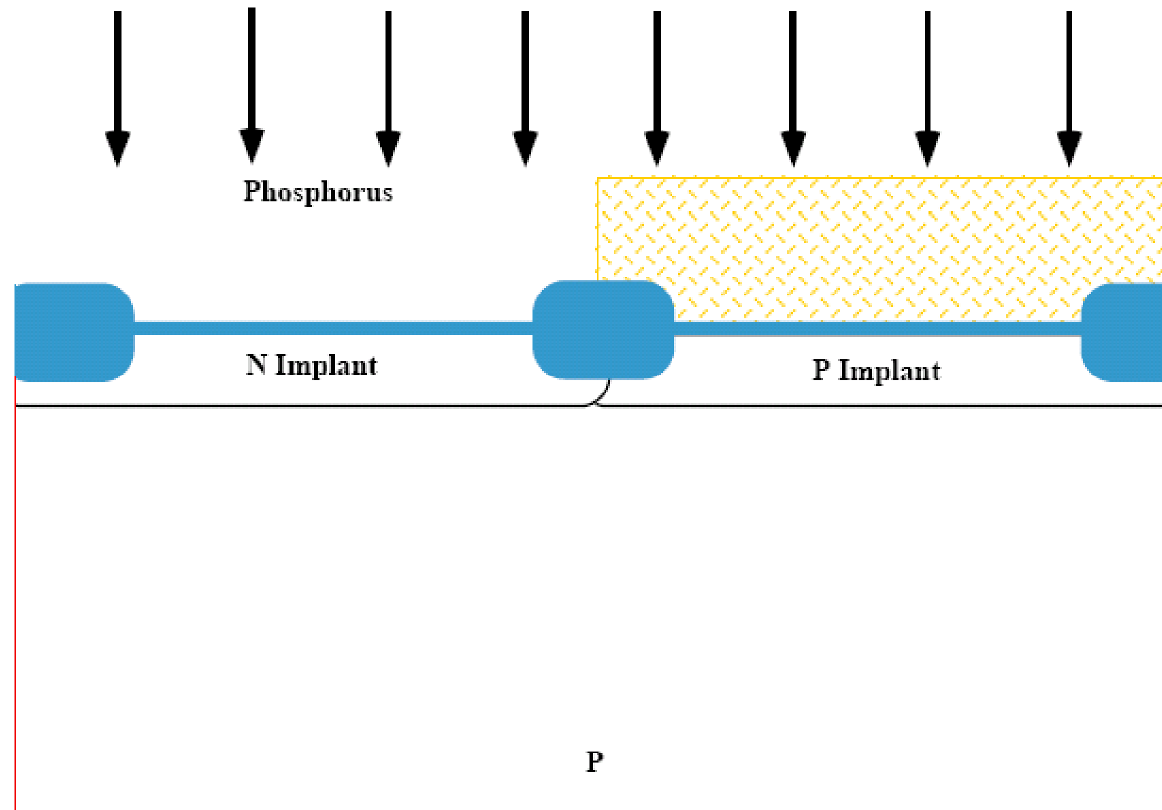
- Field oxide is grown using a LOCOS/ROX process
- Typically 90 min @ 1000 °C in H_2O grows ≈ 0.5 μm

CMOS Process Flow



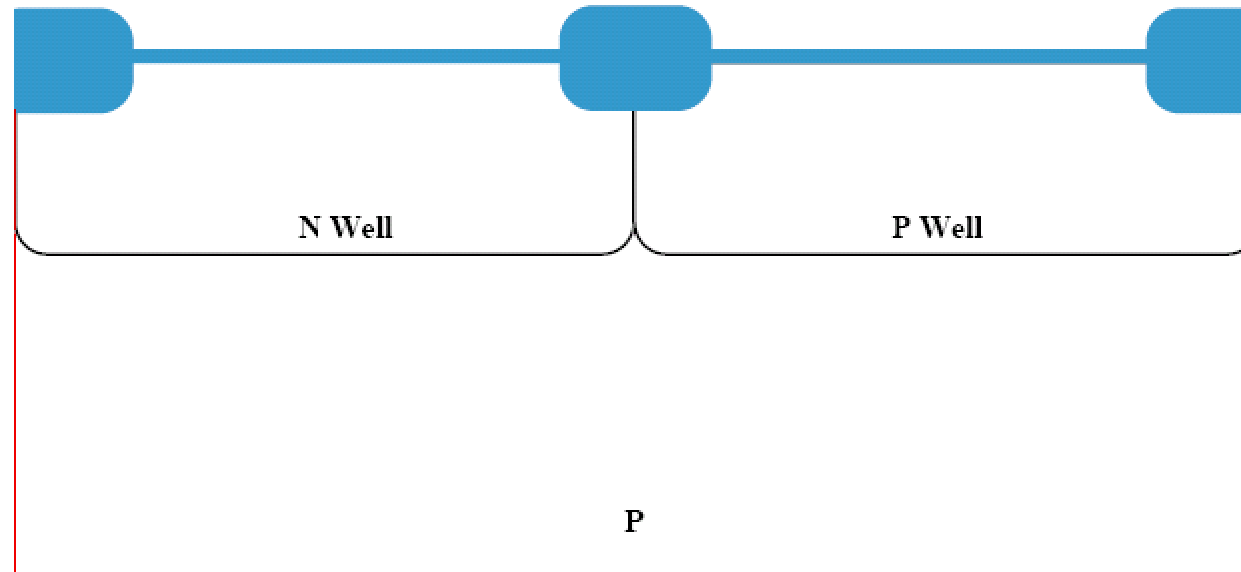
- Mask #2 blocks a B^+ implant to form the wells for the NMOS devices
- Typically 10^{13} cm^{-2} @ 150-200 KeV

CMOS Process Flow



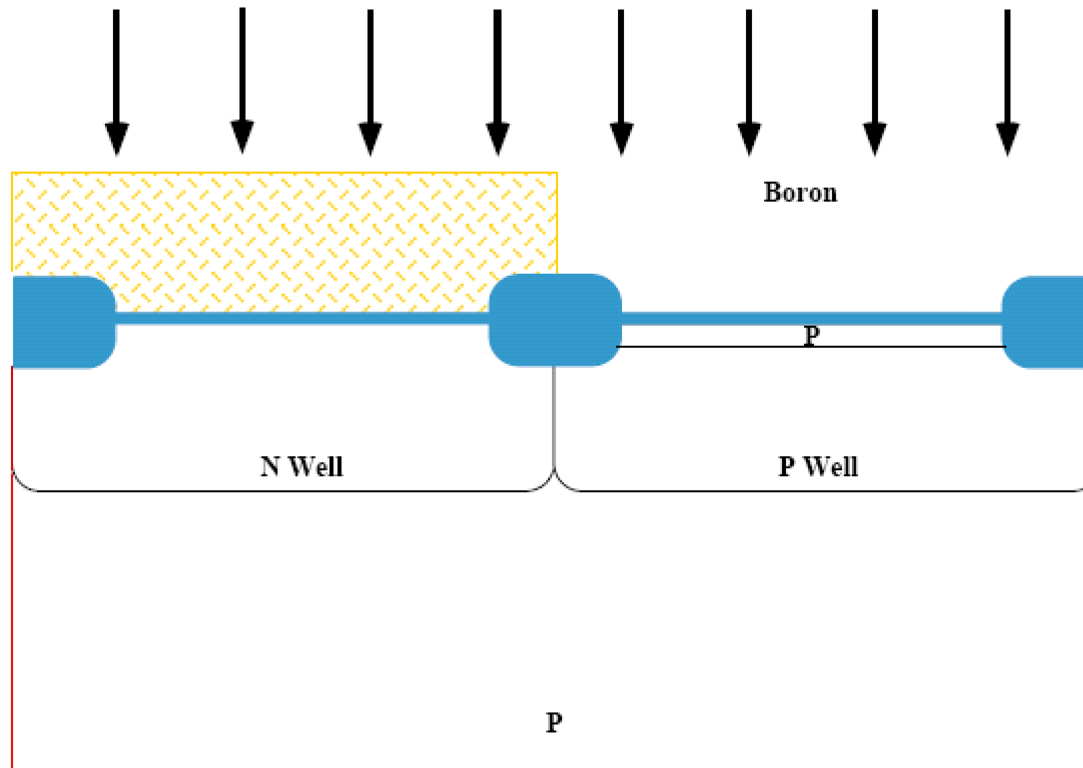
- Mask #3 blocks a P$^+$ implant to form the wells for the PMOS devices
- Typically 10^{13} cm^{-2} @ 300$^+$ KeV

CMOS Process Flow



- ”Annealing”
- A high temperature drive-in produces the “final” well depths and repairs implant damage
- Typically 4-6 hours @ 1000 °C - 1100 °C

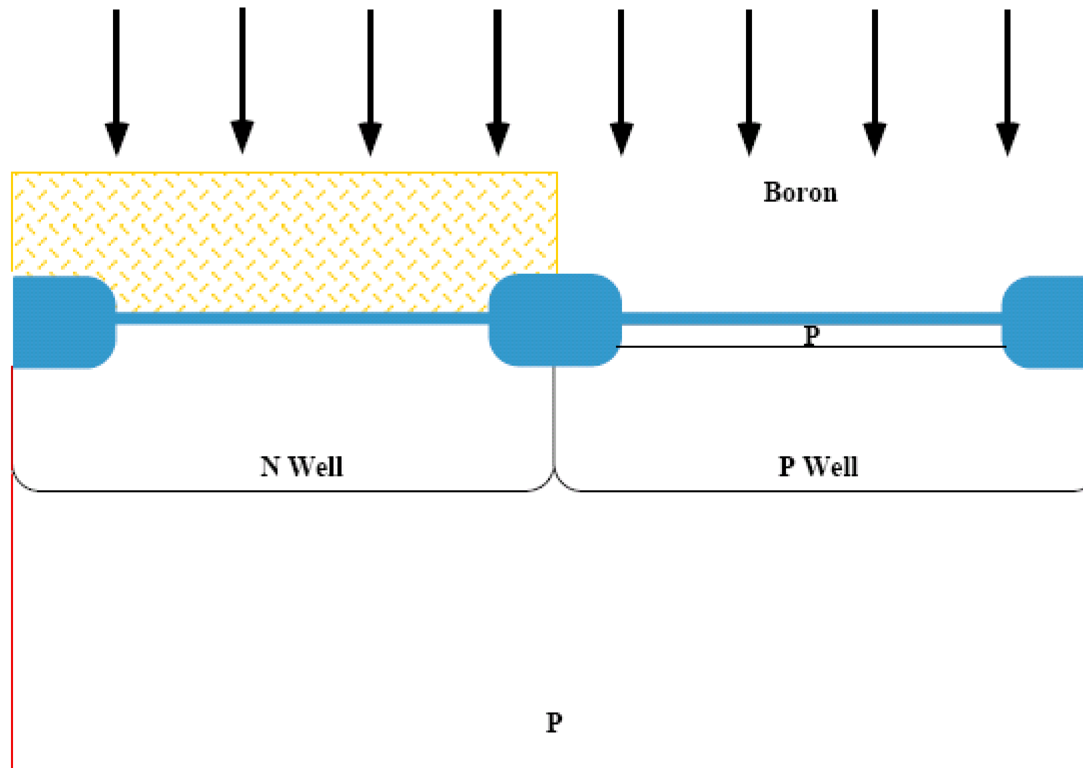
CMOS Process Flow



- Mask #4 is used to mask the PMOS devices
- An Implant is done on the NMOS devices
- Typically a 1-5 x 10^{12} cm^{-2} B^{+} implant @ 50 - 75 KeV

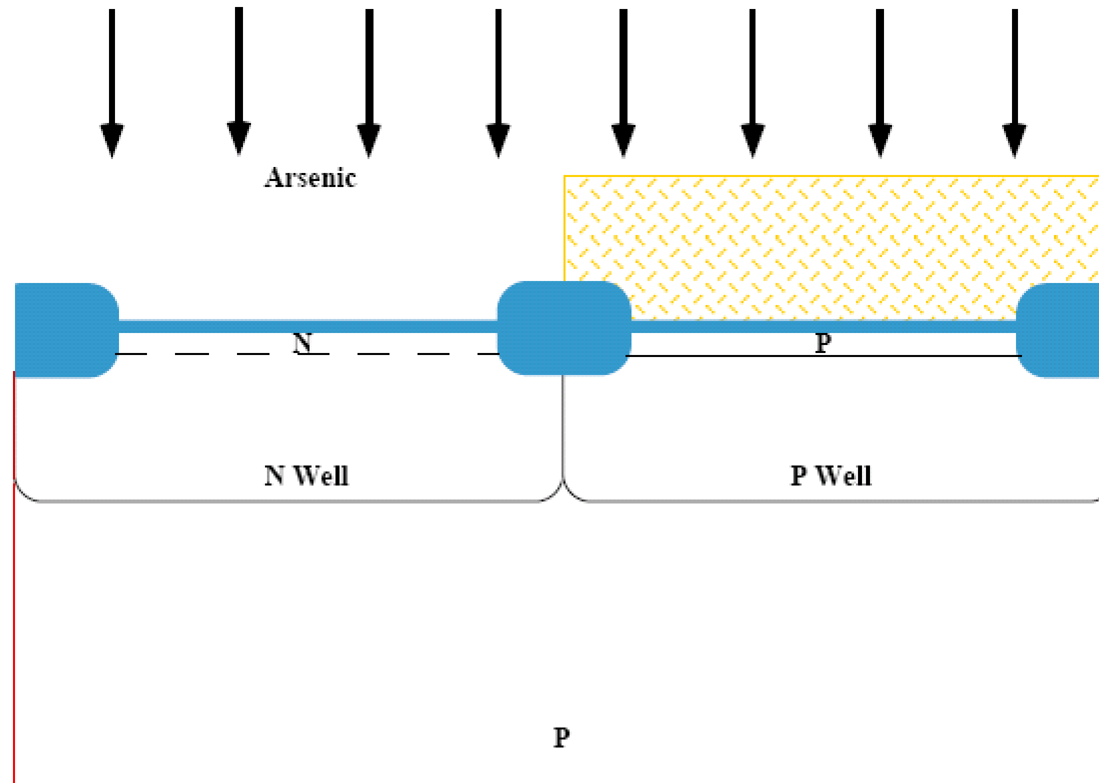
Concept Test

CMOS Process Flow



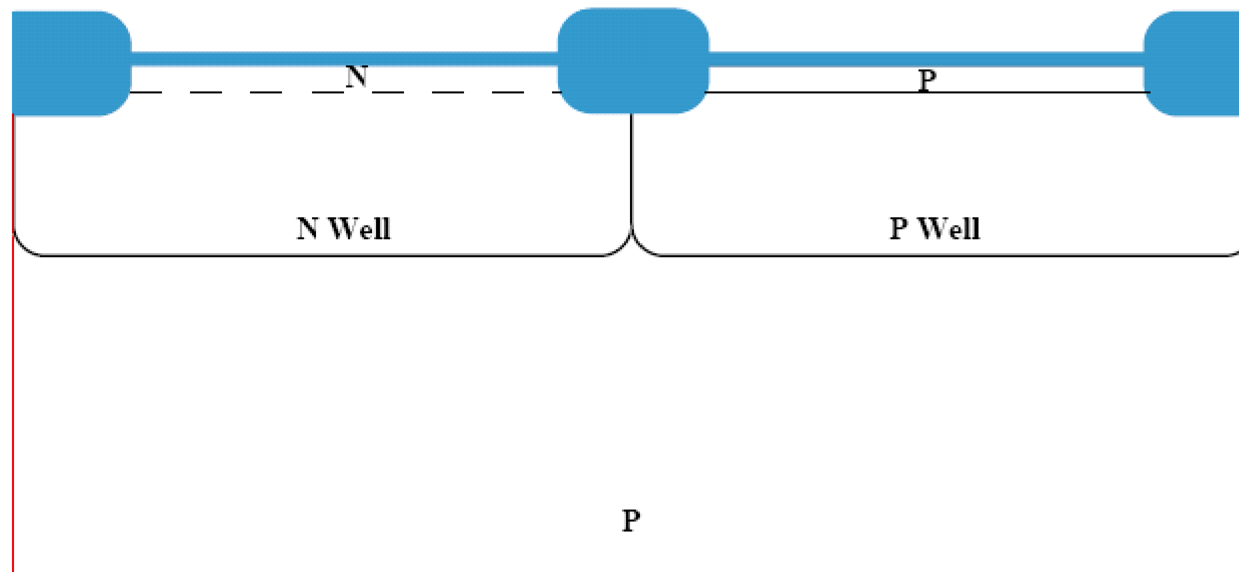
- Mask #4 is used to mask the PMOS devices
- A V_{TH} adjust implant is done on the NMOS devices
- Typically a 1-5 x 10^{12} cm^{-2} B^+ implant @ 50 - 75 KeV

CMOS Process Flow



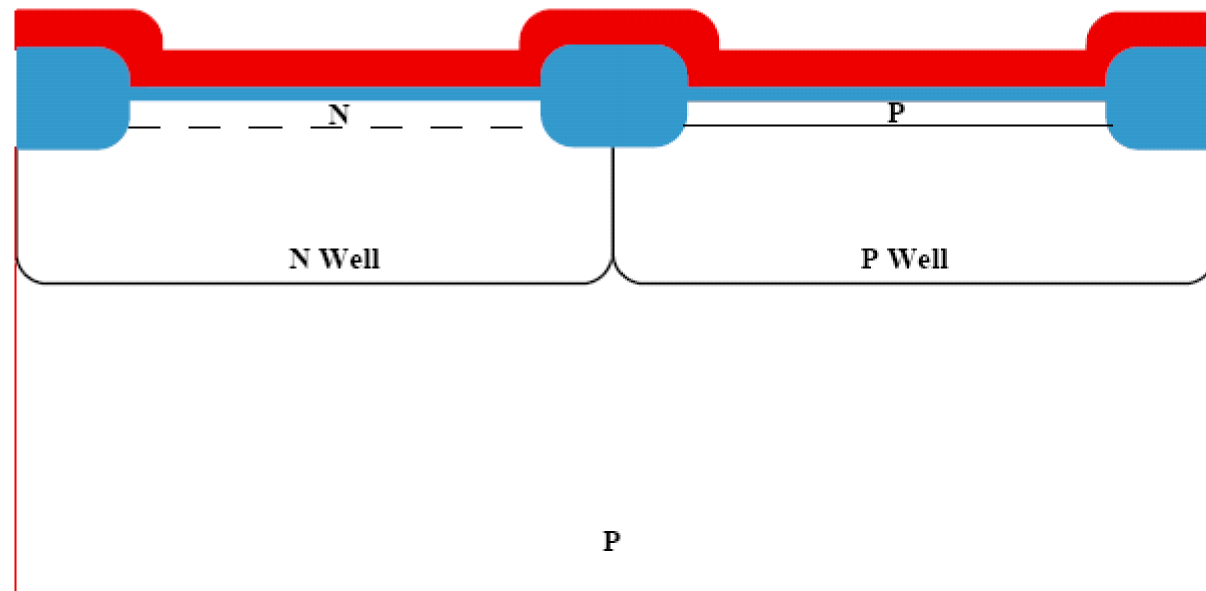
- Mask #5 is used to mask the NMOS devices
- A V_{TH} adjust implant is done on the PMOS devices,
- Typically 1-5 x 10^{12} cm^{-2} As^{+} implant @ 75 - 100 KeV.

CMOS Process Flow



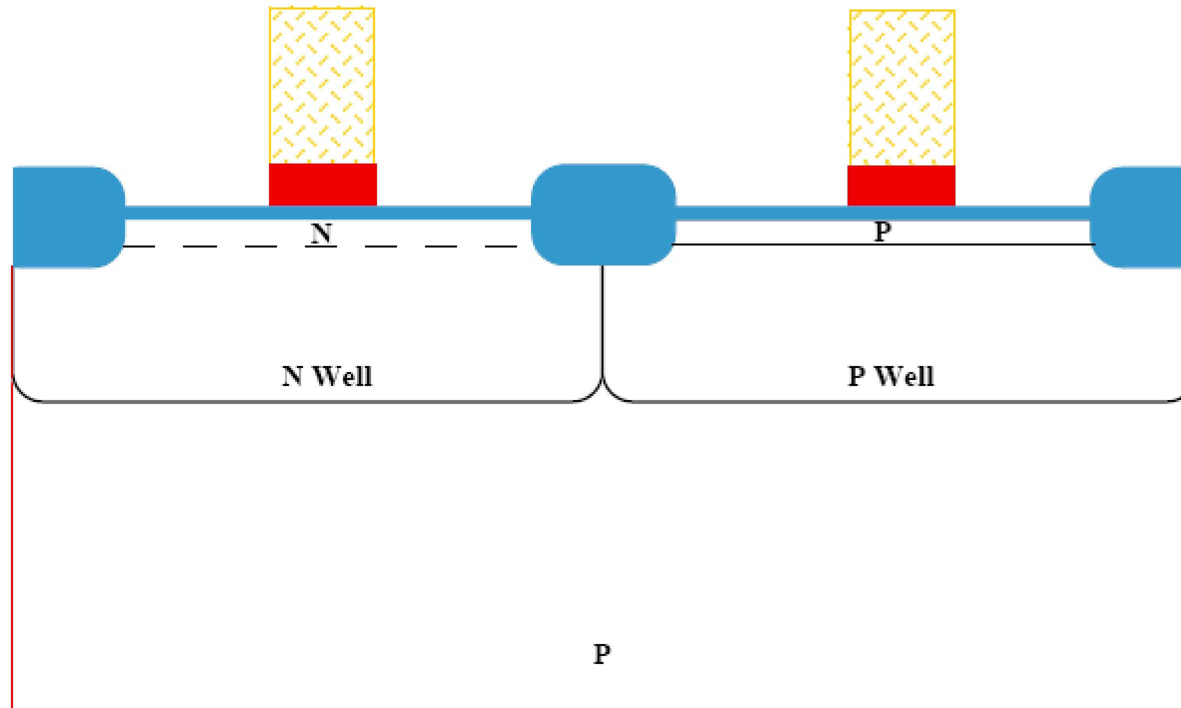
- The thin oxide over the active regions is stripped
- A high quality gate oxide grown
- Typically 3 - 5 nm, which could be grown in 0.5 - 1 hrs @ 800 °C in O_2
- Note: Today this could be entirely different for high end technology (high-k)

CMOS Process Flow



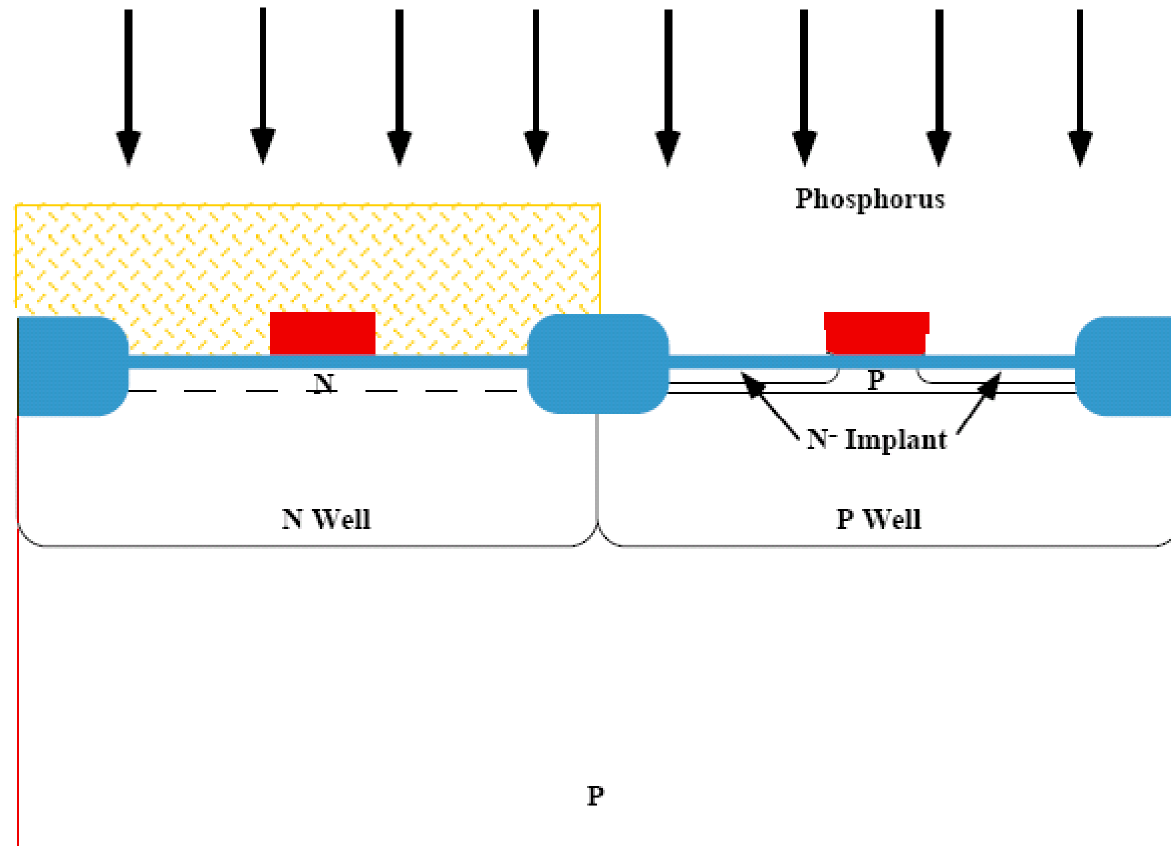
- Polysilicon is deposited by LPCVD (≈ 0.5 μm)
- An unmasked P^+ or As^+ implant dopes the poly (typically 5×10^{15} cm^{-2})
- Note: Today this could be a metal gate

CMOS Process Flow



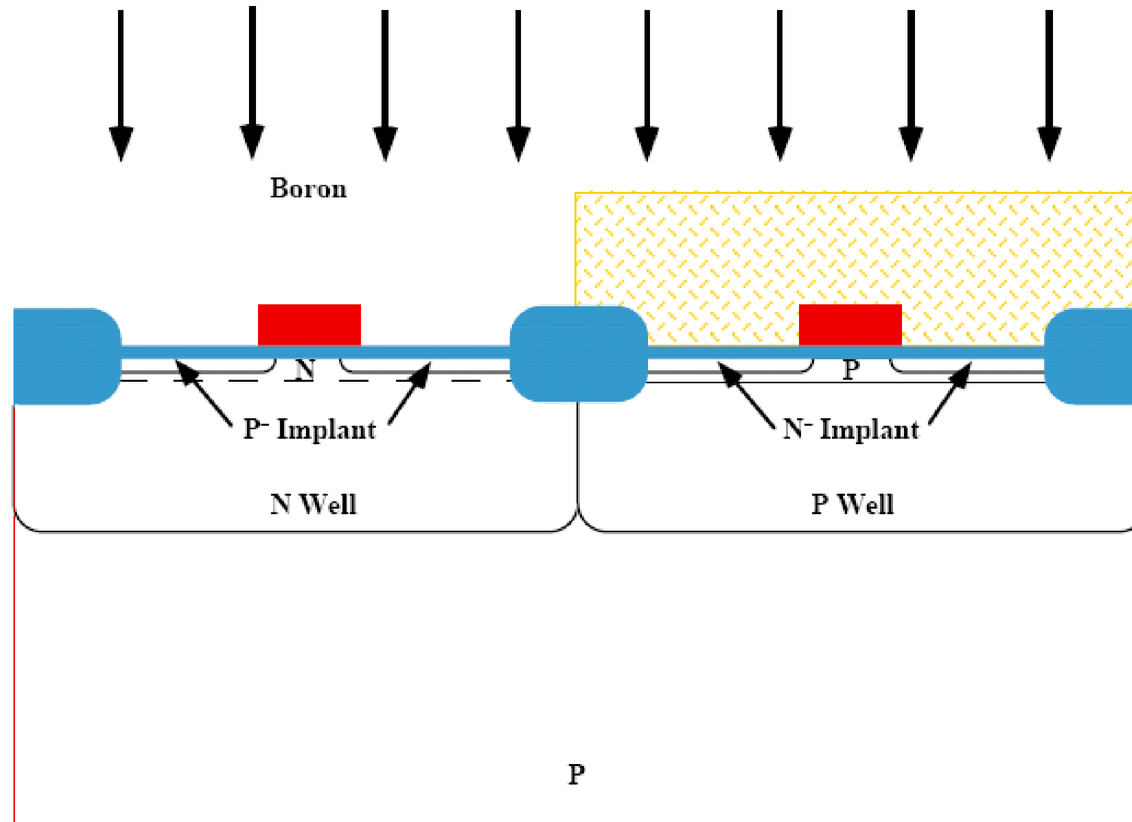
- Mask #6 is used to protect the MOS gates
- The poly is plasma etched using an anisotropic etch

CMOS Process Flow



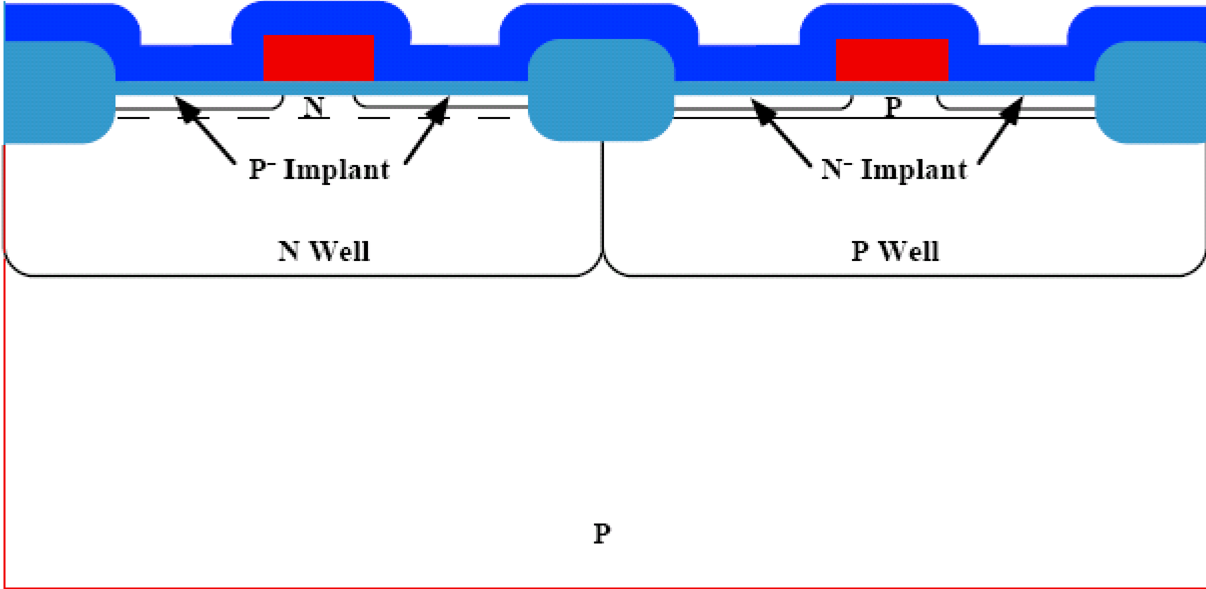
- Mask #7 protects the PMOS devices
- A P^+ implant forms the LDD regions in the NMOS devices
- Typically 5 x 10^{13} cm^{-2} @ 50 KeV

CMOS Process Flow



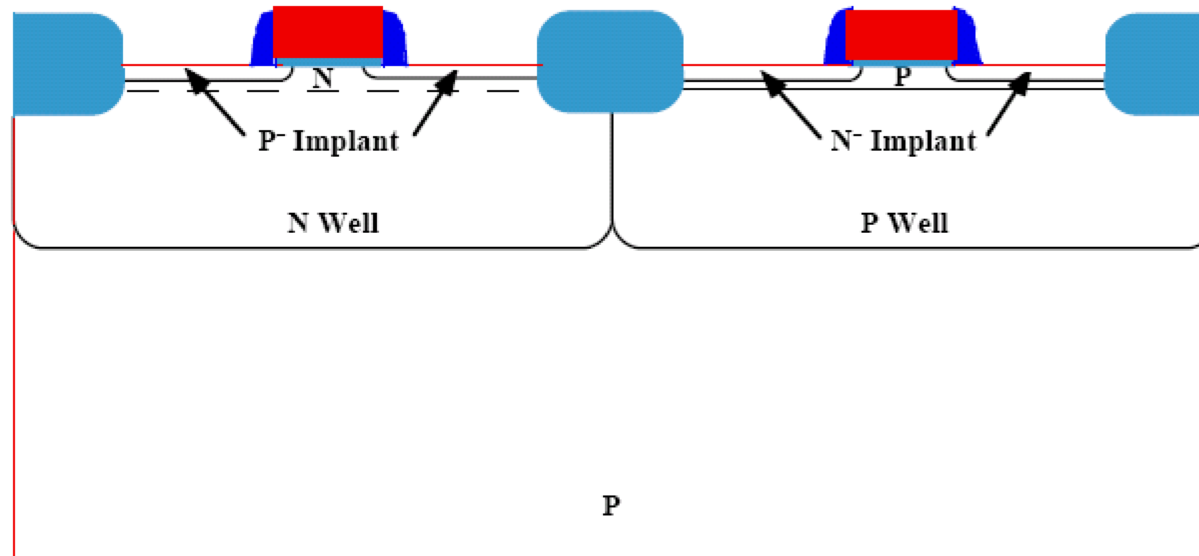
- Mask #8 protects the NMOS devices
- A B^+ implant forms the LDD regions in the PMOS devices
- Typically 5×10^{13} cm^{-2} @ 50 KeV

CMOS Process Flow



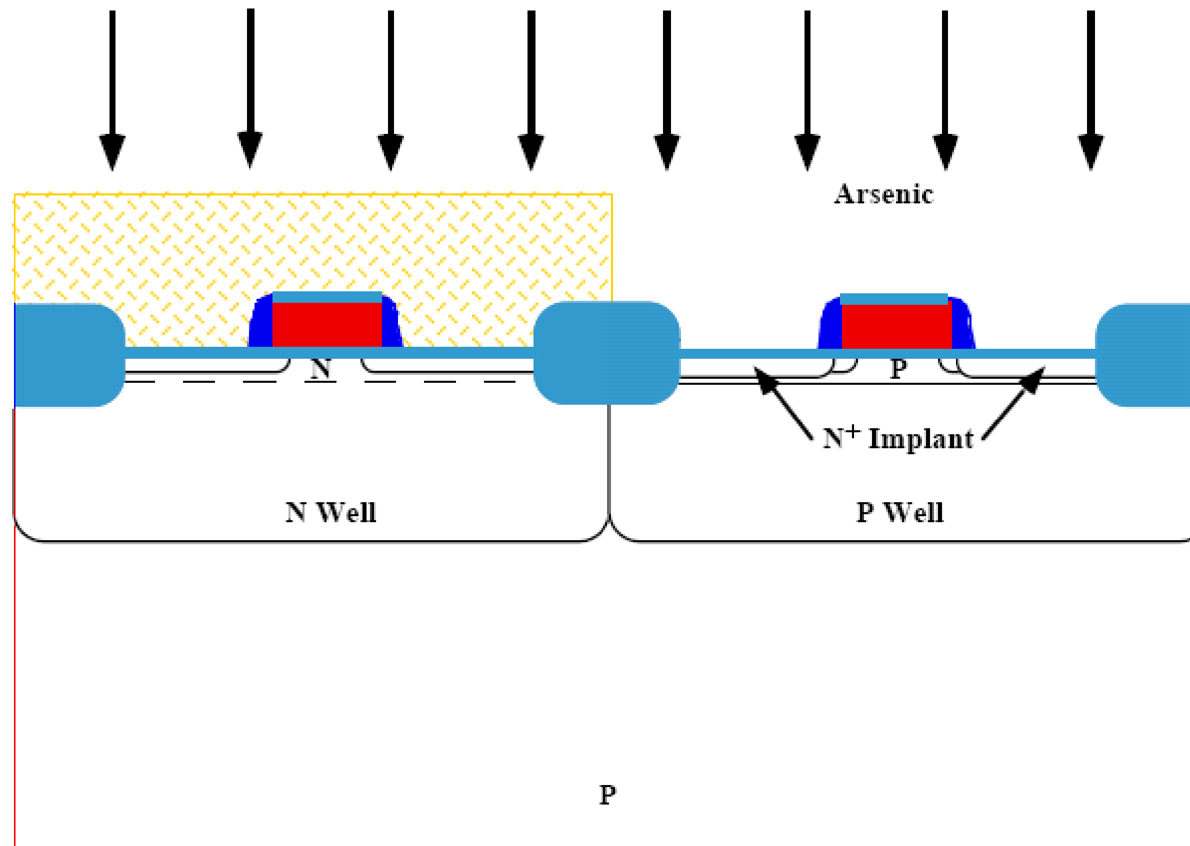
- Aonformal layer of SiO_2 is deposited (typically 0.5 µm)

CMOS Process Flow



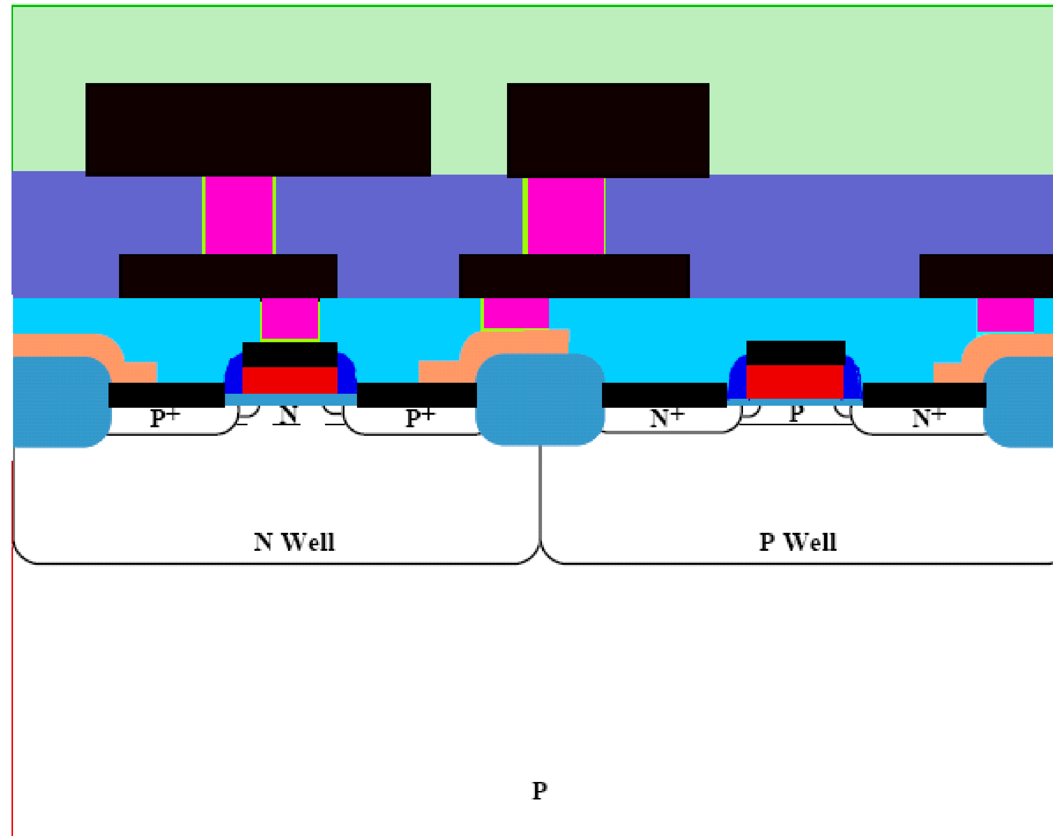
- Anisotropic etching leaves “sidewall spacers” along the edges of the poly gates

CMOS Process Flow



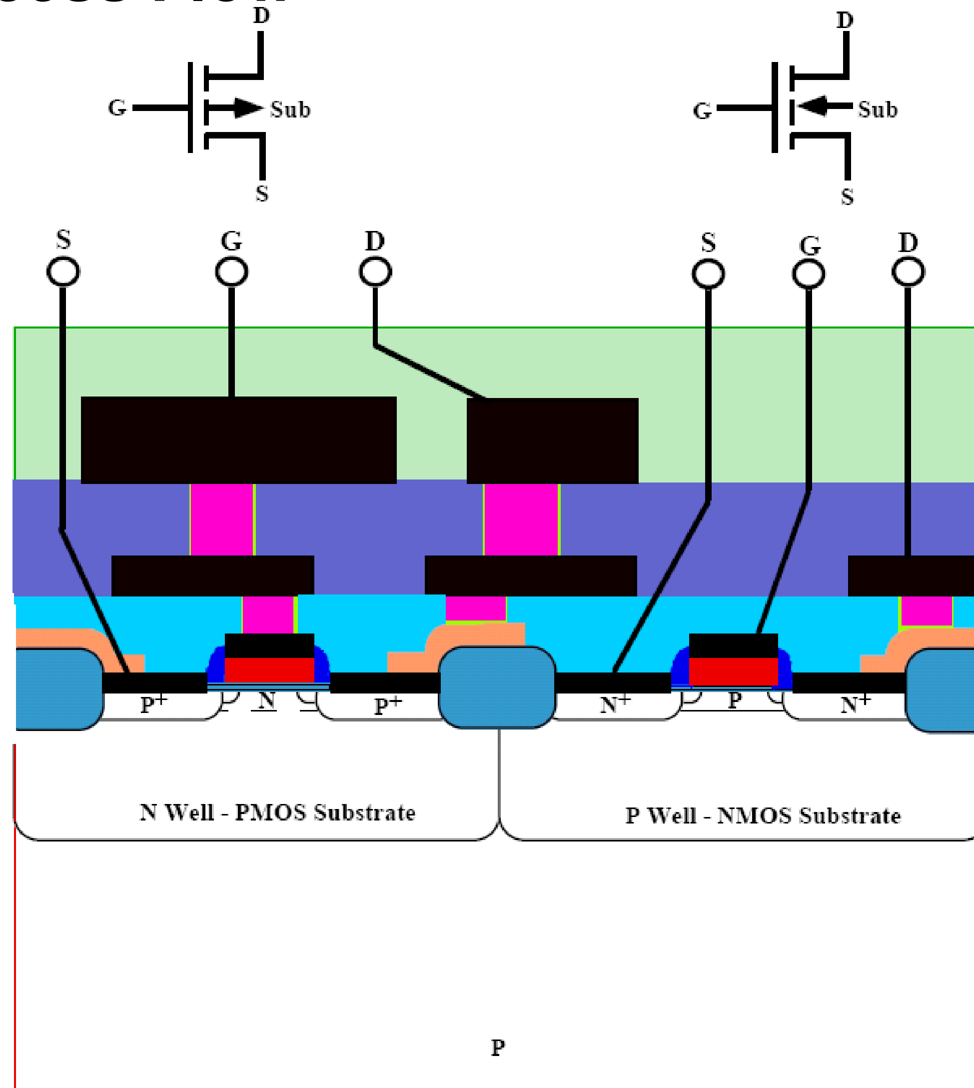
- Mask #9 protects the PMOS devices
- An As^{+} implant forms the NMOS source and drain regions
- Typically 2-4 x 10^{15} cm^{-2} @ 75 KeV

CMOS Process Flow



- Intermetal dielectric and second level metal are deposited and defined in the same way as level #1.
- Mask #14 is used to define contact vias and Mask #15 is used to define metal 2
- A final passivation layer of Si_3N_4 is deposited by PECVD and patterned with Mask #16
- This completes the CMOS structure

CMOS Process Flow



Final result of the process flow: One NMOS and one PMOS device, BUT...
They were made in parrallel and we can make 1 Billion other at the same time