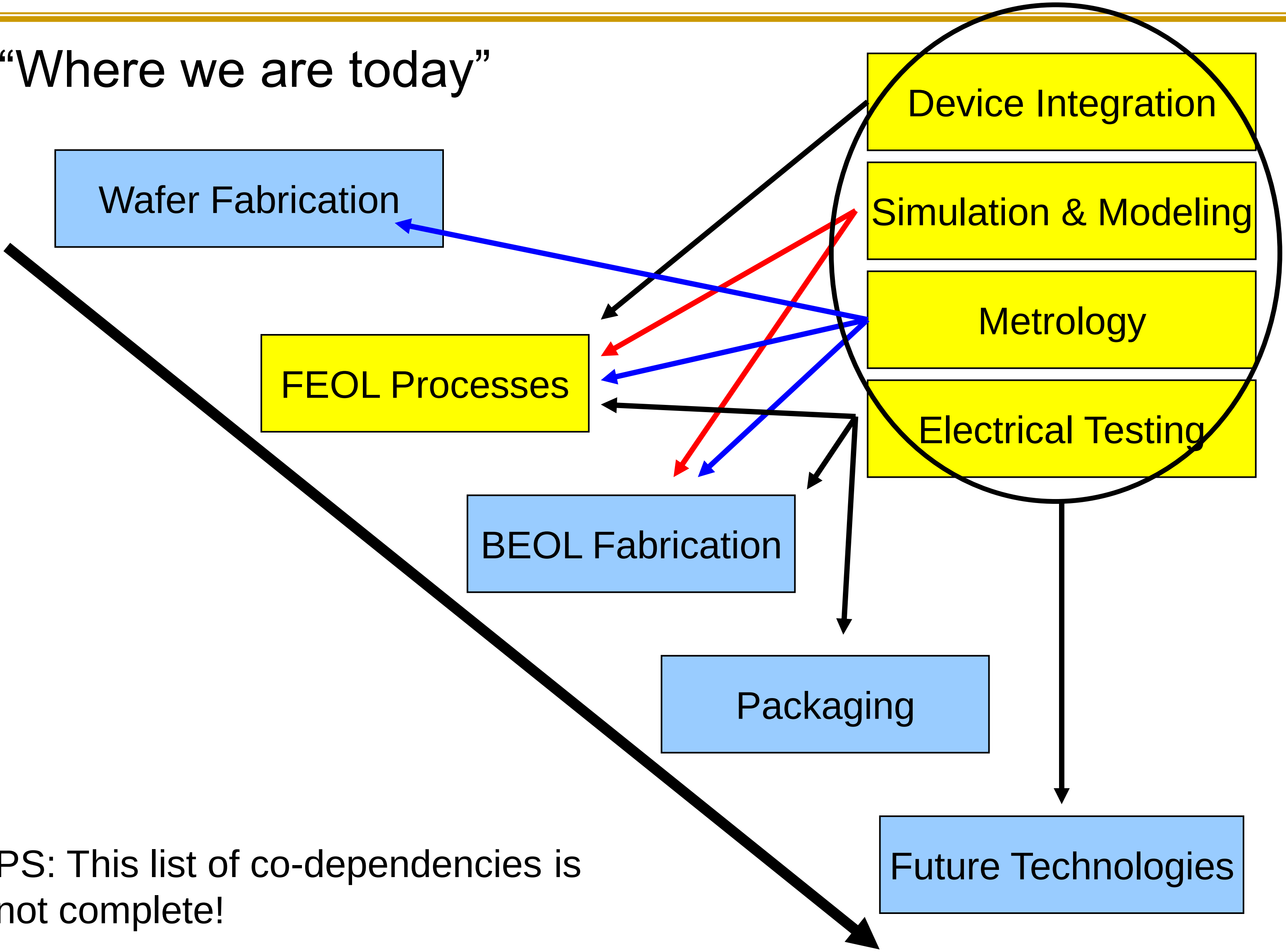
Lecture 6

I Annealing
II Diffusion
III Ion Implantation

"Where we are today"



Wafer Fabrication

FEOL Processes

BEOL Fabrication

Packaging

Future Technologies

Device Integration

Simulation & Modeling

Metrology

Electrical Testing

PS: This list of co-dependencies is not complete!

Lecture 6

I Annealing
II Diffusion
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Lecture 6

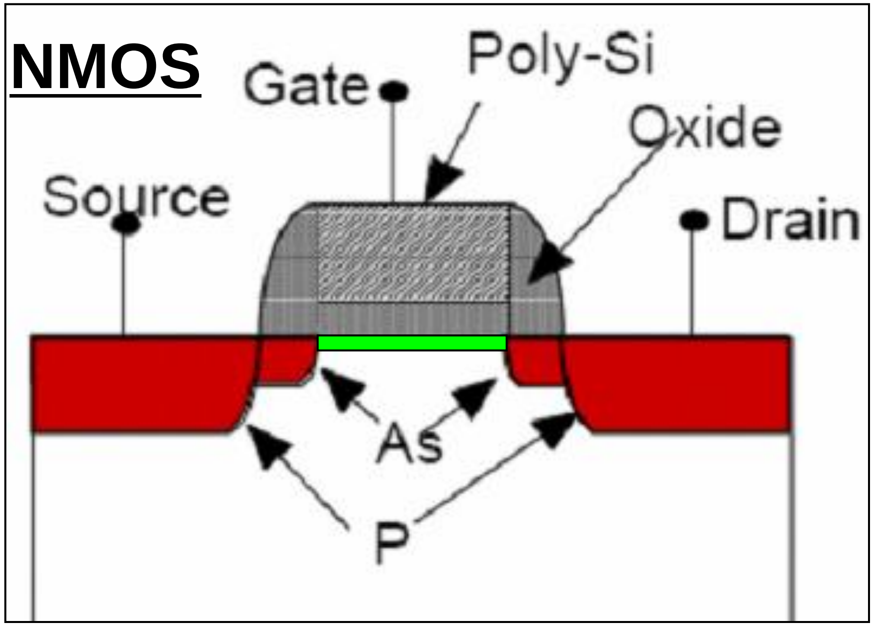
Annealing

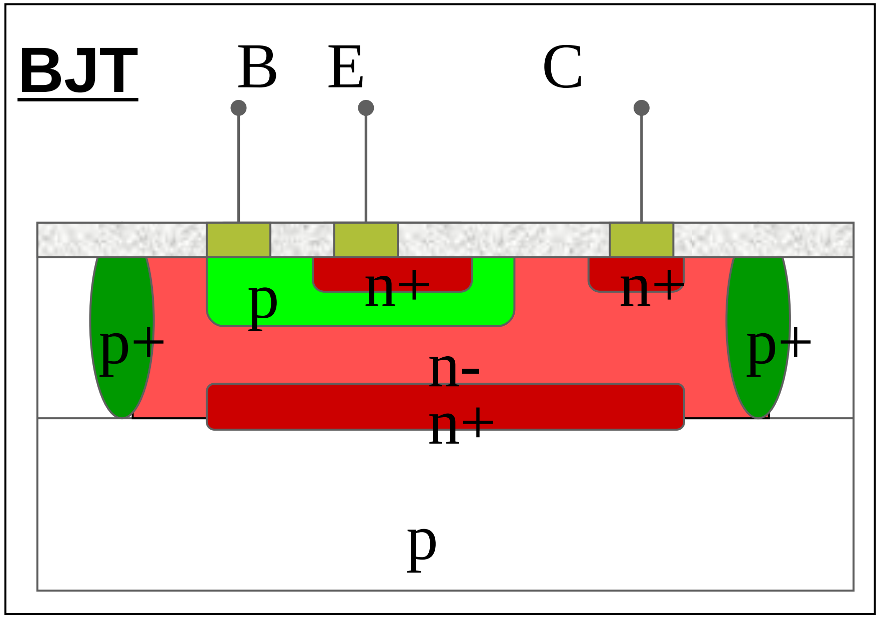
Furnace Anneal (FA), Rapid Thermal Anneal (RTA), Laser Spike Anneal (LSA)

Doping in Silicon Technology

"Introducing a certain number and type of impurities into silicon with accurate doping profile."

Examples:

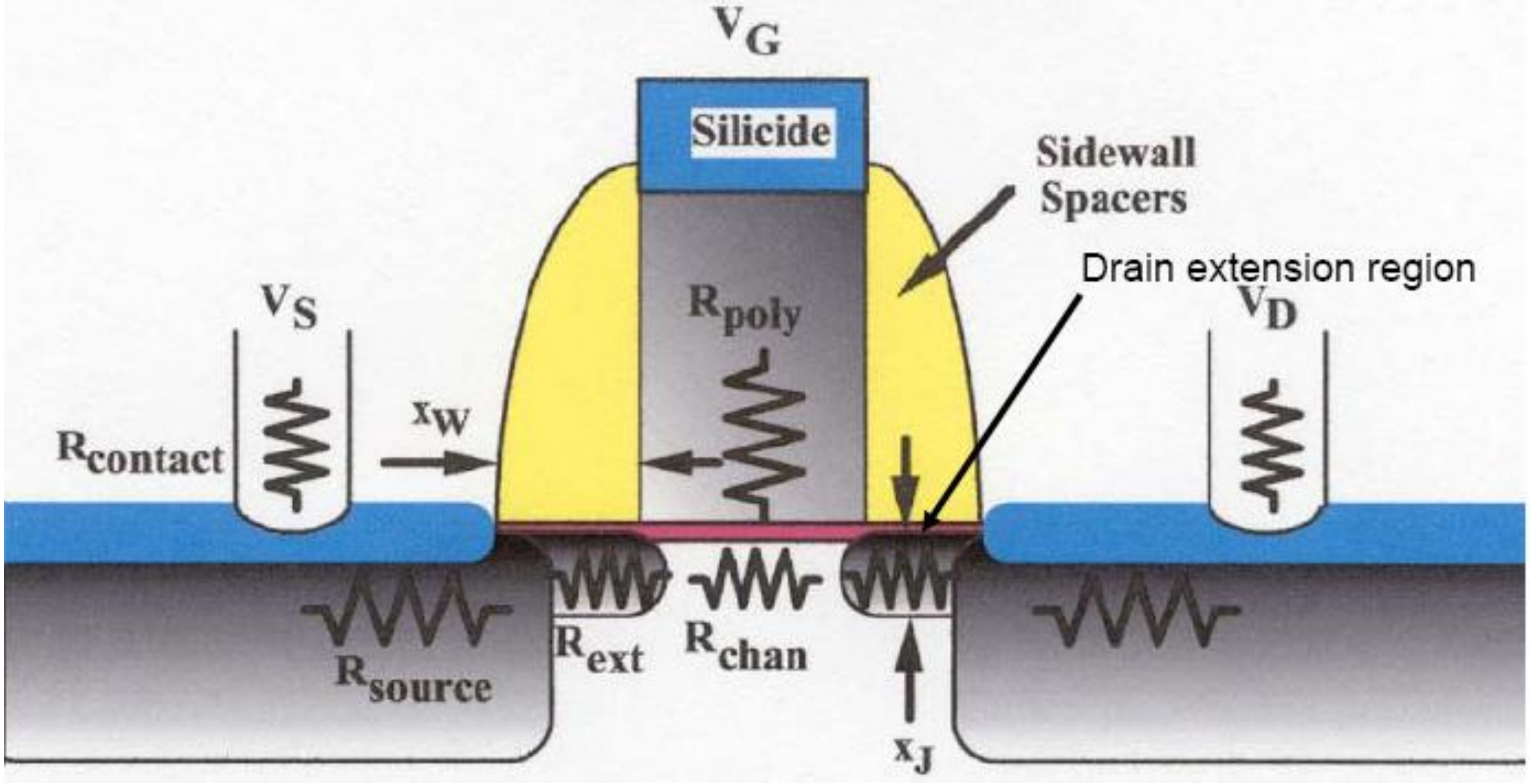




Applications: **MOSFET: Well, Gate, Source/Drain, Channel, etc.**
BJT: Base, Emitter, Collector, etc.

Doping in Silicon Technology

MOSFET: Requirements on doping



- ✓ **Junction Depth x_j**
- ✓ **Sheet Resistance R_s**
- ✓ **Solubility**

Doping in Silicon Technology: Requirements

Junction Depth x_i

x_j : At the position $x = x_j$, C_x (Diffused Impurity Concentration) = C_B (Bulk Concentration)

✓When devices are scaled down by a factor of *k*, constant-field scaling principle requires x_j should also be scaled down by *k*. Simultaneously,

$$2R_{\text{contact}} + R_{\text{source}} + R_{\text{drain}} + 2R_{\text{ext}} < \enclose{circle}{0.10}(R_{\text{channel}})$$

✓Increased control over x_j is required ⇒Short Channel Effects, DIBL (drain induced barrier lowing)

In modern CMOS technology, shallow junction and high-concentration doping are used to meet both the two requirements

Thermal Budget Crisis

- ITRS dictates scaling demands
- Technology needs to provide solutions to avoid SCEs)
- E.g. Annealing is critical for formation of shallow junctions

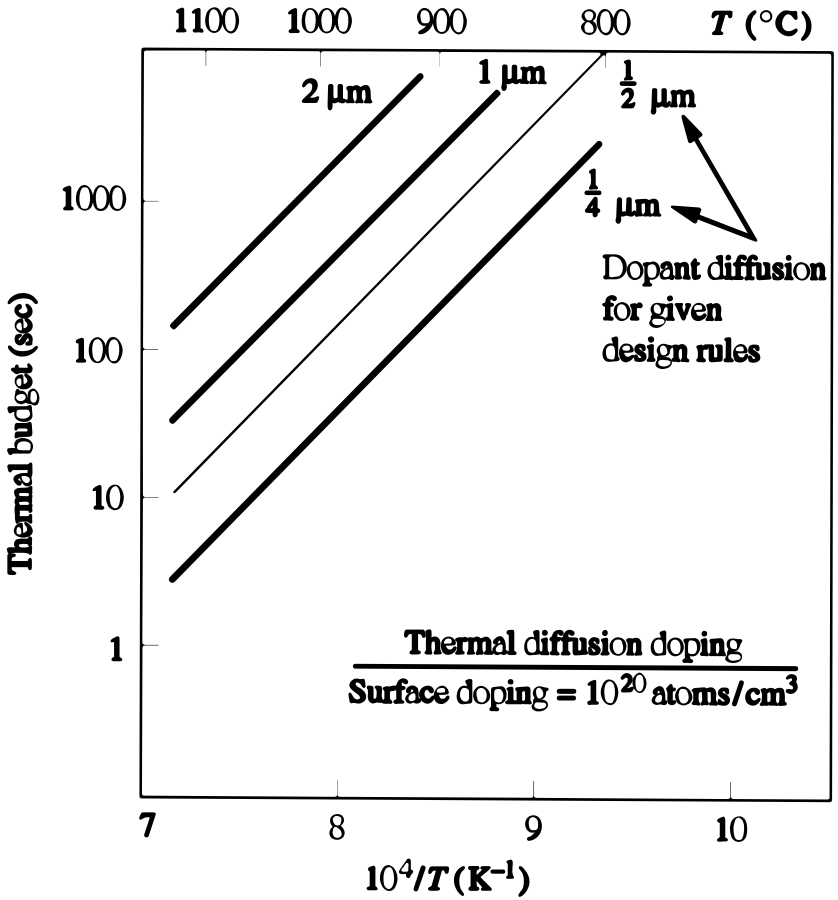
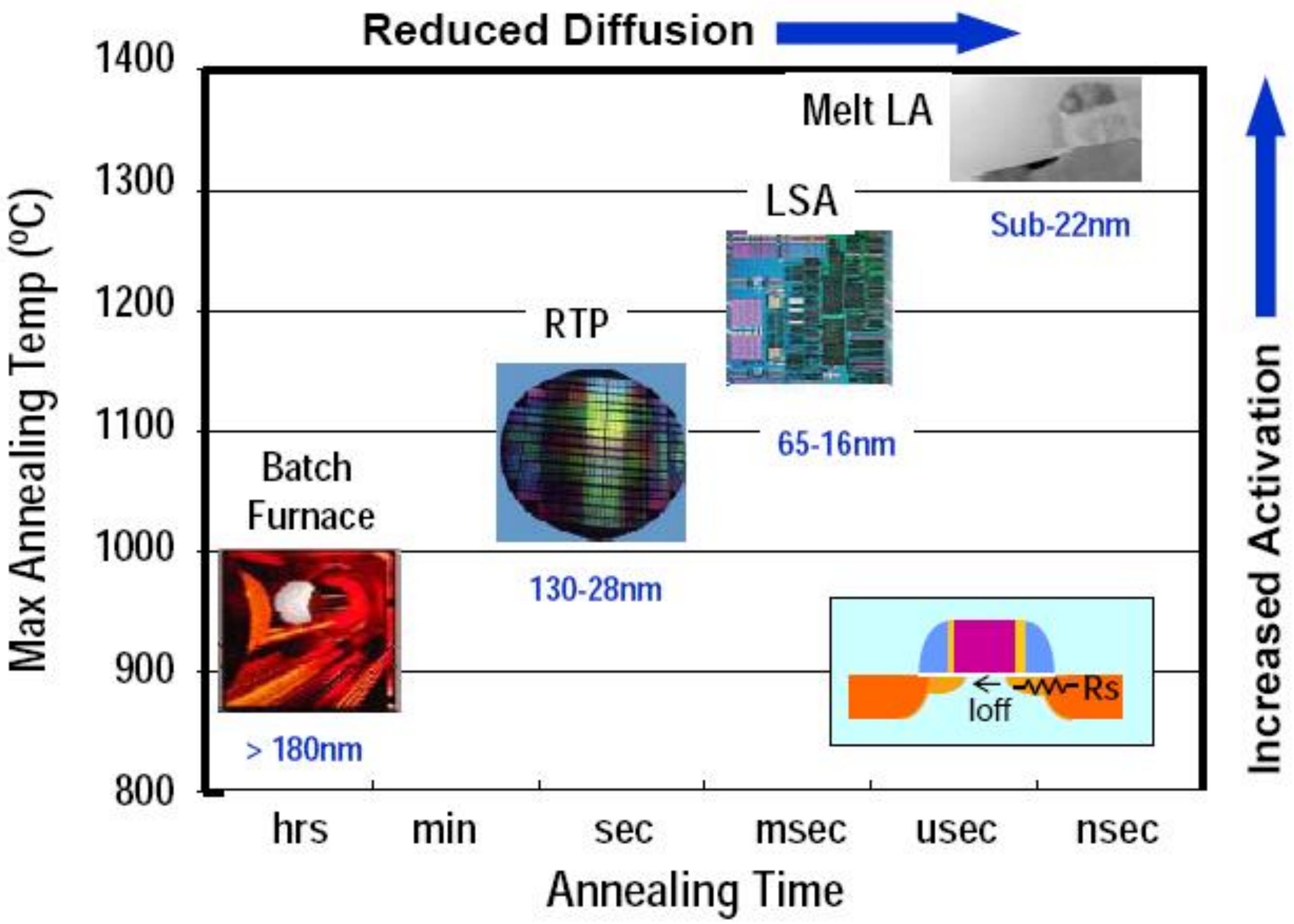


FIGURE 6
Available time-at-temperature (thermal budget) to produce scaled p^+n junction depths for four MOS technologies. Thermal diffusion sources are assumed with a fixed surface concentration of 1×10^{20} atoms/cm^3. (*After Fair, Ref. 15.* © 1990 IEEE)

Annealing Technology: Overview

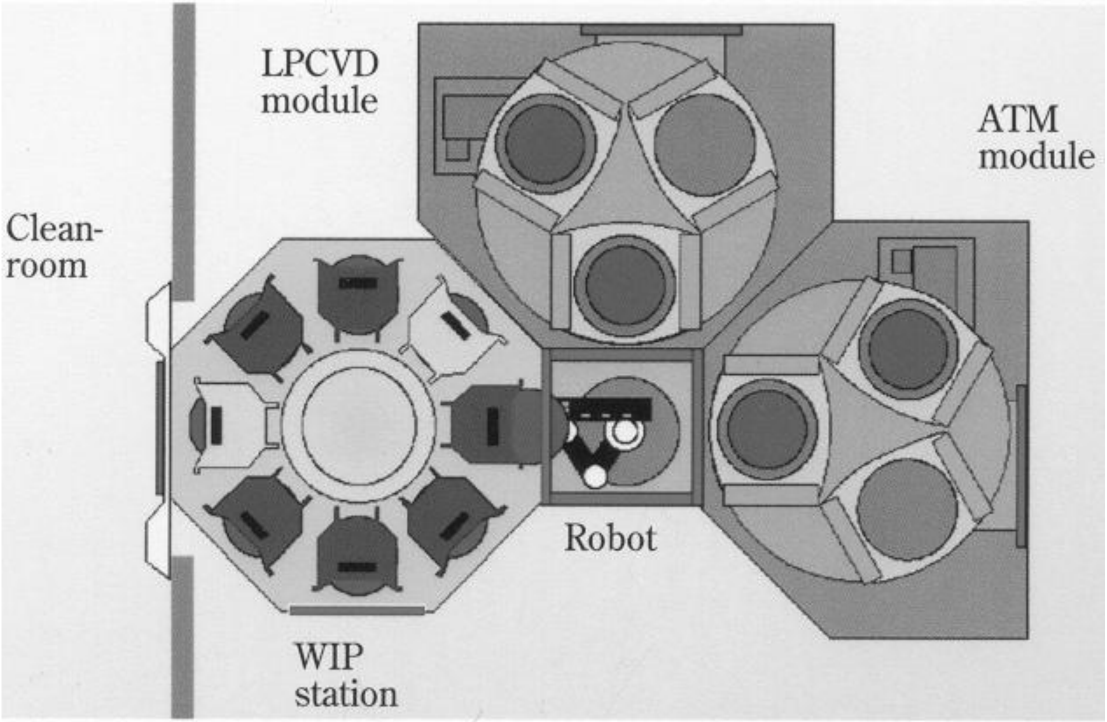
Temperature-Time Space for Junction Formation



Source: www.semiconwest.com, J. Hebb, “Laser Spike Annealing: Meeting challenges for sub-40nm CMOS devices”, Ultratech

Furnace Anneal (FA)

- Horizontal furnaces have now largely been replaced by vertical furnaces
- Example: ASM Advance 400 series



- Furnace anneal can not meet thermal budget requirements. Alternatives?
- Rapid thermal heating for rates of 10-100 C/s

Rapid Thermal Anneal (RTA)

- Ramp rate: 50-300 C°/s
- Largest concern: Temperature control
- Temperature non-uniformity due to varying emissivity

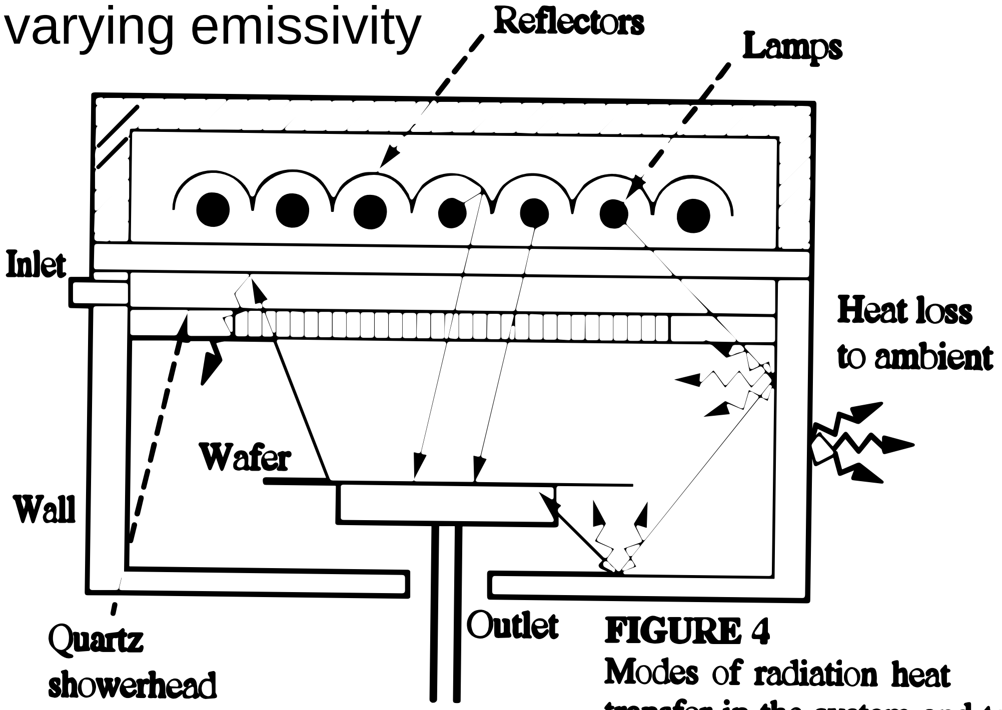


FIGURE 4
Modes of radiation heat transfer in the system and to the ambient in a typical RTP reactor. (*After Merchant et al., Ref. 9.*)

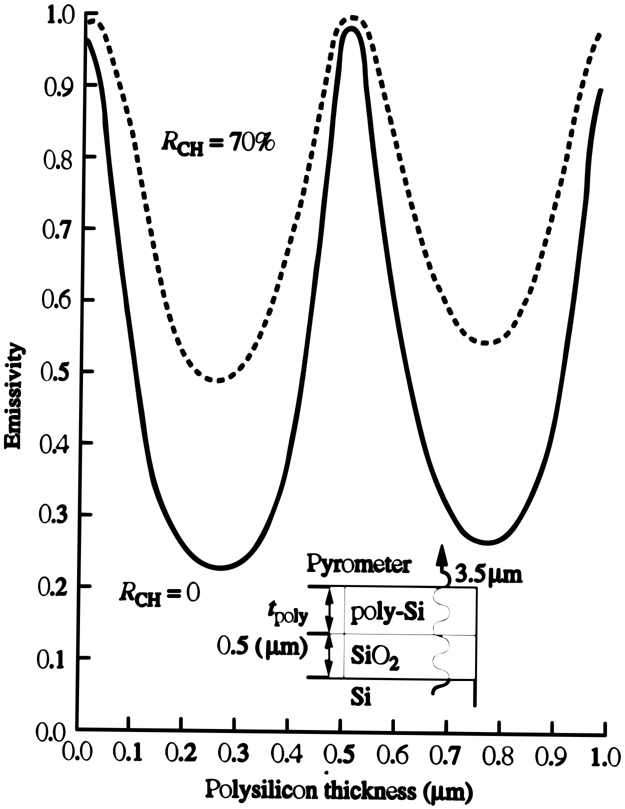


FIGURE 3
Emissivity changes with varying polycrystalline Si thickness deposited on 0.5 μm SiO_2 as measured with a pyrometer at 3.5 μm in a black chamber (reflectivity, R_{CH} = 0) and in a 70% reflecting chamber. (*After Hill, Ref. 7.*)

Rapid Thermal Anneal (RTA)

RTA is used for:

- Anneal and ultra-shallow junction formation
- Oxidation (RTO)
- Silicon epitaxy (in particular high-temp epi)
- CVD of poly and dielectrics (e.g. Centura modules)
- Silicides (Ti salicide process)
- Frequently integrated in single-wafer cluster tools

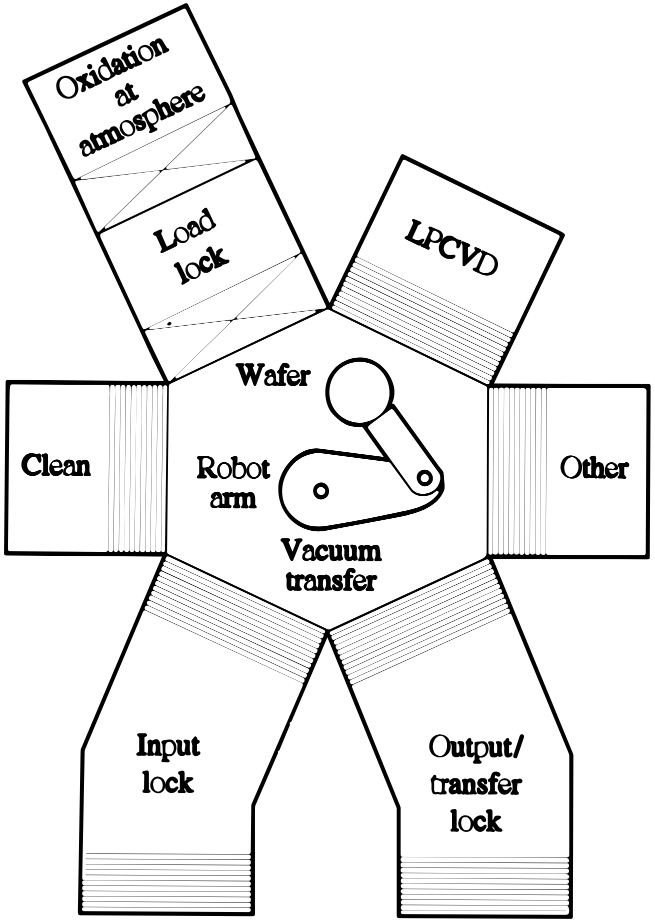


FIGURE 10
Example of rapid thermal processing modules in a radial, multichamber cluster designed for better particle exclusion, interprocess ambient control, and flexible operation. (*After Rosser, Moynagh, and Affolter, Ref. 24.*)

Laser Thermal Annealing (LTA) / Laser Spike Anneal (LSA)

Advantages of LTA/LSA

- Low thermal budget
- Ultra-fast annealing (< µs)
- Melt vs. non-melt or submelt process
- Diffusionless activation (non-melt)
- E.g. non-melt millisecond laser for 45nm CMOS
- Used heavily in Thin Film Transistor (TFT) applications to crystallize polysilicon
- For TFT, reduces temperatures from ~ 1000 C to ~ 400 C

Non-melt (red)

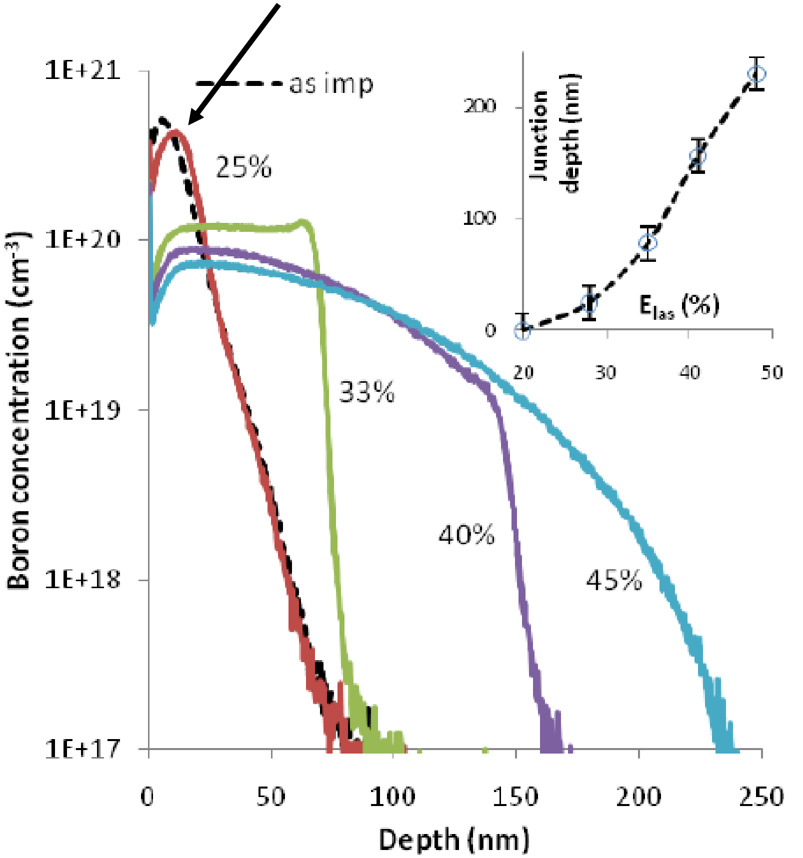
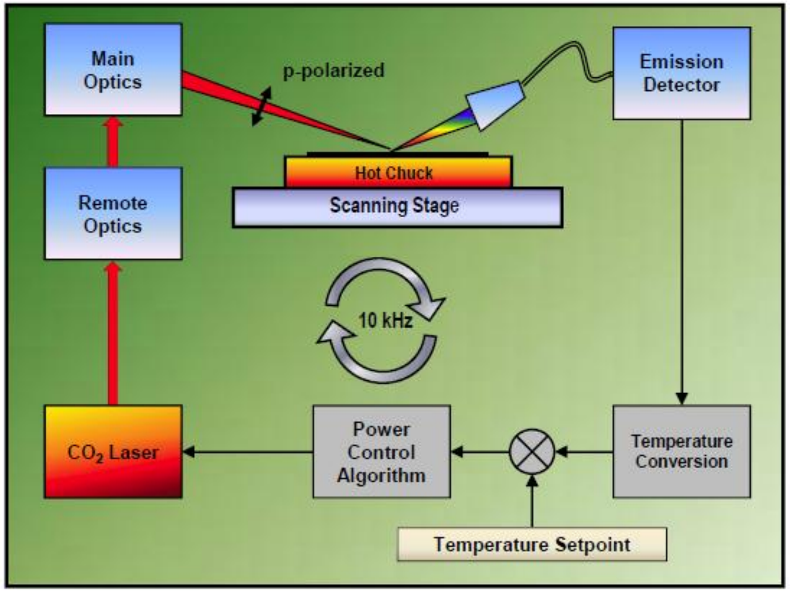


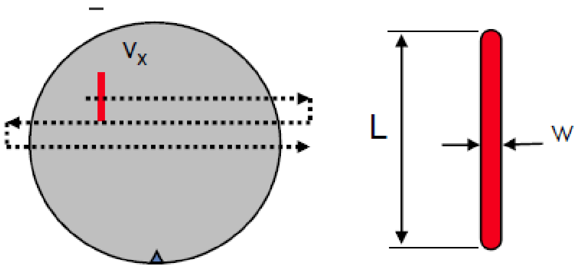
Fig. 1.Dopant profiles for as implanted, E_{las} = 20, 33, 40 and 45%. Inset: extracted junction depth.

Source: www.excico.com
“Microscale Process Uniformity by Excico LTA“

Laser Thermal Annealing (LTA) / Laser Spike Anneal (LSA)

Logic device applications today … and in the future





Long dwell applications

- Defect anneal (replace RTA spike anneal)
- Stress reduction
- Solid Phase Epitaxy (SPE) applications (e.g., Si:C, FINFET)

Low temp applications

- Nickel silicide formation (replace RTP for one or both steps)
- Post silicide activation

Source: www.semiconwest.com, J. Hebb, “Laser Spike Annealing: Meeting challenges for sub-40nm CMOS devices”, Ultratech

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I Annealing

II Diffusion

III Ion Implantation

Diffusion in Silicon

- Introduction
    - Dopants in Silicon Devices
    - Technology for diffusion
- Diffusion
    - Solid solubility
    - Intrinsic diffusion and diffusion constant
    - Extrinsic diffusion and electrical field effect
- Microscopic description
    - Diffusion during Thermal Oxidation
    - Dopant-Defect Interactions
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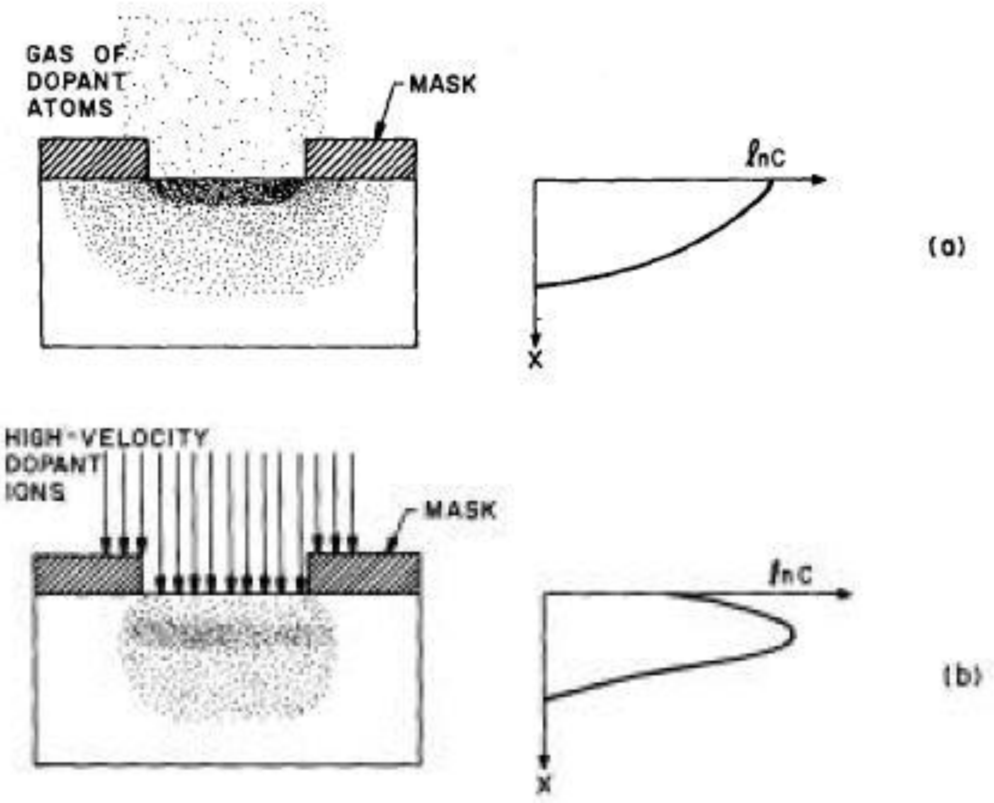
Introducing Dopants into Silicon

In the past:

Pre-deposition of dopants from gas, liquid or solid followed by diffusion ("drive-in”)

Dominating since late 70's:

Ion implantation of dopant ions followed by activation and crystal repair ("anneal")



Diffusion

Ion Implantation

(Sze p. 381)

Pre-deposition of dopants: “Classical” technology

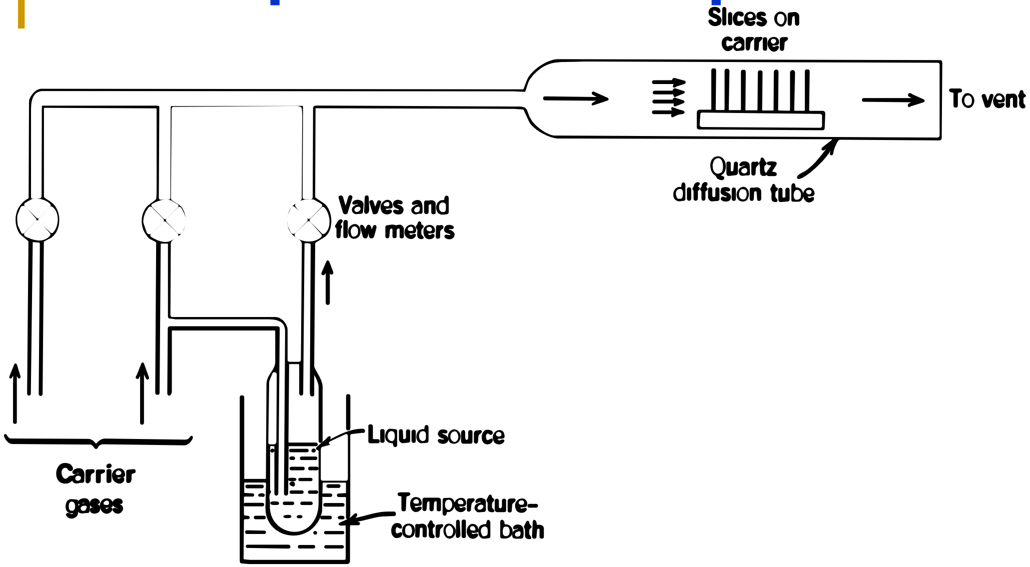


Fig. 4.27 Liquid-source diffusion system.

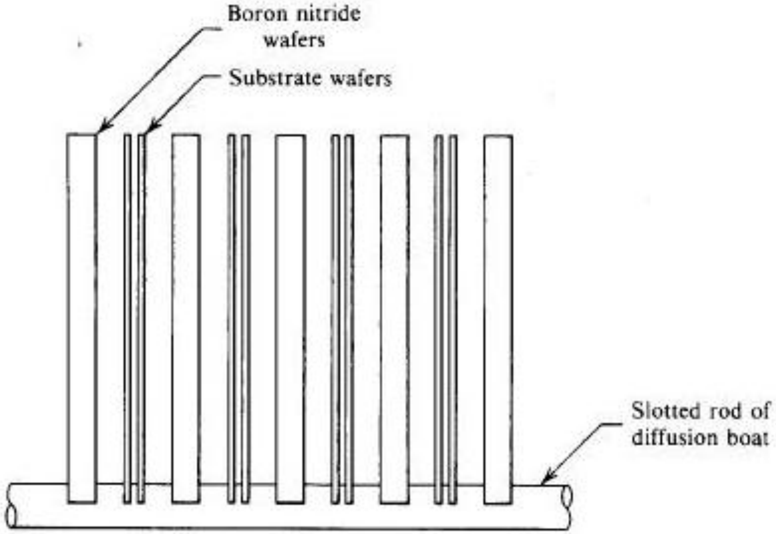


Fig. 4.29 Planar source arrangement

Table 5. SELECTED SOURCES FOR CHEMICAL DIFFUSION IN SILICON

Dopant	Gaseous Source	Liquid Source	Solid Source
As	AsH_3, AsF_3	arsenosilica^s	$AlAsO_4{}^d$
P	PH_3, PF_3	$POCl_3$, phosphosilica^s	$NH_4H_2PO_4{}^d$, $(NH_4)_2H_2PO_4{}^d$
B	B_2H_6, BF_3, BCl_3	BBr_3, $(CH_3O)_3B$ borosilica^s	BN^d
Sb	$SbH_3{}^I$	Sb_3Cl_5, antimonysilica^s	Sb_2O_3, Sb_2O_4

d = disc source s = spin on source I = ion implantation source only

Diffusion in Silicon

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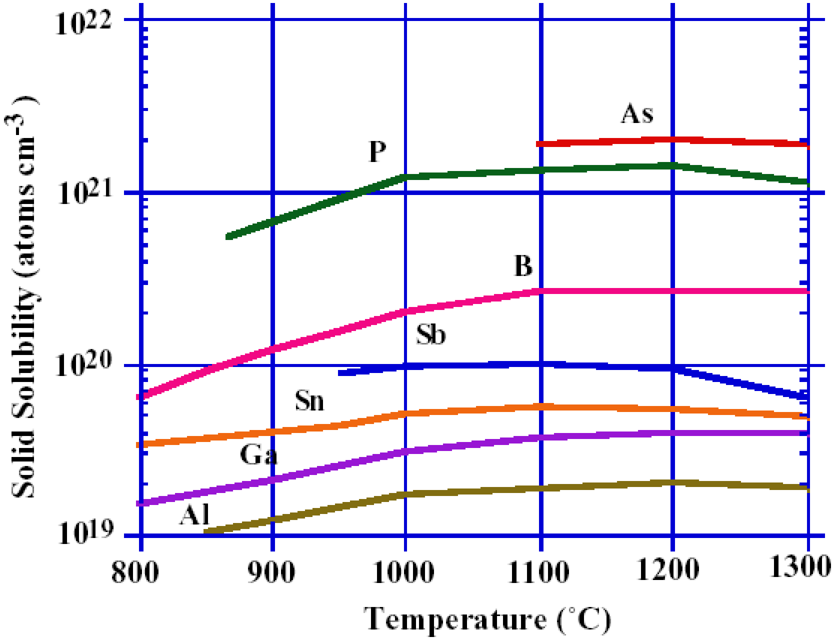
Dopant Solid Solubility

- ✓ **Solid solubility:** **The maximum concentration in equilibrium states for impurities dissolved in silicon but without any segregation phase.**
- ✓ **Solid solubility - the maximum thermodynamic concentration**
- ✓ **The maximum impurity concentration below which the electrical activity can be restricted/changed dynamically - electrical solid solubility**
- ✓ **Impurities beyond electrical solid solubility may form neutral complex and hence have no contribution to carriers in the doped region**



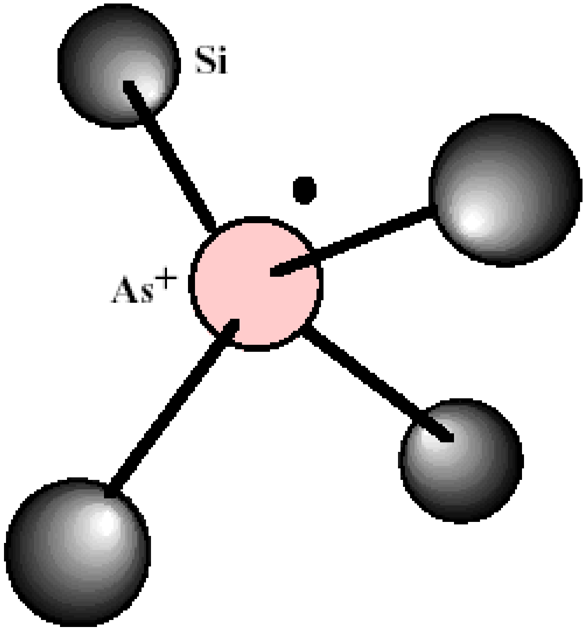
n-type: P, As, Sb

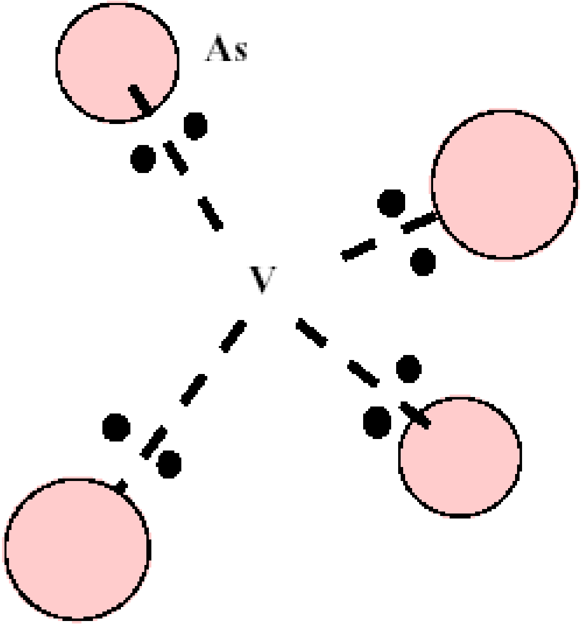
p-type: B, Al, Ga, Al

-for most dopants highest concentration below the melting point of Si

Active and Inactive Dopants in Silicon

Substituional





- As_4V is one possible electrically inactive form.

Solid solubility of As in silicon: 2×10^{21} cm^{-3}

Electrically-activable concentration of As: 2×10^{20} cm^{-3}

Intrinsic Diffusion (classical case)

Fick's two diffusion laws

Fick I: $F = -D\dfrac{\partial C}{\partial x}$

F = flow of atoms [cm^{-2}s^{-1}]
C= C(x,t) = dopant concentration [cm^{-3}]

where D = *diffusion constant* (or diffusivity) [cm^2/s]

Continuity equation: $\dfrac{\partial C}{\partial t} = -\dfrac{\partial F}{\partial x}$

Fick II: $\dfrac{\partial C}{\partial t} = \dfrac{\partial}{\partial x}\left(D\dfrac{\partial C}{\partial x}\right)$ (1)

"What goes in and does not go out, stays there."

Assume D is independent of C (and hence *x*) →

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \qquad (2)$$

Simple solution: no variation over time (C= a + bx, see oxidation).
Boundary conditions yield two different analytical solutions for *C(x,t)*.

Solution 1: Constant number of Dopants on the Surface

For example from a low-energy ion implant followed by anneal

$C(x,0) = 0$ $C(\infty,t) = 0$

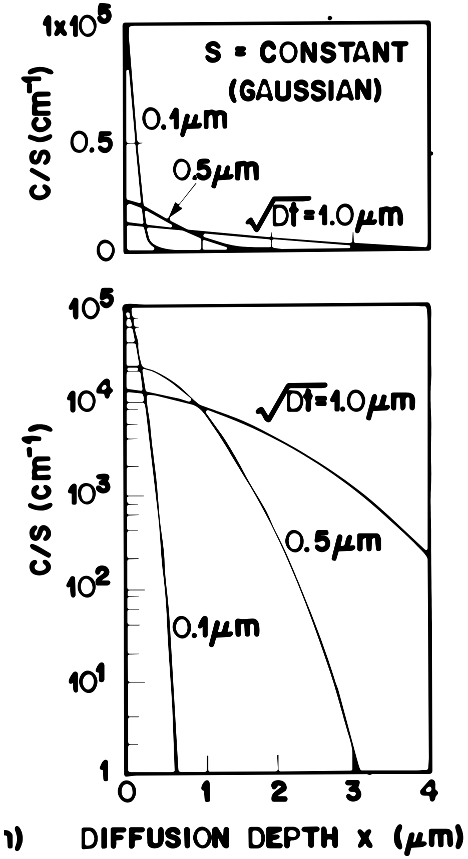
$$\int_0^\infty C(x,t)\,dx = S$$

Solution to Eq. (2) is a Gaussian profile:

$$C(x,t) = C_s(t)e^{-x^2/4Dt}$$

$$C_s(t) = \frac{S}{\sqrt{\pi Dt}}$$

$\sqrt{Dt}$ = diffusion length

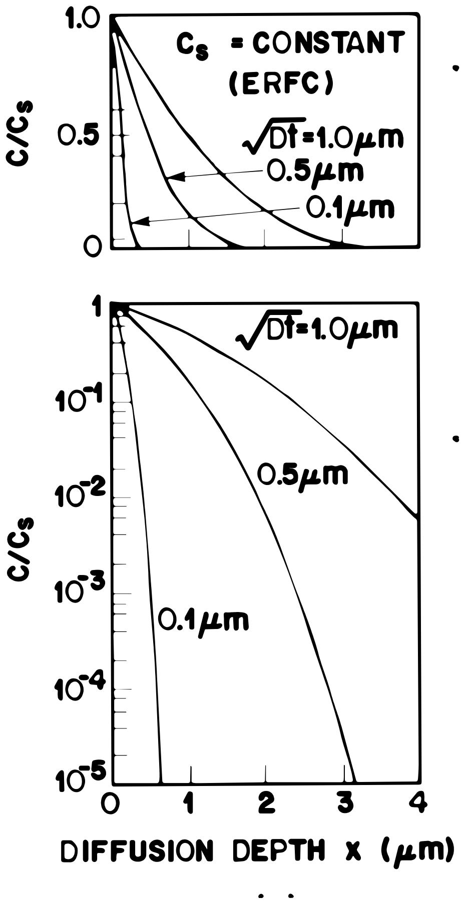


(Sze p 387)

Solution 2: Infinite number of Dopants on the Surface

Corresponds to a constant surface concentration *(= C_s)*

For example from a deposited chemical dopant source ($POCl_3$…) followed by drive-in



(Sze p 387)

$C(x,0) = 0$ $\qquad$ $C(\infty,t)=0$

$C(0,t) = C_s$

Solution to Eq. (2) is a so-called complementary error function *erfc*

$$C(x,t) = C_s\,erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

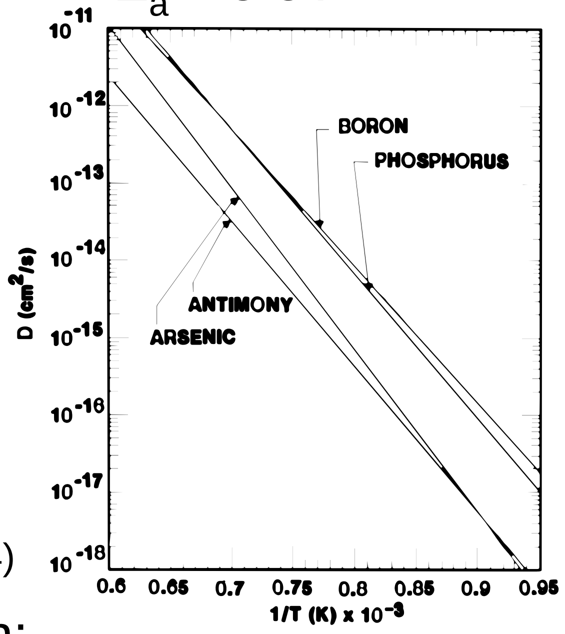
$$erfc(z) = 1 - \frac{2}{\sqrt{\pi}}\int_0^z e^{-a^2}\,da$$

Diffusion: Temperature dependence

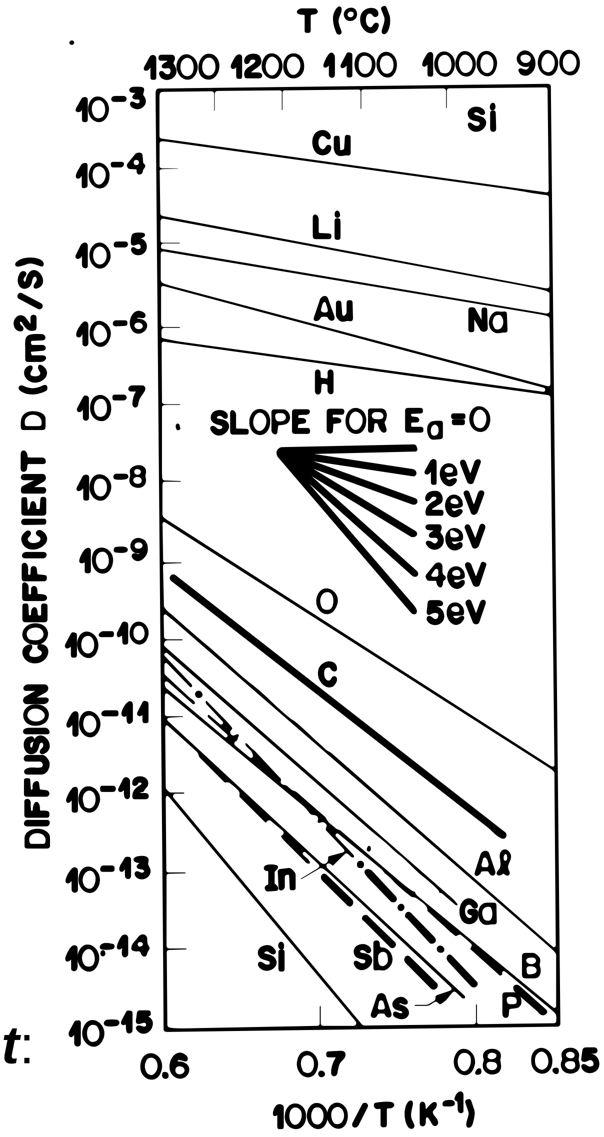
$$D = D_o e^{-E_a/kT}$$ where E_a = activation energy

Dopant diffusion in Si: E_a= 3.5-4.5 eV

Self-diffusion in Si: E_a = 5 eV



(Sze p. 384)



Process Integration:

Thermal budget in a process is often attributed to the *Dt* product. Total process ***thermal budget***:

$$Dt = D_1t_1 + D_2t_2 + D_3t_3 + \dots$$

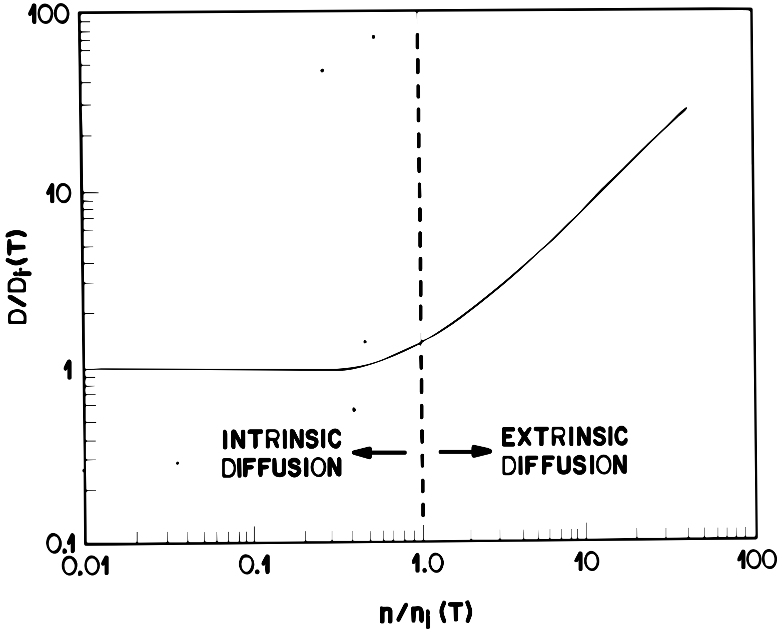
Extrinsic Diffusion: Concentration Dependence

High impurity concentrations 10^{19} - 10^{20} cm^{-3}

Denoted *extrinsic* diffusion case since

$C > n_i$ (intrinsic carrier concentration) →

$D = D(C)$ → Solution of Eq. (1) required (numerically computed)



E.g. N_i (T=1000ºC) = 7×10^{18} cm^{-3}

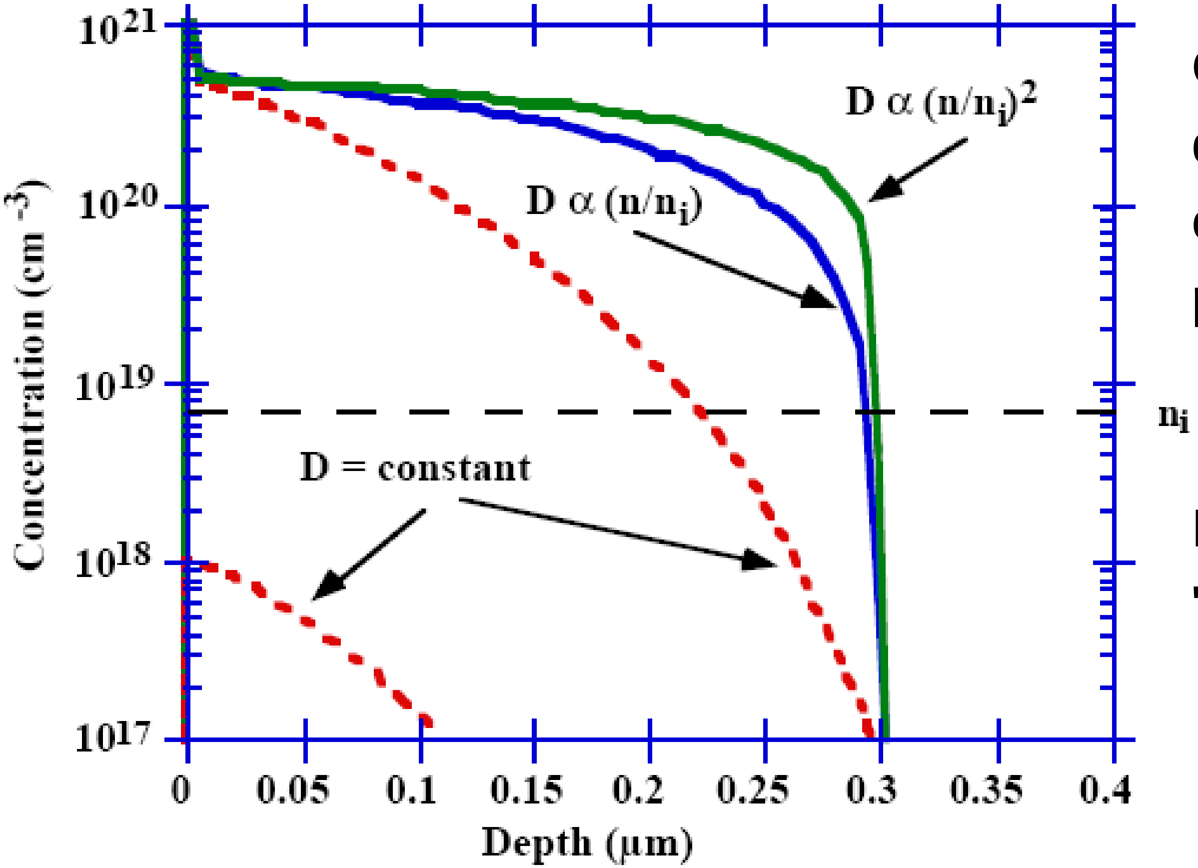
Fig. 7 Donor impurity diffusion coefficient versus electron concentration showing regions of intrinsic and extrinsic diffusion.[8]

(Sze p. 392)

Extrinsic Diffusion: Concentration Dependence

Modifications to Fick’s law:

Generalized D expression (n-type Si): $D = D_0 + D^{-}\left(\frac{n}{n_i}\right) + D^{=}\left(\frac{n}{n_i}\right)^2$



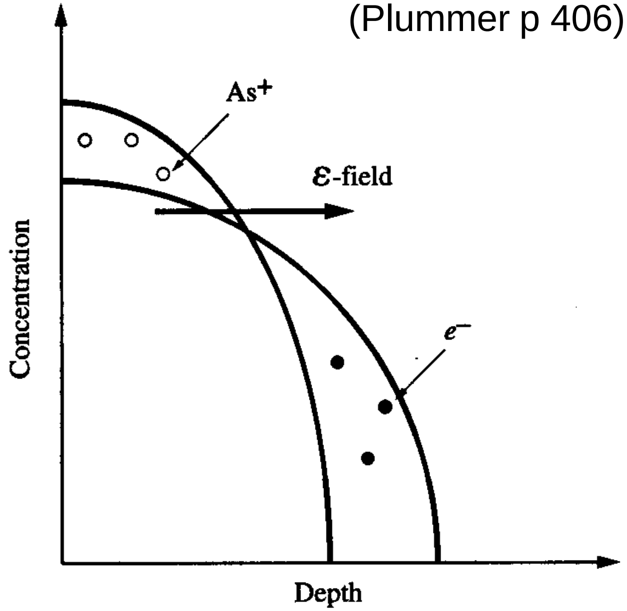
On atomic level, D-terms are determined by neutral and charged point defects (D^+ for p-type)

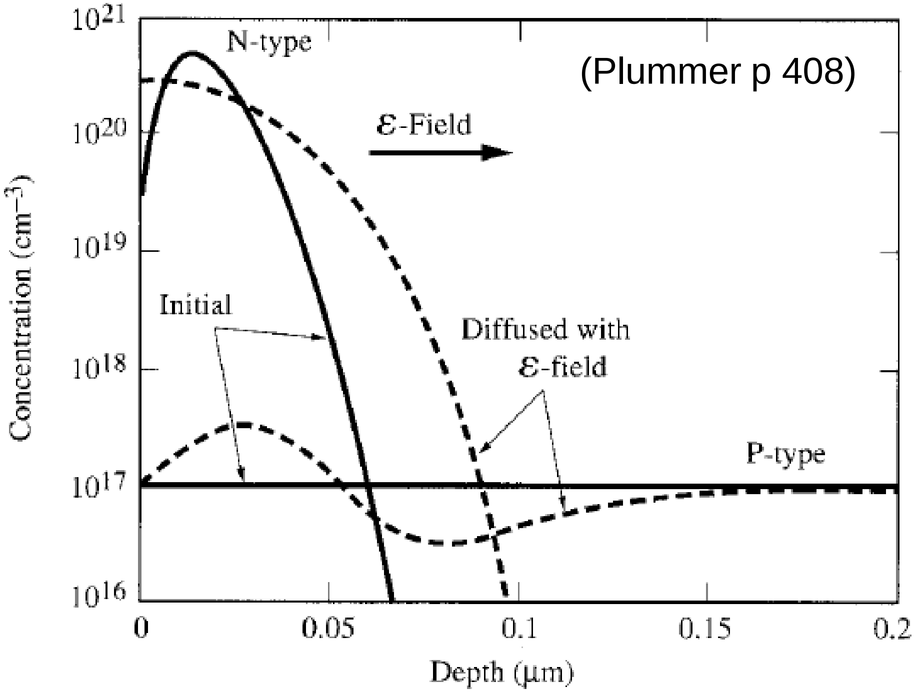
Result:

"Box-like" diffusion profiles

Extrinsic Diffusion: Electrical Field Effect

- For extrinsic diffusion, electrical fields from dopants affect final profiles.
- E.g. electrons diffuse faster than donors


(Plummer p 406)


(Plummer p 408)

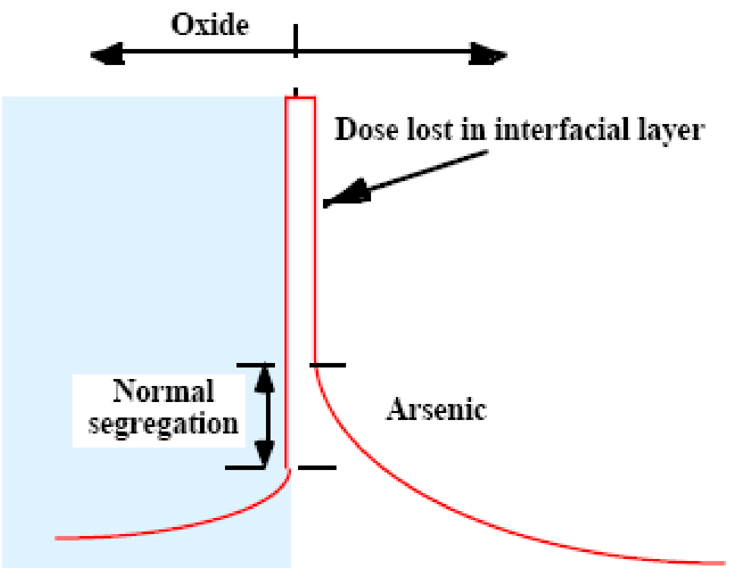
- Electrical field drags dopants into the bulk: Enhanced diffusion by a factor 1-2
- Simulation example pn junction

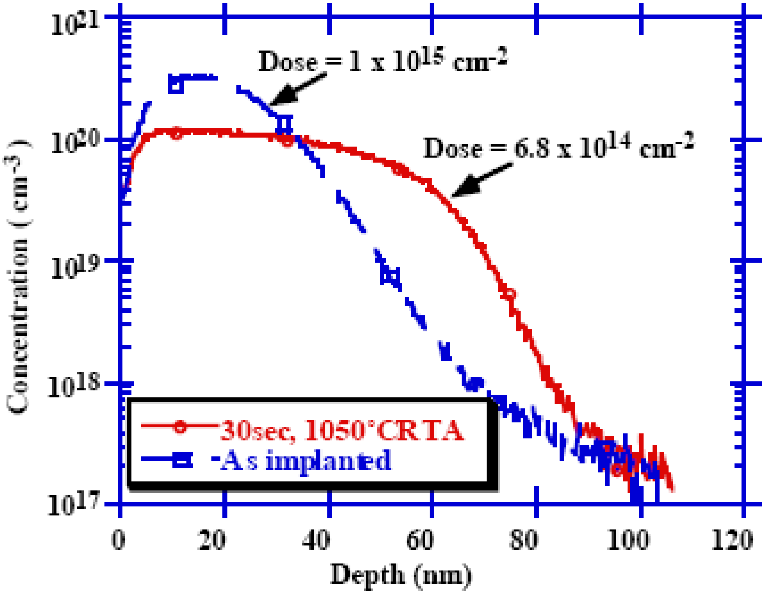
Figure 7–26 Simulation of the ℰ-field effect using TSUPREM IV [7.14] at 1000°C. The electric field causes the diffusion of the low-concentration boron to be drastically affected in the vicinity of the junction.

Process simulators include concentration dependence and electric field effect

Diffusion: Dopant Pileup (on addition to Segregation)

- Dopants may also segregate to an interface layer, perhaps only a monolayer thick. Interfacial dopant dose loss or pile-up may consume up to 50% of the dose in a shallow layer.





- In the experiment (right) 40% of the dose was lost in a 30 sec anneal.

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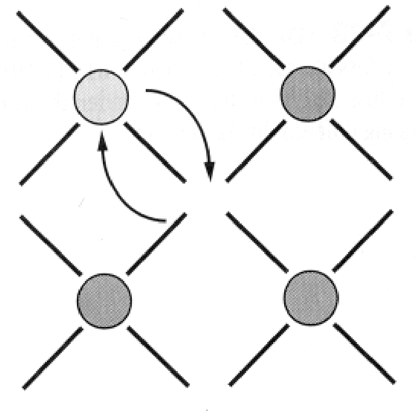
Microscopic Description of Diffusion

- The extended diffusion model is not able to explain several anomalies observed in diffusion of impurities in Si.
- A microscopic (atomistic) description is needed.
- Diffusion is the interaction between individual impurity atoms and point defects in the lattice:

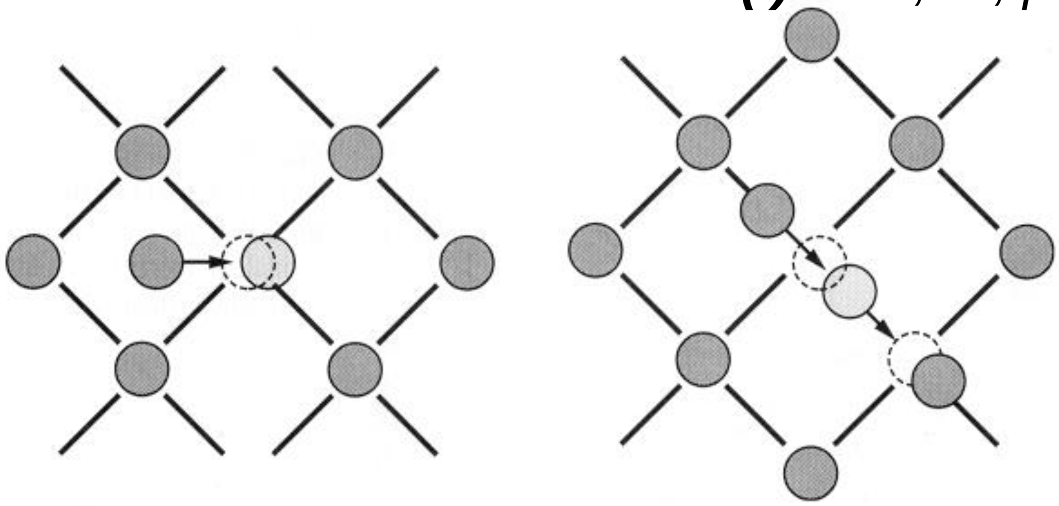
Vacancy-assisted diffusion: *(V)* *Sb, partly As*



Large atoms e.g. Sb prefer *V*

Microscopic Description of Diffusion

Interstitial-assisted diffusion: *(I)* *B,Ph, partly As*



Small atoms, e.g. B prefer *I*

Figure 7–35 Schematic of interstitial assisted kick-out diffusion (left) and interstitialcy-assisted diffusion (right) mechanisms.

(Plummer p 418-9)

Formulation: $A + I \leftrightarrow AI$ where A is impurity atom

Defects I and *V* can be neutral or charged

Diffusion during Thermal Oxidation

Formation of SiO2 → volume expansion → compressive stress which is relieved by injection of *I*

Consequences:

Diffusion of B and Ph enhanced

OED = oxidation-enhanced diffusion

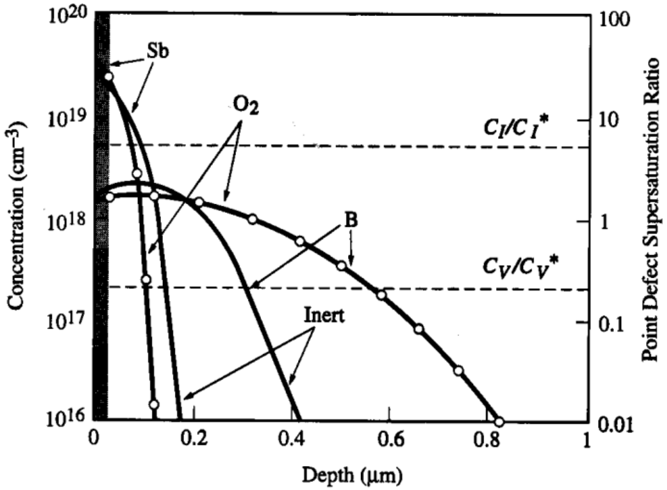
Diffusion of Sb retarded

ORD = oxidation-retarded diffusion

Concentration of *V* is reduced by recombination with *I*

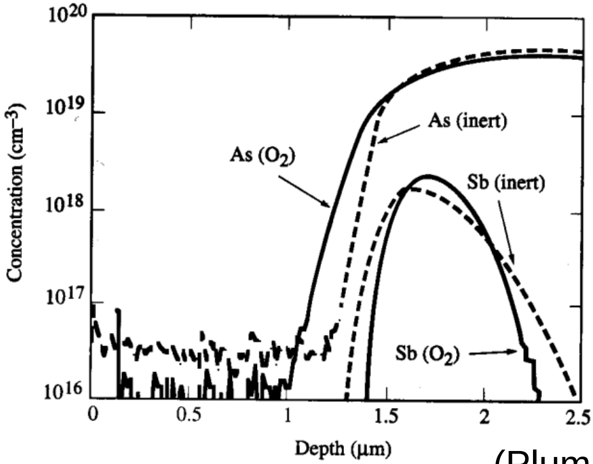
Diffusion of As somewhat enhanced

Simulations:



(Plummer p 420)

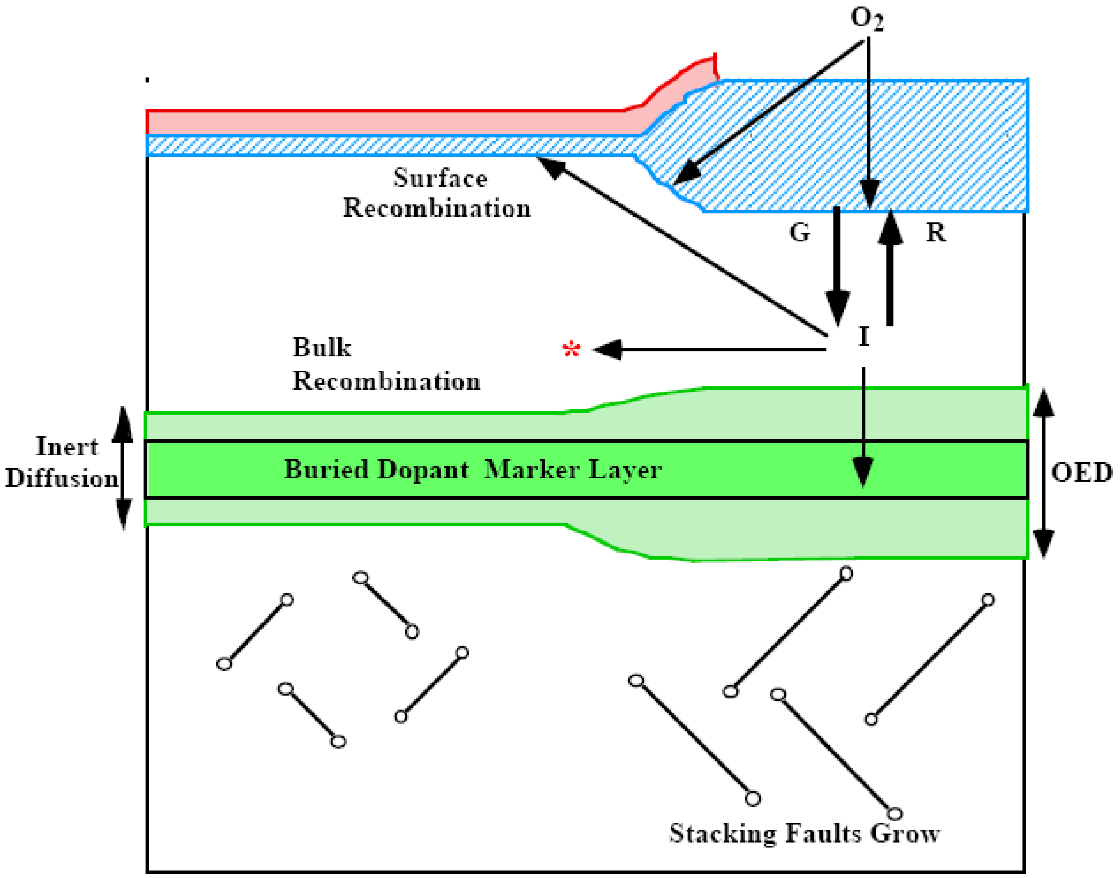
Experiment:



(Plummer p 422)

Also oxidation-induced stacking faults (OSF) explained by *I* injection

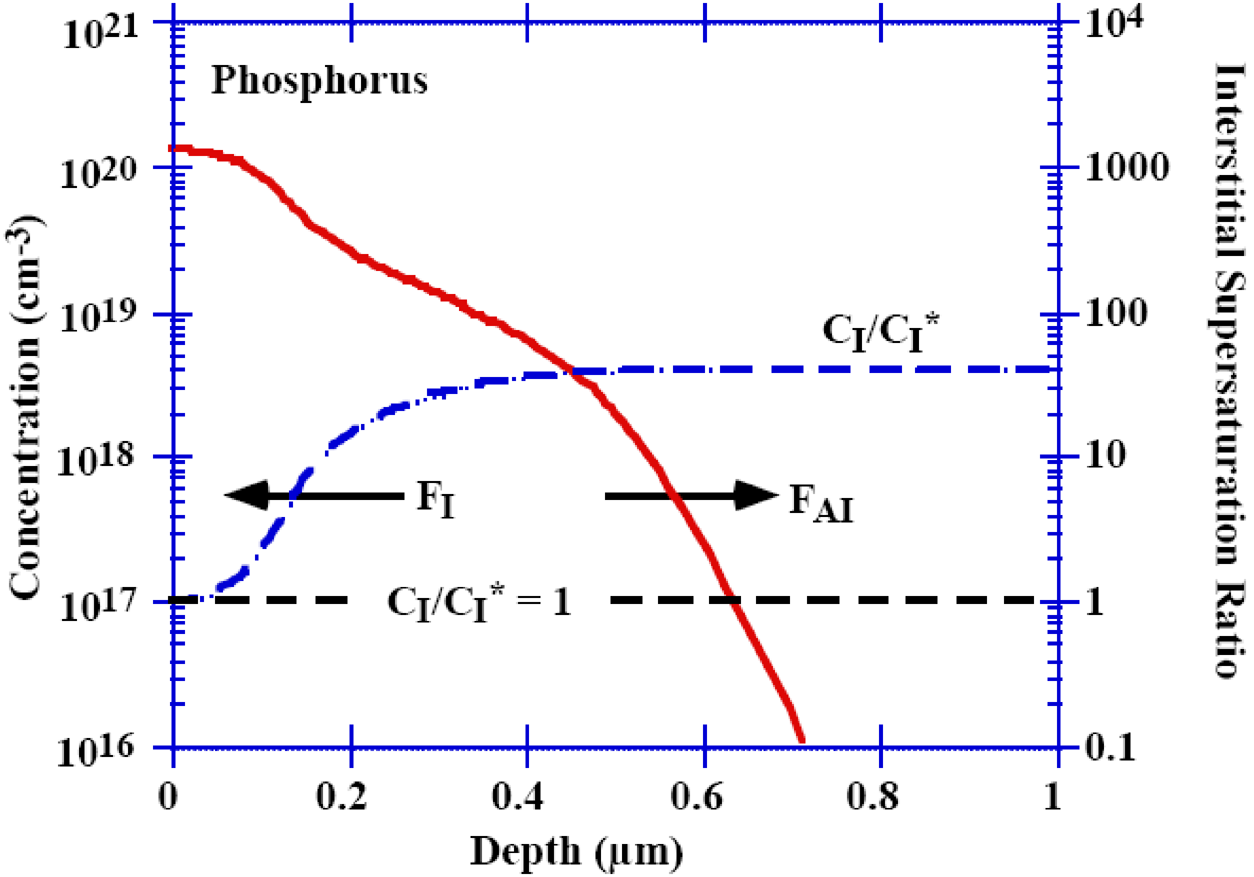
Diffusion during Thermal Oxidation



- Oxidation provides an I injection source.
- Nitridation provides a V injection source.
- Stacking faults serve as "detectors" as do dopant which diffuse.

Dopant-Defect Interactions

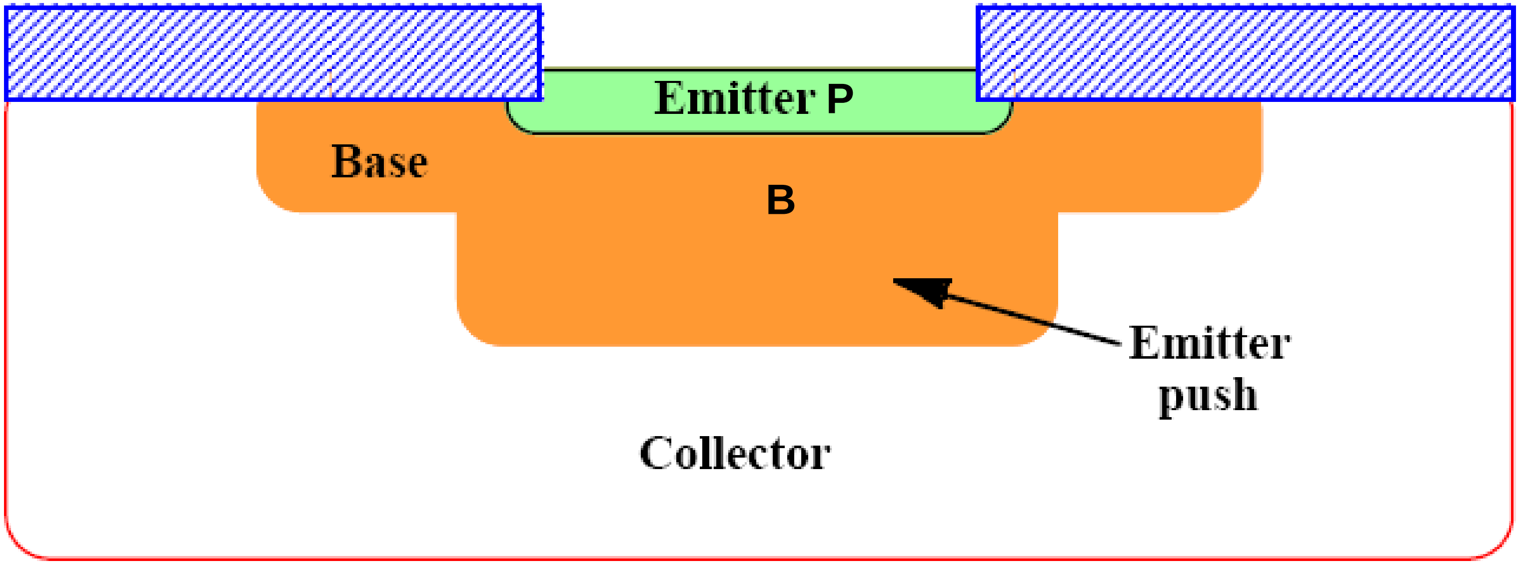
- P diffusion at high conc. generates silicon ***interstitials*** which are "pumped" into the bulk
- → from surfaces a strong source of interstitials from kinks and ledges, this causes a supersaturation of interstitials in the substrate



Dopant-Defect Interactions

Example:

- Pumping of *I* from kink region is responsible for the "emitter push" effect in bipolar transisitors, *i.e.* base widening
- The injected *I* from the emitter will act to enhance B diffusion
- Primary reason why As replaced P as emitter dopant



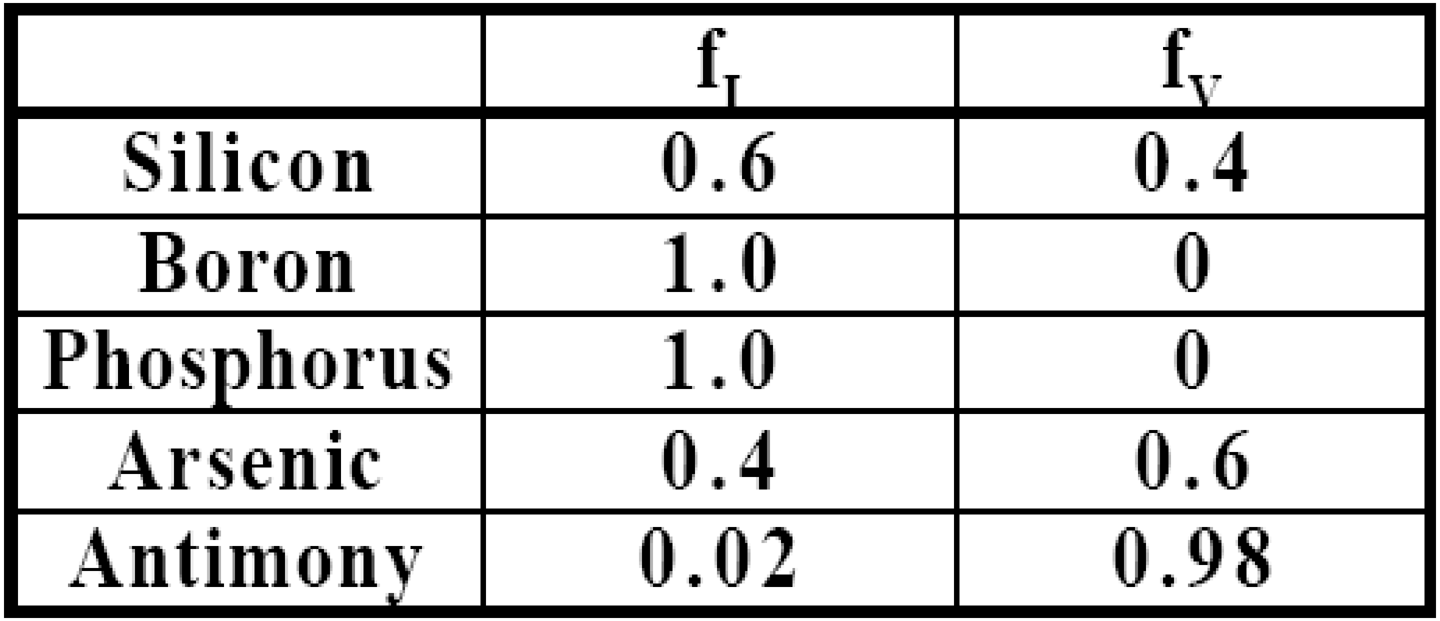
Dominant Diffusion Mechanism

Dopants diffuse with a fraction

f_I interstitial-type diffusion mechanism

AND with a fraction

$f_V = 1 – f_I$ vacancy-type mechanism



	f_I	f_V
Silicon	0.6	0.4
Boron	1.0	0
Phosphorus	1.0	0
Arsenic	0.4	0.6
Antimony	0.02	0.98

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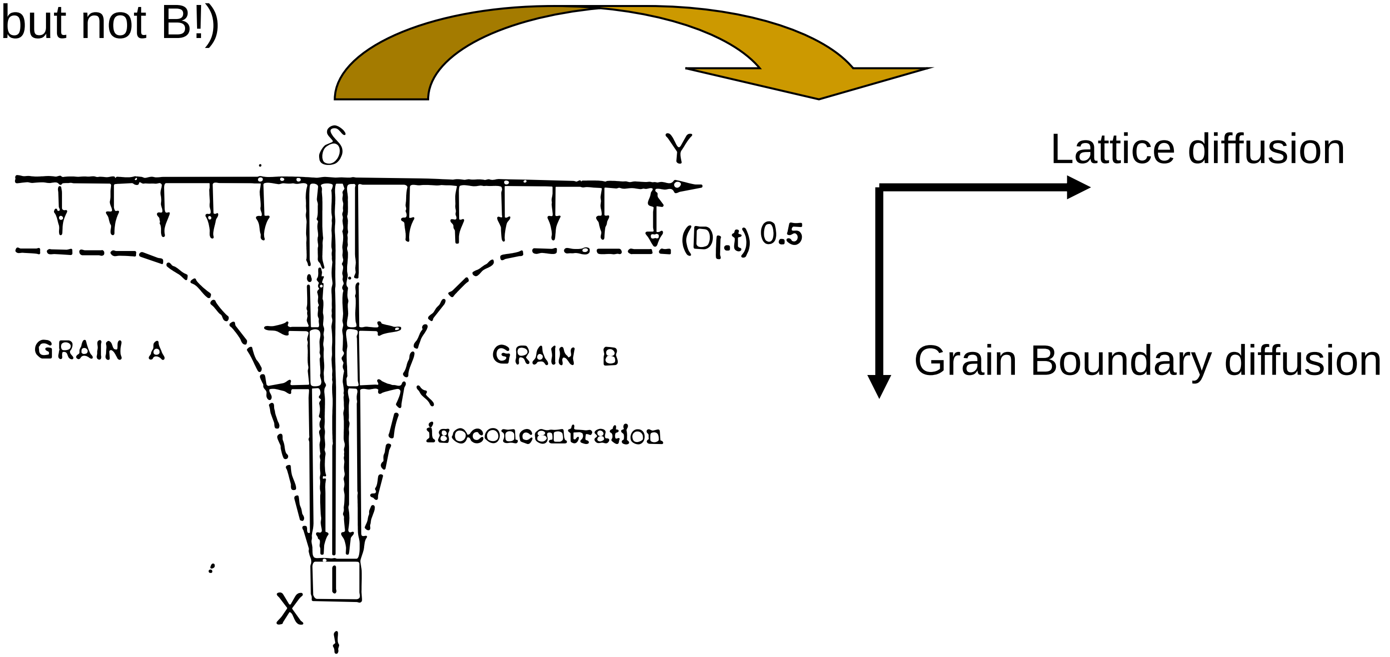
    - Dopant-Defect Interactions
- Diffusion in Polysilicon
- Characterization

Impurity Diffusion in Polysilicon

Diffusion of dopants occurs both inside grains and between grains (*i.e*. in grain boundaries)

- Diffusion in grain-boundary is typically 100-1000 larger than inside a grain
- Texture and grain size of the poly largely influence the electrical properties
- Impurities themselves also affect grain growth (e.g. P enhances grain growth)
- During activation of heavily-doped polysilicon segregates P and As impurities to grain boundaries (but not B!)



Diffusion in silicon

- Introduction
  - Dopants in Silicon Devices
  - Technology for diffusion
- Diffusion
  - Solid solubility
  - Intrinsic diffusion and diffusion constant (Fick’s Law)
  - Extrinsic diffusion and electrical field effect
- Microscopic description
  - Diffusion during thermal oxidation
  - Dopant-Defect Interactions
- Diffusion in Polysilicon
- Characterization

Characterization of Diffused Profiles

1-D profiles:

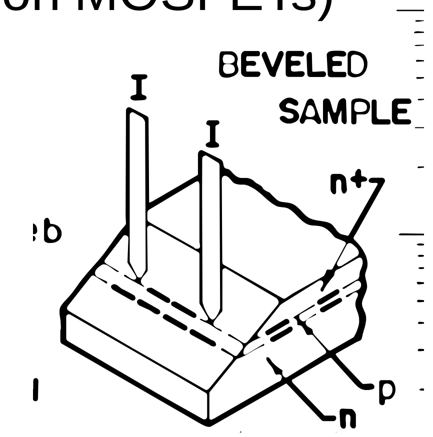
Chemical profile:
SIMS (Secondary ion mass spectrometry) gives chemical concentration with very good sensitivity (ppb) and resolution

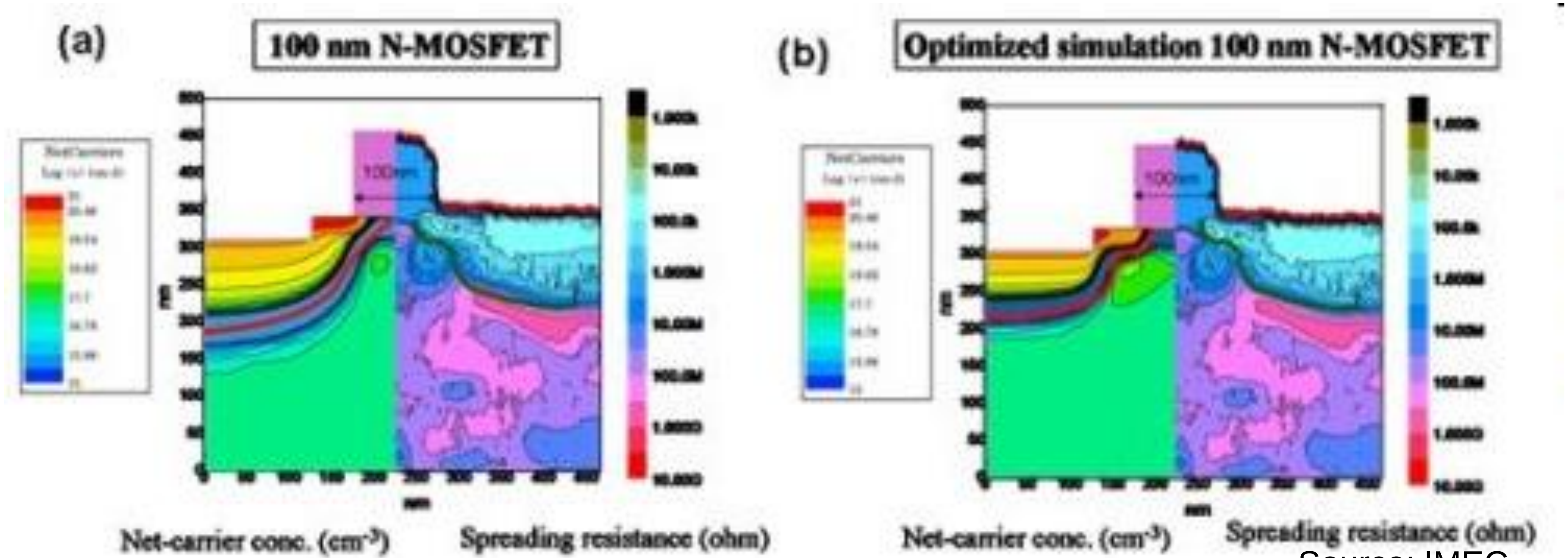
Electrically-activated dopants:
Sheet resistance
Spreading resistance (see picture on next slide)
Differential conductivity such as Hall (DHE) (anodic oxidation for depth profiling)
C-V

Characterization of Diffused Profiles (SSRM)

2-D profiling very difficult (but needed for deep-submicron MOSFETs)

- XTEM + FIB with chemical etches
- Scanning capacitance microscopy (SCM)
- Scanning Spreading Resistance Microscopy (SSRM)
  - E.g. fine tune the Kinetic Monte Carlo simulations of laser annealing





Source: IMEC

Summary of key ideas

- Selective doping is a key process in fabricating semiconductor devices.
- Doping atoms generally must sit on substitutional sites to be electrically active.
- Both doping concentration and profile shape are critical in device electrical characteristics.
- Ion implantation is the dominant process used to introduce dopant atoms. This creates damage and thermal annealing is required to repair this damage.
- During this anneal dopants can diffuse much faster than normal
- Atomistic diffusion processes occur by pairing between dopant atoms and point defects.
- In general diffusivities are proportional to the local point defect concentration.
- Point defect concentrations depend exponentially on temperature, and on Fermi level, ion implant damage, and surface processes like oxidation.
- As a result dopant diffusivities depend on time and spatial position during a high temperature step.
- Powerful simulation tools exist today which model these processes and which \ can predict complex doping profiles.

Lecture 6

I Annealing

II Diffusion

III Ion Implantation

Lecture 6: Overview

- Introduction
- Technology and Applications
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- Extended Model for *a*-Si
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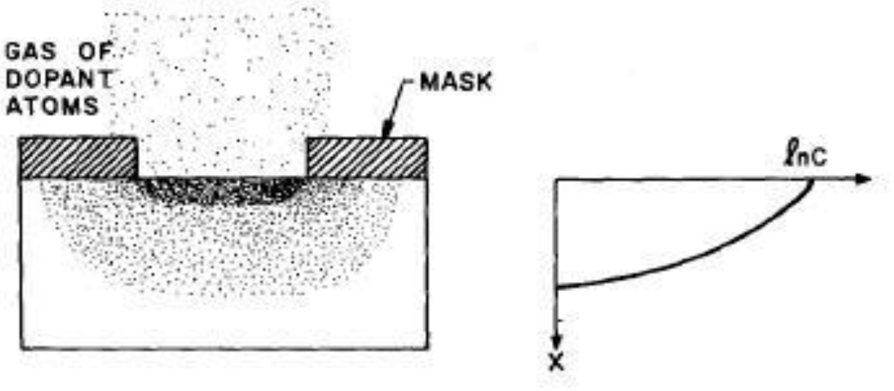
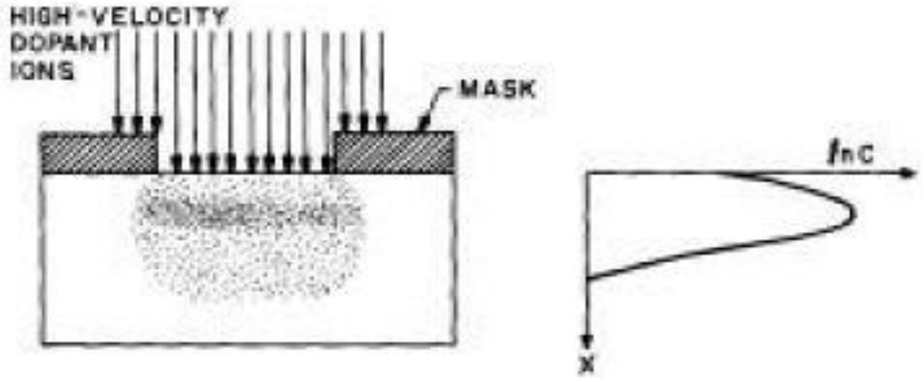
- Annealing
  - Damage
  - Activation

Ion Implantation: Introduction

Doping method	**Control parameters**
Diffusion	Time and temperature
Ion implantation (I/I)	Current (dose) and voltage (energy)



Diffusion



Ion Implantation

:e p.381)

Ion Implantation: Introduction

Advantages of Ion Implantation (I/I):

- Low temperature process (hardened resist mask can be used up to ~120°C)
- Accurate measurement of dose using a Faraday cup
- Good control of resulting vertical dopant profile
- Lateral engineering possible by tilted implants
- Very uniform doping across wafer

Disadvantages of I/I:

- I/I introduces crystal damage which requires subsequent annealing at high temperature
- Anomalous enhanced impurity diffusion during annealing after I/I

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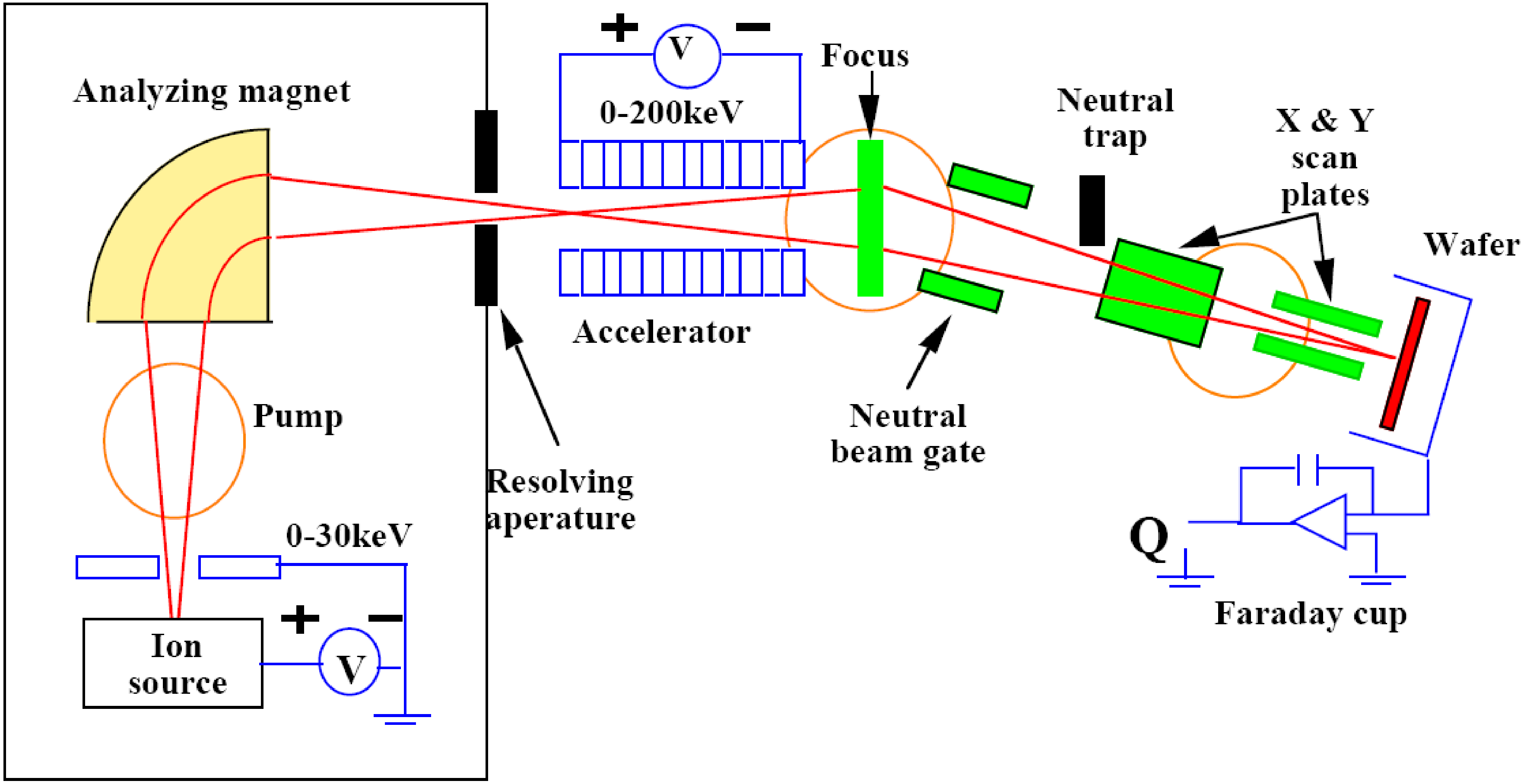
Ion Implantation Technology

Schematics of an Implantation Tool



Ion Implantation Technology

Basic Operation

Energy range	200 eV up to several MeV
Ion current *I*	Up to 30 mA
Dose range	10^{11} up to $2\text{x}10^{16}$ cm^{-2}
Gaseous ion sources	BF_3 (for BF_2 and B), Ar
Solid ion sources	As, Sb, Ph, Ge, Si

$$Dose = \frac{1}{A}\int \frac{I}{q} dt$$

where *A* = implanted area

Mass separation

$$\frac{Mv^2}{R} = q \cdot \vec{v} \times \vec{B}$$

V= extraction voltage
B = magnetic field
R = radius of analyzing magnet
v = ion velocity

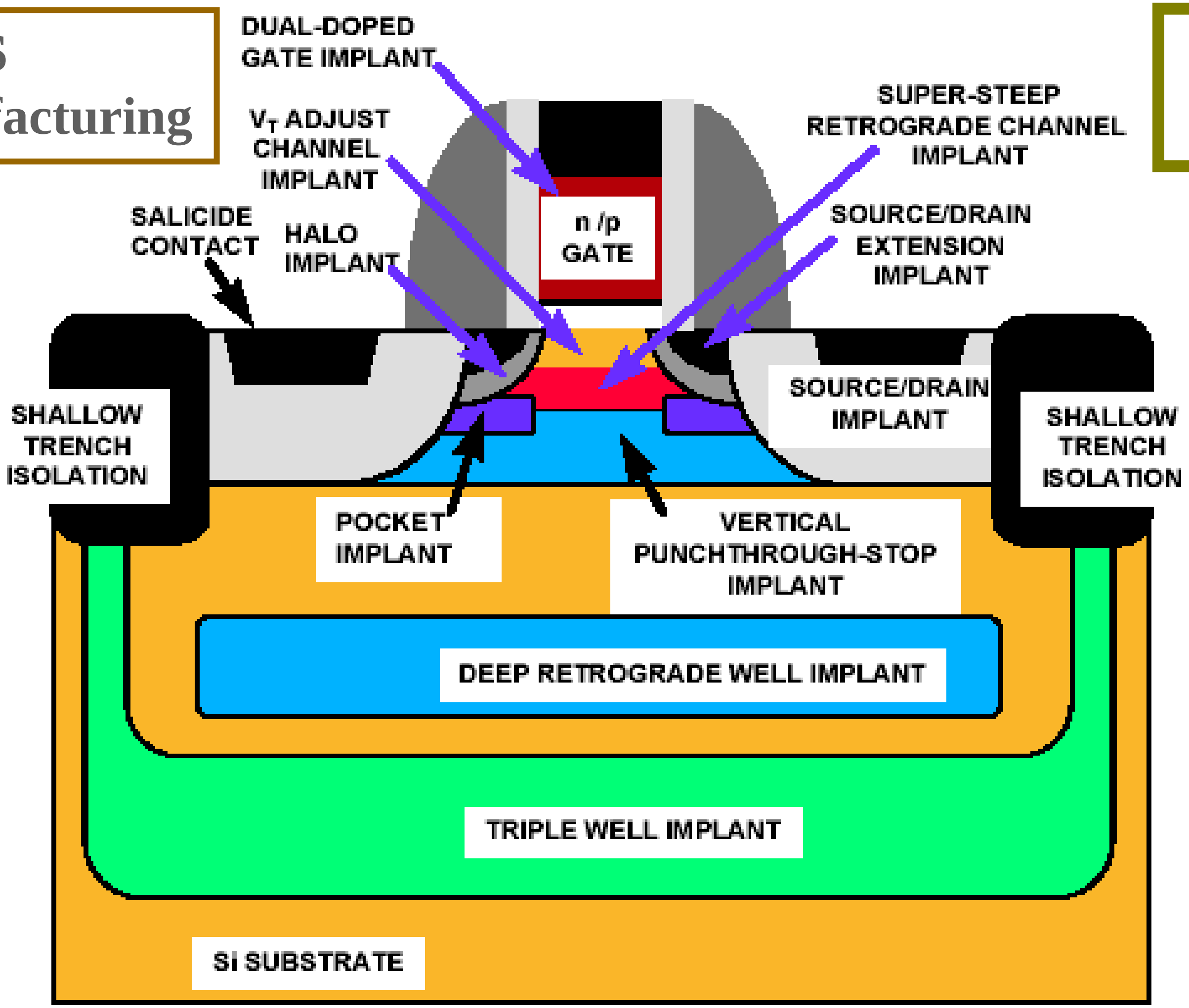
$$RB = \sqrt{\frac{2MV}{q}}$$

Permits separation of ion with mass *M* and charge *q*

Ion Implantation: Application in ICs

CMOS Manufacturing

9-10 different I/I identified !

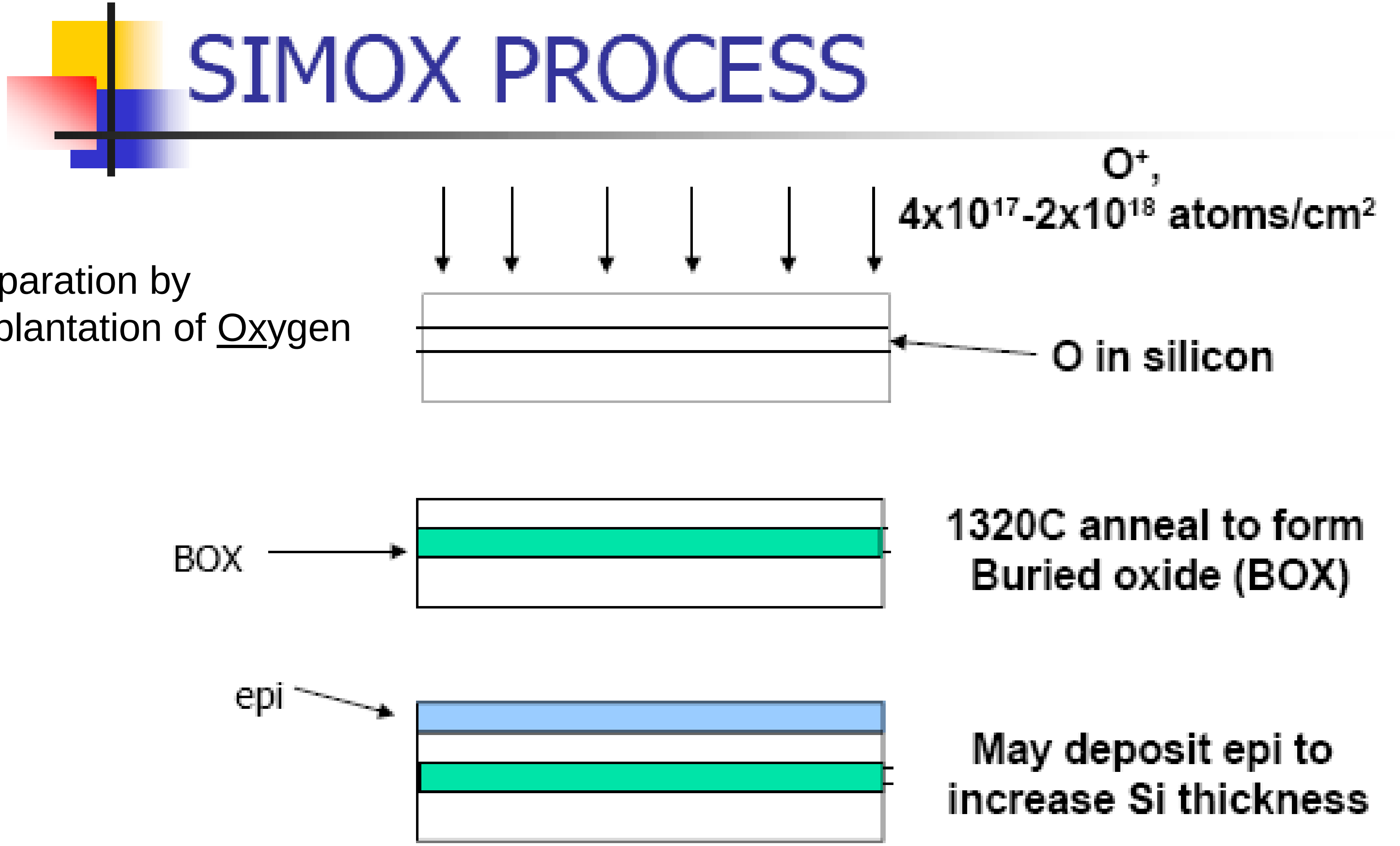


Source/Channel/Drain
50-200 nm deep
10^{17}-10^{20} atoms/cm^3

CMOS Well
500-3000 nm deep
10^{15}-10^{17} atoms/cm^3

Ion Implantation: Application in SOI Wafer Fabrication

Separation by
Implantation of Oxygen



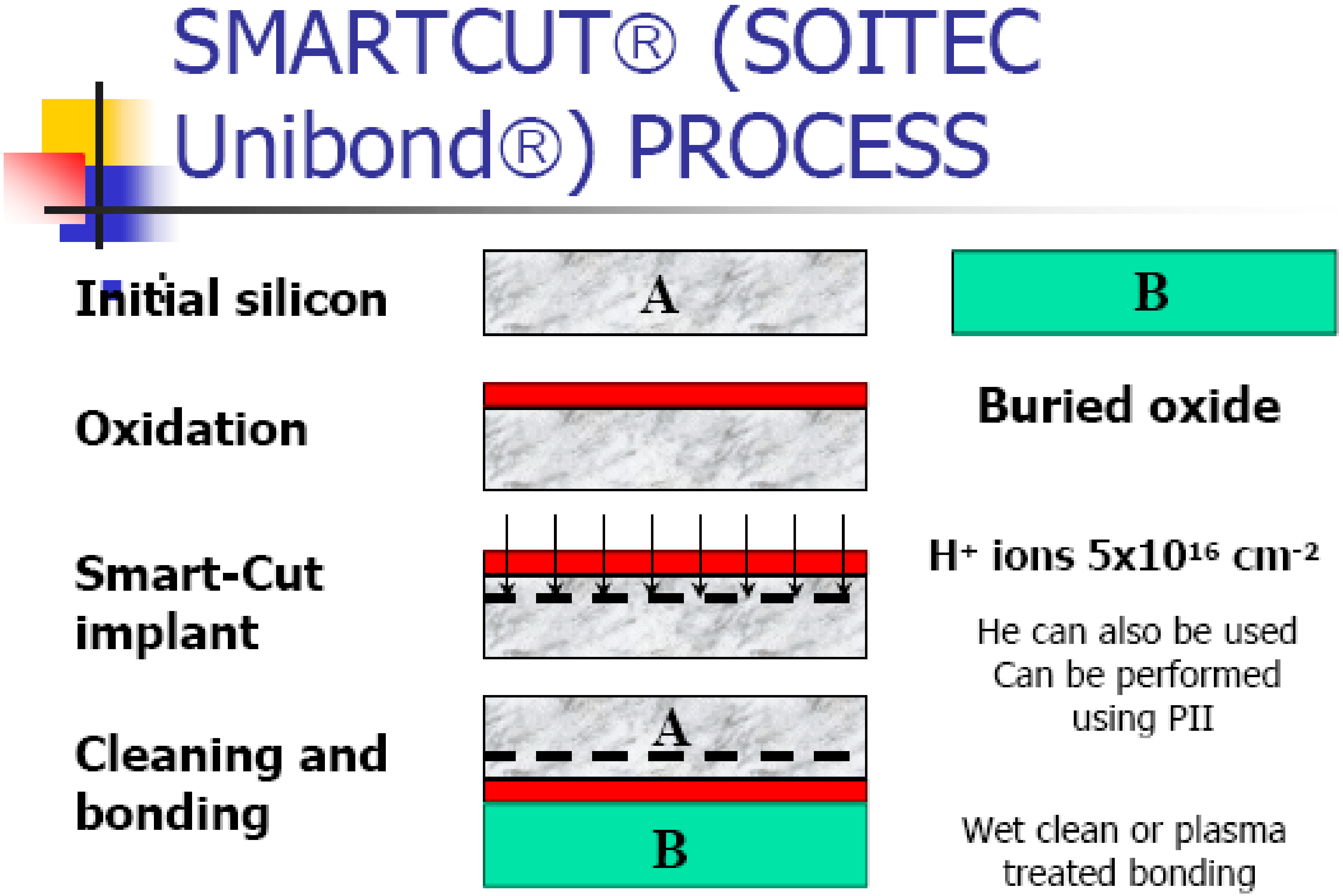
SIMOX PROCESS

O^+,
4×10^{17}-2×10^{18} atoms/cm^2

1320C anneal to form
Buried oxide (BOX)

May deposit epi to
increase Si thickness

Ion Implantation: Application in SOI Wafer Fabrication



SMARTCUT® (SOITEC Unibond®) PROCESS

Initial silicon	
Oxidation	Buried oxide
Smart-Cut implant	H^+ ions 5×10^{16} cm^{-2} He can also be used Can be performed using PII
Cleaning and bonding	Wet clean or plasma treated bonding

Lecture 6-2: Overwiew

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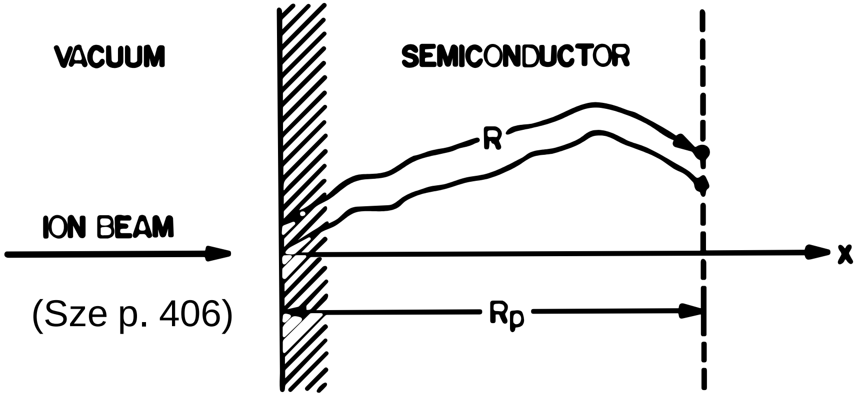
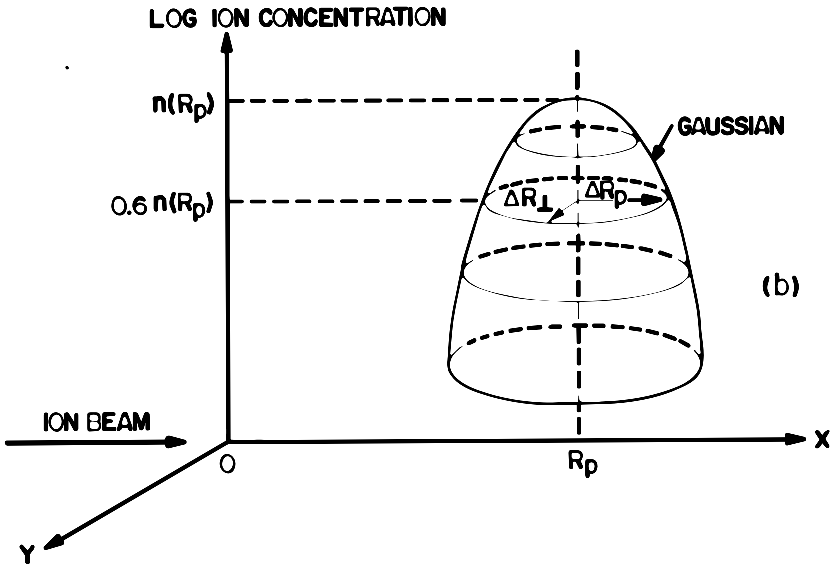
Range of Implanted Ions

- Random collisions in crystal determine the ion path
- First-order model neglecting backscattering, sputtering, secondary e^-



(Sze p. 406)

Schematic of the ion range R and projected range R_p



Two-dimensional distribution of the implanted ions

Statistical fluctuations in R→ standard deviation expressed as:

Projected straggle = ΔR_p,
Lateral straggle = $\Delta R_\perp$

Ion Implantation: Basic Theory

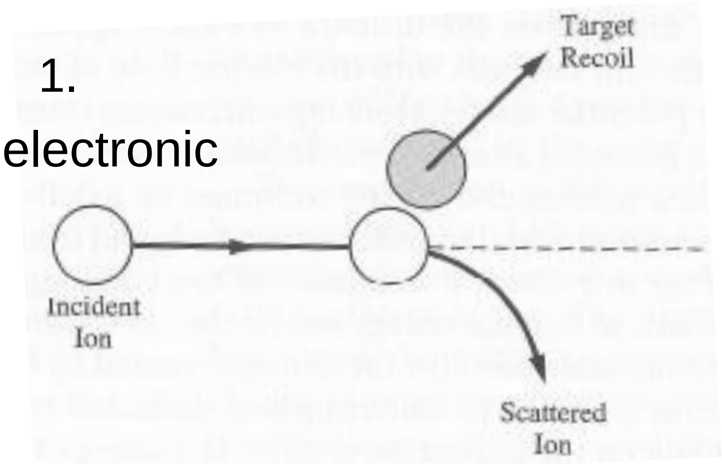
M_1 = Ion mass
M_2 = Target atom mass
E_0 = Initial energy

Range R is calculated from:

$$R = \int_0^R dx = \int_0^{E_0} \frac{dE}{S_n(E) + S_e(E)}$$

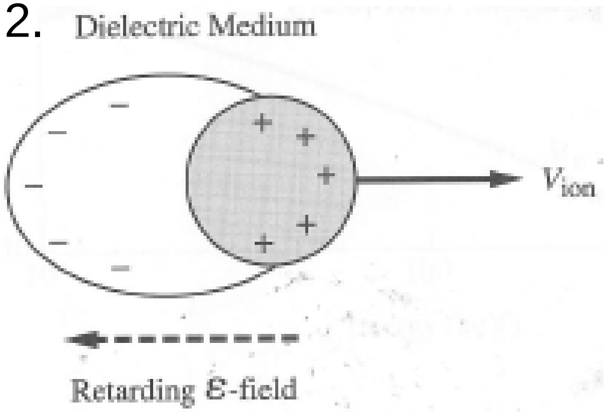
where $S_n(E)$ and $S_e(E)$ are the nuclear and electronic stopping power, respectively.

1.



1. Nuclear stopping $S_n(E)$
   Elastic collisions → $S_n(E) \propto E$ at low energies, then decreases [screening function]

2.



2. Electronic stopping $Se(E) \propto E^{1/2}$
   Polarization lags behind moving ion

Basic theory cont'

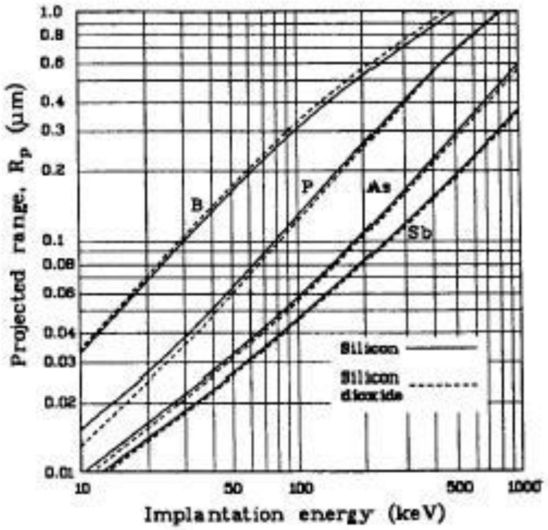
Total stopping: $S = \frac{dE}{dx} = S_n(E) + S_e(E)$ [eV/Å]

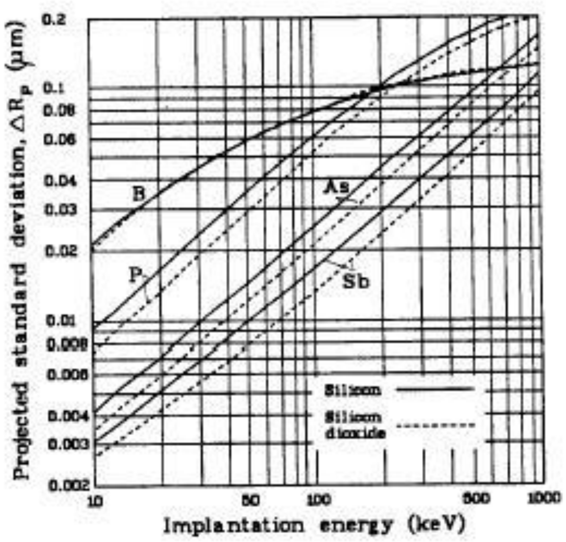
R_p and ΔR_p from the Lindhard-Scharff-Schiott theory:

$$R_p \cong \frac{R}{1 + \frac{M_2}{3M_1}}$$

Range and straggle for *amorphous* Si:

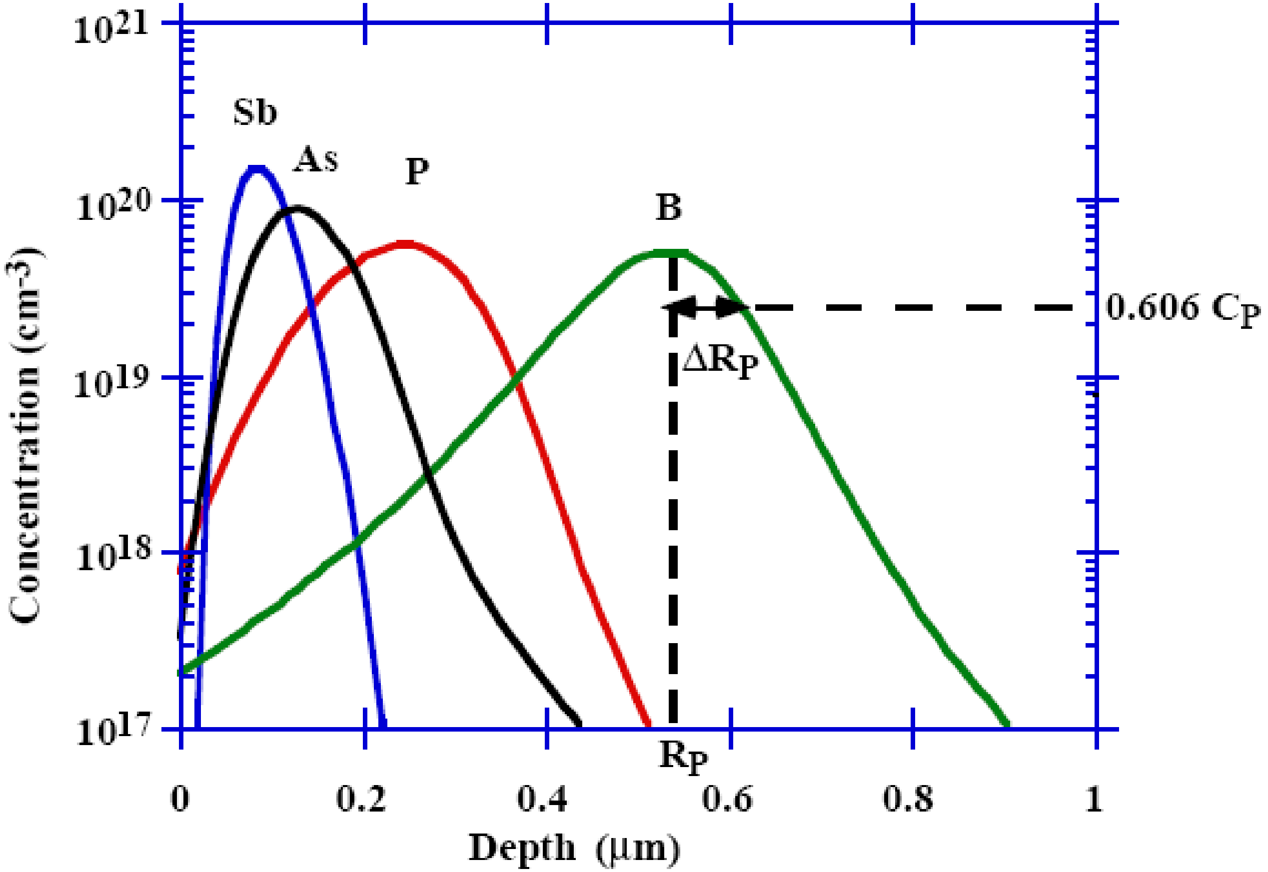
$$\Delta R_p \cong \frac{2}{3}\left[\frac{\sqrt{M_1 M_2}}{M_1 + M_2}\right] R_p$$





Distribution of Implanted Ions

- Profiles can often be described by a Gaussian distribution, with a projected range and standard deviation
- Example: 200keV implants of Sb, As, P and B



Distribution of Implanted Ions

Simplest model:

Gaussian with standard deviation ΔR_p symmetric around R_P

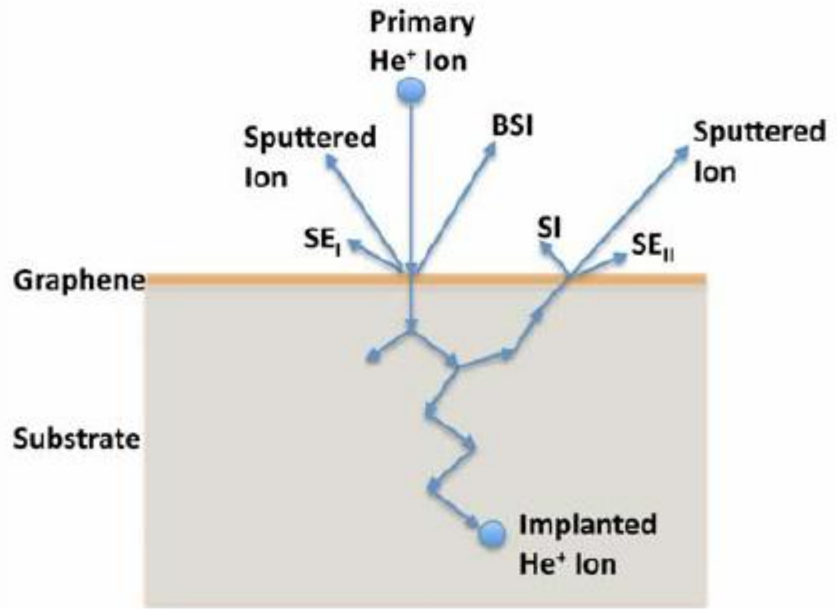
$$N(x) = N_0 e^{\left(\frac{-(x-R_p)^2}{2\Delta R_p^2}\right)}$$

$$N_0 = \frac{\Phi}{\sqrt{2\pi}\Delta R_p}$$ (peak concentration)

Definition implanted dose: $\Phi = \int_{-\infty}^{+\infty} N(x)dx$

However, experimental profiles are quite different, *e.g.* B

Primarily because of back-scattering of B ions during I/I.
→ Extended Model →



Schematic of the interactions of primary energetic He ions with a graphene layer on SiO2 substrate, showing the production of secondary electrons (SEI at the primary beam and SEII at the secondary scattered ion exiting the surface), back scattered ions (BSI) and secondary ions (SI).

Bell et al. Nanotechnology **20** (2009) 455301

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Extended Model: Four-moment distribution

Realistic profiles using the so-called Pearson IV distribution

Range: $$R_P = \frac{1}{Q}\int_{-\infty}^{\infty} x\, C(x)\, dx$$

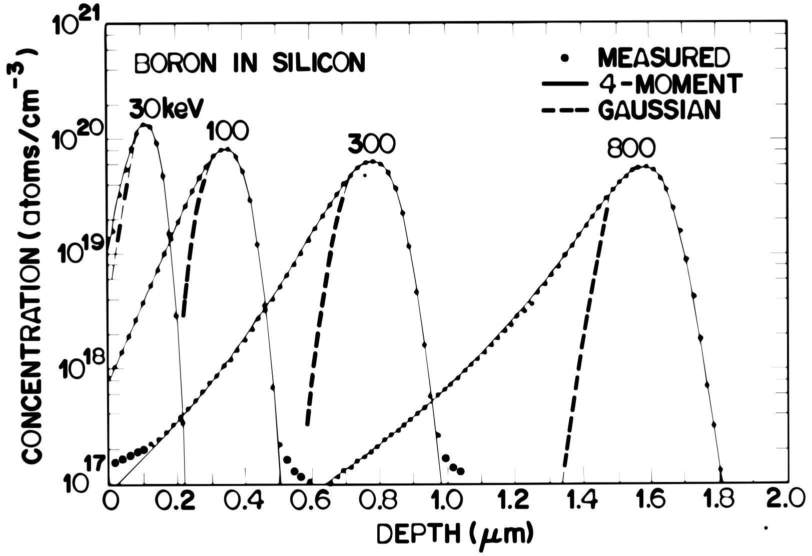
Std. Dev: $$\Delta R_P = \sqrt{\frac{1}{Q}\int_{-\infty}^{\infty} (x - R_P)^2\, C(x)\, dx}$$

Skewness: $$\gamma = \frac{\int_{-\infty}^{\infty} (x - R_P)^3\, C(x)\, dx}{Q\, \Delta R_P^3}$$

asymmetry of distribution

Kurtosis: $$\beta = \frac{\int_{-\infty}^{\infty} (x - R_P)^4\, C(x)\, dx}{Q\, \Delta R_P^4}$$

flatness of top region
“peakedness”



(Sze, VLSI p 335)

Provided Si surface amorphous, the Pearson IV can also be applied to crystalline Si.

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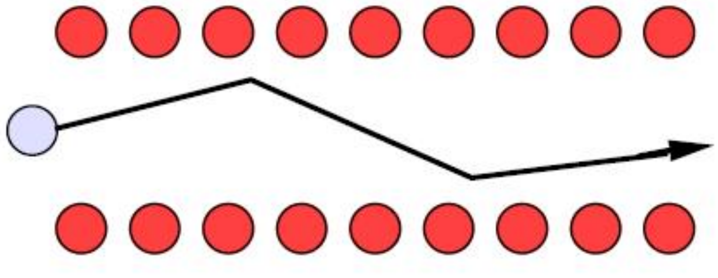
Channelling

Channeling can produce unexpectedly deep profi



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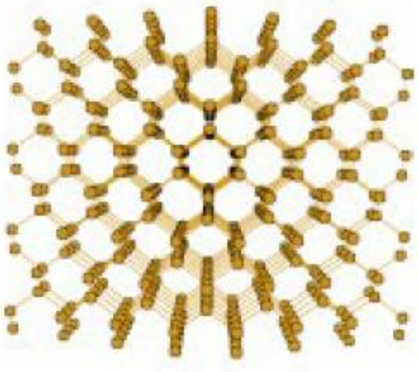

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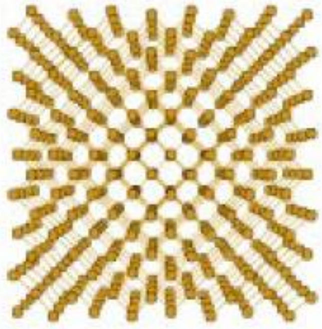
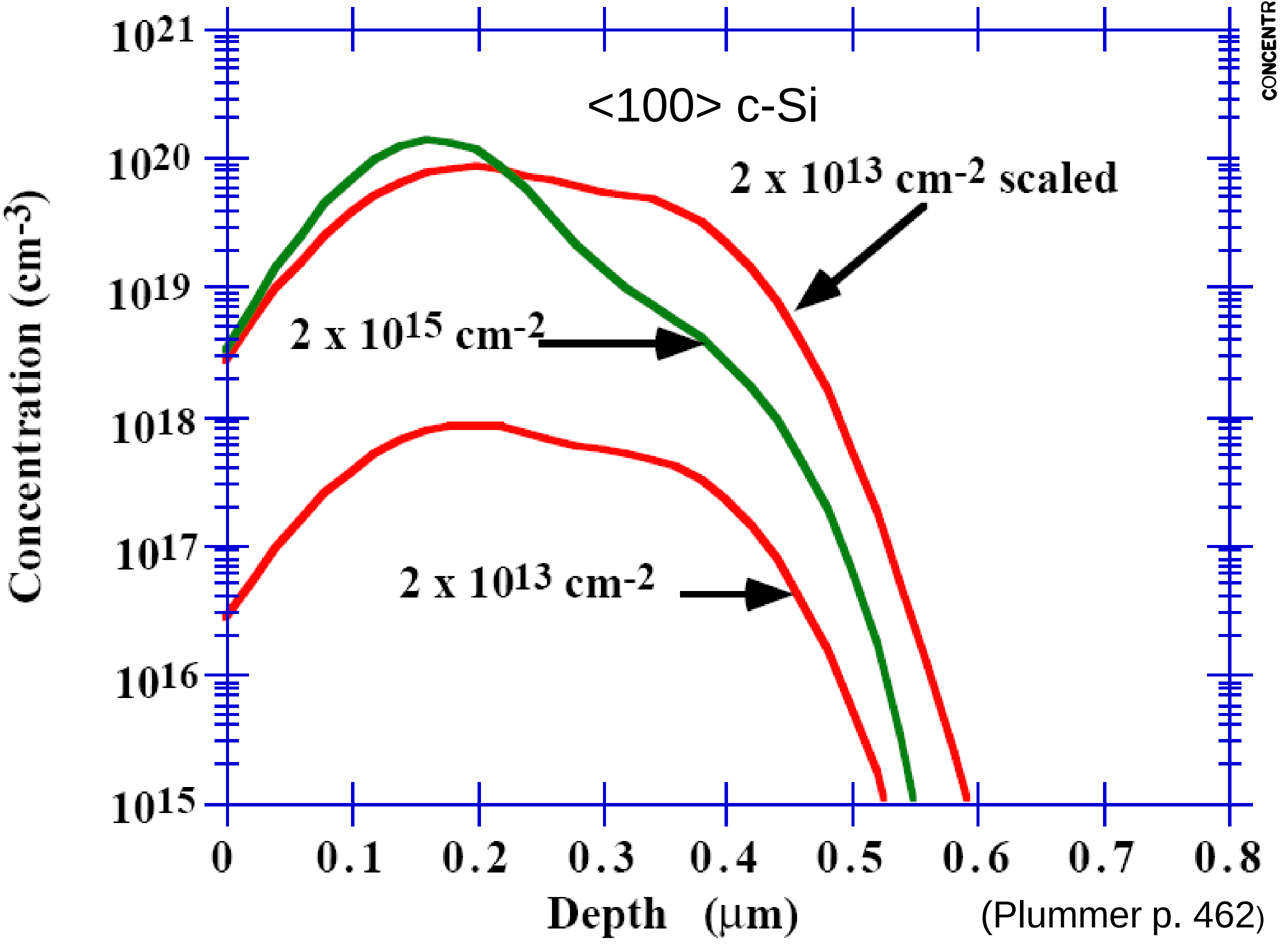


Random orientation

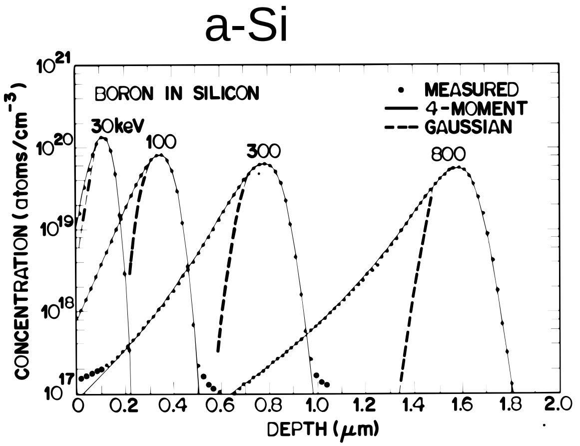
Channelling

Channel tails in B profiles implanted in <100> Si

Zero tilt and rotation



(Plummer p. 462)



Channelling

Two distributions ("dual-Pearson") needed to describe I/I in crystalline Si. Further on, dose dependence must be added.

Dose dependence: Channeling decreases with dose because of accumulated damage

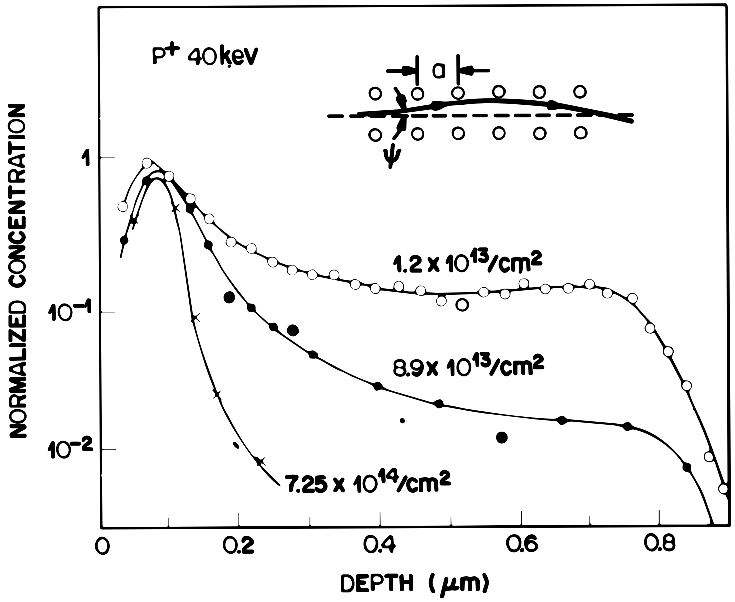
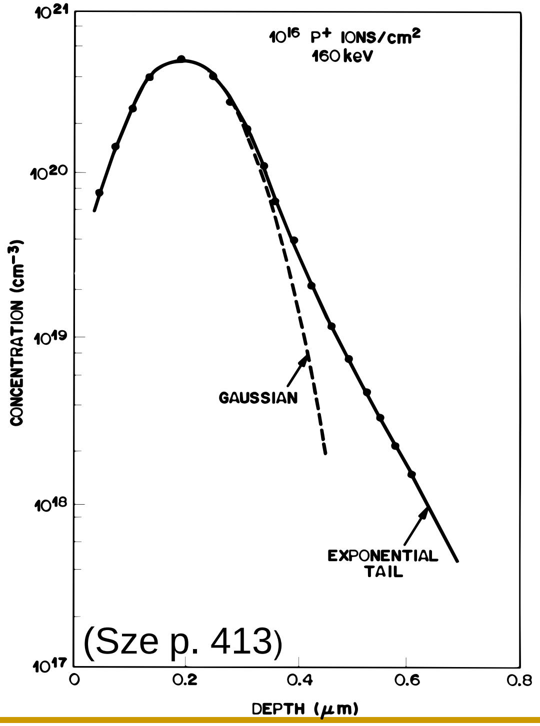


Fig. 28 Channeling of phosphorus ions in silicon. Insert shows the schematic trajectory of a channeled particle.[21]

(Sze p. 414)

Channeling in Si reduced by:
Wafer tilt typically around 7° during I/I
Pre-amorphize surface by Ar, Si or Ge
implant through surface oxide and/or nitride thin layer



(Sze p. 413)

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  - Activation

Lattice disorder caused by I/I in crystalline material

Light ions (B): mainly electronic stopping
Heavy ions (P, As, Sb): mainly nuclear stopping → amorphous layer created!
(compare schematic on slide 24)

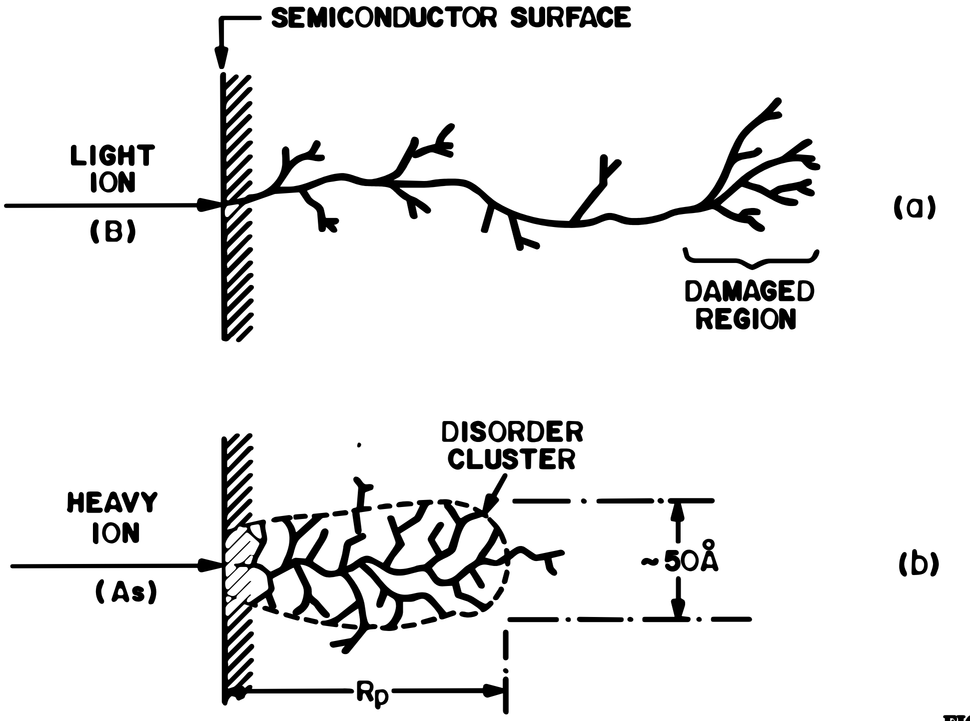


Fig. 29 Implantation disorder due to (*a*) light ions and (*b*) heavy ions.[3, 15]

(Sze p. 416)

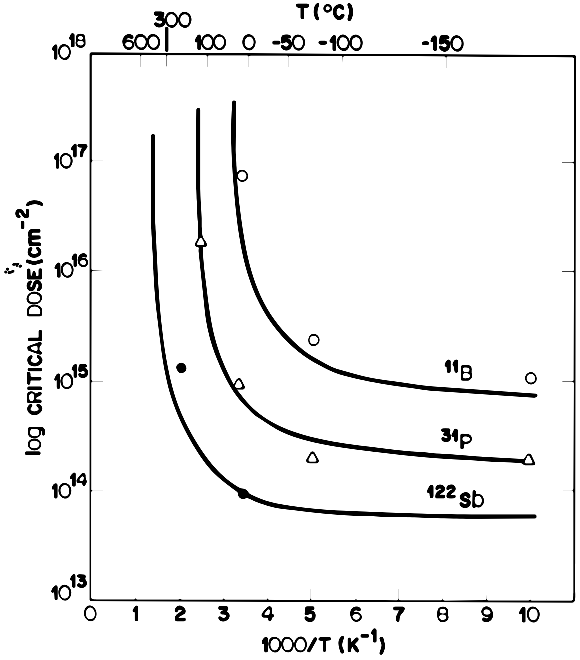


FIGURE 12
A plot of the critical dose necessary to make a continuous amorphous layer as a function of temperature. (*After Morehead and Crowder, Ref. 23.*)

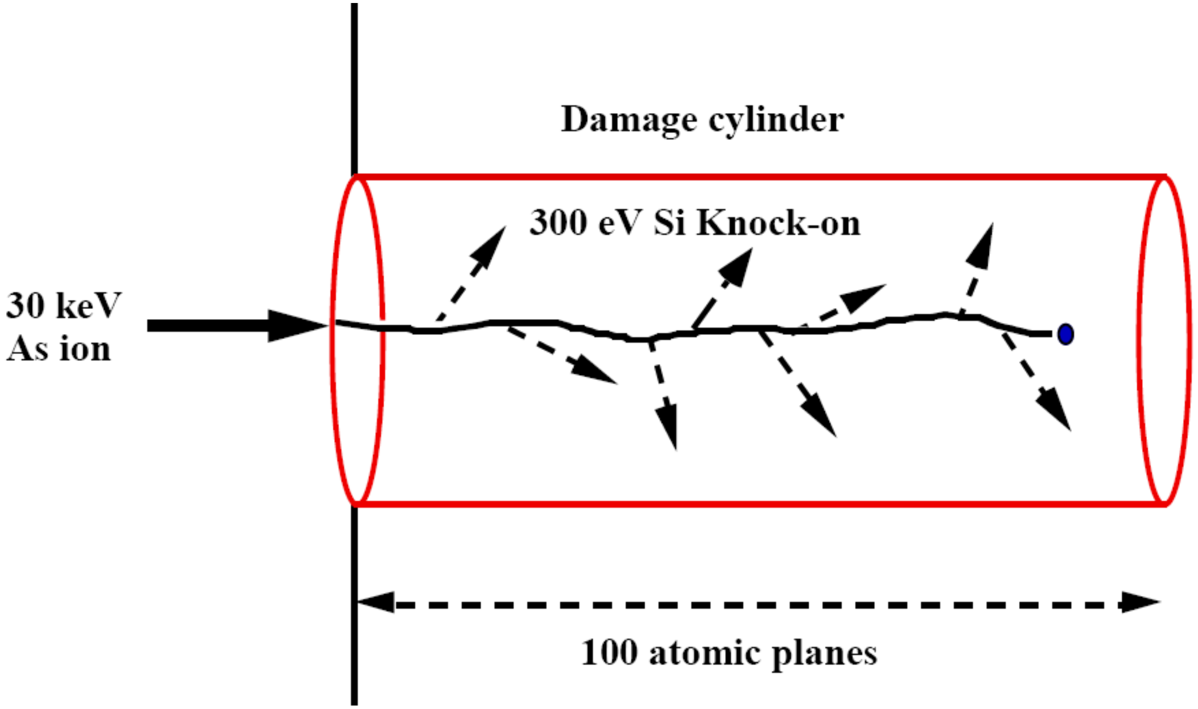
(VLSI p. 343)

Lattice disorder caused by I/I in crystalline material

Consider a 30keV arsenic ion, which has a range of 25 nm, traversing roughly 100 atomic planes.
The number of displaced particles per incoming ion is

$$\mathbf{n = \frac{E_n}{2E_d} = \frac{30,000}{2 \times 15} = 1000 \quad ions}$$

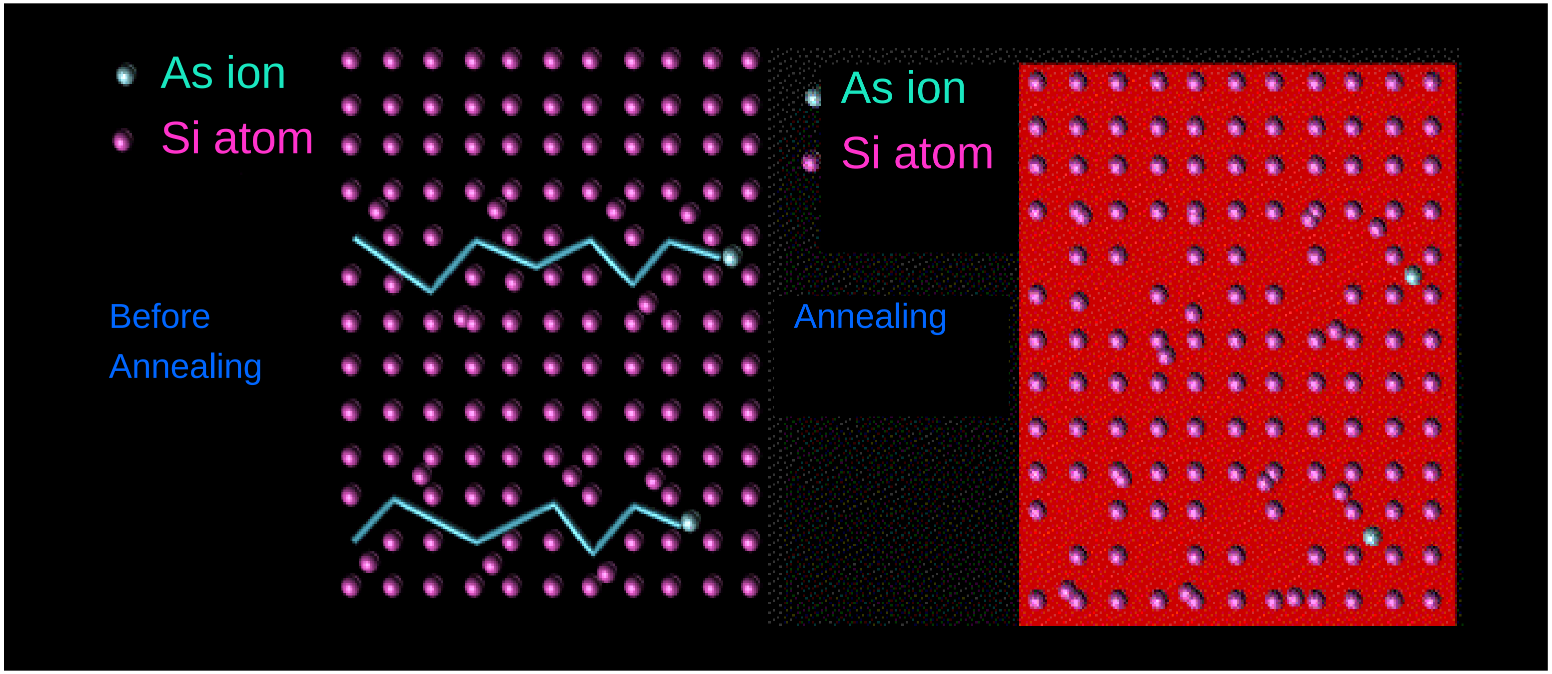
E_d= 15eV
(displacement energy in silicon)



Damage annealing

- Remove damages caused by implantation and recover si lattice to its original perfect crystalline structure
- Drive impurity into electrically active sites - substitutional sites
- Restore carrier mobility

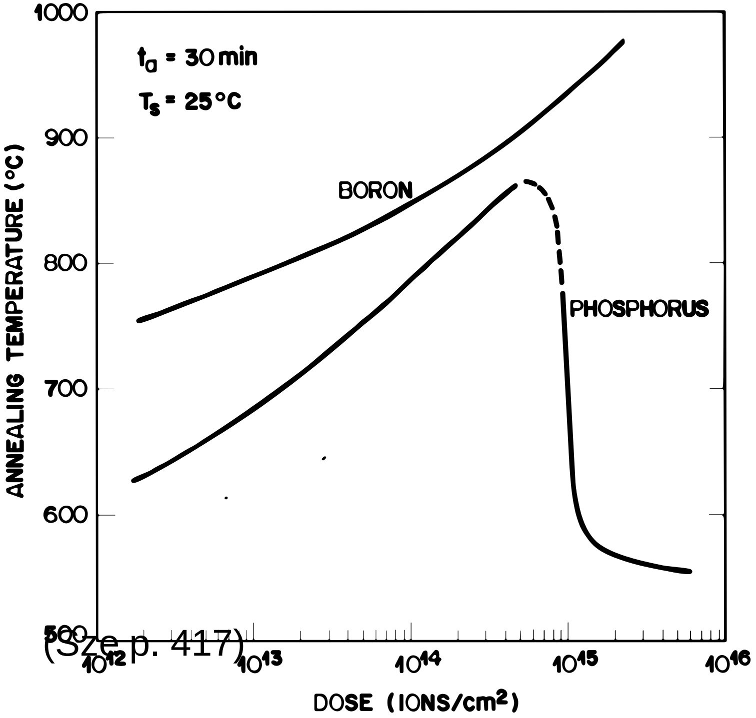
Note: Annealing should avoid substantial impurity redistribution.



Damage annealing

Anneling:
Repairing lattice damage and dopant activation
Furnace anneal and/or RTA

Plot of required anneal temperature for 90% activation:



(Sze p. 417)

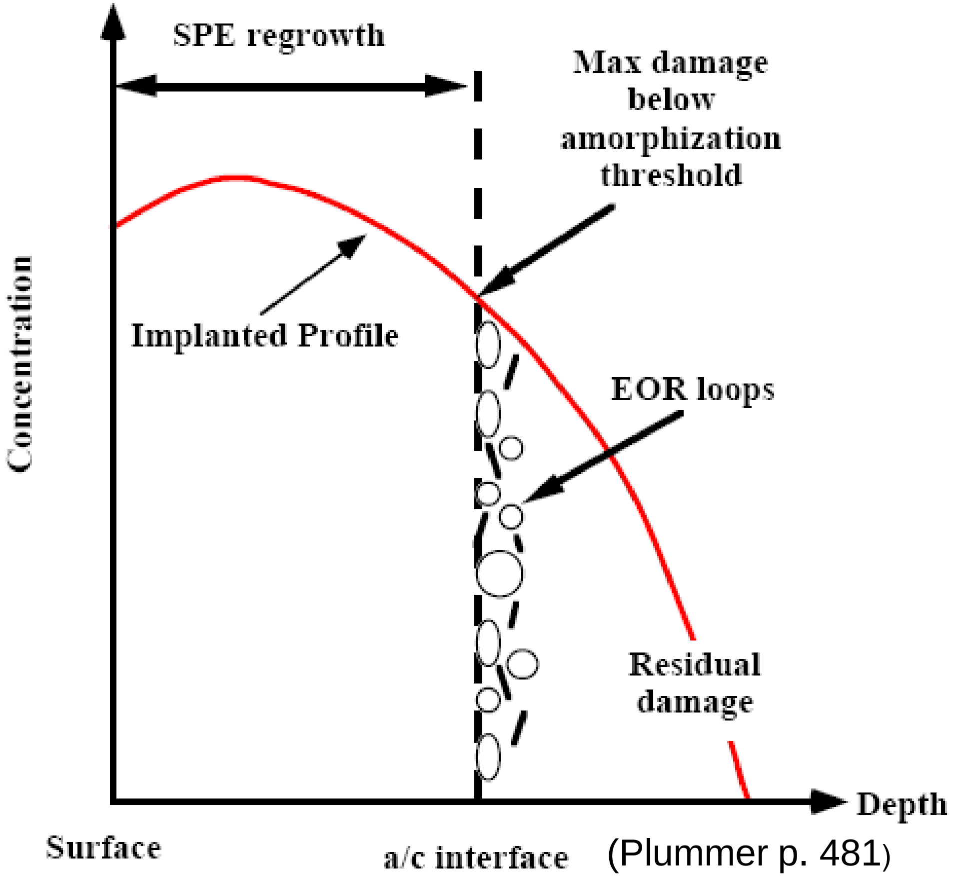
Fig. 30 Annealing temperature versus dose for 90% activation of boron and phosphorus ions.[2, 18]

Drastic reduction in anneal temp. for Ph dose > 1E15 cm^{-2} due to amorphization
Leads to ***solid phase epitaxy*** (SPE) of damaged material.
SPE is rapid and requires relatively low temperatures.

Damage annealing: SPE

Problem during SPE

- Material below amorphization threshold can be very difficult to anneal out:
- End-of-Range (EOR) defects

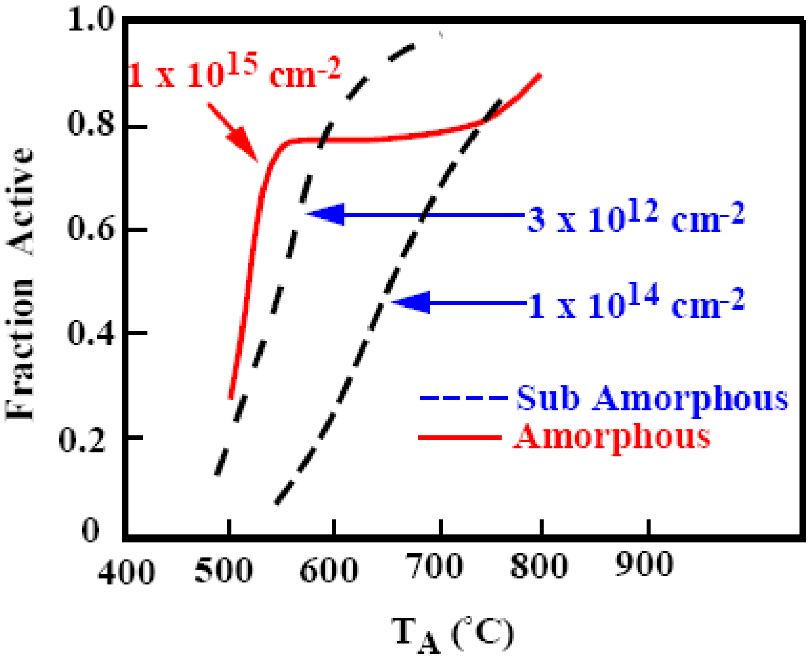


(Plummer p. 481)

Damage annealing: SPE

- When the substrate is amorphous, SPE provides an ideal way of repairing the damage and activating dopants (except that EOR damage may remain).

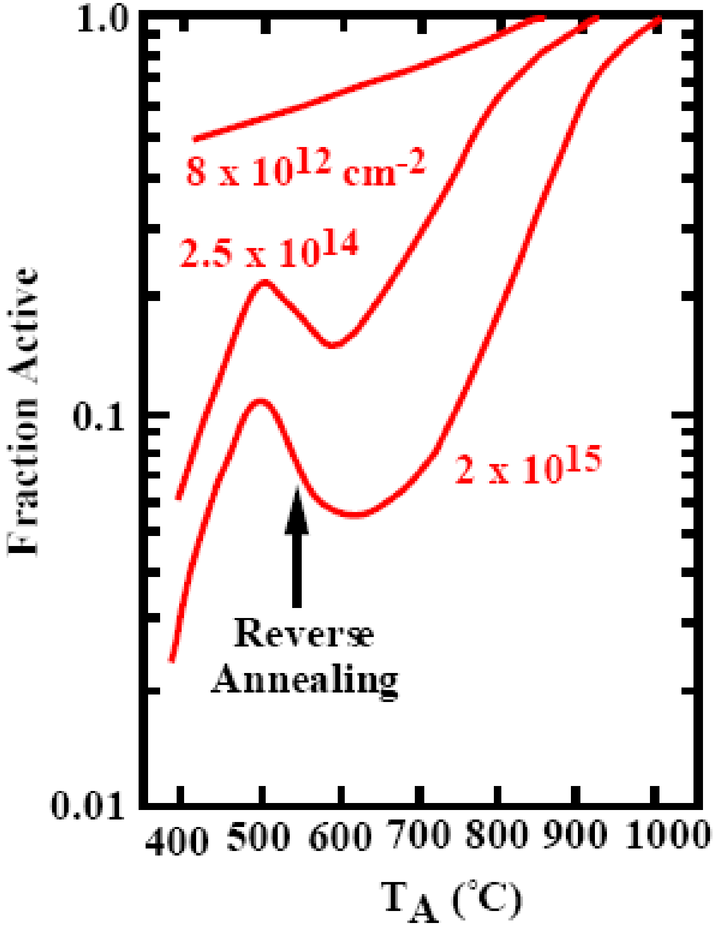
- At lower implant doses, activation is much more complex because stable defects form.



Anomalies during dopant activation

1. Reverse annealing of implanted B and Ph

In certain region, dopant activation decreases with T!



Explanation:

- Implantation generates silicon interstitials.
- These compete with B / Ph for substitutional sites (e.g. $B_S + I \rightarrow B_I$)
- Interstitial pairing of inactive complexes

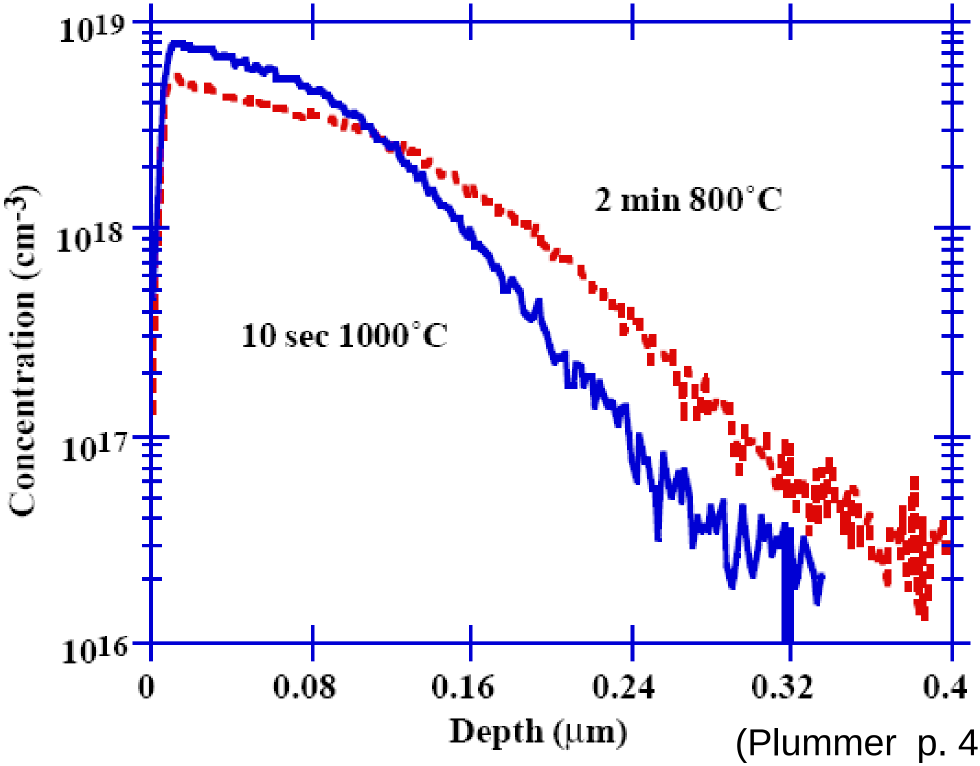
Solved by increasing temperature (must be traded off against diffusion!)

Anomalies during dopant activation (TED)

2. Transient enhanced diffusion (TED) of B

Diffusion in implanted B sample *larger* for an activation of 800°C, 2 min than 1000°C, 10 s!

Burst of diffusion several 1000 times faster than undamaged



(Plummer p. 486)

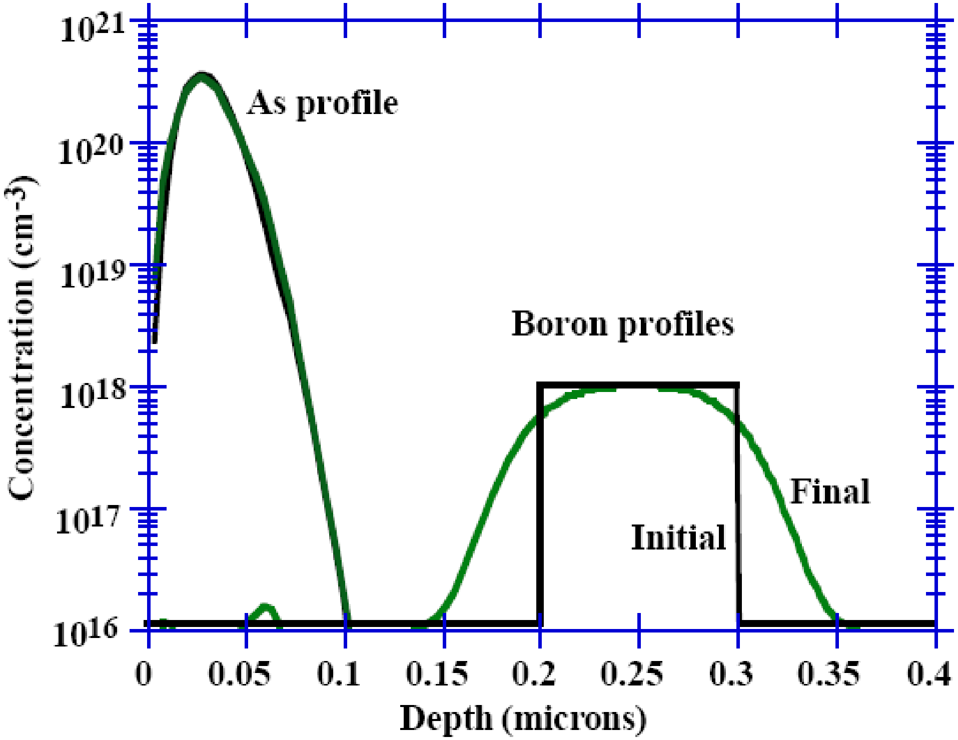
Anomalies during dopant activation (TED)

Explanation:

- Implant damage, in particular interstitial-type, is much slower restored at lower temperatures.
- These interstitials enhance B diffusion which then can be much larger than what is expected from normal thermal diffusion.

- TED is a problem in modern CMOS and bipolar technology
- Mitigated by low-energy I/I trend

- Simulation example: Buried B profile is affected by surface As I/I
- SPE regrowth in As region
- Interstitials affect mainly B region



(Plummer p. 486)

Summary of Key Ideas

- Ion implantation provides great flexibility and excellent control of implanted dopants.

- Since implanted ion energies are >> Si-Si binding energy (≈ 15 eV), many Si lattice atoms are displaced from lattice positions by incoming ions.

- This damage accumulates with implanted dose and can completely amorphize the substrate at high doses.

- The open structure of the silicon lattice leads to ion channeling and complex as-implanted profiles.

- TED is the biggest single problem with ion implantation because it leads to huge enhancements in dopant diffusivity and difficulty in achieving shallow junctions.

- Physically based understanding of TED has led to methods to control it (RTA annealing).

- Nevertheless, achieving the shallow junctions required by the NTRS will be a real challenge in the future since ion implantation appears to be the technology choice.