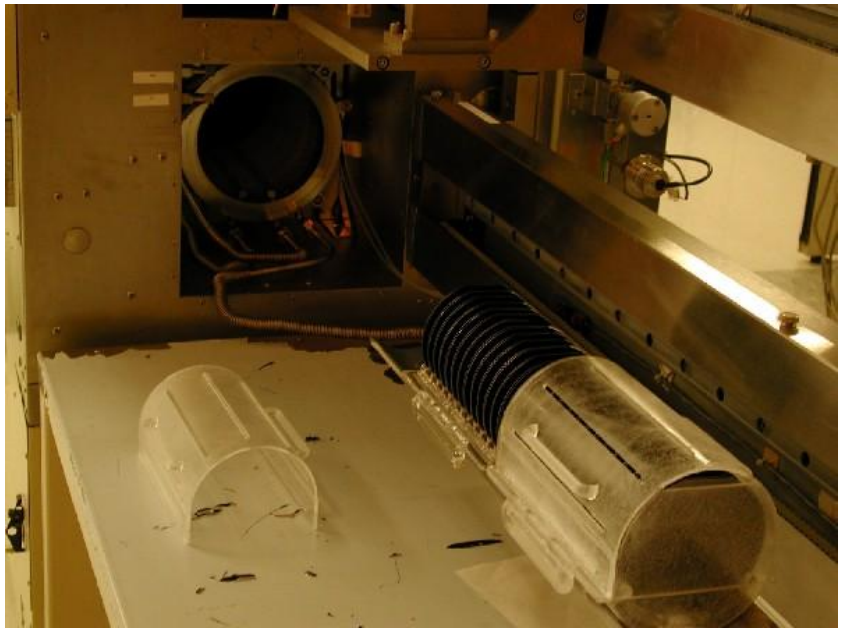
Lecture 7.1

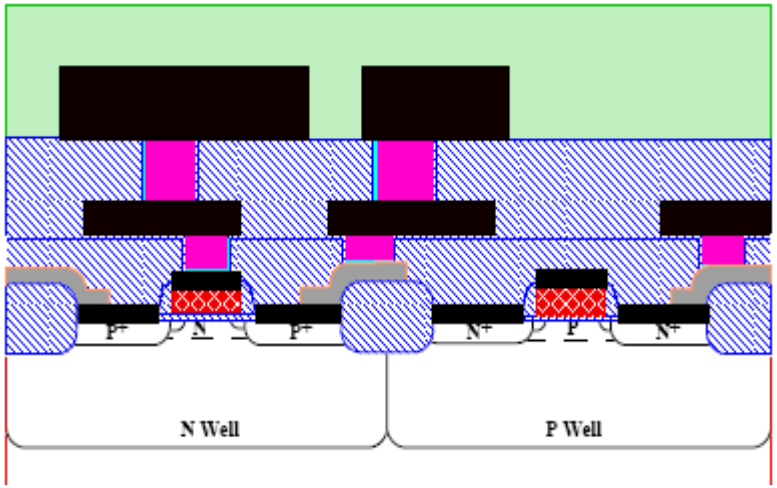
Deposition of dielectrics and metal gate stacks
(CVD, ALD)



Thin Film Deposition Requirements

Many films, made of many different materials are deposited during a standard CMOS process.

- Gate Electrodes (poly and metal)
- Vias
- Interconnects
- Interconnect insulators
- Shallow Trench Isolation (ATI)
- Dielectrics (High-k, DRAM)
- Diffusion barriers



Requirements or desirable traits for deposition:

1. Desired composition, low contaminates, good electrical and mechanical properties
2. Uniform thickness across wafer, and wafer-to-wafer
3. Good step coverage (“conformal coverage”)
4. Good filling of spaces
5. Planarized films

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CVD and ALD of polysilicon and dielectric thin films

- Chemical Vapor Deposition (CVD)
  - Basic definitions
  - Reactor designs
  - Examples
    - Polysilicon CVD
    - Silicon Dioxide CVD
    - Silicon Nitride CVD
  - Modeling
- Atomic Layer Deposition (ALD)
  - Basic Definitions
  - Reactor Designs
  - Example
    - Aluminum Oxide ALD

Chemical vapor deposition (CVD) - Definition

Constituents of the films are delivered through the gas phase. For CVD reactant gases are introduced into the deposition chamber and chemical reactions are used to deposit a thin film on the wafer surface.

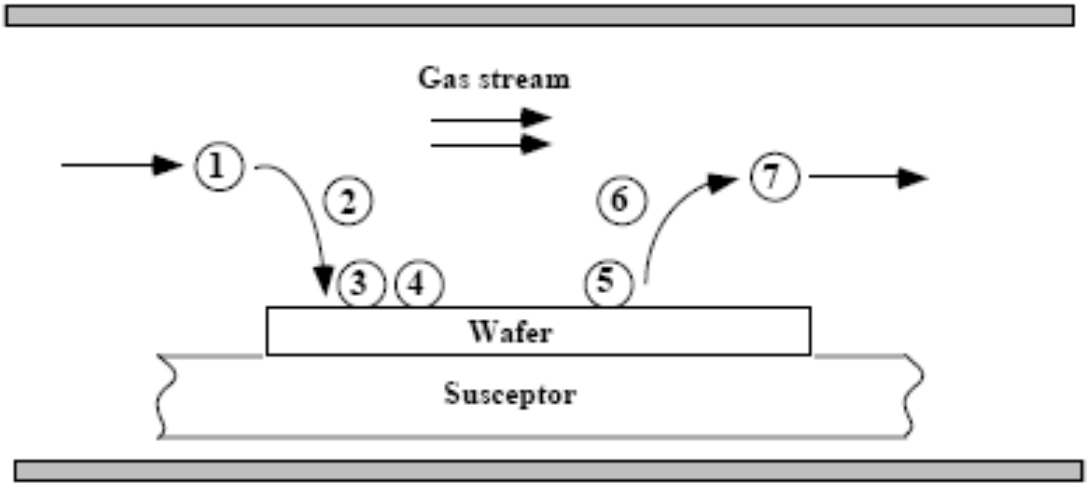
Energy for this reaction can origin from heat, radiation or from a plasma.

Typical pressure range: 0.01 to 1 bar

Good film quality and step coverage.

CVD Process (compare L2)

1. Transport of reactants to the deposition region
2. Transport of reactants by diffusion from the main gas stream through the b*oundary layer* to the wafer surface
3. *Adsorption* of reactants on the wafer surface
4. Surface processes: *migration*, *decomposition, reaction, site incorporation*
5. *Desorption* of byproducts from surface
6. Transport of byproducts through the boundary layer
7. Transport of byproducts from the deposition region



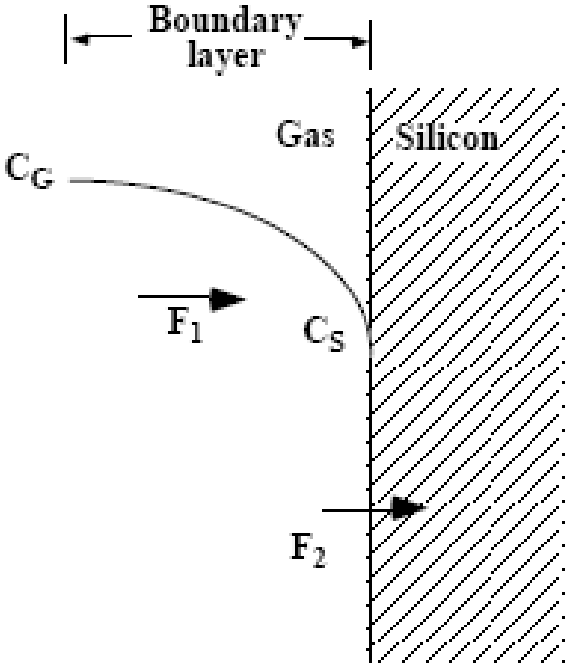
(Plummer Fig 9-5 p 514)

CVD Process (compare L2)

Growth limited by mass-transfer or surface reaction

$$F_1 = h_g (C_g - C_s)$$

$$F_2 = k_s C_s$$



(Plummer 9-6, p.515)

F_1, F_2: flux of reactant species to the wafer / of reactant consumed at surface
h_g: mass transfer coefficient (cm/s)
C_g, C_s: concentration of reactant species in gas / at surface
K_s: surface reaction constant

The Grove Model for Epitaxial Growth
Growth limited by mass-transfer or surface reaction

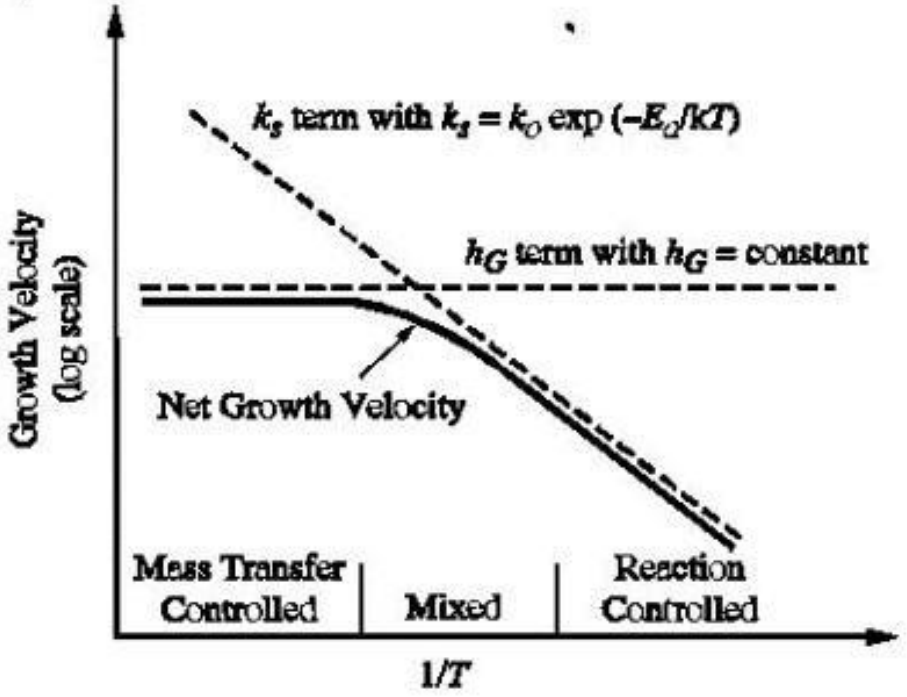


Figure 9–7 Arrhenius plot of growth velocity (or deposition rate) vs. $1/T$ for CVD process. The net growth velocity is the result of the surface reaction and gas-phase mass transfer processes acting in series so that the slower of the two dominates at any temperature.

(Plummer Fig 9-7)

$_t$ is the total number of gas molec/cm^3 ➔

$$\cong k_s \left(\frac{C_t}{C_a} \right) y ; \qquad C_s \rightarrow C_g$$

$$\cong h_g \left(\frac{C_t}{C_a} \right) y ; \qquad C_s \rightarrow 0$$

k_s: surface reaction constant
h_g: vapor mass transfer coefficient (cm/s)

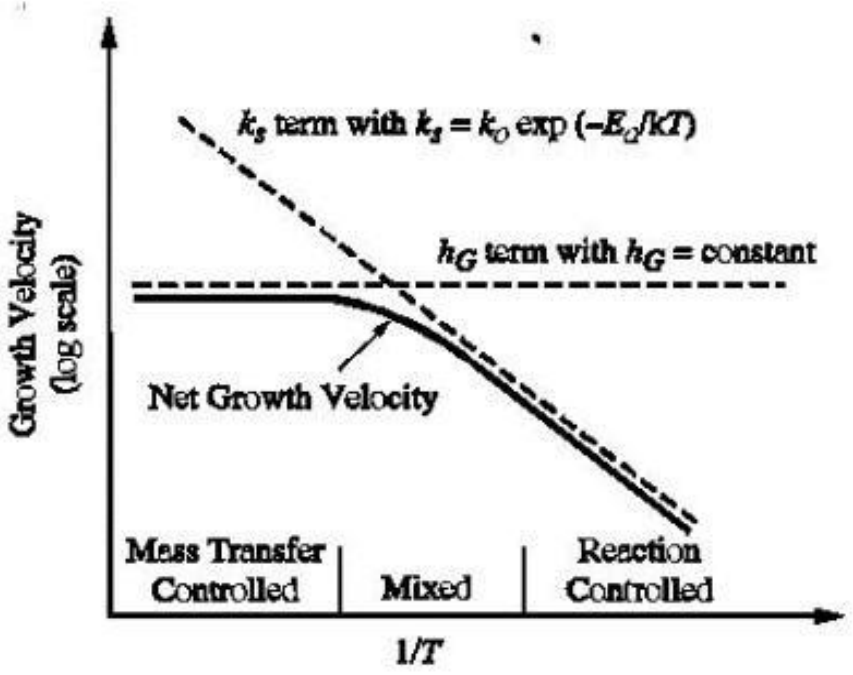
The Grove Model for Epitaxial Growth
Growth limited by mass-transfer or surface reaction

$C_g = yC_t$ where y is the mole fraction and C_t is the total number of gas molec/cm^3 ➔

$$v = \frac{F}{N} = \frac{k_s h_g}{k_s + h_g}\left(\frac{C_t}{C_a}\right)y$$

$$v \cong k_s\left(\frac{C_t}{C_a}\right)y$$

$$v \cong h_g\left(\frac{C_t}{C_a}\right)y$$



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(Plummer Fig 9-7)

Chemical vapor deposition (CVD) - Methods

Thermal CVD typically between 400-900°C :
Low-pressure CVD (LPCVD): 0.1- 1 torr
Atmospheric-pressure CVD (APCVD)

Lower temperature budget by:
Plasma-enhanced CVD (PECVD)
Photon-induced CVD: Photon generation by UV or laser.

Present CVD trends:
Rapid Thermal CVD (RTCVD) > 10 torr
High-density PECVD (HDPCVD)

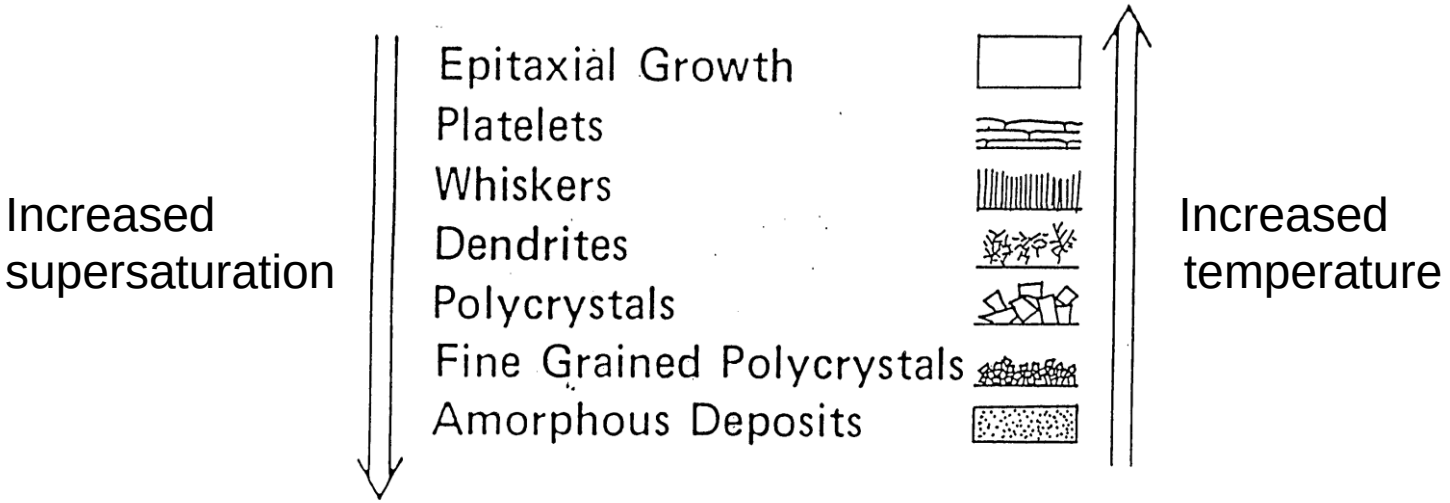
CVD parameters important for film properties:
Reactor design
Temperature
Pressure

Fundamental CVD Aspects

Compare Lecture 2: CVD Epitaxy!

- Thermodynamics and kinetics
- Transport phenomena
- Nucleation and thin film growth

Effect of supersaturation and temperature on thin film structure:*



*Vapor that has higher partial pressure than its equilibrium vapor pressure is supersaturated

CVD and ALD of polysilicon and dielectric thin films

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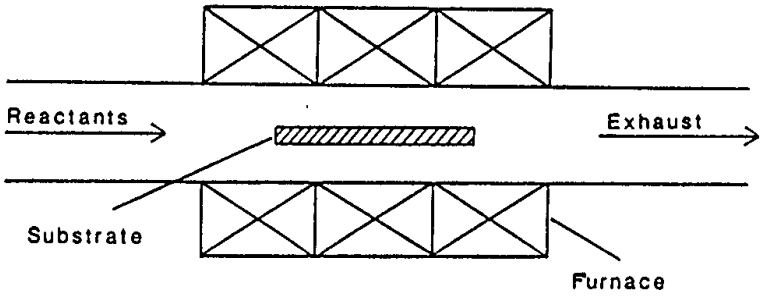
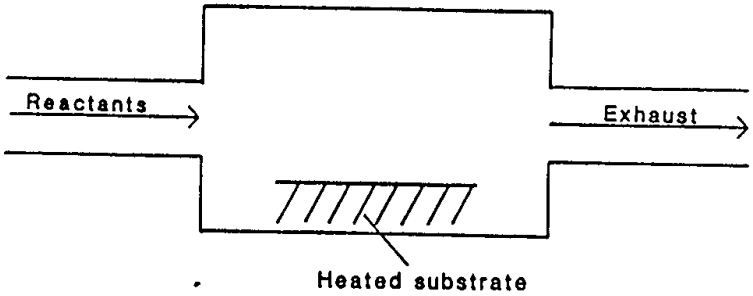
CVD basic reactor design

Hot wall



Cold wall

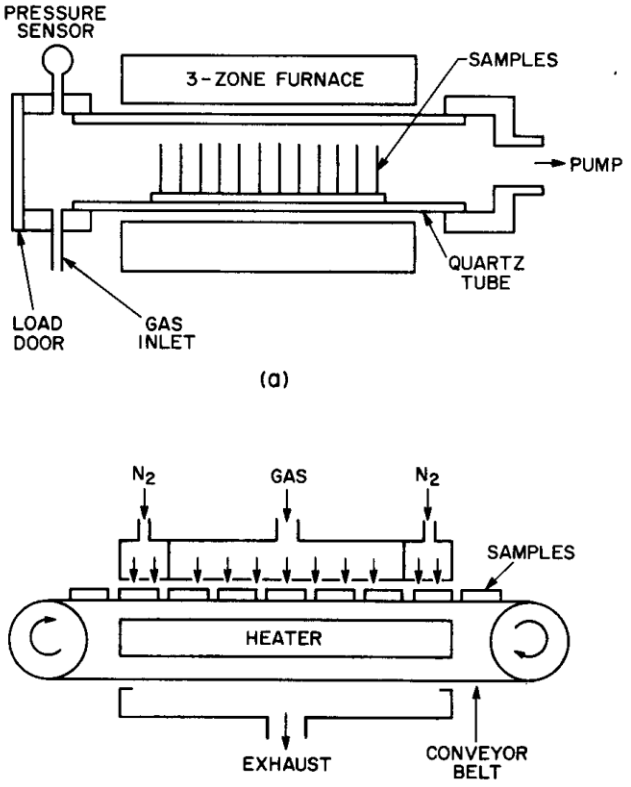


Trend is from hot-wall batch reactors to cold-wall single-wafer tools

Thermal CVD

LPCVD hot-wall. Most common in production. Both horizontal and vertical deisgn.

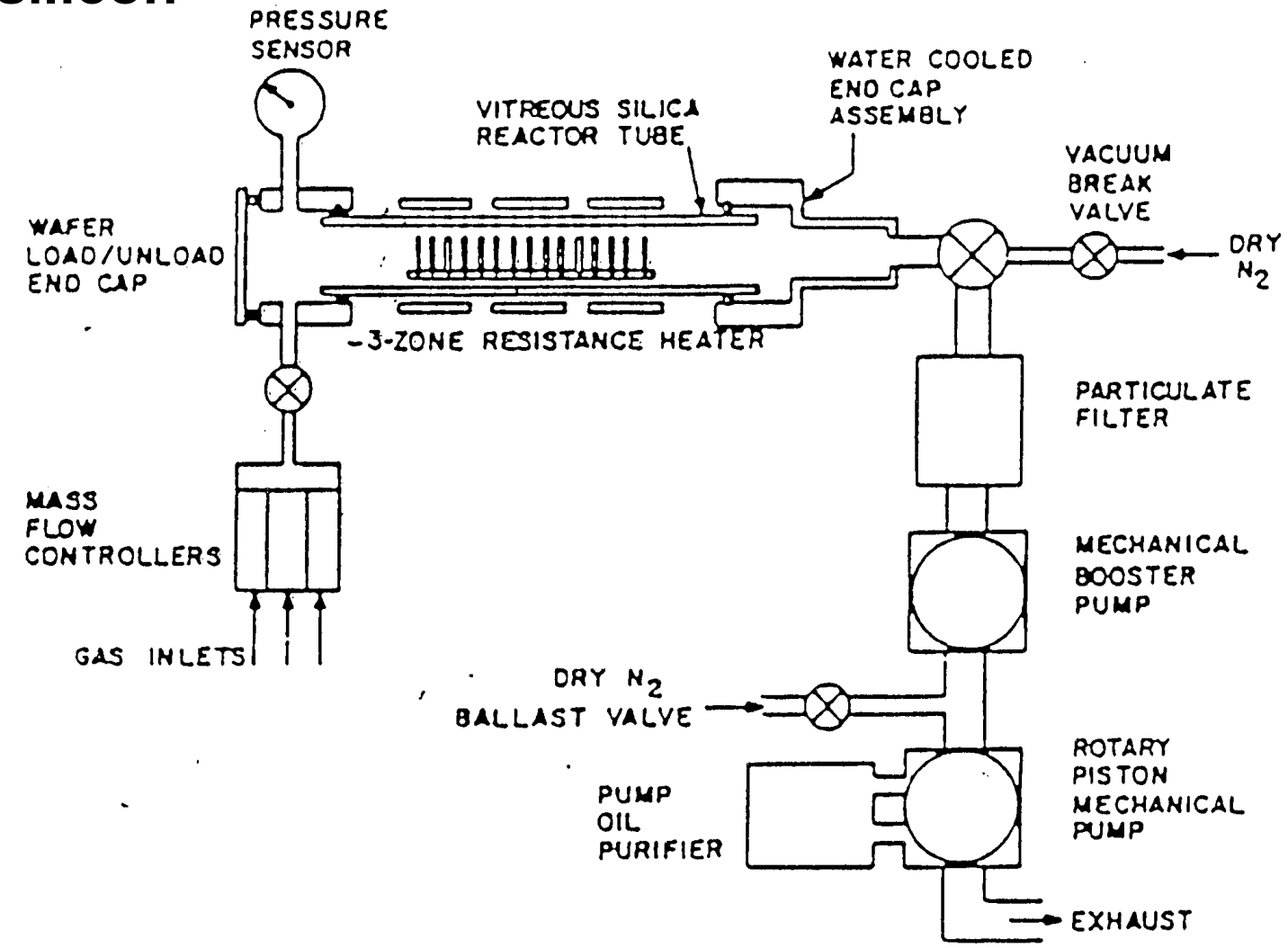
APCVD. Not very common today.



(Fig. 6.1 VLSI Techn. p. 236)

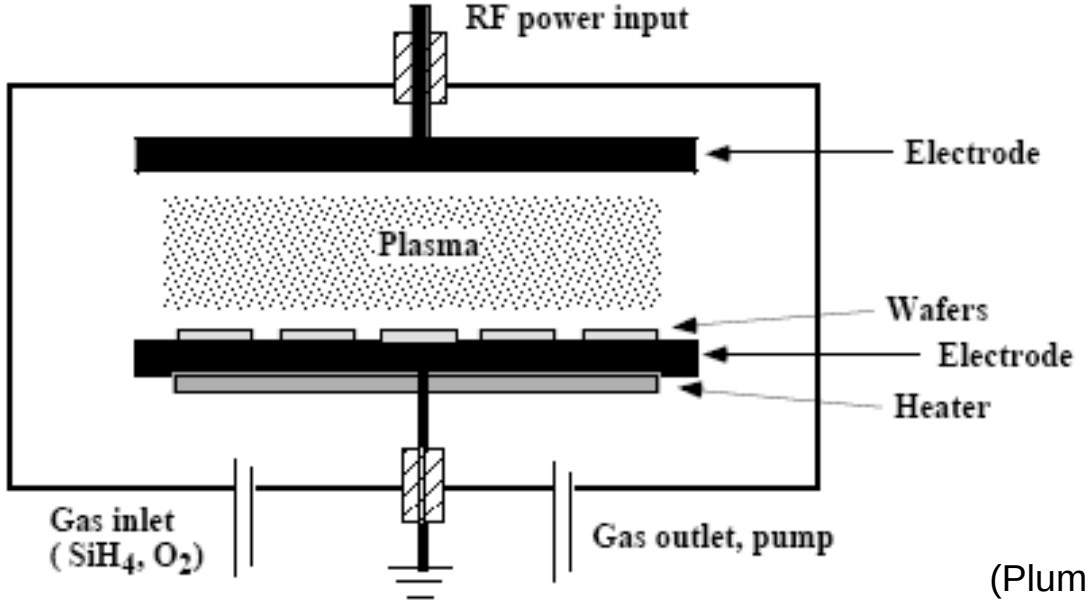
FIGURE 1
Schematic diagrams of CVD reactors: (a) Hot-wall, reduced-pressure reactor. (b) Continuous, atmospheric-pressure reactor.

The LPCVD workhorse system for Si_3N_4, silicon oxide and polysilicon



Plasma Enhanced CVD (PECVD)

- Non-thermal energy to enhance processes at lower temperatures.
- Plasma consists of electrons, ionized molecules, neutral molecules, neutral and ionized fragments of broken-up molecules, excited molecules and free radicals.
- Free radicals are electrically neutral species that have incomplete bonding and are extremely reactive. (e.g. SiO, SiH3, F)
- The net result from the fragmentation, the free radicals, and the ion bombardment is that the surface processes and deposition occur at much lower temperatures than in non-plasma systems.



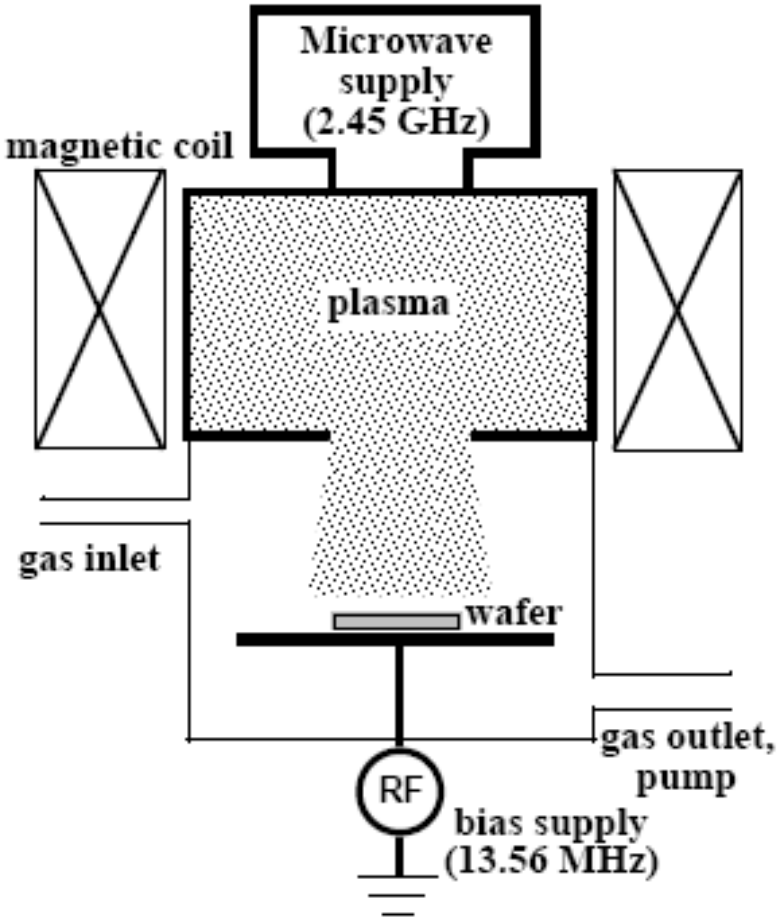
Details on plasma reactors:
see Lecture 7.1 Etching

(Plummer 9-14, p.528)

High Density Plasma CVD (HDPCVD)

Properties

- Extension of PECVD
- Remote high density plasma with independent RF substrate bias
- Allows simultaneous deposition and sputtering for better planarization and void-free films
- Mostly used for SiO_2 deposition in backend of the line (***BEOL***) processes



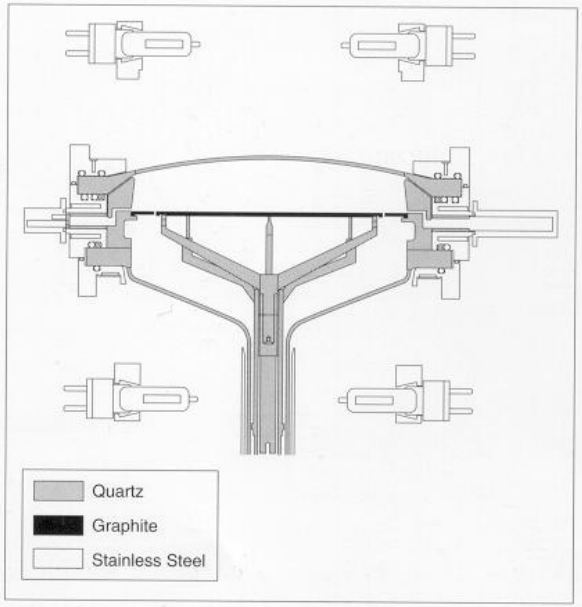
Modern RTCVD process

Deposition module in cluster tool

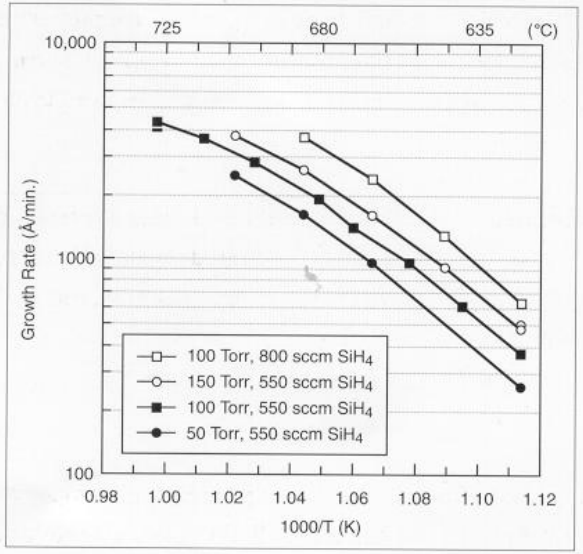
Similar to LT epi process:

Single-wafer system > 10 torr
Hydrogen as carrier gas
In situ doping
In situ cleaning (HCl or NF_3)

Polysilicon deposition chamber.



Polysilicon process growth rate vs. temperature dependence.



Centura poly process (Applied Materials)

Characteristics of various CVD processes

Table 1. CHARACTERISTICS and APPLICATIONS OF CVD REACTORS

PROCESS	ADVANTAGES	DISADVANTAGES	APPLICATIONS
APCVD (Low Temperature)	Simple Reactor, Fast Deposition, Low Temperature	Poor Step Coverage, Particle Contamination	Low Temperature Oxides, both doped and undoped
LPCVD	Excellent Purity and Uniformity, Conformal Step Coverage, Large Wafer Capacity	High Temperature Low Deposition Rate	High Temperature Oxides, both doped and undoped, Silicon Nitride, Poly-Si, W, WSi_2
PECVD	Low Temperature, Fast Deposition, Good Step Coverage	Chemical (e.g. H_2) and Particulate Contamination	Low Temperature Insulators over Metals, Passivation (Nitride)

(Table 1. ULSI Technology p. 211)

CVD and ALD of polysilicon and dielectric thin films

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Polysilicon

Used in VLSI for:
n+ or p+ gate electrode material in CMOS (see below)
n+ emitter contact in BIP (see below), so-called polysilicon emitter technology
Diffusion source (double-poly bipolar process for formation of E and B) (see below)
Local interconnects
Deep-trench filling (see below)
Resistances

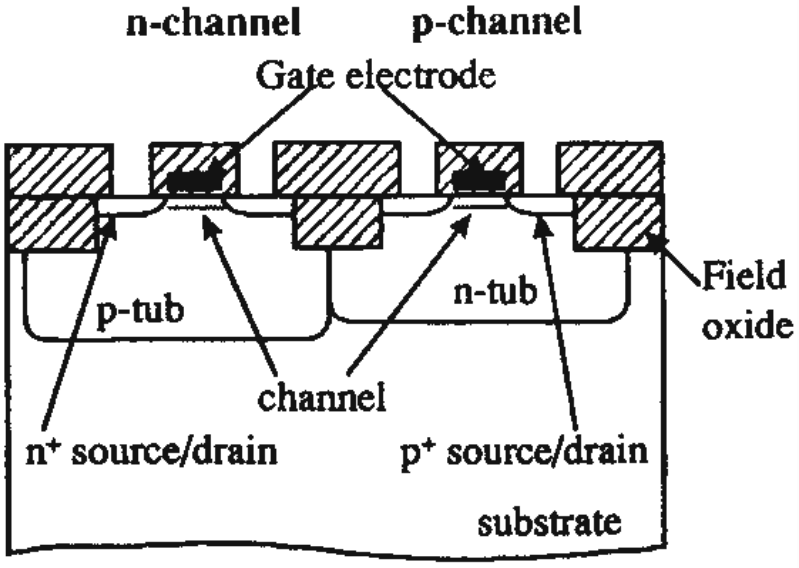
Also poly-SiGe of interest as common p+-gate electrode in CMOS (so-called mid bandgap material)

Example: Polysilicon CVD

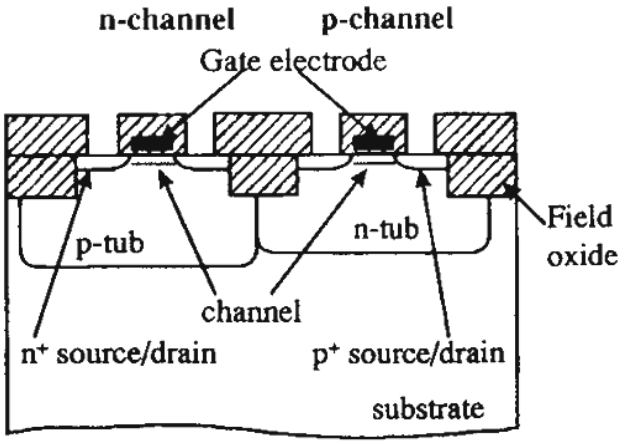
Application

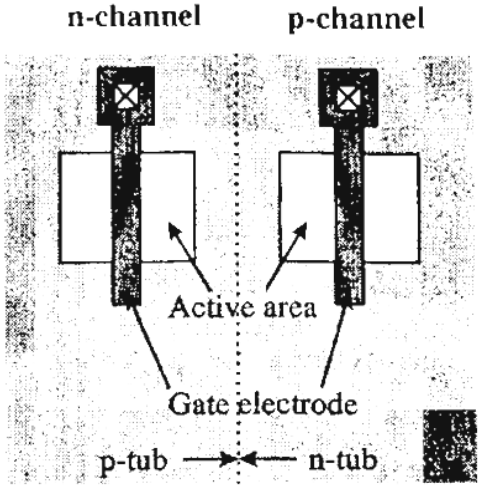
- n+ or p+ gate electrode material in CMOS (see below)
- n+ emitter contact in BIP (“polysilicon emitter technology”)
- poly-SiGe of interest as common p+-gate electrode in CMOS (mid bandgap material)
- Diffusion source (double-poly bipolar process for formation of E and B)
- Local interconnects
- Deep-trench filling
- Resistances
- Solar cells
- Thin Film Transistors (TFTs)

…

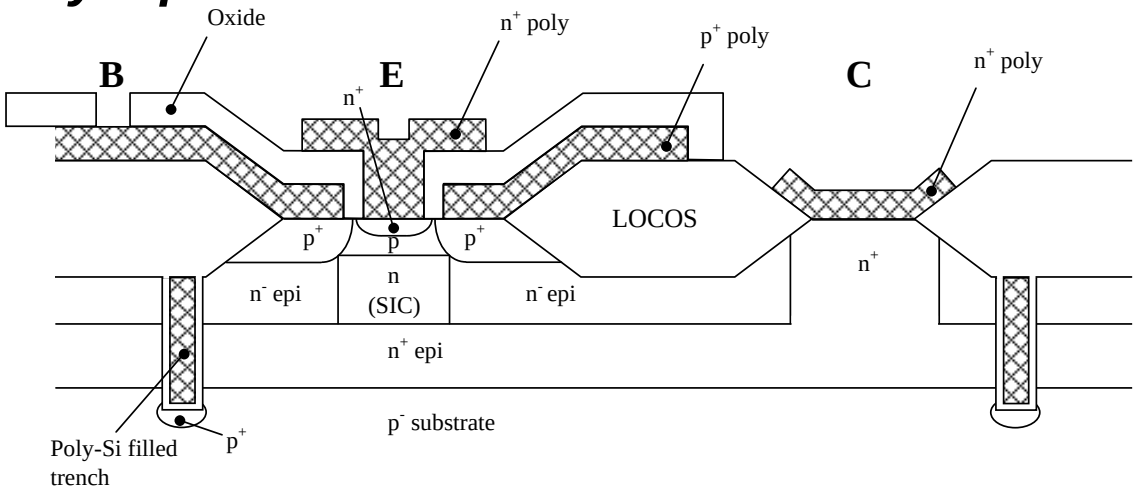


CMOS structure with poly gate electrode:





Double-poly bipolar structure:



Also many other applications of polysilicon: Solar cells, TFTs etc

Conventional LPCVD process

Polysilicon deposition using silane at 600-650°C

$SiH_4 \Leftrightarrow SiH_2 + H_2$
$SiH_2 \Leftrightarrow Si + H_2$

Alternative: Si_2H_6 (disilane). Permits lower deposition temperatures.

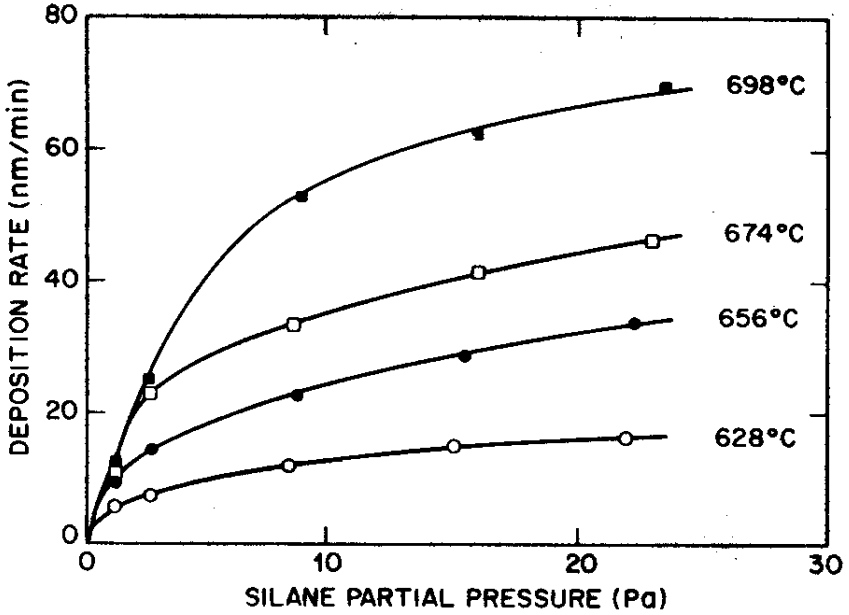


FIGURE 5
The effect of silane concentration on the polysilicon deposition rate.

(VLSI Tech. Fig. 5 p. 243)

Arrhenius plot of SiH_4 deposition at different partial pressures of SiH_4

Activation energy of 1.7 eV

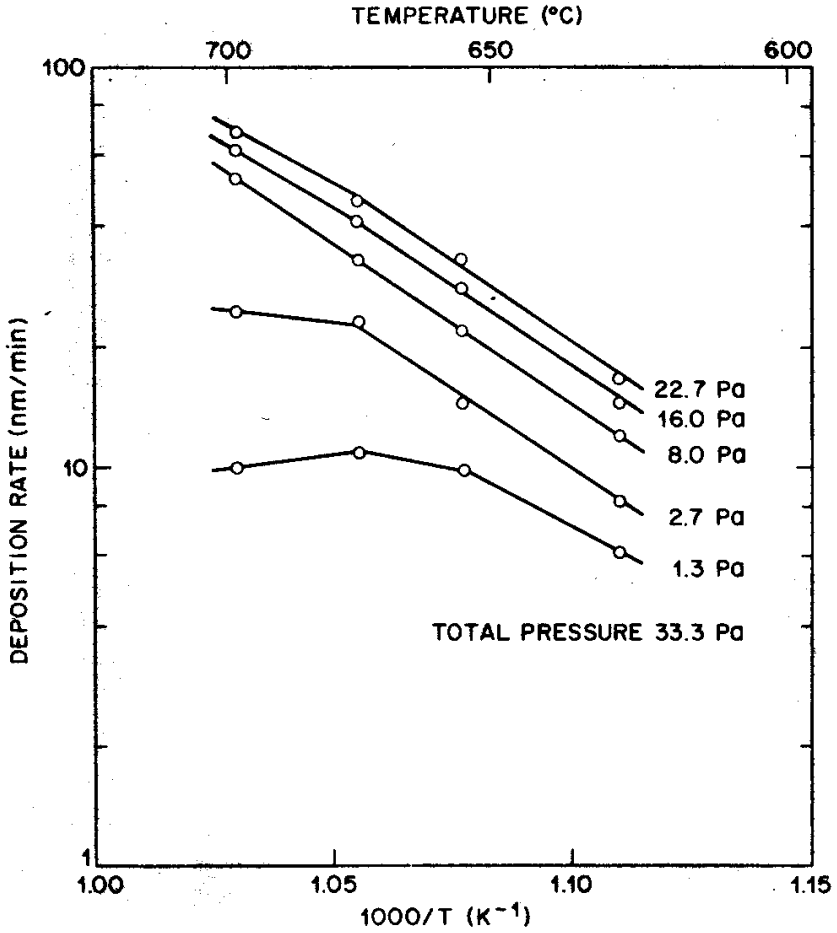


FIGURE 3
Arrhenius plot for polysilicon deposition for different silane partial pressures.

(VLSI Tech. Fig. 5 p. 240)

Microstructure of polysilicon

T > 625°C Columnar growth.
Preferential (110) orient.

T < 575°C Amorphous

T ~ 600°C Microcrystalline polysilicon

Exact microstructure depends on a number of factors:
Pressure, dopants, temperature, thickness, recrystallization etc

Grain growth important for final electrical properties

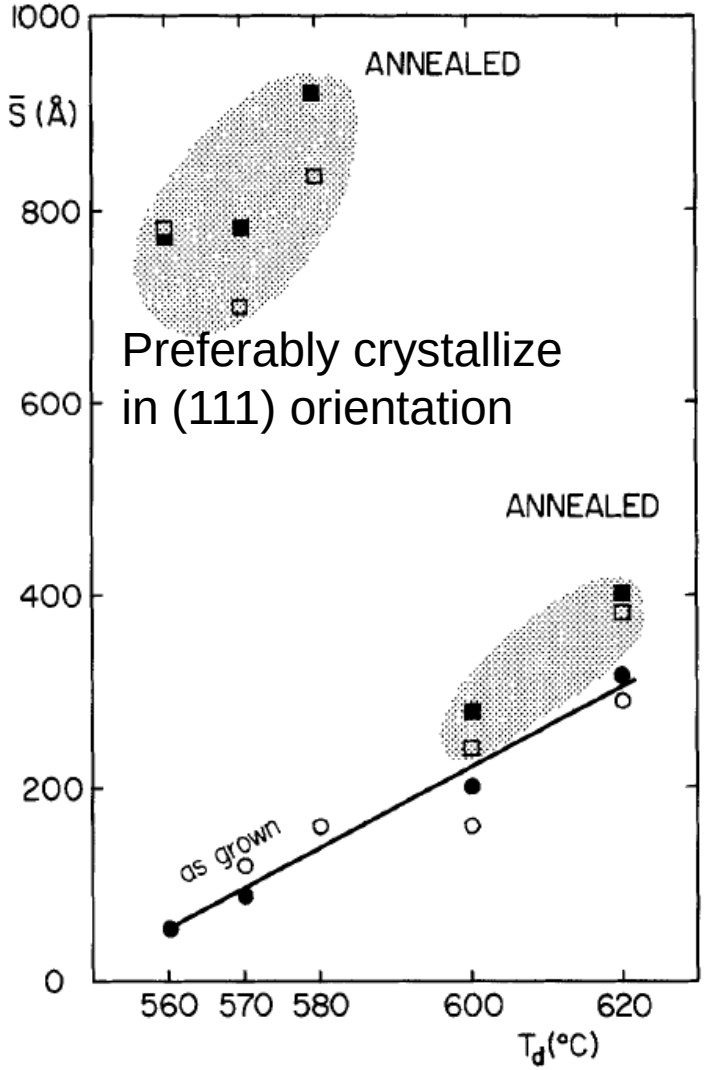


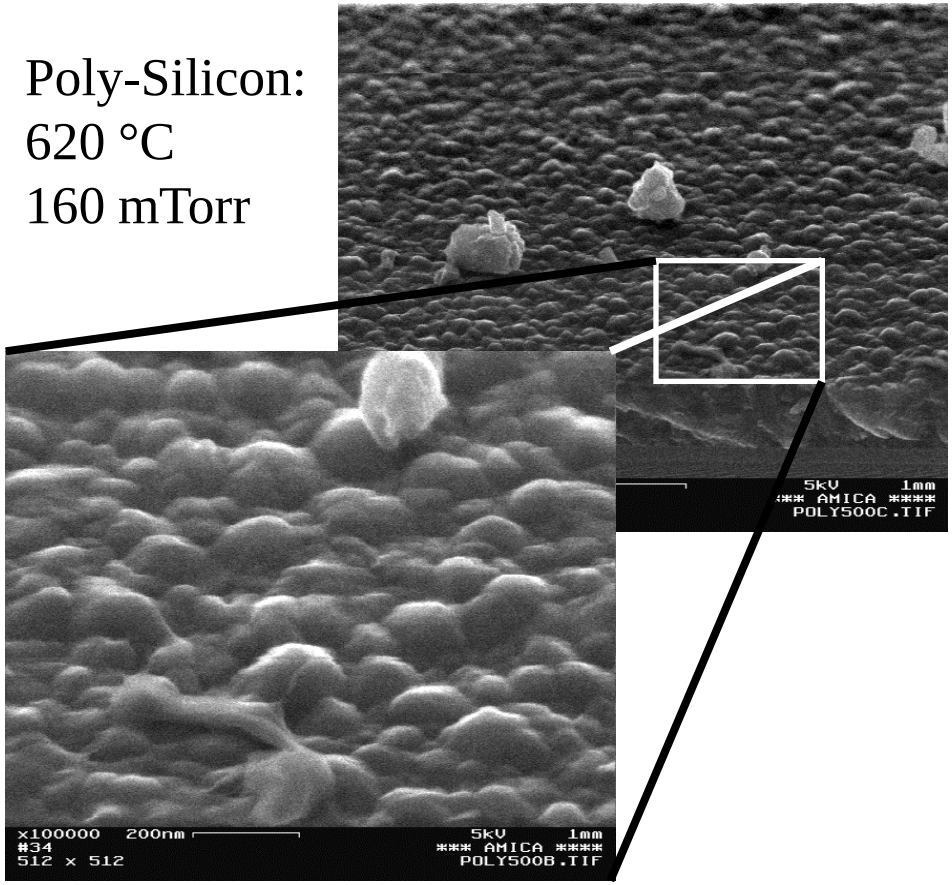
Fig. 4. Average crystallite size $\bar{S}$ for LPCVD Si-layers, as-grown (○ : interface, ● surface) and annealed at 1000°C (□ : interface, ■ surface) as a function of T_d.

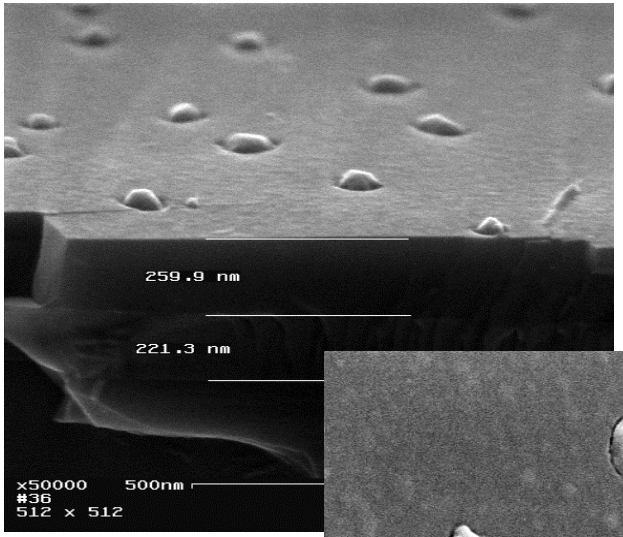
Growth and Physical Properties of I.PCVD Polycrystalline Silicon Films, G. Harbeke, SOLID-STATE SCIENCE AND TECHNOLOGY 1984

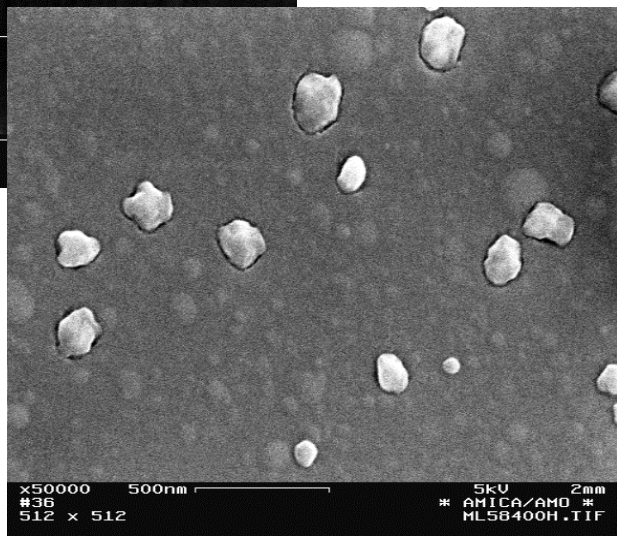
Example: Polysilicon CVD

Temperature and Pressure Dependence

Poly-Silicon:
620 °C
160 mTorr







α-Silicon:
580 °C
400 mTorr

- grain size >> functional structure
- surface roughness complicates etch stop

+ smooth surface
- gas phase nucleation
- recrystalization after annealing

Microstructure of polysilicon

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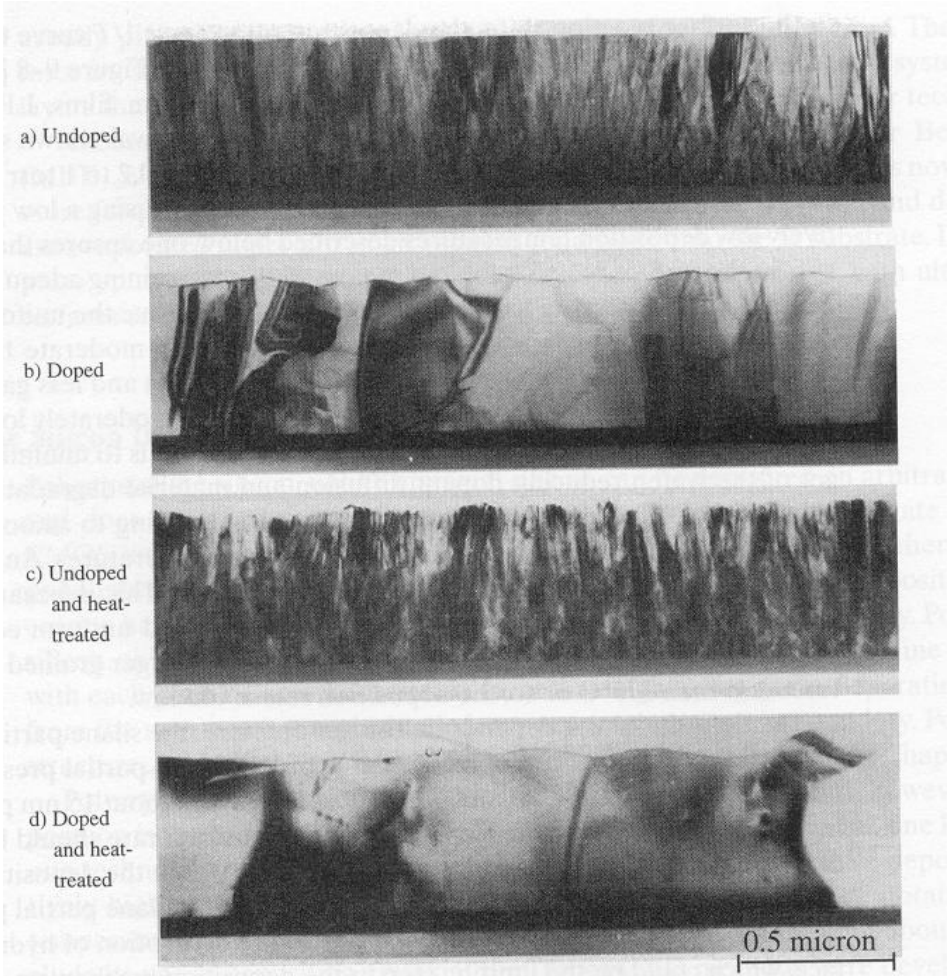


Figure 9–32 TEM cross sections of CVD polycrystalline films deposited at 625°C: (a) as-deposited, undoped film, showing the thin grains in a columnar structure; (b) as-deposited phosphorus-doped film, showing much larger grain size; c) annealed (1000°C), undoped film, showing little grain growth as compared to (a); (d) annealed (1000°C), phosphorus-doped film, showing evidence of grain growth as compared to (b). Reprinted with permission of the Electrochemical Society [9.19].

(Plummer Fig 9-32 p. 560)

Doping of polysilicon

Doping by diffusion, ion implant or *in situ* during CVD deposition

→ resistivity < 1 mWcm after annealing

Ion implantation most common today

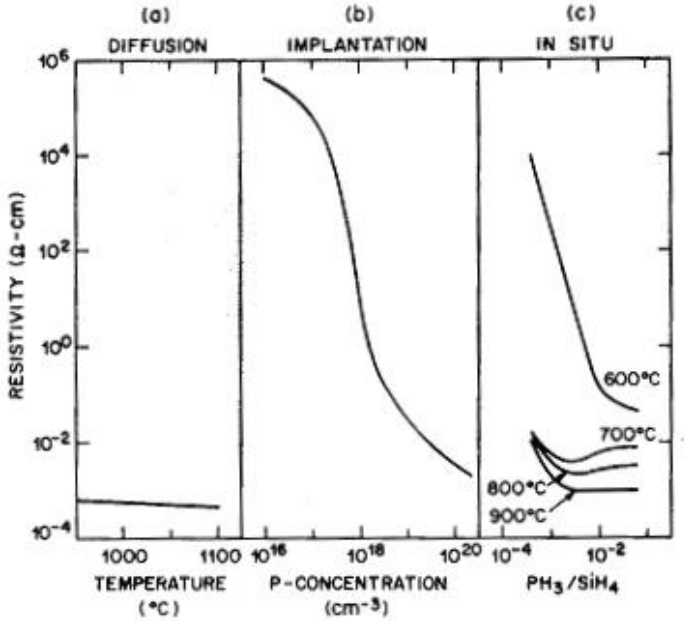


FIGURE 8
Resistivity of P-doped polysilicon. (a) Diffusion: 1 h at the indicated temperature. (*After Kamins, Ref. 11.*) (b) Implantation: 1 h anneal at 1100°C. (*After Mandurah, Saraswat, and Kamins, Ref. 12.*) (c) In situ: as deposited at 600°C and after a 30-min anneal at the indicated temperature. (*After A. C. Adams, unpublished data.*)

(VLSI Techn, Fig. 8 p. 245)

Complex behavior of dopants in polysilicon during subsequent procesing: Segregation of Ph and As (but not B) to the grain boundaries

Dopant diffusion is typically around 1000x faster in grain boundaries than inside the grains

In situ doping of polysilicon

Difficult process in batch furnace, in particular during n-type doping.
Non-uniformities and very low deposition rates
Requires quartz cage for wafers in LPCVD tube
Preferably deposited in amorphous phase and subsequently crystallized

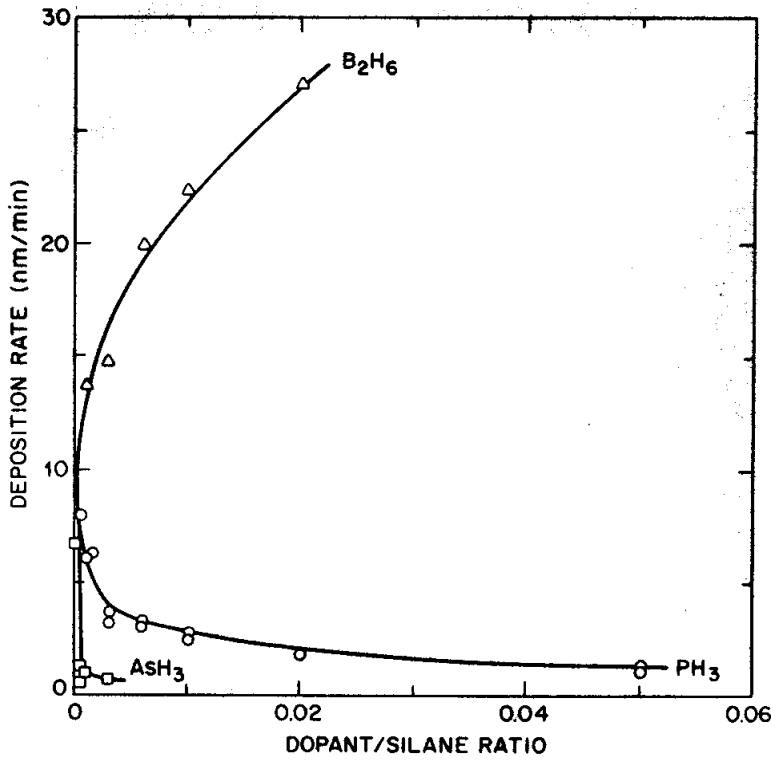


FIGURE 6
The effect of dopants on the polysilicon deposition rate at 610°C.

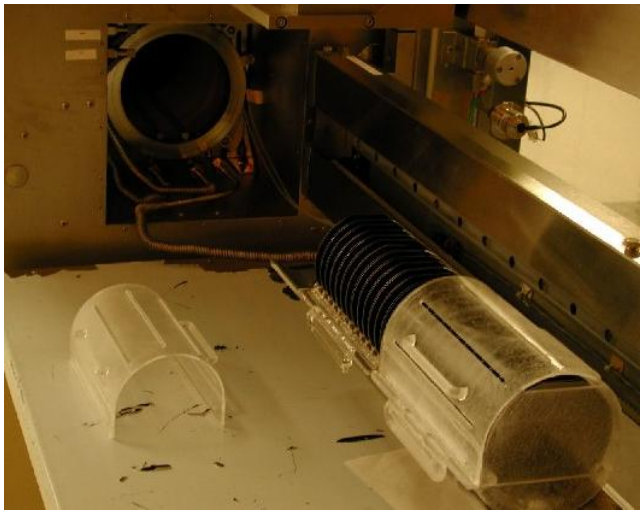
(VLSI Techn, Fig. 6 p. 243)

Example: SiO_2 CVD

Application

Isolation in active devices as well as between metal layers

Essential reactions for SiO_2 depositions:



LPCVD:

Tetraethylorthosilicate (TEOS): (liquid source!)
$Si(OC_2H_5)_4$ 650-750°C

Low-temperature oxide (LTO):
$SiH_4 + O_2$ 400-450°C

Note: Dichlorosilane (DCS): $SiCl_2H_2 + N_2O$ uncommon today

PECVD:

$SiH_4 + 2N_2O$ 200 - 350°C
Plasma TEOS 300 - 360°C

Sub-atmospheric CVD (SACVD):

TEOS + O_3 300-550°C

TABLE 3
Properties of silicon dioxide

Deposition	Plasma	$SiH_4 + O_2$	TEOS	$SiCl_2H_2 + N_2O$	Thermal
Temperature (°C)	200	450	700	900	1000
Composition	$SiO_{1.9}$(H)	SiO_2(H)	SiO_2	SiO_2(Cl)	SiO_2
Step coverage	nonconformal	nonconformal	conformal	conformal	conformal
Thermal stability	loses H	densifies	stable	loses Cl	stable
Density (g/cm^3)	2.3	2.1	2.2	2.2	2.2
Refractive index	1.47	1.44	1.46	1.46	1.46
Stress (10^9dyne/cm^2)	3C–3T	3 T	1 C	3 C	3 C
Dielectric strength (10^6V/cm)	3–6	8	10	10	11
Etch rate, nm/min (100:1 H_2O:HF)	40	6	3	3	2.5
Dielectric constant	4.9	4.3	4.0	—	3.9

(VLSI Techn. p. 259)

Typically TEOS results in porous films which may need densification. Also C in films!

PECVD films generally contains a lot of H or N

Comparison of TEOS and LTO: Arrhenius plots

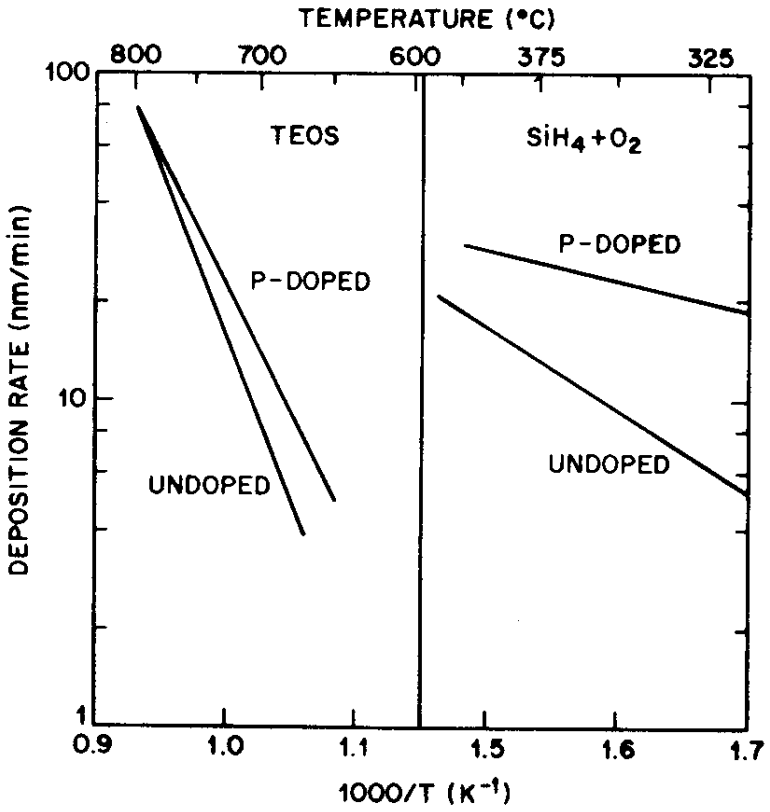


FIGURE 12
Arrhenius plots for the low-pressure deposition of SiO_2. (*After Adams and Capio, Ref. 30, for the TEOS data and after Learn, Ref. 29, for the silane–oxygen data.*)

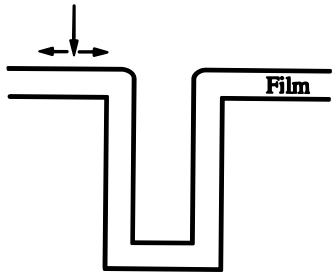
(VLSI Techn. p.252)

Example: SiO_2 CVD

Comparison of TEOS and LTO: Step coverage

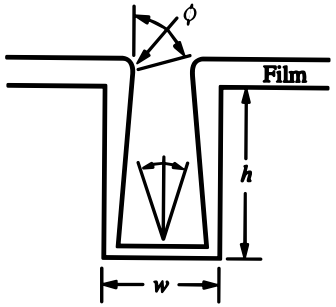
(a) typical for TEOS
(c) typical for LTO

Difference rather due to different sticking than surface transport (sticking of TEOS lower than for LTO)



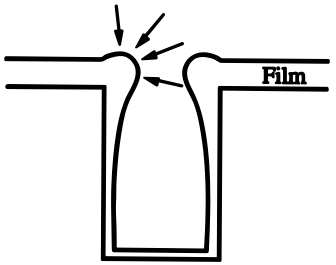
(a)

Uniform
Rapid surface migration



(b)

Nonconformal
Long mean free path
No surface migration



(c)

Nonconformal
Short mean free path
No surface migration

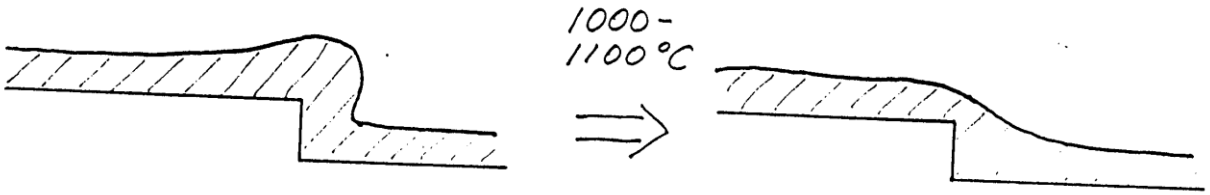
Example: SiO_2 CVD

Phosphosilicate Glass (PSG)

Phosphorous introduced in SiO_2

- Gettering of impurities in intermetallic dielectric
- Permitting glass flow at high temperature around 1000-1100°C

Glass flow improves poor step coverage of LTO:



By adding B → B-PSG = *BPSG*

B will help to reduce softening point to 800°C

Silicon nitride

Applications:

For mask in LOCOS process (barrier against oxygen diffusion)
Passivation layer: (barrier against H_2O, sodium)

LPCVD

$3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6H_2$ 650-800°C
(most common)

$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$ 700-900°C

Excess of NH_3 used in reaction!

PECVD

Si_3N_4 used for passivation using silane and NH_3 at 200-400°C
Contains much H! Usually non-stoichiometric!
Stress can be tuned by plasma parameters
New trend: High-density plasma systems

Properties of silicon nitride

Large tensile stress.

Typically max 2000 Å Si_3N_4 can be deposited on Si

TABLE 4
Properties of silicon nitride

Deposition	LPCVD	Plasma
Temperature (°C)	700–800	250–350
Composition	$Si_3N_4(H)$	SiN_xH_y
Si/N ratio	0.75	0.8–1.2
Atom % H	4–8	20–25
Refractive index	2.01	1.8–2.5
Density (g/cm^3)	2.9–3.1	2.4–2.8
Dielectric constant	6–7	6–9
Resistivity (ohm-cm)	10^{16}	10^6–10^{15}
Dielectric strength (10^6V/cm)	10	5
Energy gap (eV)	5	4–5
Stress (10^9 dyne/cm^2)	10 T	2C–5 T

(VLSI Techn. p. 263)

CVD and ALD of polysilicon and dielectric thin films

- Chemical Vapor Deposition (CVD)
  - Basic definitions
  - Reactor designs
  - Examples
    - Polysilicon CVD
    - Silicon Dioxide CVD
    - Silicon Nitride CVD
  - Modeling
- Atomic Layer Deposition (ALD)
  - Basic Definitions
  - Reactor Designs
  - Example
    - Aluminum Oxide (Al_2O_3) ALD

Atomic Layer Deposition (ALD)

Definition:

- CVD-based deposition mode
- But: Gases introduced sequentially
- But: Self-limiting surface reaction

	ALD	MBE	PVD	CVD
Step coverage	Excellent	Poor	Poor	Varies
Deposition rate	Acceptable	Acceptable	Excellent	Excellent
Thickness uniformity	Excellent	Acceptable	Excellent	Excellent
Material availability	Acceptable	Excellent	Excellent	Acceptable
Defects	Acceptable	Excellent	Poor	Acceptable

Atomic Layer Deposition (ALD)

Definition:

•CVD-based deposition mode

•But: Gases introduced sequentially

•But: Self-limiting surface reaction

Application:

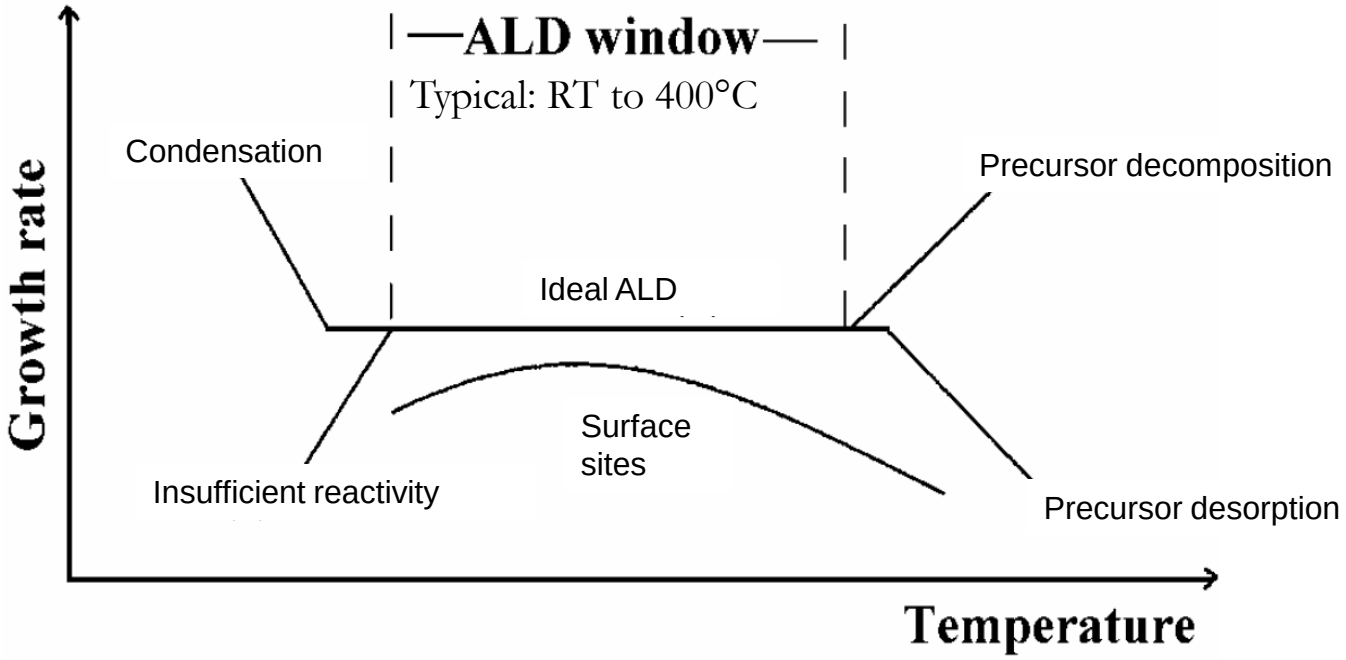
•Thin films from 1-500 nm

•High aspect / 3D structures

•Good film quality

•Most viable sub-5 nm deposition technique

Basic Principle of Atomic Layer Deposition



L. Niinistö, physica status solidi (a) 201, p. 1443-1452(2004)

Atomic Layer Deposition (ALD)

The principle of ALD is based on sequential pulsing of chemical precursor vapors, forming one atomic layer during each pulse sequence.

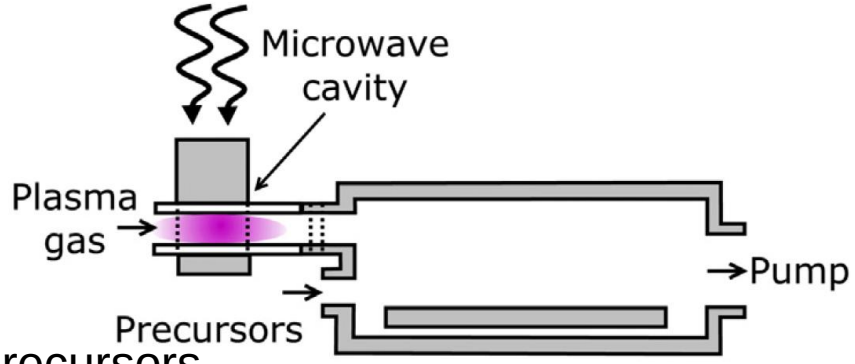
- Precise control of depositions down to the atomic scale
- Deposit nanometer thin films with special properties
- Pinhole free coatings, extremely uniform in thickness
- Deposition deep inside pores, trenches, and cavities
- A wide variety of thin films can be deposited (dielectrics and metals)
- A wide range of precursors available (gas, liquid or solid)
- Described in terms of “cycles”, a cycle consists of four basic steps

System in Electrum at KTH used in electronics, MEMS…

ALD: Reactor Designs

Thermal ALD

- Chemistry relies on substrate temperature
- Radiative heating or direct heat transfer
- Traveling wave cross-flow reactors and perpendicular flow (showerhead)
- Limited pressure range 1-10 Torr
- Single wafer or batch configuration commercially available from ASM, Picosun, ***Beneq***, Cambridge Nanotech, etc.



Radical enhanced ALD

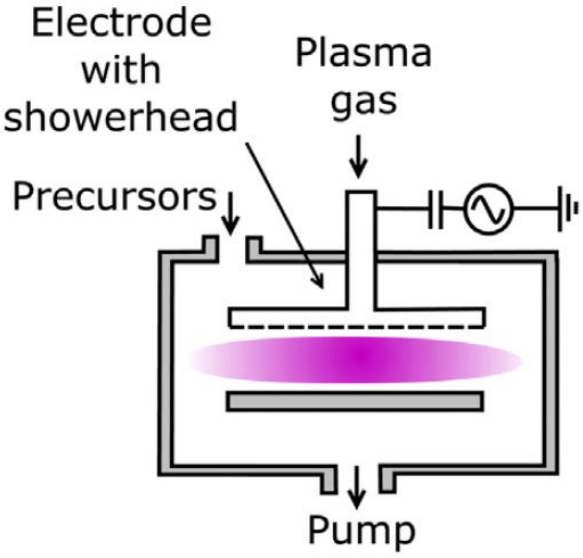
- Chemistry thermally activated for one of the precursors
- Radical source is attached to reactor or the reactor consists of radical beams in UHV
- Reactors based on this concept are so far not commercially available, but separate radical sources are, such as the MKS R*Evolution

S. Heil, “Plasma-Assisted Atomic Layer Deposition of Metal Oxides and Nitrides” PhD Thesis, 2008

ALD: Reactor Designs

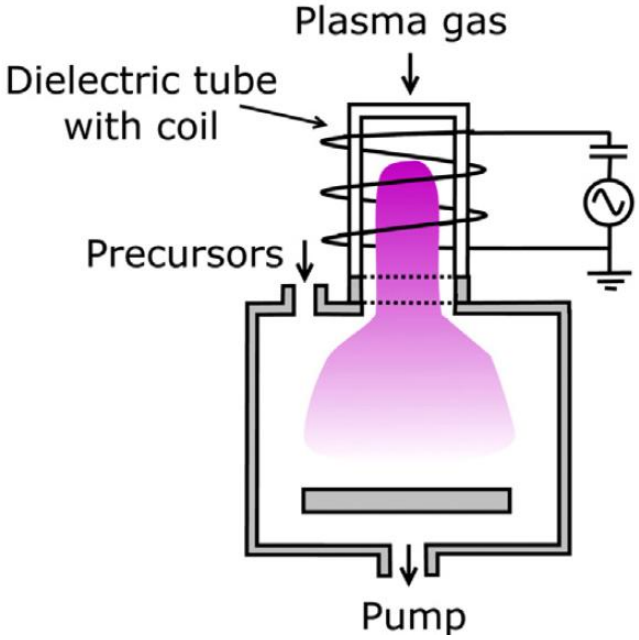
Direct plasma ALD

- Precursor injection through a showerhead or in the background (due to low pressure (1-10 mTorr))
- Ion bombardment (ion energy > ~100 eV) is an issue when depositing on sensitive substrates
- Reactors commercially available from ASM etc.



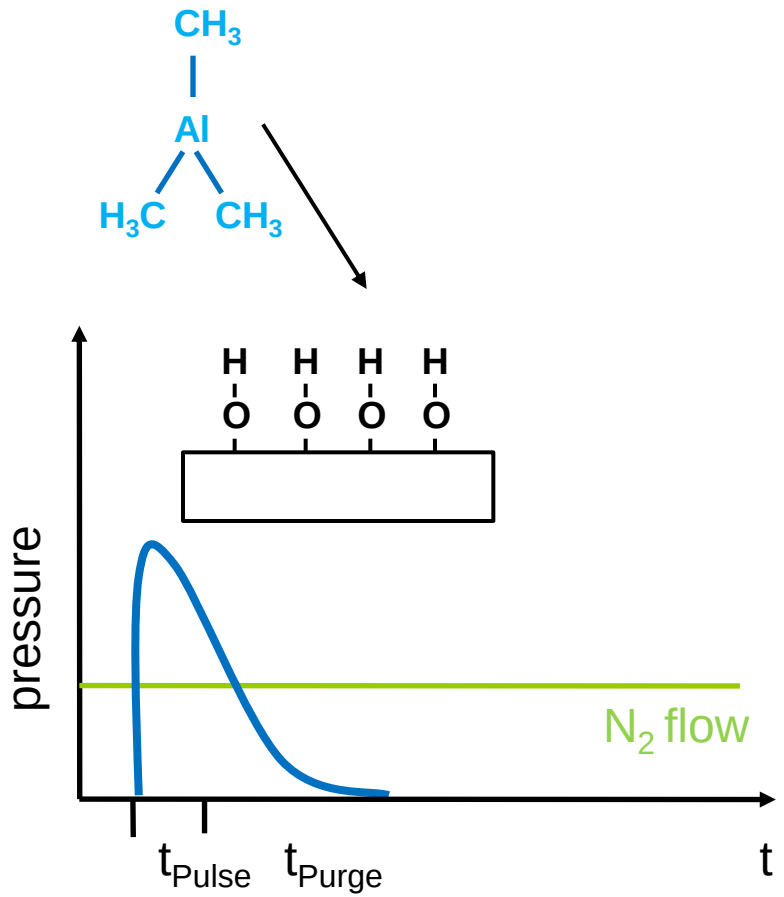
Remote plasma ALD

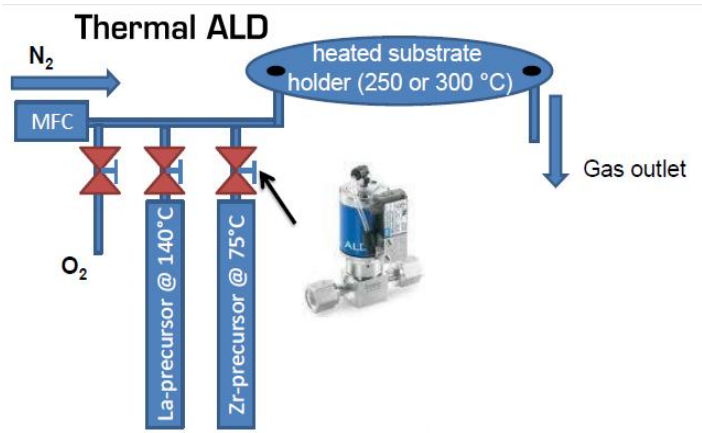
- ICP plasma source most common
- Wide pressure range (1-1000 mTorr)
- Low ion bombardment (energy < ~20 eV)
- Commercially available from Oxford Instruments, Cambridge Nanotech etc.



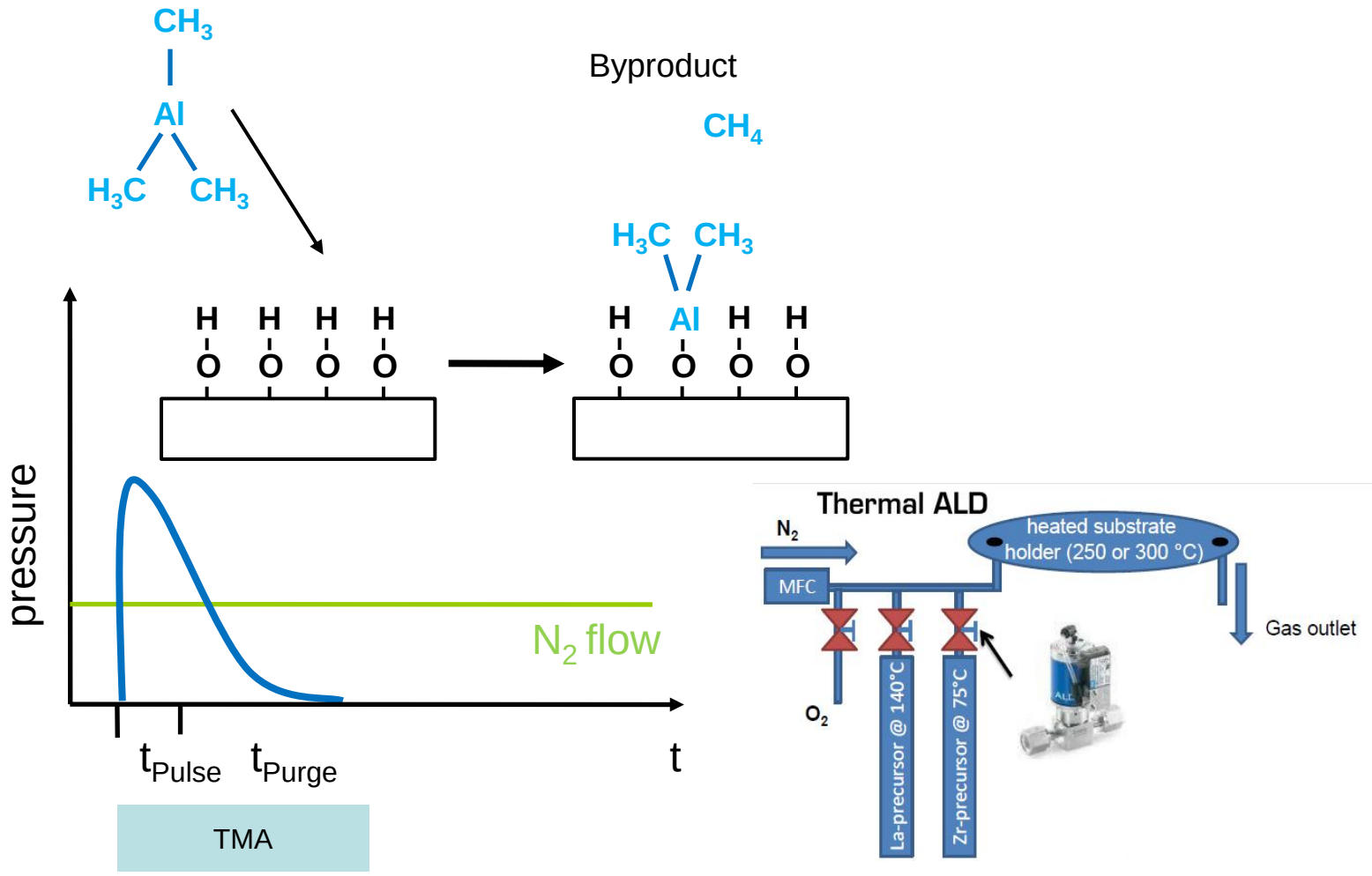
S. Heil, “Plasma-Assisted Atomic Layer Deposition of Metal Oxides and Nitrides” PhD Thesis, 2008

Basic Principle of Atomic Layer Deposition

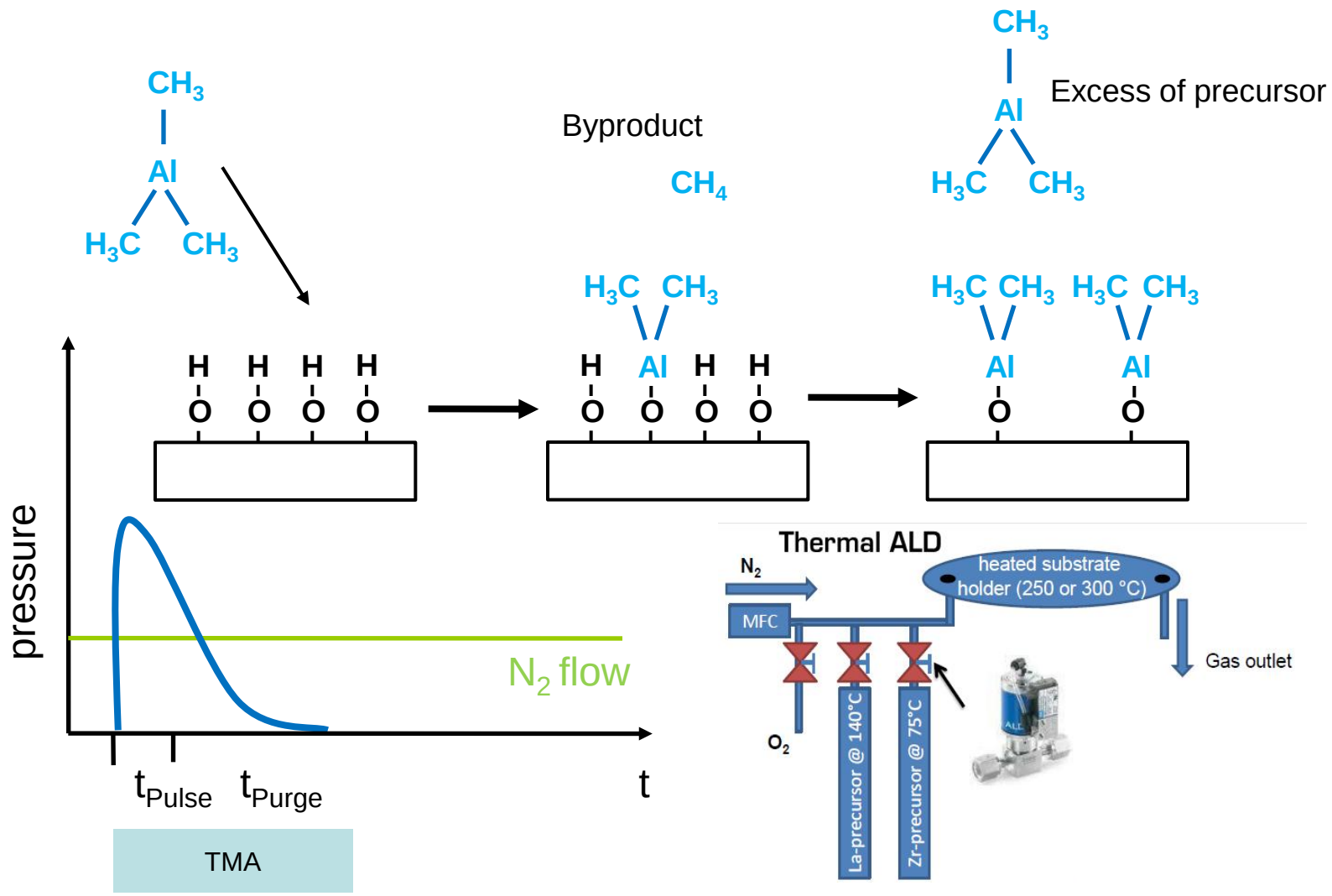




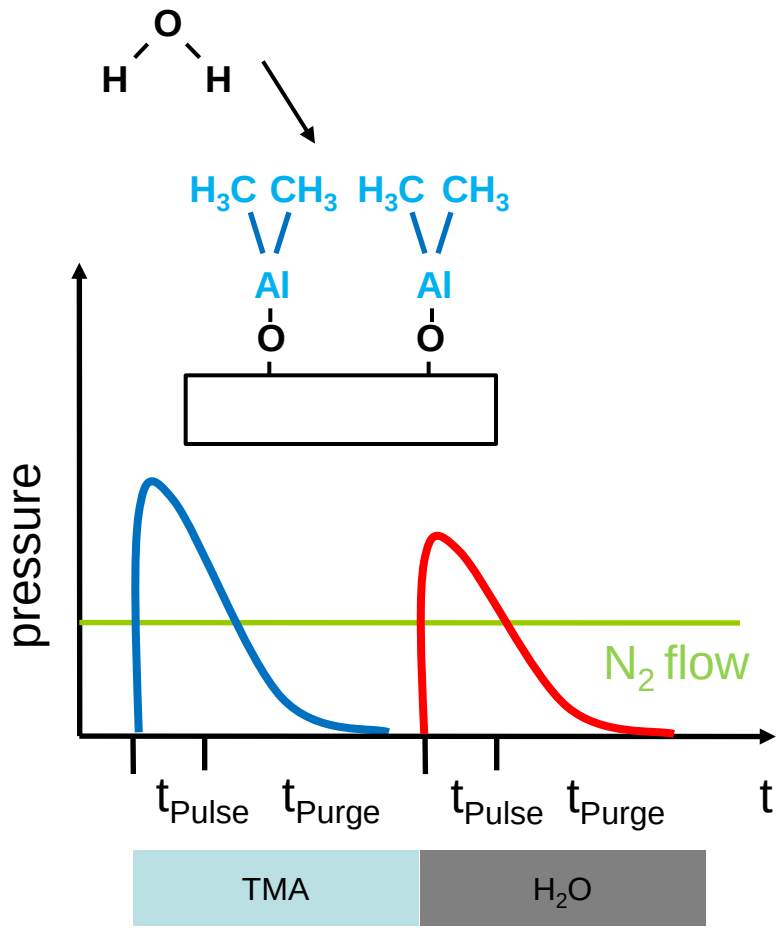
Basic Principle of Atomic Layer Deposition

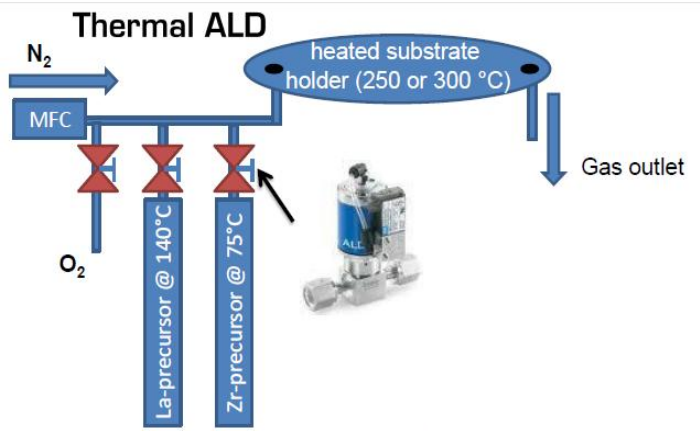


Basic Principle of Atomic Layer Deposition

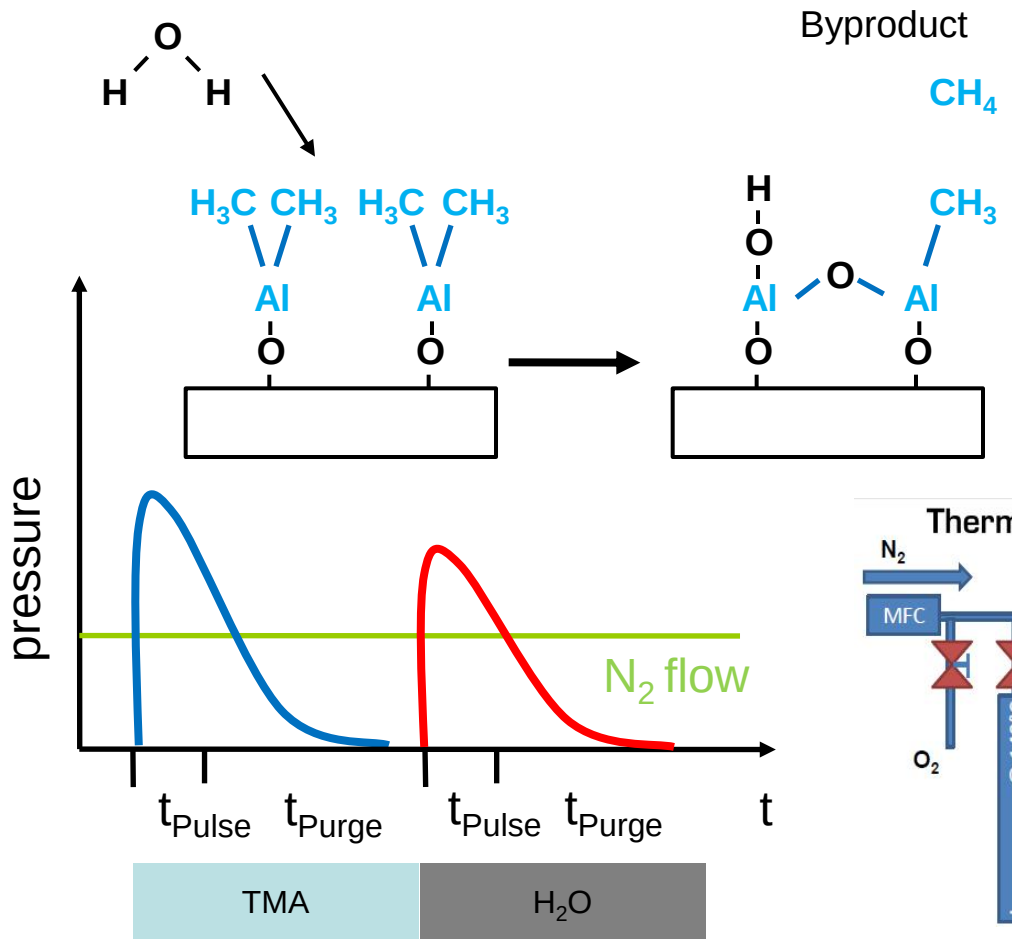


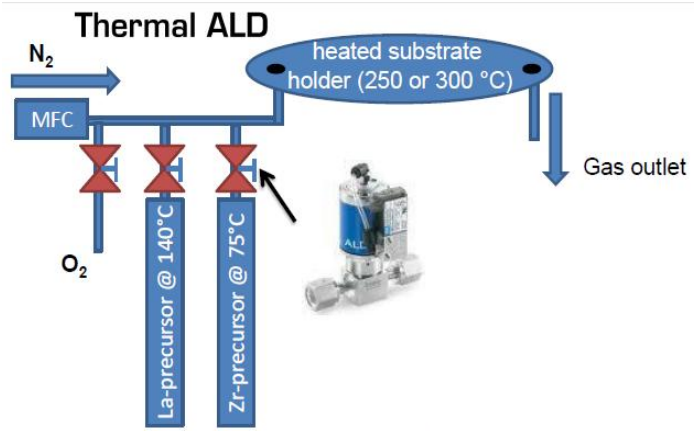
Basic Principle of Atomic Layer Deposition



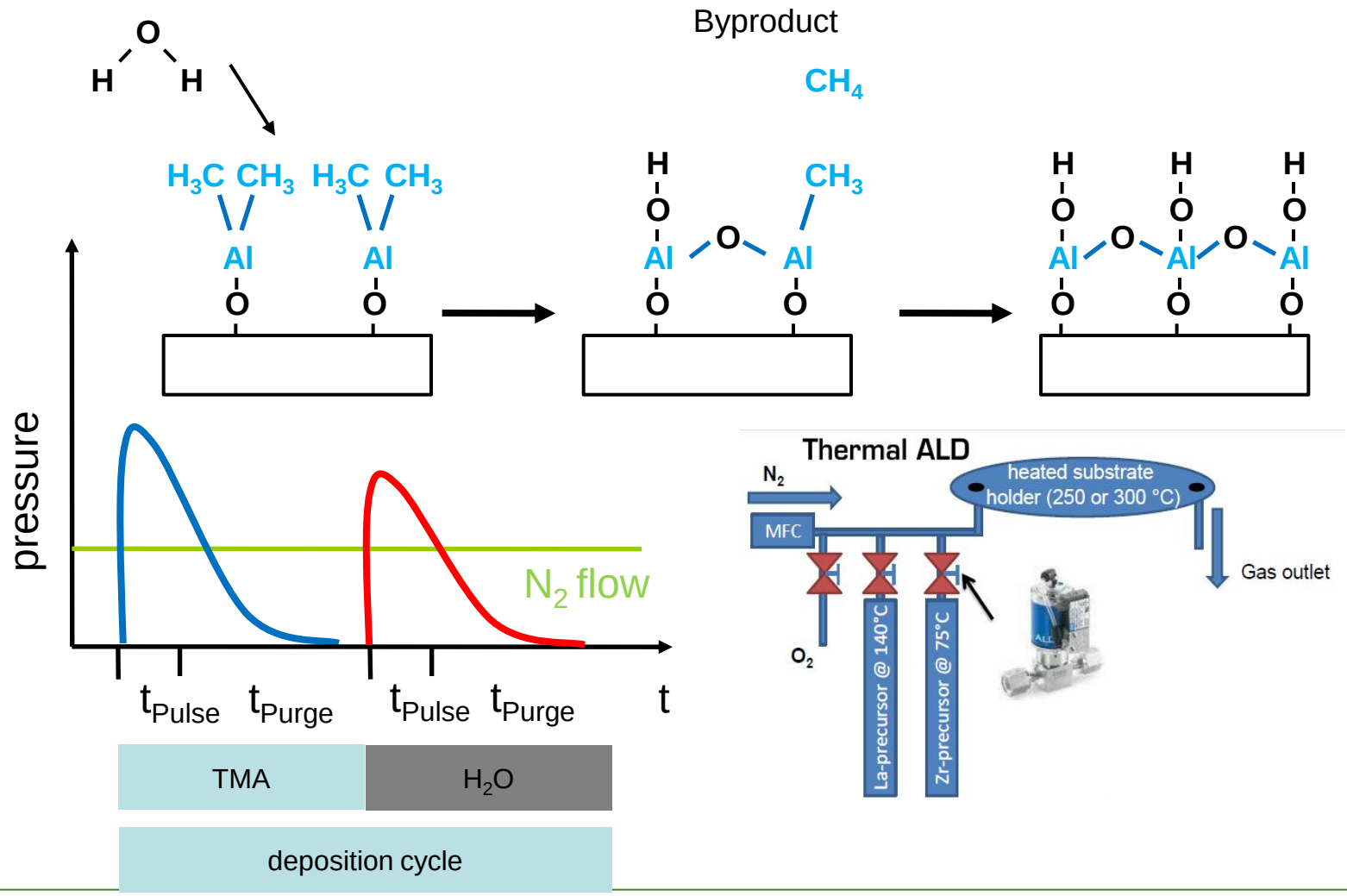


Basic Principle of Atomic Layer Deposition

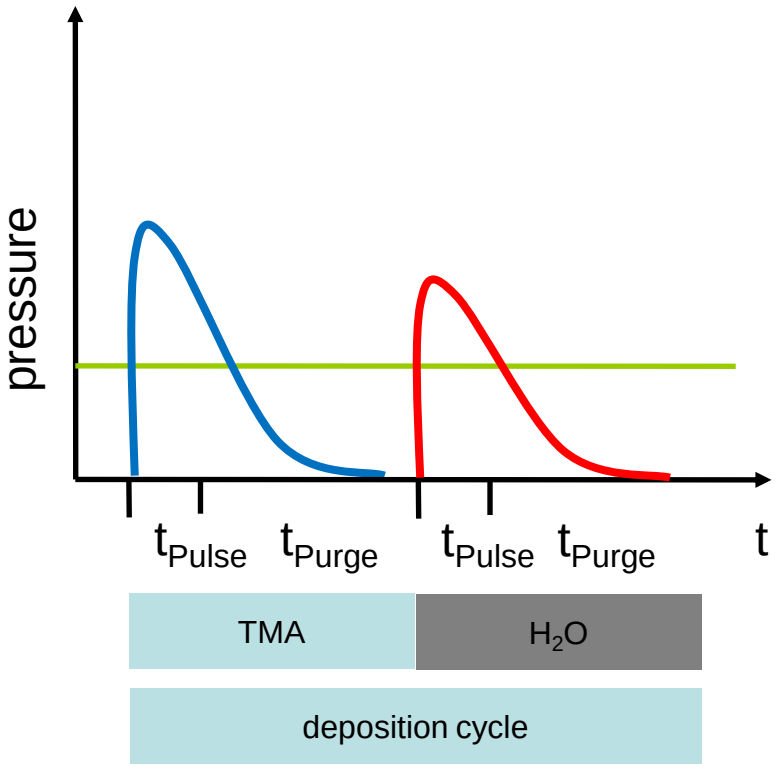


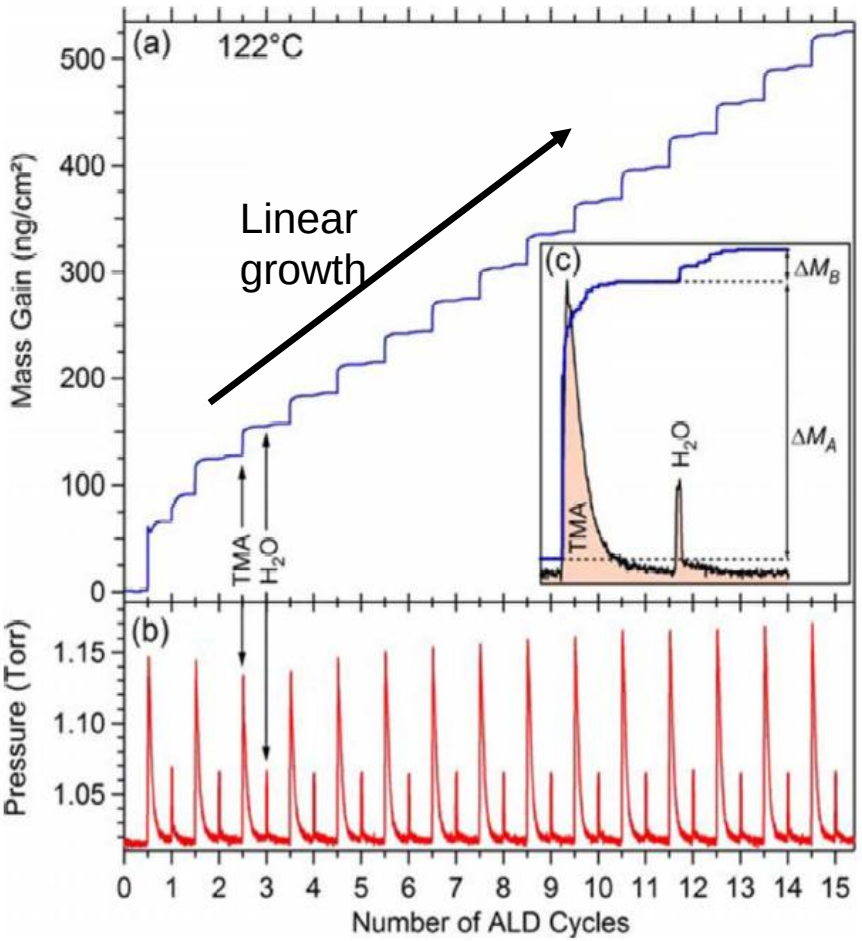


Basic Principle of Atomic Layer Deposition



Basic Principle of Atomic Layer Deposition

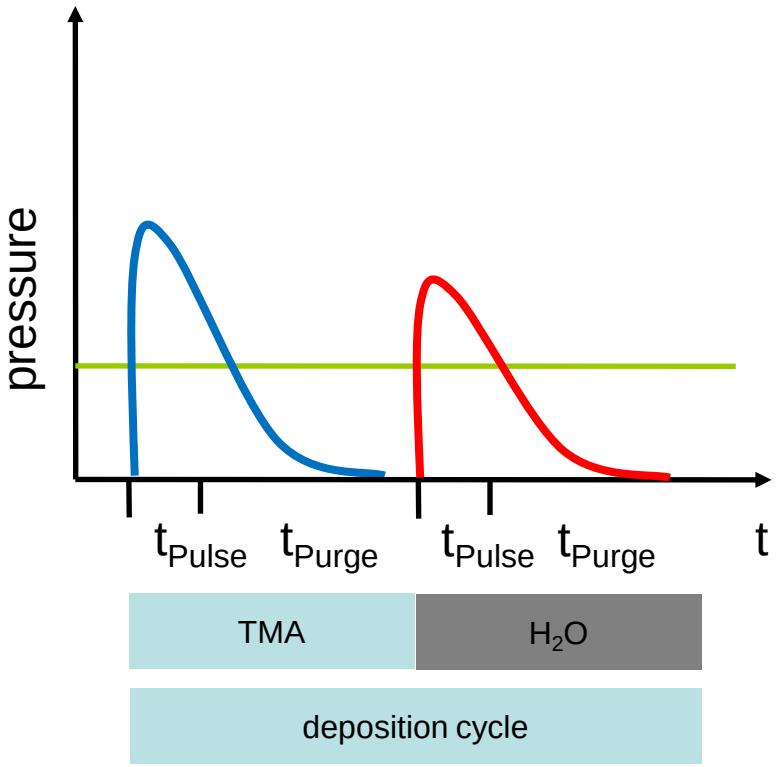


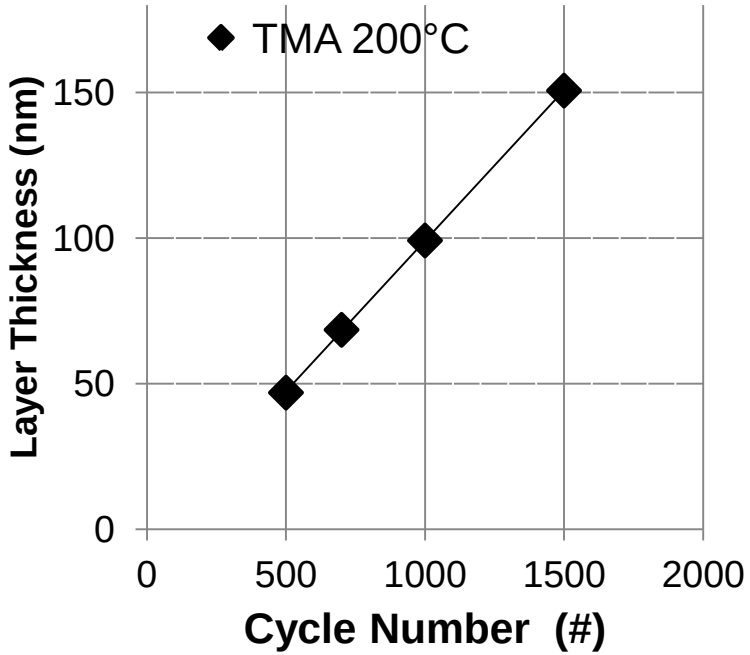


Al_2O_3 on fluorinated W surface

R.W. Wind, JAP 105, 074309 (2009)

Basic Principle of Atomic Layer Deposition





Si, H-terminated surface

Atomic Layer Deposition (ALD)

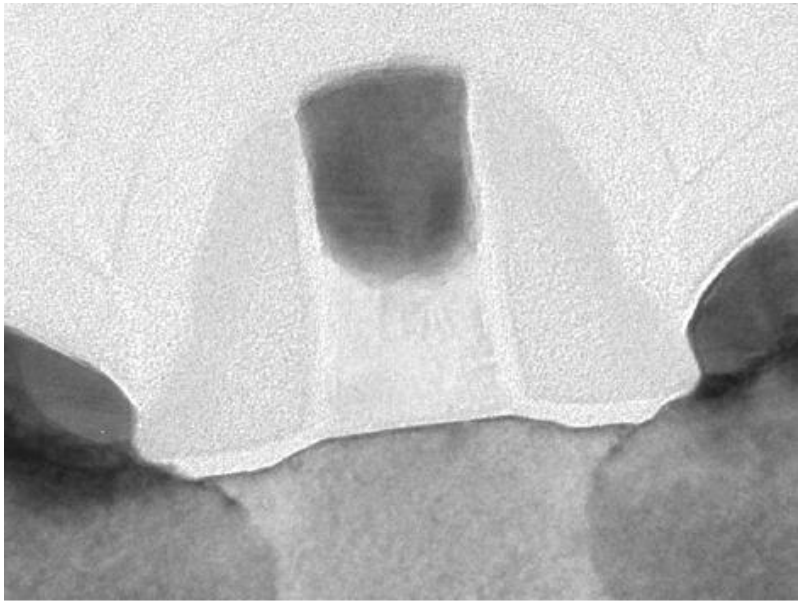
Properties and Applications

- High-k dielectrics

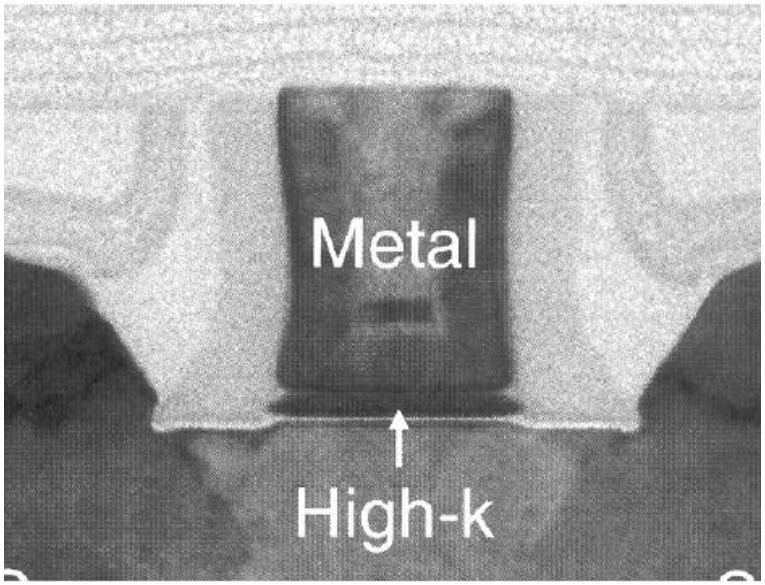
ALD Film	Min. Deposition Temperature C	Dielectric Constant (k)
Al_2O_3	>25	6-9
SiO_2	>100	3.9
HfO_2	>80	>15
TiO_2	>80	>20
Ta_2O_5	>100	>22
ZrO_2	>80	>14

- Metal Gate eliminate poly-Si depletion effects
- Solve pinning of V_T of poly-Si on high-k dielectrics

Poly-Si with SiON



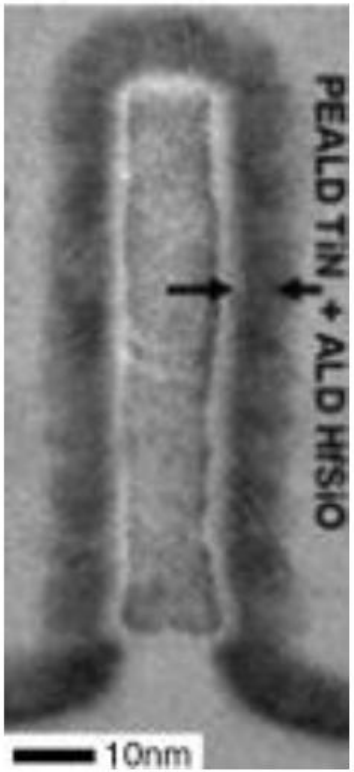
65 nm

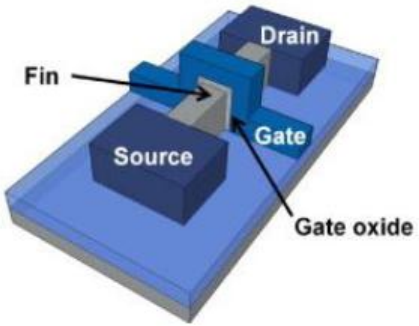


45 nm

Images from Intel © (Kelin Kuhn / SSDM / Japan / 2009)

- High aspect ratios and 3D structures

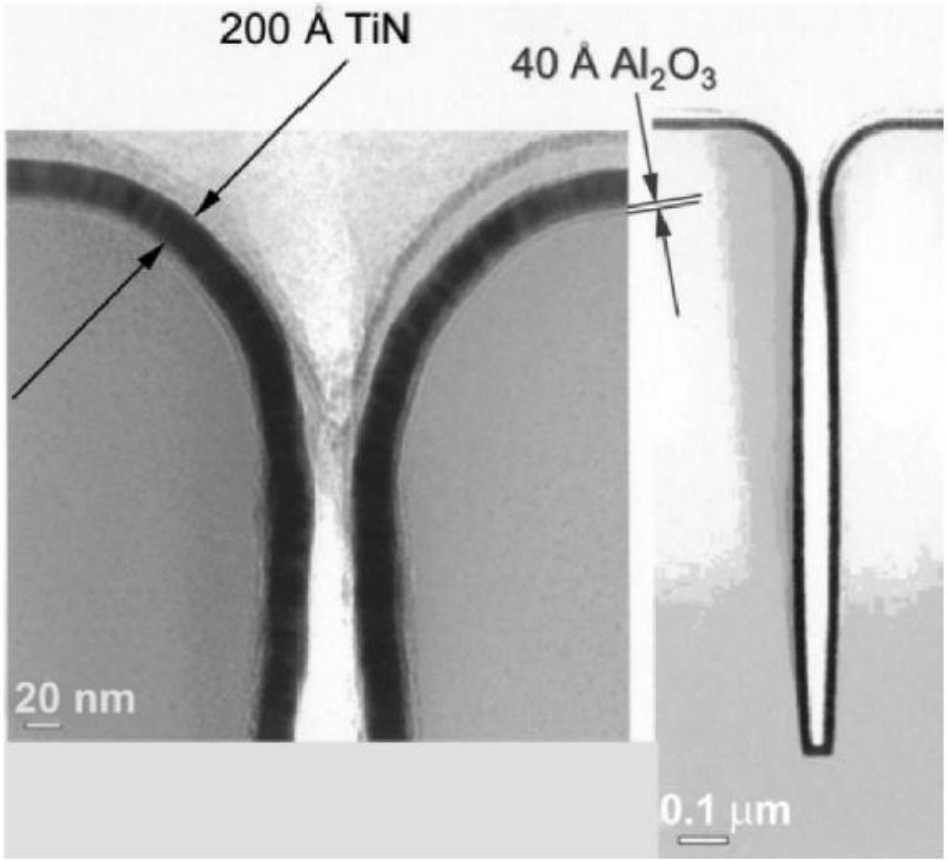




Plasma Enhanced ALD TiN + ALD HfSiO

H. Kim, Thin Solid Films 517, p.2563-2580 (2009)
And references therein.

- High aspect ratios and 3D structures



O. Sneh, Thin Solid Films, **402** p.248-261 (2002).

Atomic Layer Deposition (ALD) - Advantages

Perfect films :

Thickness control to atomic level (deposited one atomic layer at a time)

Pinhole free films, even over very large areas

Excellent repeatability

Wide process windows: ALD is not sensitive to temperature or precursor dose variations

Amorphous or crystalline depending on substrate and temperature

Digital control of sandwiches, heterostructures, nanolaminates, mixed oxides, graded index layers and doping

Oxides, nitrides, metals, semiconductors possible

100% film density guarantees ideal material properties (n, E_{bd}, k, etc)

Conformal Coating :

Perfect 3D conformality, 100% step coverage: uniform coatings on flat, inside porous and around particle samples

Atomically flat and smooth coating

Large area thickness uniformity

Challenging Substrates :

Gentle deposition process for sensitive substrates, no plasma needed (though it is available as an option)

Low temperature deposition possible (RT-400 °C)

Coats on everything, even on teflon

Excellent adhesion due to chemical bonds at the first layer

Low stress because of molecular self assembly