Lecture 8

Microlithography

Lithography

- Introduction
- Process Flow
- Wafer Exposure Systems
- Masks
- Resists
- State of the Art Lithography
- Next Generation Lithography (NGL)
  - Recommended videos:
  - http://www.youtube.com/user/asmlcompany#p/search/1/jH6Urfqt_d4
  - http://www.youtube.com/user/asmlcompany#p/search/3/u4uTn4lq7Kw
  - http://www.youtube.com/user/asmlcompany#p/search/4/3cfDMVnjAgE

Introduction

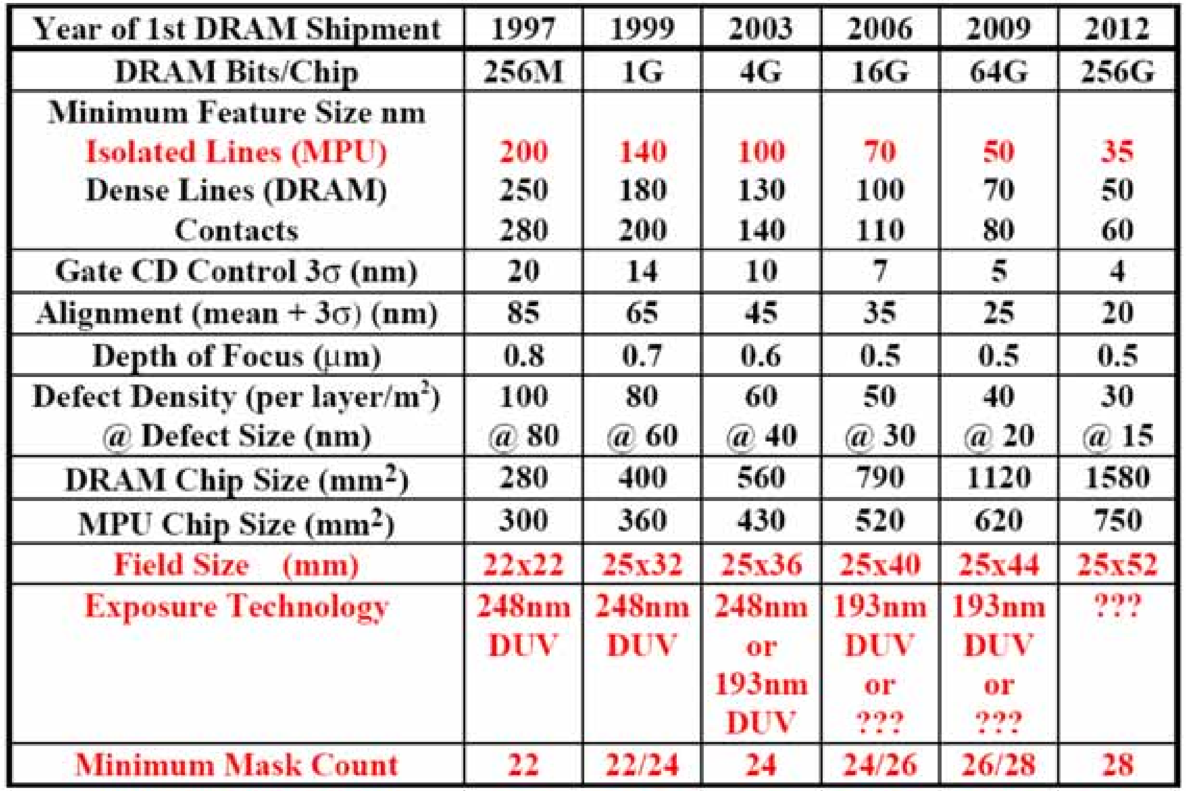
- Lithography is arguably the single most important technology in IC manufacturing.
- The SIA NTRS / ITRS is driven by the desire to continue scaling device feature sizes.

0.7X in linear dimension every 3 years.

Placement accuracy » 1/3 of feature size.

» 35% of wafer manufacturing costs for lithography.

Note the ???. These represents the single biggest uncertainty about the future of the roadmap.

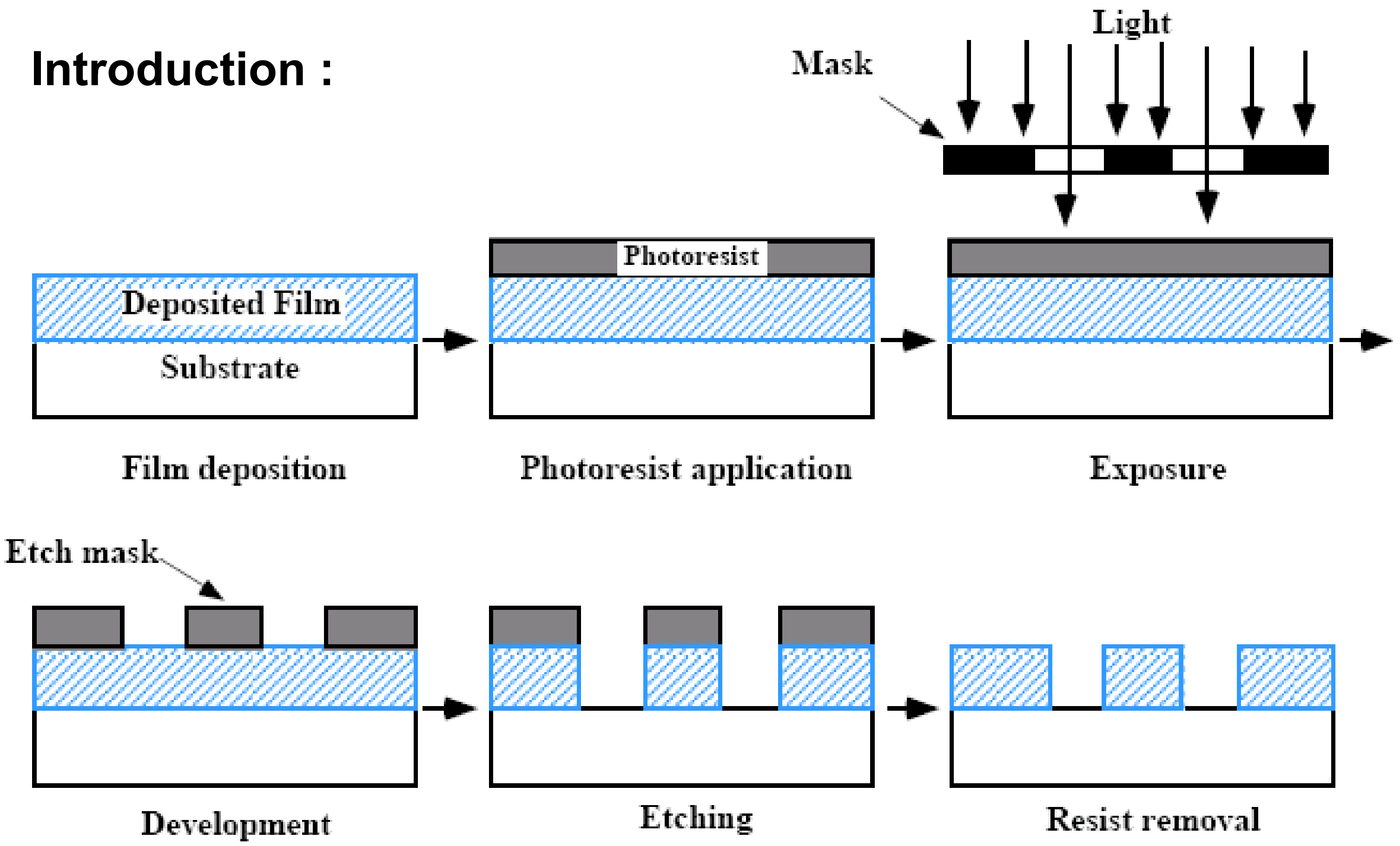


Year of 1st DRAM Shipment	1997	1999	2003	2006	2009	2012
DRAM Bits/Chip	256M	1G	4G	16G	64G	256G
Minimum Feature Size nm						
Isolated Lines (MPU)	200	140	100	70	50	35
Dense Lines (DRAM)	250	180	130	100	70	50
Contacts	280	200	140	110	80	60
Gate CD Control 3σ (nm)	20	14	10	7	5	4
Alignment (mean + 3σ) (nm)	85	65	45	35	25	20
Depth of Focus (μm)	0.8	0.7	0.6	0.5	0.5	0.5
Defect Density (per layer/m^2) @ Defect Size (nm)	100 @ 80	80 @ 60	60 @ 40	50 @ 30	40 @ 20	30 @ 15
DRAM Chip Size (mm^2)	280	400	560	790	1120	1580
MPU Chip Size (mm^2)	300	360	430	520	620	750
Field Size (mm)	22x22	25x32	25x36	25x40	25x44	25x52
Exposure Technology	248nm DUV	248nm DUV	248nm or 193nm DUV	193nm DUV or ???	193nm DUV or ???	???
Minimum Mask Count	22	22/24	24	24/26	26/28	28

NTRS 1997

Introduction

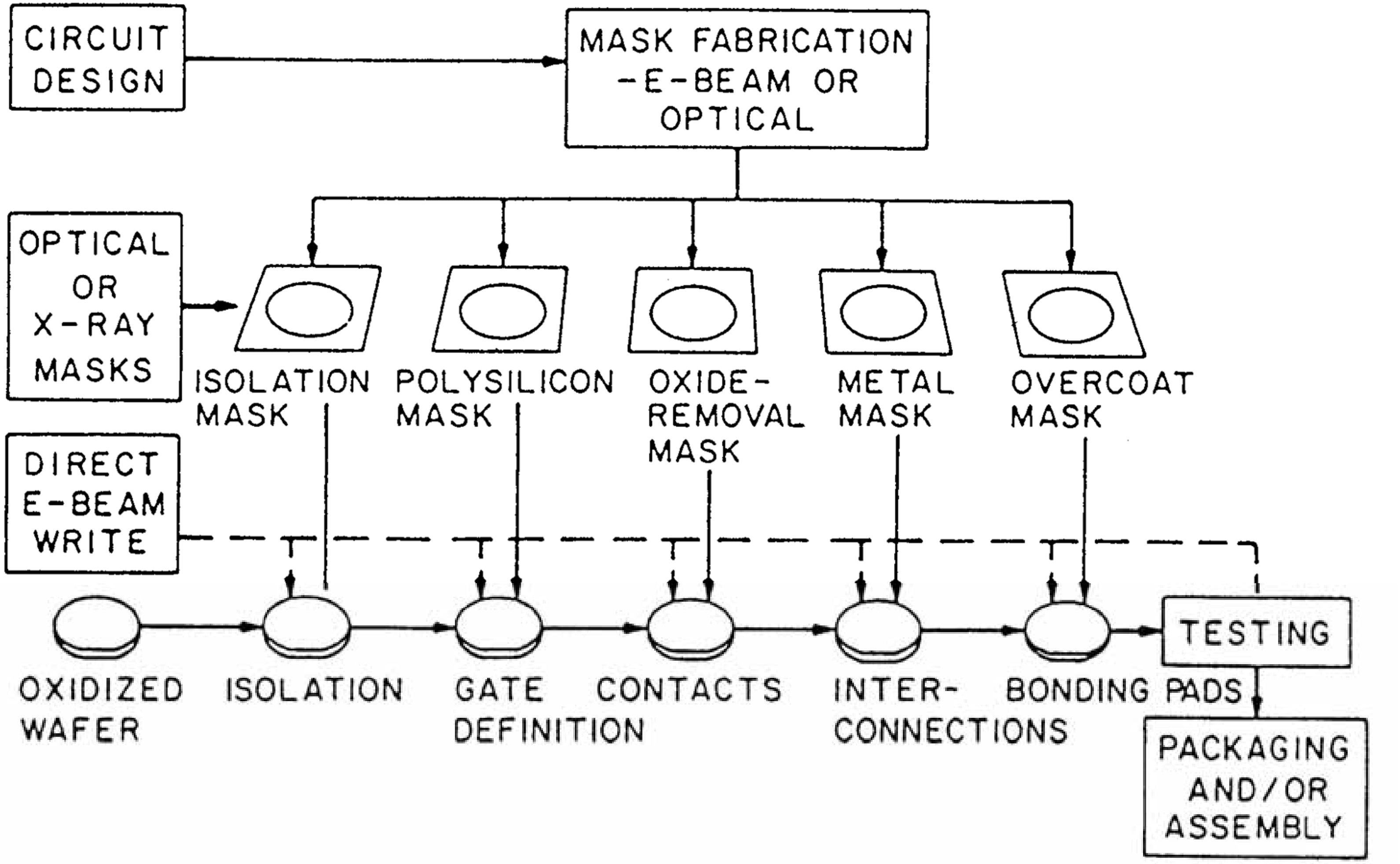
Introduction :



- Lithography is a very common but critical process step.
- High reolution and feature density are important aspects.

Introduction

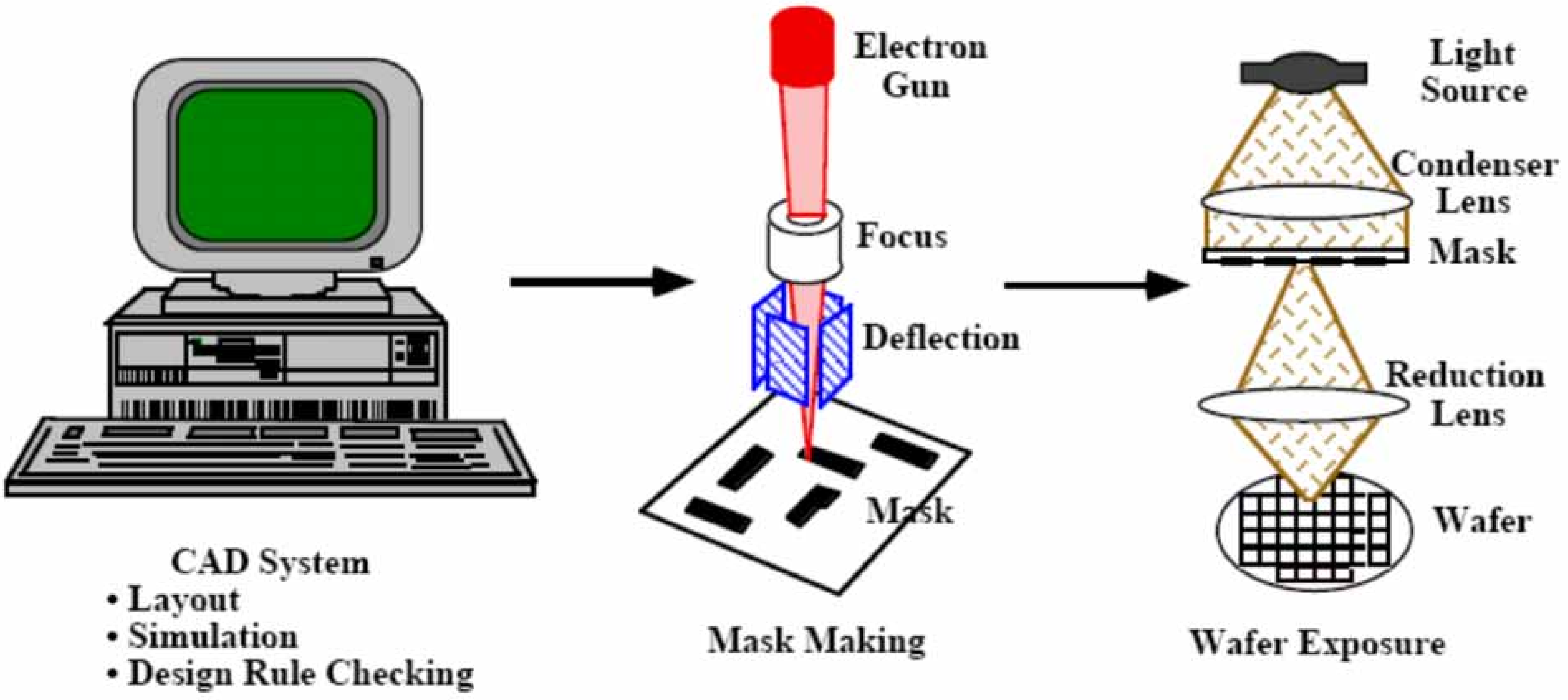
Lithography in manufacturing



Introduction

Patterning process consists of:

1. Mask design
2. Mask fabrication
3. Wafer printing.



(Plummer p 203)

Introduction

Lithography is the most critical step in scaling as described in ITRS

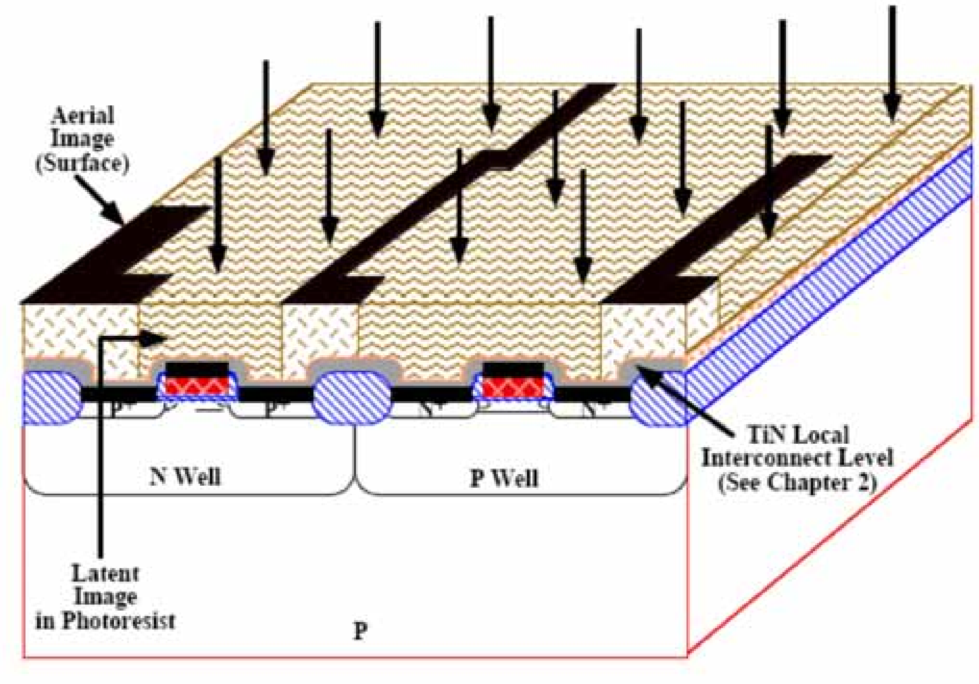
This “wafer printing process” can be divided into three parts

A. Wafer Exposure Systems

B. Light source

C. Resist

- Aerial image: pattern of optical radiation striking the top of the resist
- Latent image: is the 3D replica produced by chemical processes in the resist



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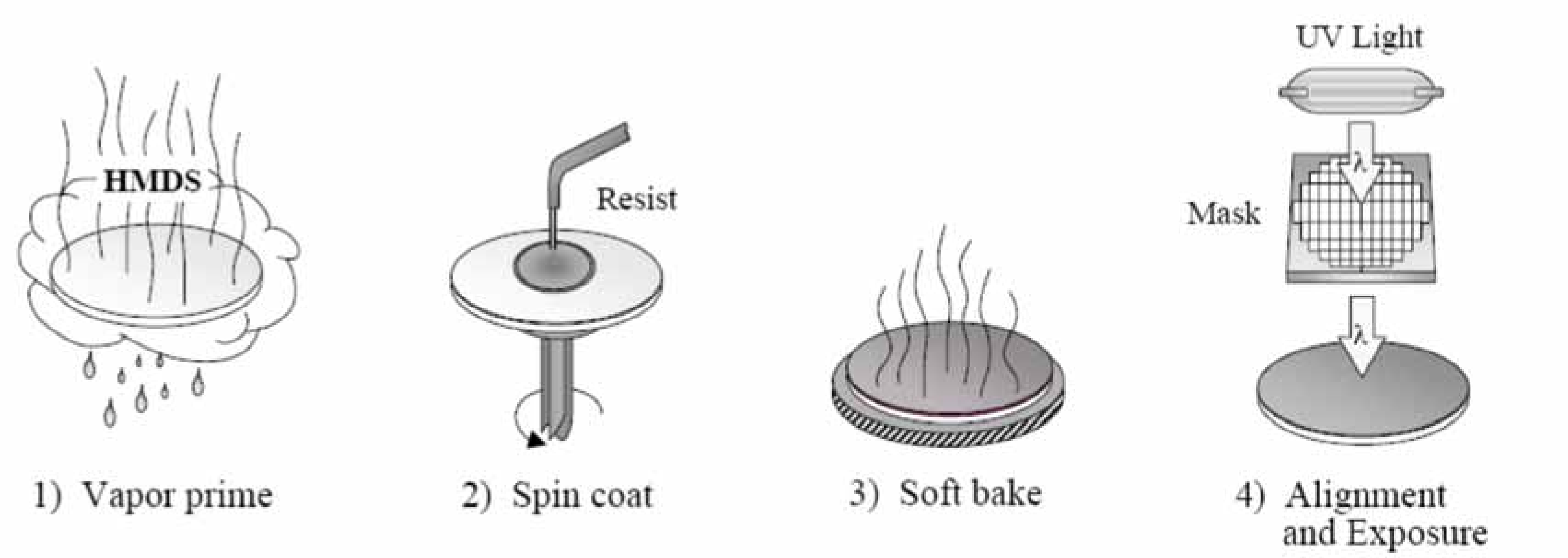
Lithography Process Flow

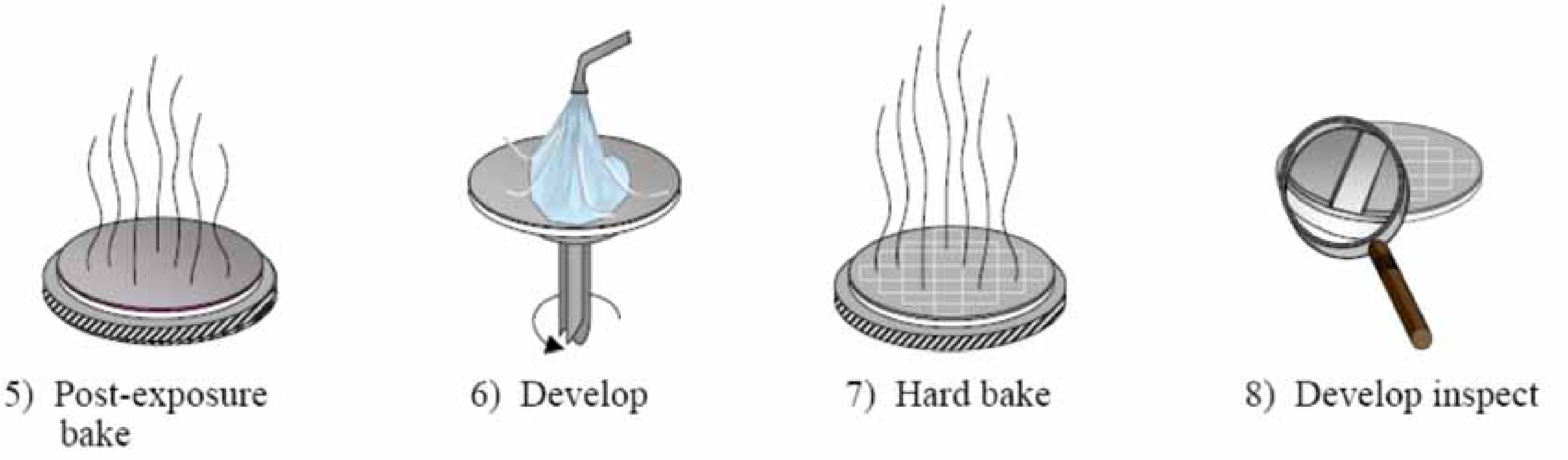


Before applying photo resist: Surface cleaning and/or dehydration baking

Adhesion promoter: HMDS(hexamethyldisilane)

Soft bake (Pre-bake): 90-100°C at 10-30‘

Lithography Process Flow

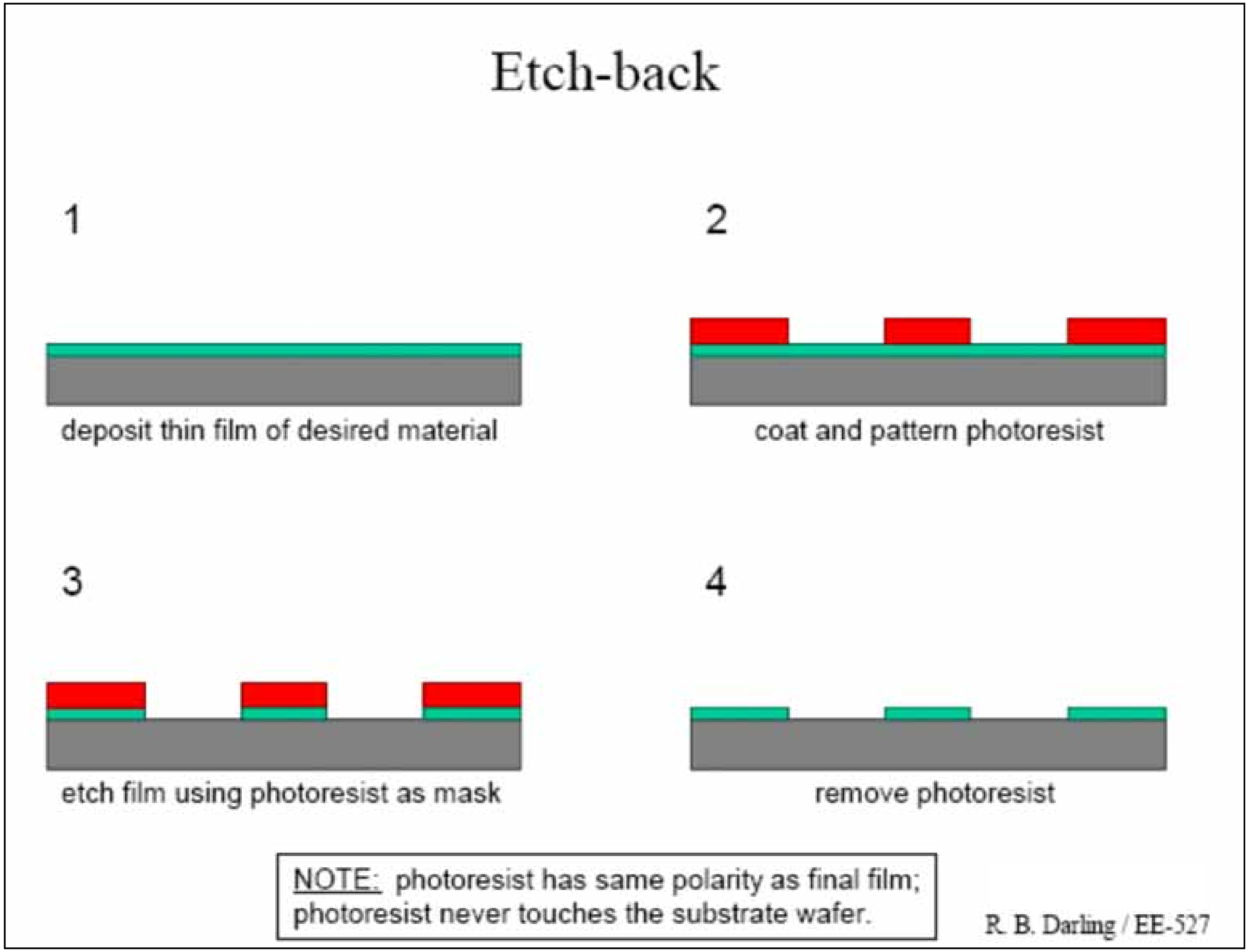


Optional post-exposure bake (PEB) for suppressing standing waves in PR

Develop: 30s to several minutes at room temperature (RT)

Hard bake (Post-bake): 100-140°C at 10-30'

Lithography Process Flow: Pattern Transfer - Etching



Etch-back

1

deposit thin film of desired material

2

coat and pattern photoresist

3

etch film using photoresist as mask

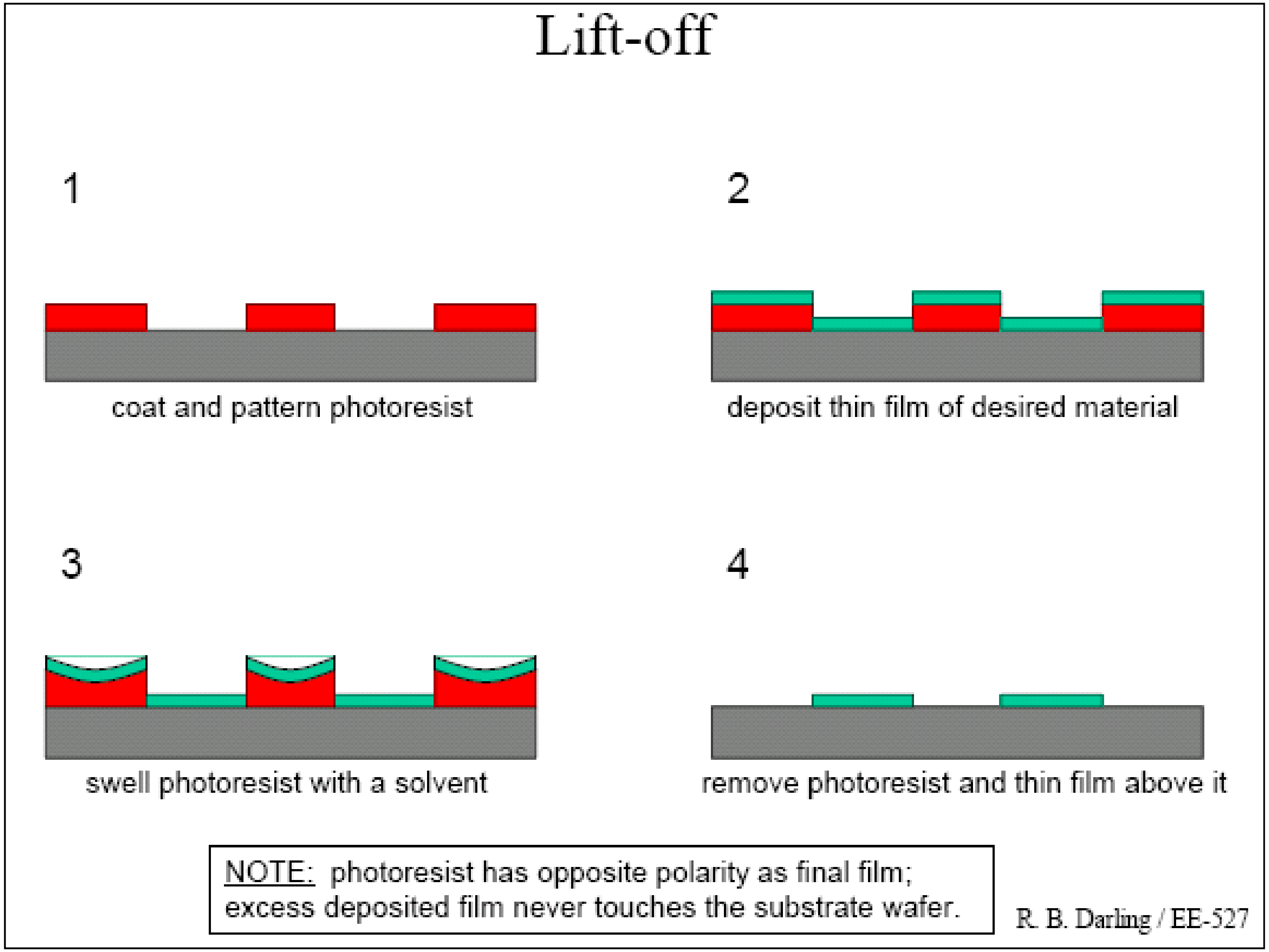
4

remove photoresist

NOTE: photoresist has same polarity as final film; photoresist never touches the substrate wafer.

R. B. Darling / EE-527

Lithography Process Flow: Pattern Transfer - Lift-off



NOTE: photoresist has opposite polarity as final film; excess deposited film never touches the substrate wafer.

R. B. Darling / EE-527

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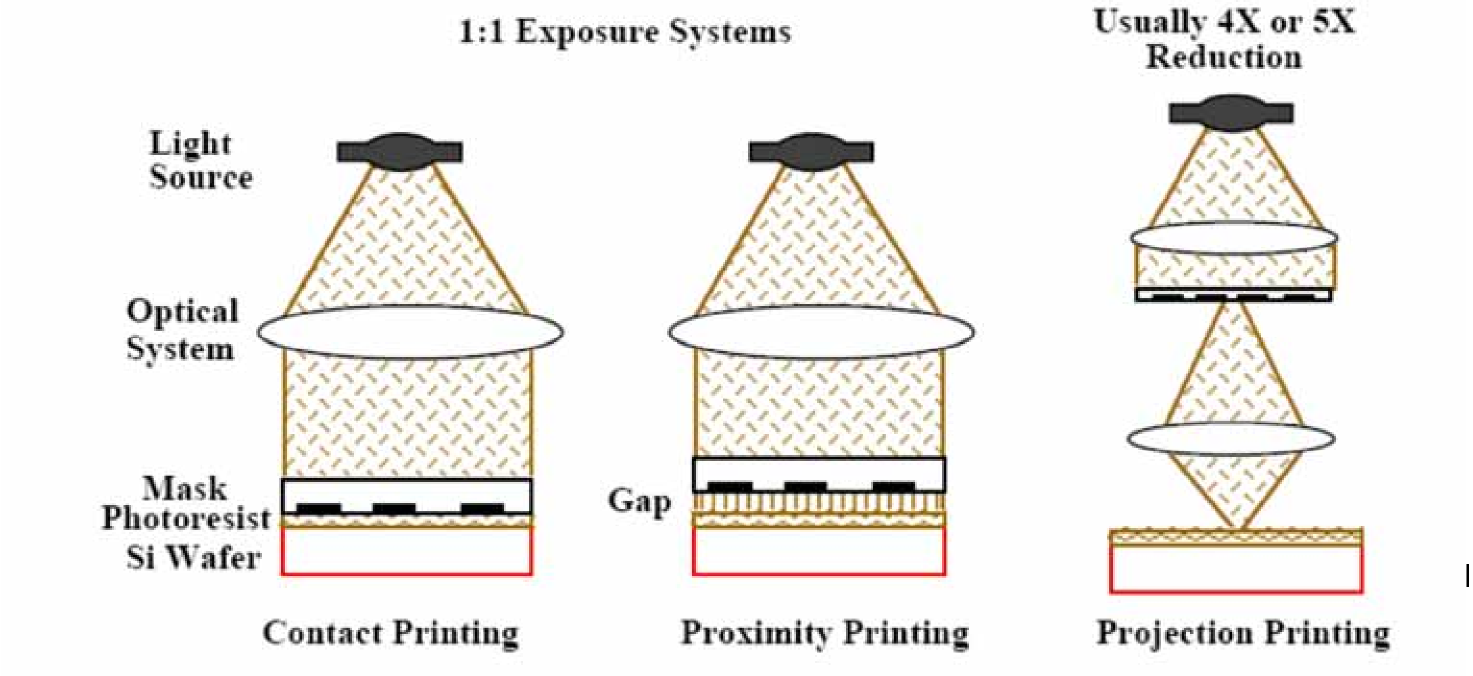
Wafer exposure systems using mask



lummer p 208)

Printing system	Magn.	Resolution (µm)	Use
Contact	1:1	0.1 - 1	Research
Proximity	1:1	2 - 4	Low cost processes
Projection	4/5:1	0.1 - 1	Stepper litho - mainstream in VLSI

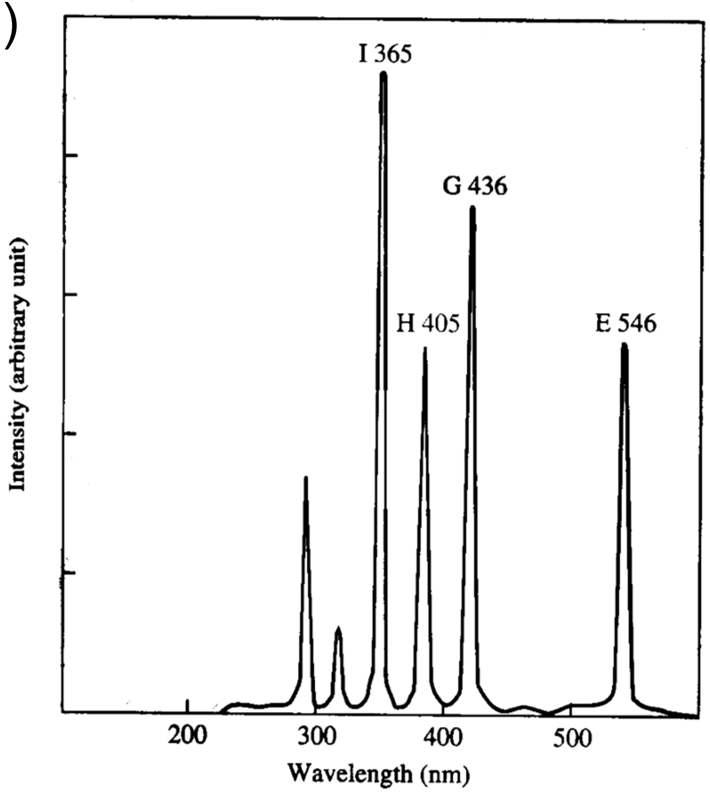
Light Sources

Classical: *Hg (mercury) vapor lamp* with photon emission lines e,g,h,i

Proximity and contact litho: Often broadband exposure (several lines)

Projection: Monochromatic exposure at wavelength λ:

- g-line: 436 nm (for > 0.6-0-7 µm linewidths)
- i-line: 365 nm (for 0.5 µm and 0.35 µm)



Deep UV (DUV) litho systems based on *excimer lasers:*

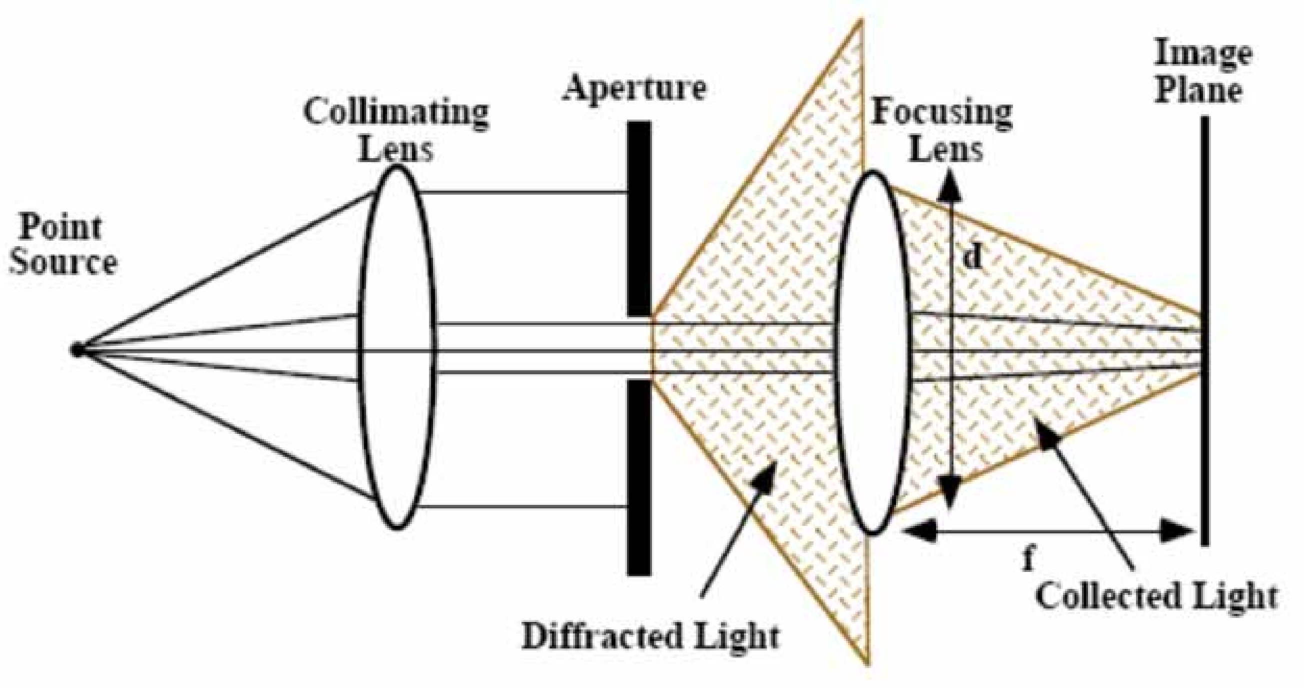
- KrF: 248 nm (for 0.25 and 0.18 µm)
- ArF: 193 nm (for 0.13 and 0.10 µm)
- F2: 157 nm (for sub-0.1 µm)

Excimer lasers used in flash mode

Diffraction

Modern lithography tools are limited by the spreading of light (and *not* their optical elements)

- If the aperture is on the order of λ, the light spreads out after passing through the aperture (The smaller the aperture, the more it spreads out)
- If we want to image the aperture on an image plane (resist), we can collect the light using a lens and focus it on the image plane
- The finite diameter of the lens means some information is lost



Diffraction is usually described in terms of two limiting cases

Fresnel diffraction - near field

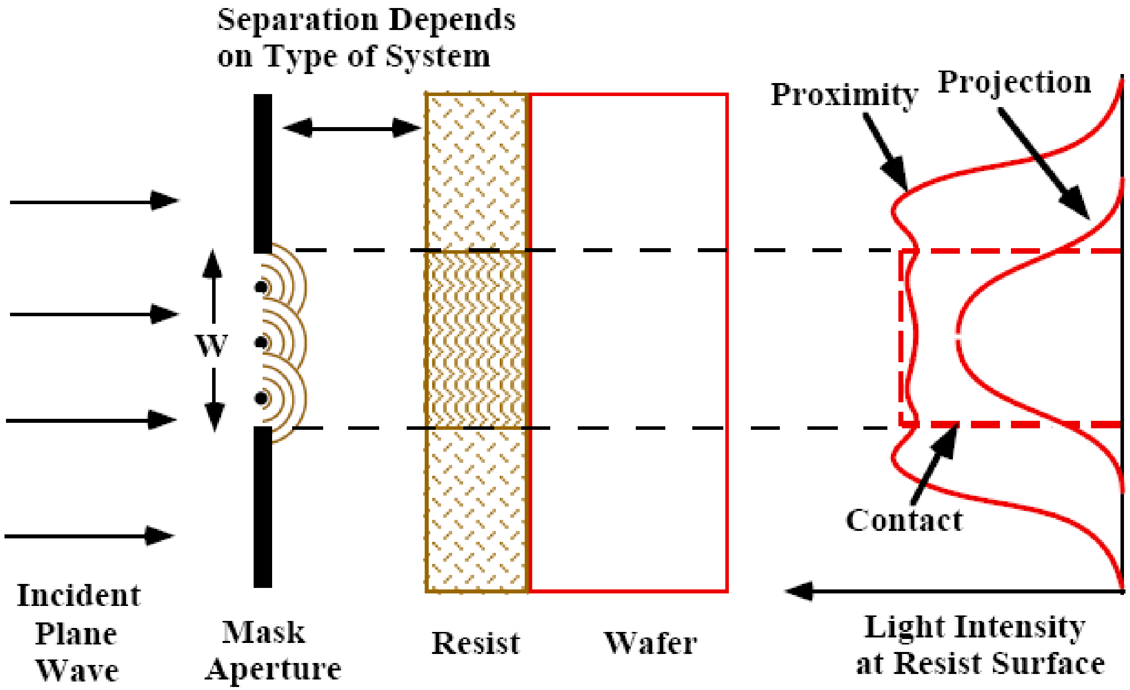
Fraunhofer diffraction - far field

Diffraction

Modern lithography tools are limited by the spreading of light (and *not* their optical elements)

Type of spreading depends on separation mask - wafer:

Hard contact	(Almost) no diffraction
Proximity	Near field or Fresnel diffraction
Projection	Far field or Fraunhofer diffraction



Fraunhofer Diffraction: Improving Resolution

These are the dominant systems in use today.

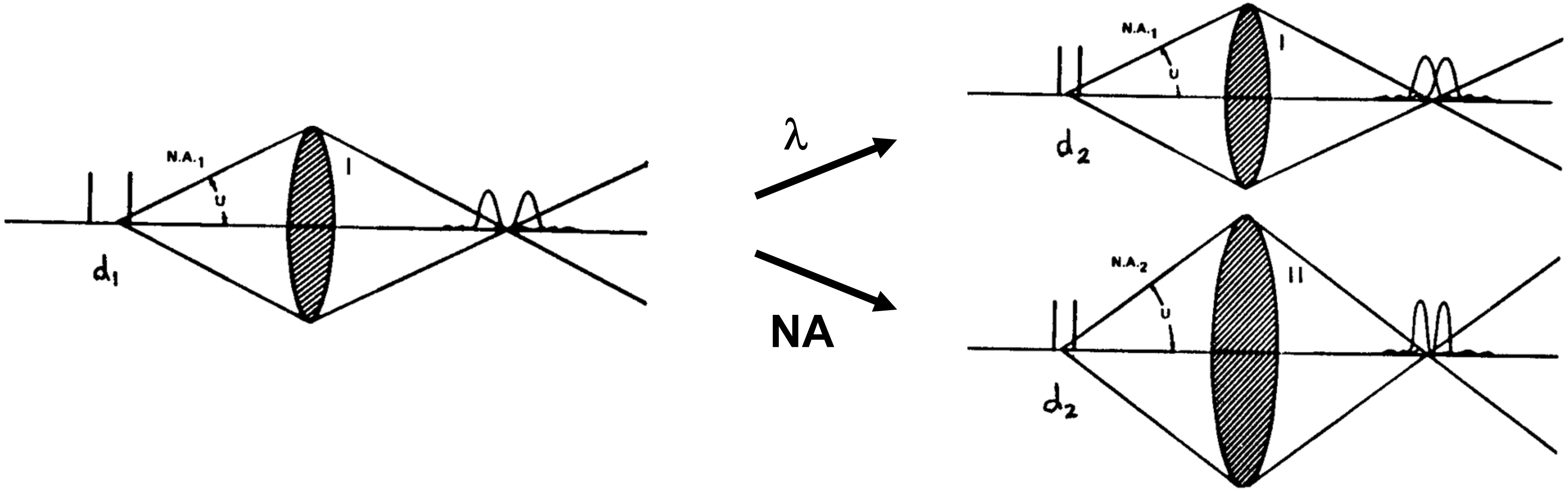
Experimental parameter depending on system and resist

Resolution *R*

Rayleigh resolution: $R = \frac{0.61\lambda}{NA}$

Practical resolution: $R = k_1 \frac{\lambda}{NA}$ where $0.6 < k_1 < 0.8$

Improve resolution by reducing λ or increasing NA:



Mikael Östling / Max Lemme KTH (Wolf p 464)

Fraunhofer Diffraction: Improving Resolution

Depth of Focus (*DOF)*

Experimental parameter

- **Defined as:**

$$DOF = \pm \frac{\lambda}{2(NA)^2} = \pm k_2 \frac{\lambda}{(NA)^2}$$

- **λ depends on availability of adequate light source**
- **Higher NA lenses also decrease the depth of focus**
- **DOF a problem in modern steppers! → Careful control over image plan, resist smoothness, etc**

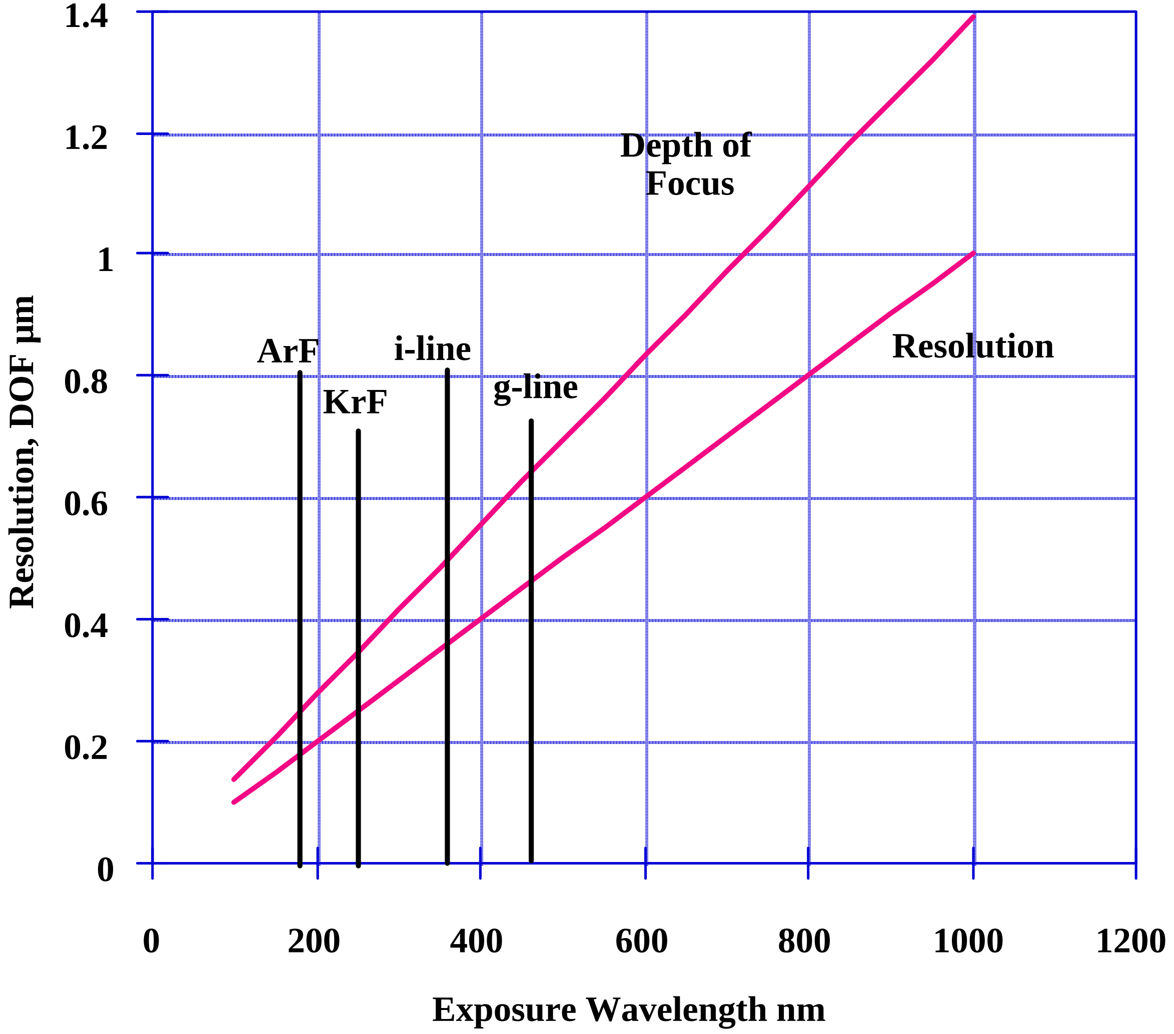
Example

A 248nm (KrF) exposure system with a NA = 0.6 would have a resolution of

- **R~ 0.3 μm (k1 = 0.75) and a**
- **DOF ~ ± 0.35 μm (k2 = 0.5)**

Resolution and DOF

$$\therefore R = k_1 \frac{\lambda}{NA} = 0.6 \frac{\lambda}{0.6} \quad \text{and} \quad \mathrm{DOF} = \pm \mathrm{k}_2 \frac{\lambda}{(NA)^2} = \pm 0.5 \frac{\lambda}{(0.6)^2}$$

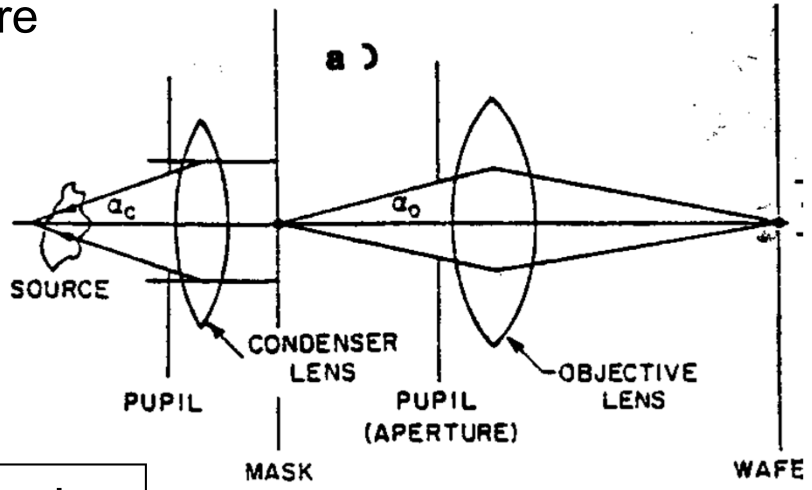


Numerical aperture NA

Condenser: Filters out the desired wavelength
Objective: Demagnifies and projects mask image

NA represents the collected light by the condenser or objective

NA for objective is also the geometrical ratio between focal length and aperture



(Wolf p. 463)

$$\boxed{\begin{aligned} NA_c &= n\sin\alpha_c \\ NA_o &= n\sin\alpha_o \end{aligned}}$$

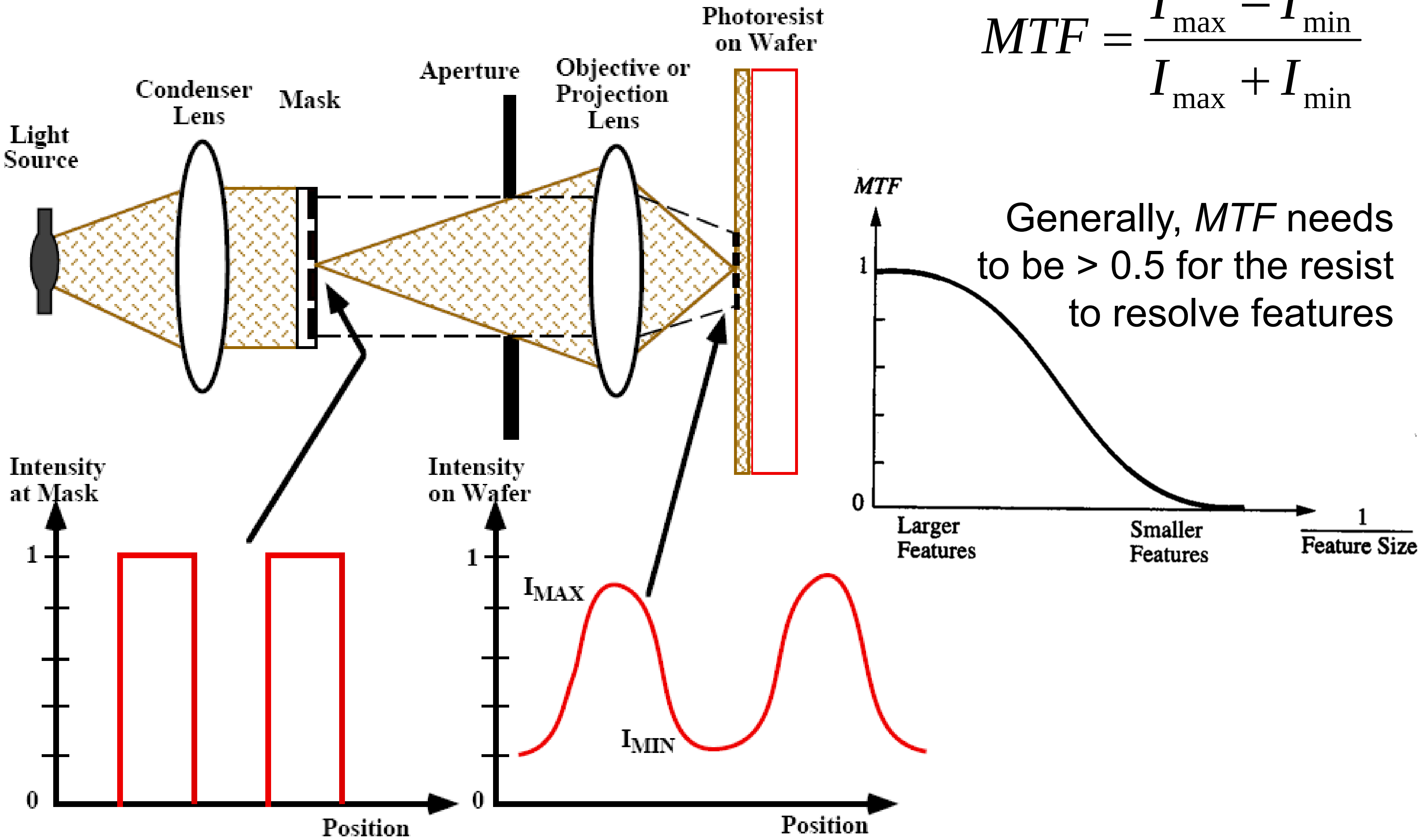
where *c* and *o* stand for the condenser and objective, respectively

n is index of refraction of the material between wafer and lens (usually air with *n*=1)

Modulation Transfer Function (MTF)

Function describing contrast as a function of size of features on mask

$$MTF = \frac{I_{\max} - I_{\min}}{I_{\max} + I_{\min}}$$



Generally, *MTF* needs to be > 0.5 for the resist to resolve features

(Plummer p 216)

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Mask Fabrication

Starting material for reticle manufacturing is ~80 nm thick film of *chromium* covered with resist and anti-reflective coating (ARC)

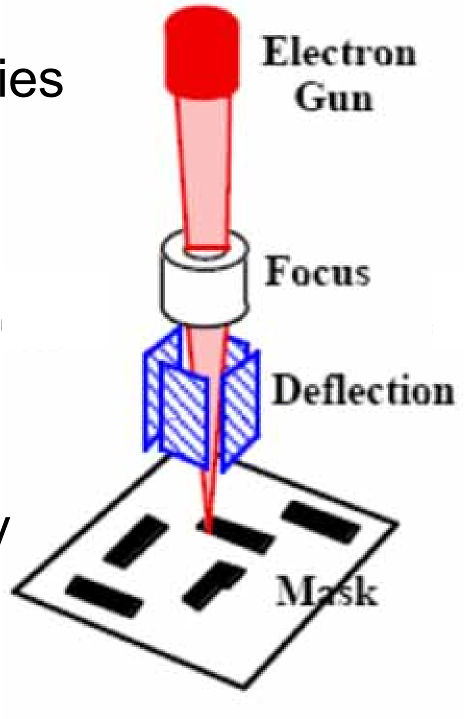
Chromium has very good adhesion and opaque properties

Substrate: quartz glass plate

Patterned by direct writing using e-beam or laser
Usually wet etching of Cr after exposure

4 or 5x magnification is normal for projection lithography

Pellicle used for dust protection of reticle



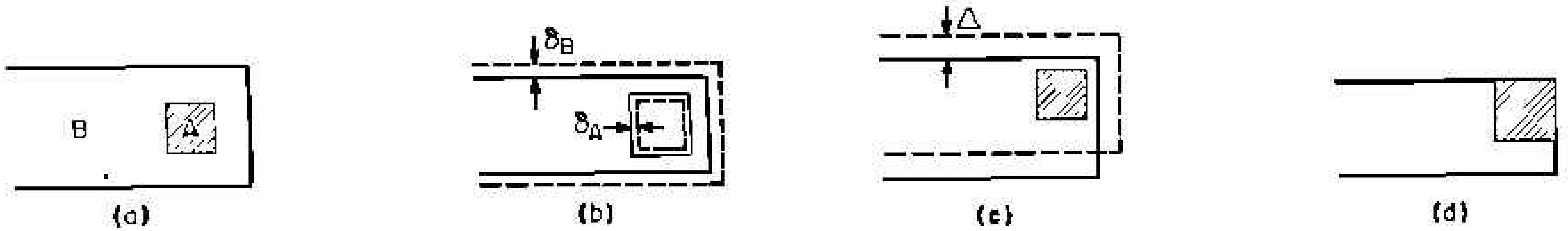
Mask Making

Nesting Tolerance

Design rules during mask layout depend on nesting tolerance:

$\delta_{A,B}$: uncertainty in feature size for mask level A and B
Δ : alignment (or overlay) error between A and B
n : number of alignment levels

Minimum separation between level A and B = $\sqrt{n\Delta^2+\delta_A^2+\delta_B^2}$
$\pm 3\sigma$ values usually given (99%)



(VLSI p. 472)

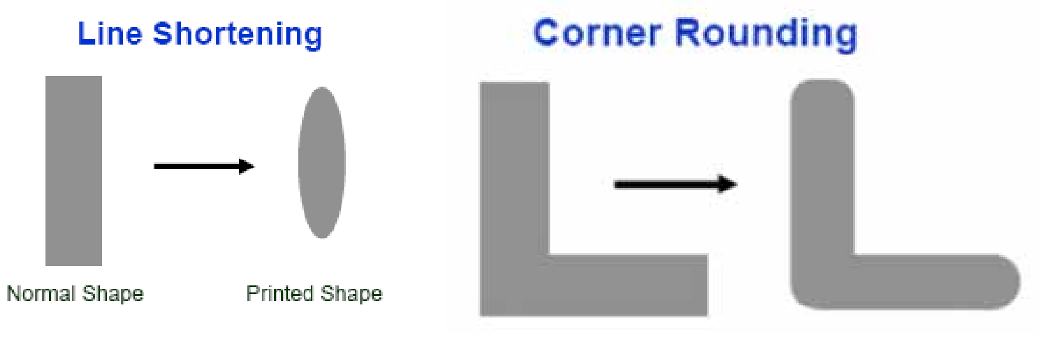
Total 3σ must consider overlay error, magnification error, lens distortion, stepper-to-stepper error, and reticle error (registration and linewidth)

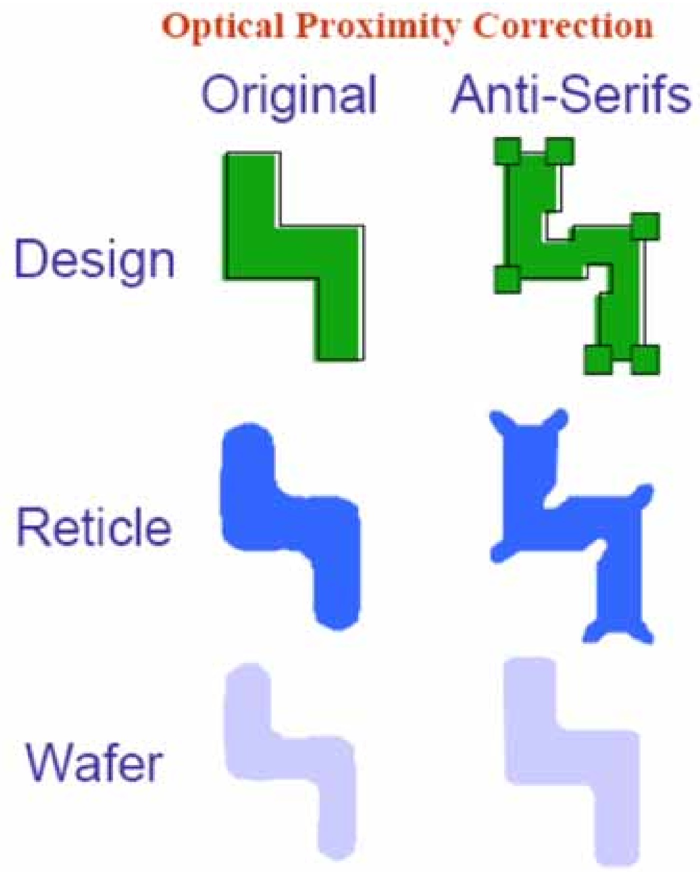
Inspection and linewidth measurement of resist patterns by CD SEM (CD = critical dimension)

Mask engineering

1. Optical Proximity Correction (OPC)

- High-frequency components of the diffracted light is lost because of finite apertures, circular lenses etc → Ends and bows of narrow lines are not ideal
- OPC: Clever mask engineering based on software algorithms can compensate some of this error:

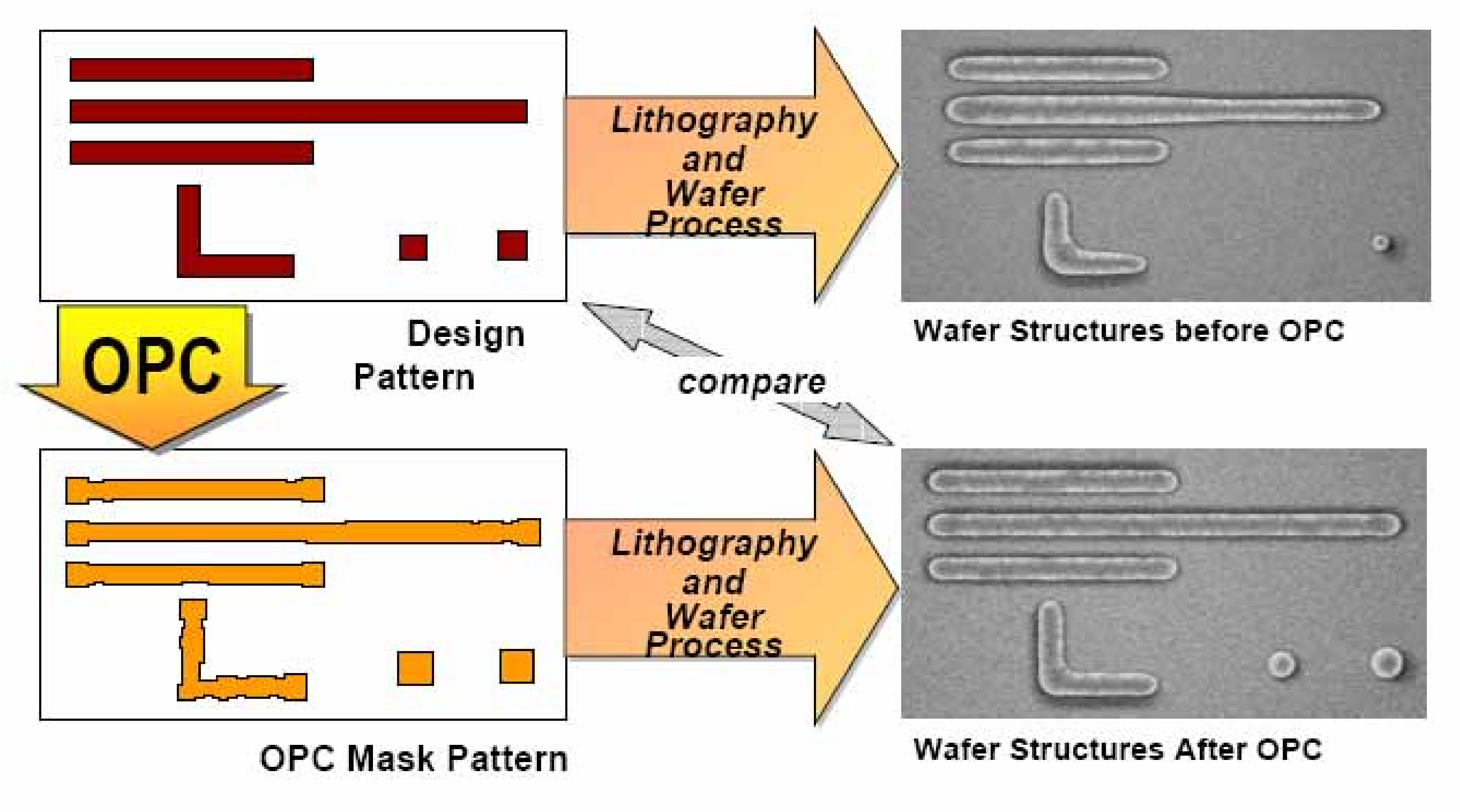




- Rule-based OPC
- Model-based OPC

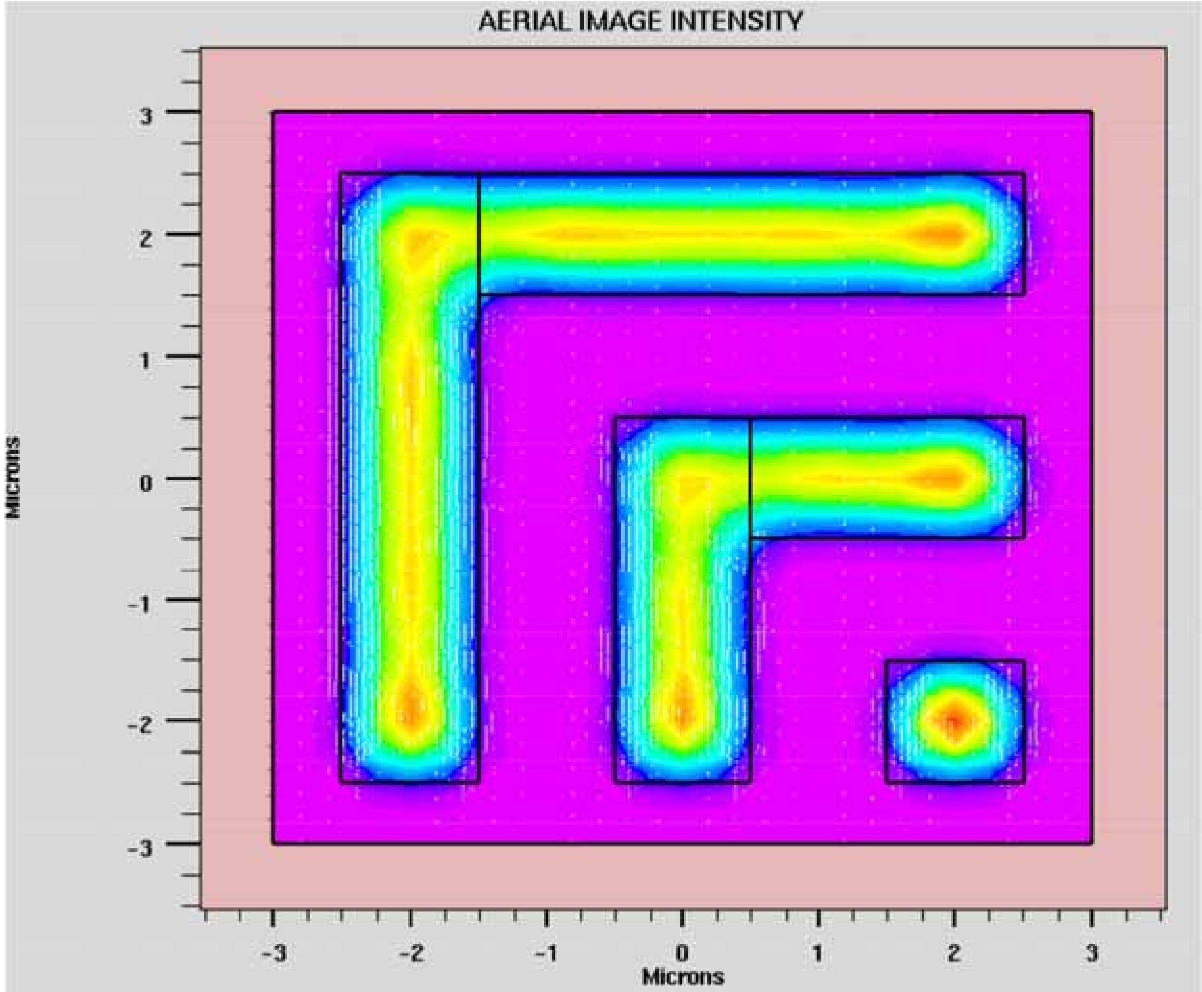
Mask engineering

1. Optical Proximity Correction (OPC) Examples



Mask engineering

1. Optical Proximity Correction (OPC) Examples

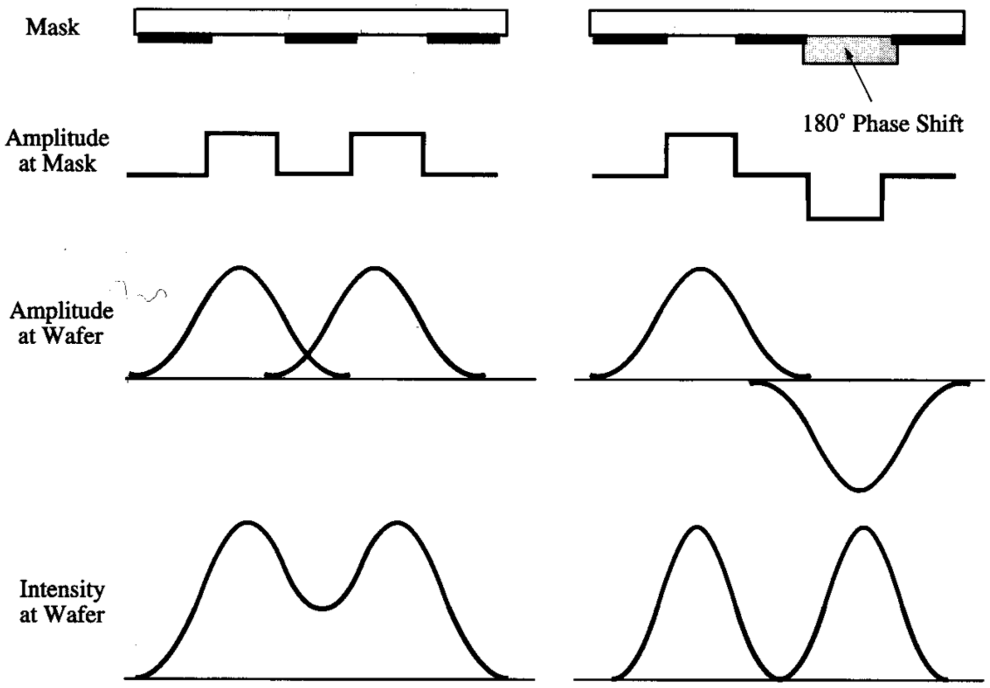


Mask engineering

2. Phase shifting masks (PSM)

Introducing material which shifts the light by 180° for adjacent mask patterns barely resolved → improved resolution

Intensity $\propto$ (Electrical amplitude)^2



(Plummer p. 233)

Concept Test 8.1

8.1 Moore’s law and the ITRS dictate that further scaling in the semiconductor industry is needed. The following options contribute to further scaling.

A. High resolution lithography only works in the front end of the line (FEOL) because the depth of focus is limited.

B. Chemical Mechanical Polishing (CMP) is a method to enhance lithography resolution.

C. Optical Proximity Correction (OPC) uses models to predict changes in device behavior due to diffraction.

D. Atomic Layer Deposition (ALD) enables the deposition of smooth films on the atomic scale, reducing some of the issues of lithography.

E. Selective epitaxy can be used in the BEOL to smooth surface topography and enhance resolution of lithography.

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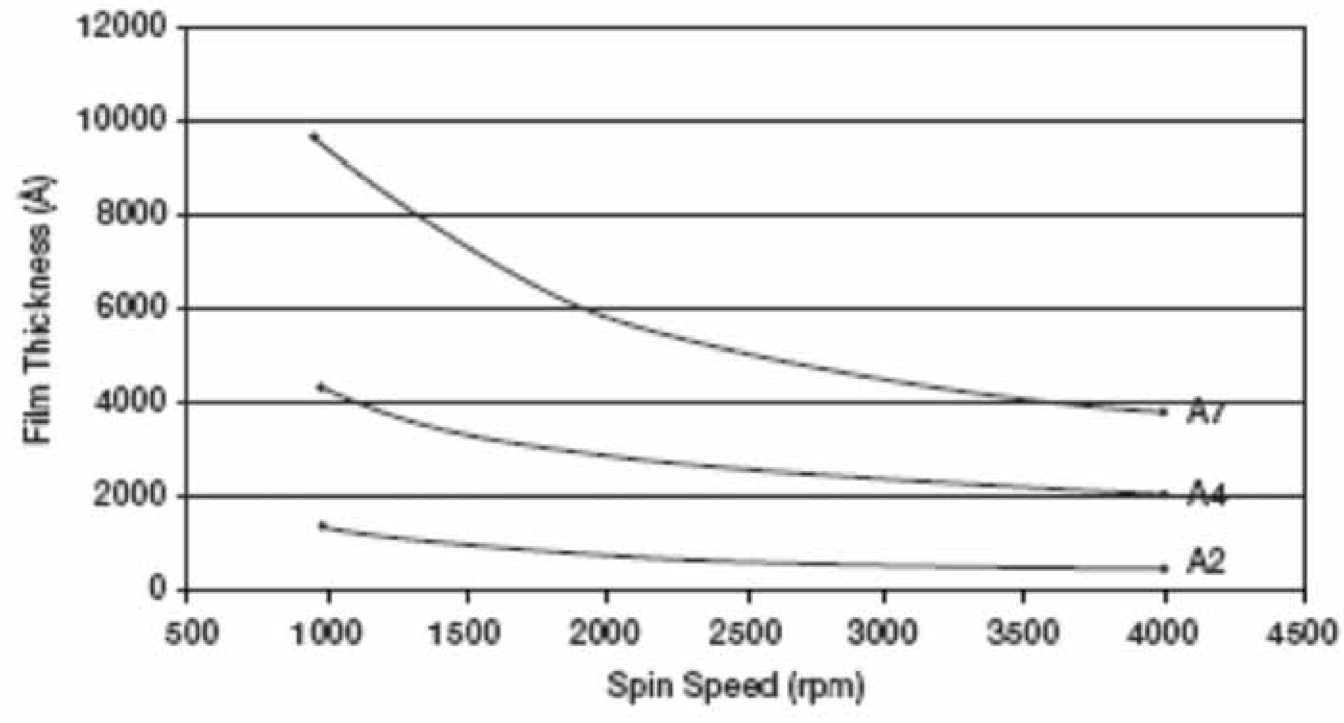
Resist Technology

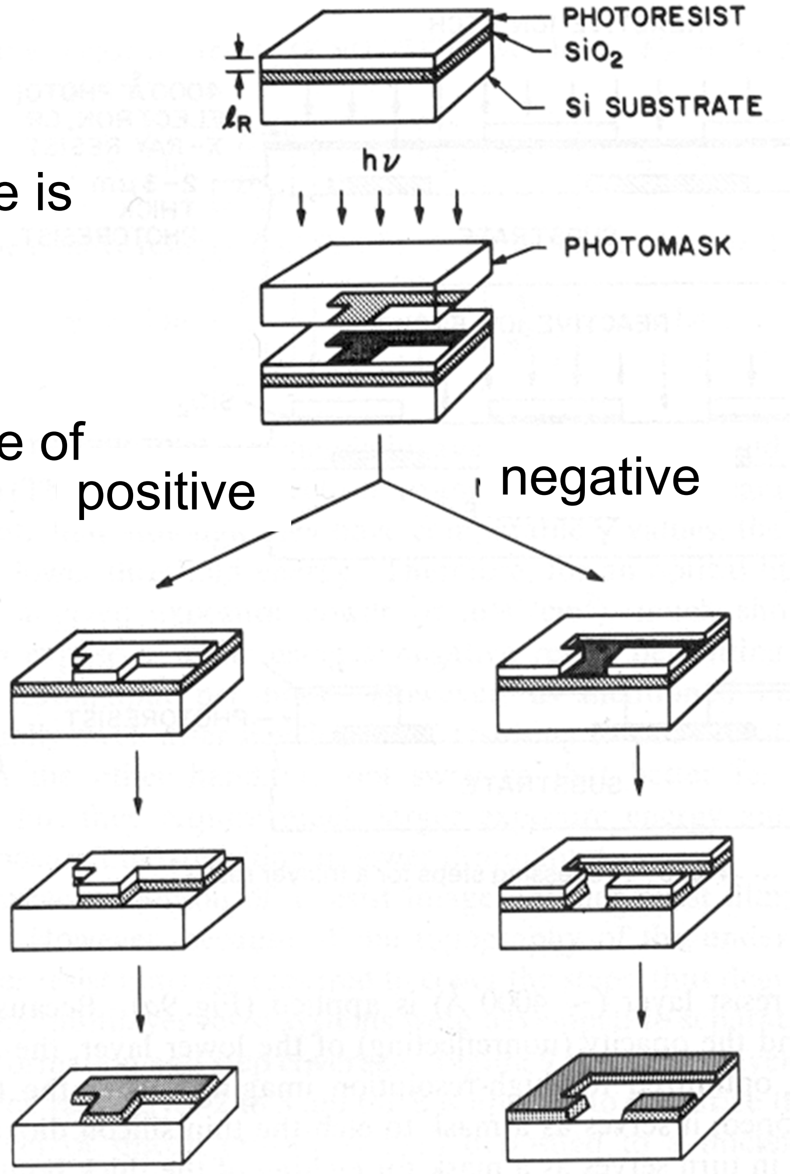
Spin Curves

- Plot of spin speed versus film thickness
- Actual results will vary: equipment, environment, process and application specific
- Additional resist dilution to obtain other film thicknesses



Source: MicroChem NanoPMMA data sheet

Resist Technology



Positive and negative resist:

Solubility in developer after light exposure is

- *increased* for positive resist
- *decreased* for negative resist

Negative resist uncommon today because of limited resolution

The resist is composed of:

- Resin, usually novolac
- Solvent
- Photoactive compound (PAC)

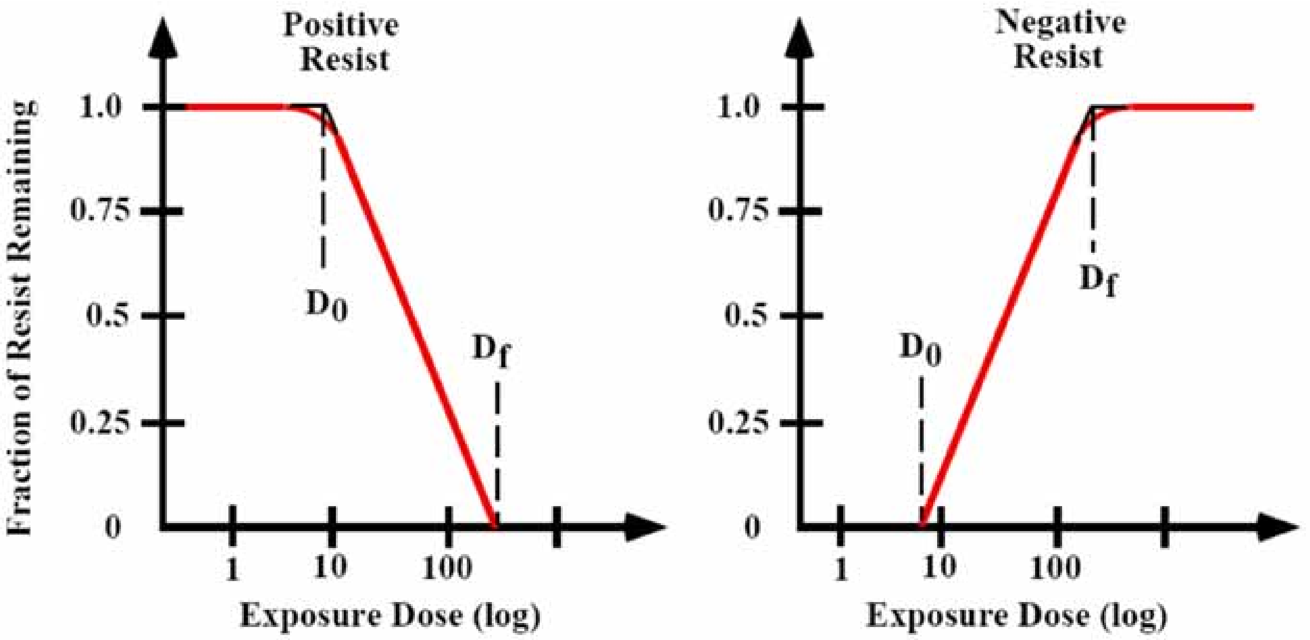
Contrast of Resist

Contrast γ is experimentally determined

- D_0: onset of exposure effect
- D_f: dose at which exposure is complete
- High γ → high resolution
- γ = F(process conditions)

$$\gamma = \frac{1}{\log_{10}\frac{D_f}{D_0}}$$

Chemical amplification steepens transition in DUV resists



DNQ (g-line, i-line): γ = 2-3, D_f = 100 mJcm^{-2}

Deep UV (DUV): γ = 5-10, D_f = 20-40 mJcm^{-2}

Critical Modulation Transfer Function (CMTF)

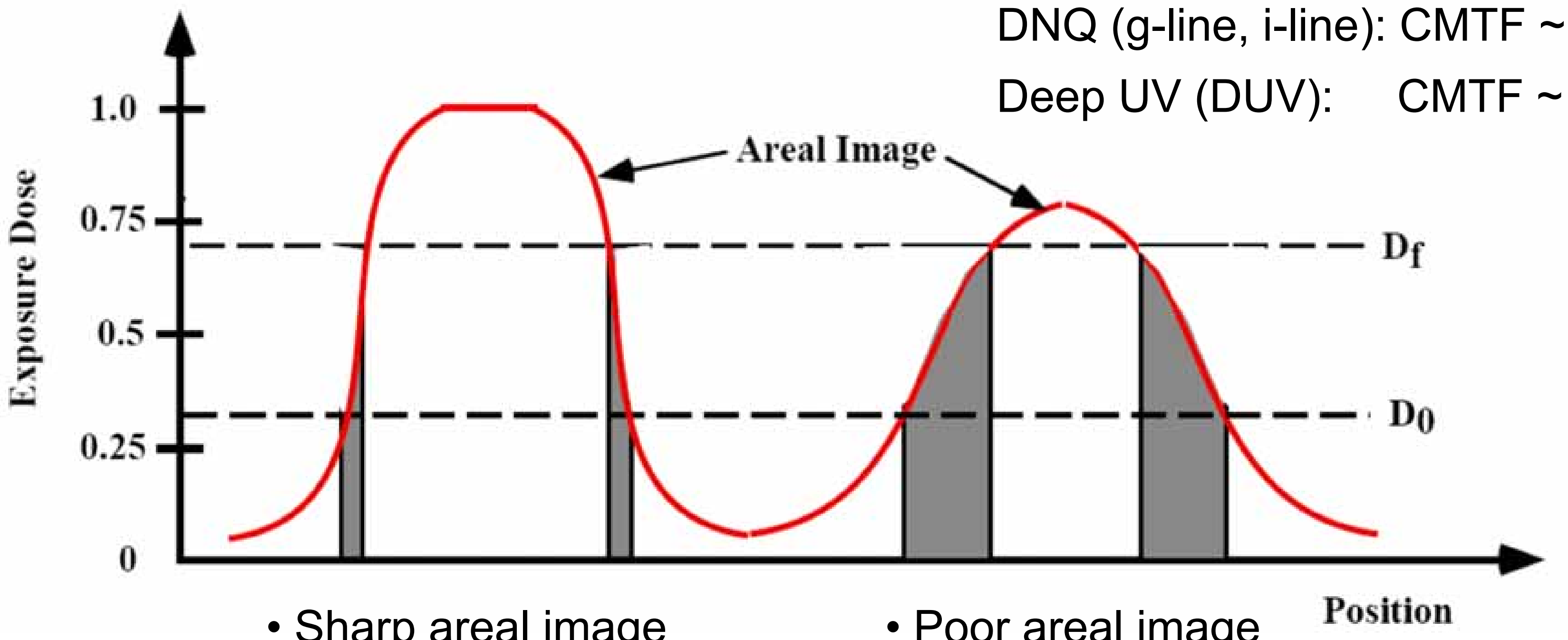
The aerial image and the resist contrast in combination, result in the quality of the latent image produced. (Gray area is “partially exposed” area which determines the resist edge sharpness.)

The CMTF for resists is defined as

$$CMTF_{resist} = \frac{D_f - D_0}{D_f + D_0} = \frac{10^{1/\gamma} - 1}{10^{1/\gamma} + 1}$$

DNQ (g-line, i-line): CMTF ~ 0.4

Deep UV (DUV): CMTF ~ 0.1-0.2



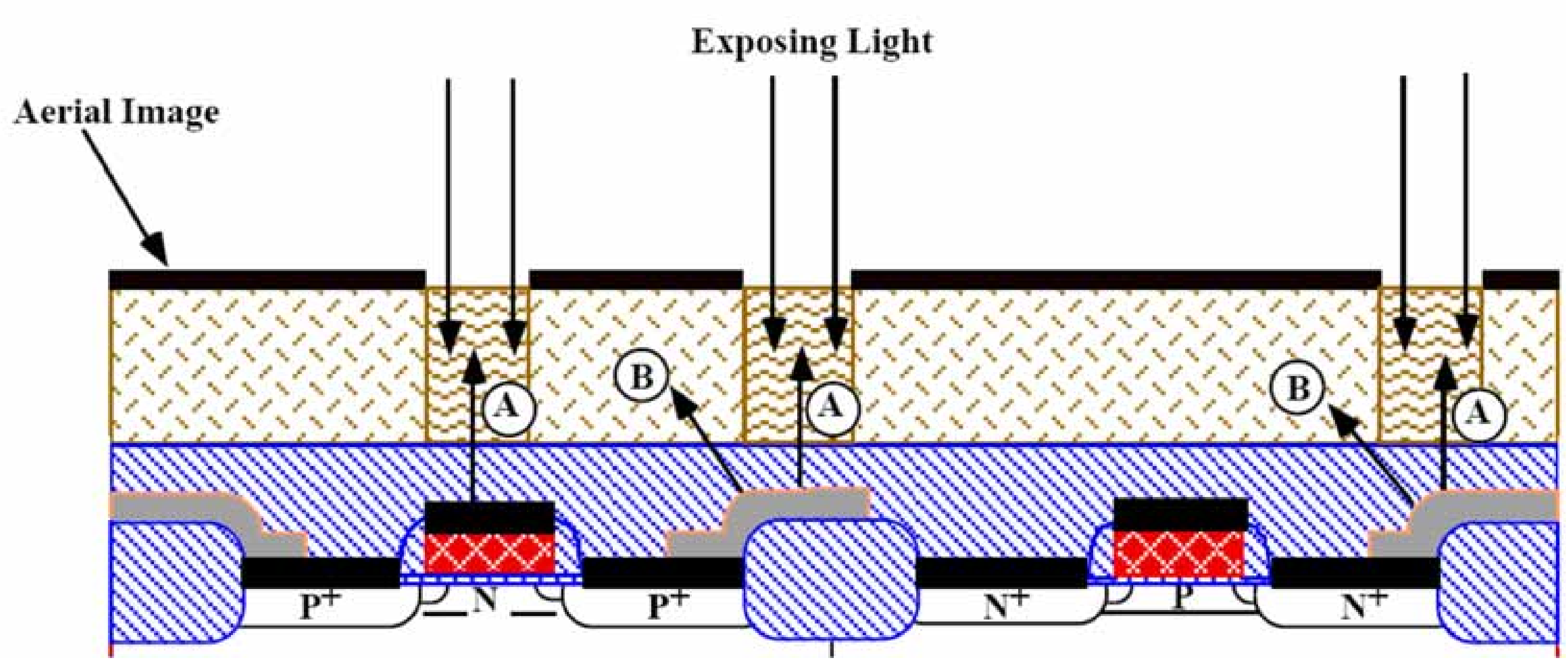
- Sharp areal image
- Steep resist profile

- Poor areal image
- Resulting gradual profile

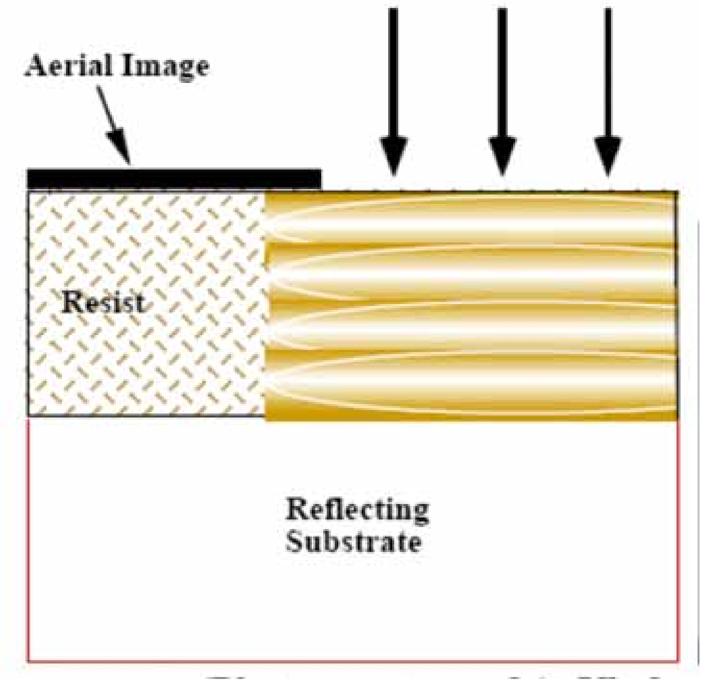
Effects of Standing Waves on Patterns

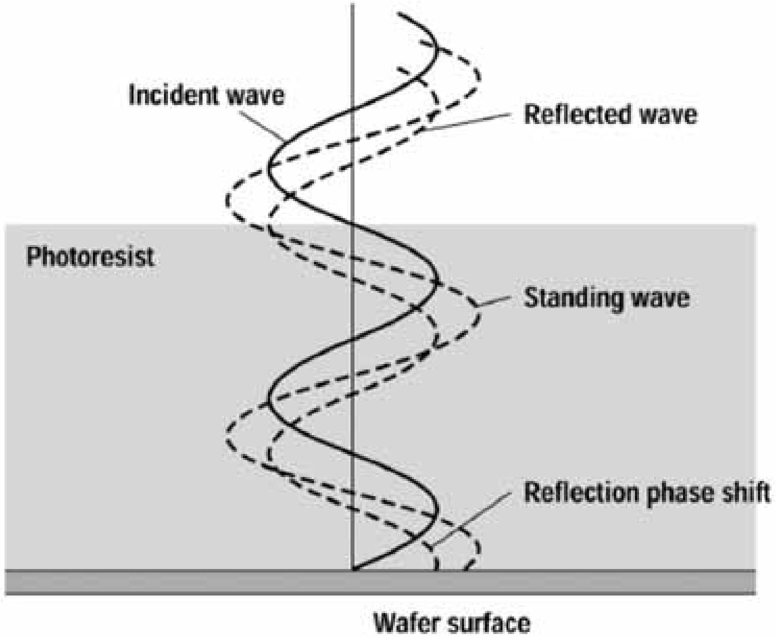
- Standing waves a problem, in particular when exposing on reflective layers such as metals

- Suppressed by antireflective coating (ARC) prior to resist spinning



Effects of Standing Waves on Patterns





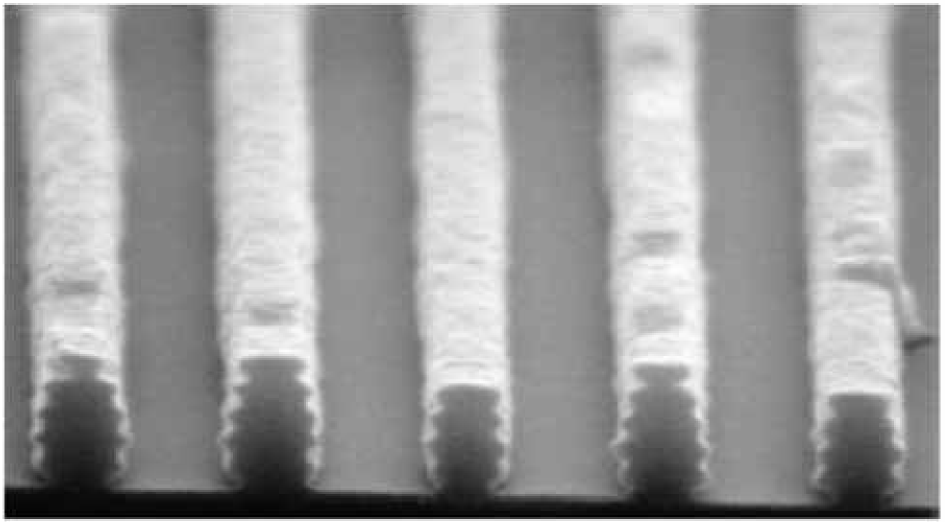
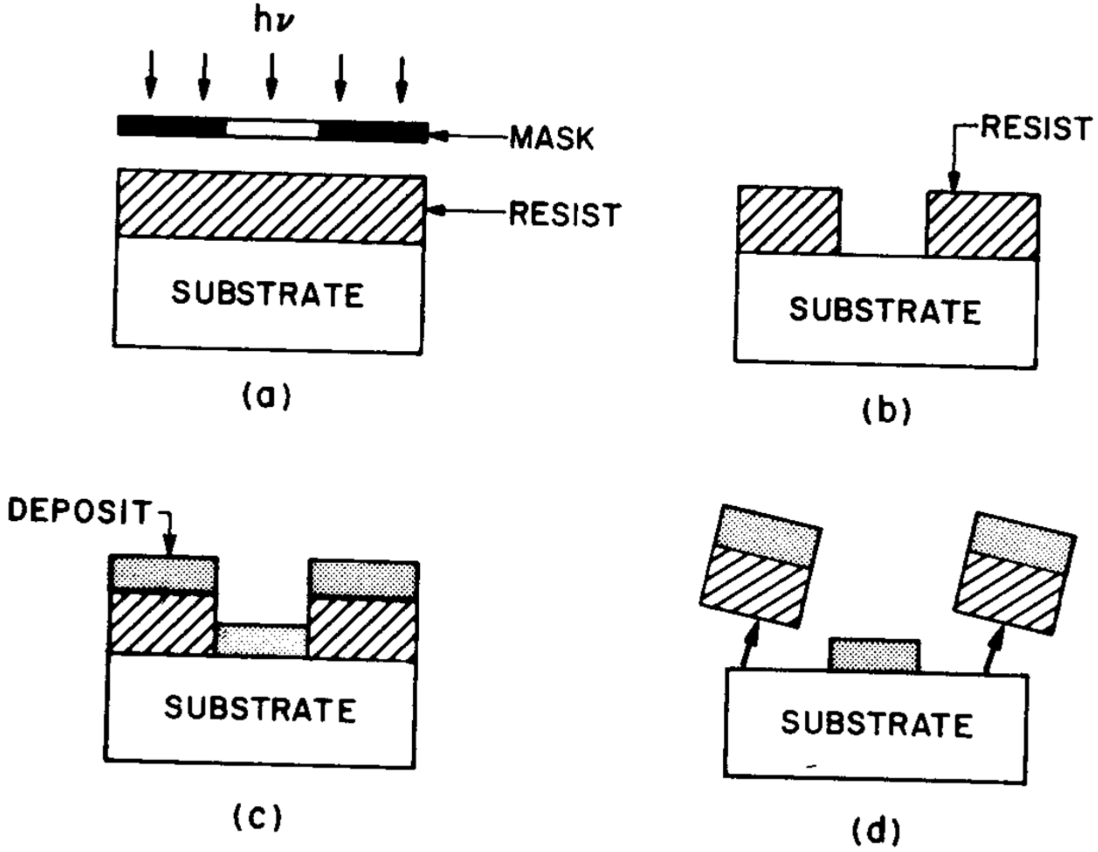


Photo courtesy of A. Vladar and P. Rissman, Hewlett Packard

Resist Process Integration

1. Lift-off

- Avoid etching of difficult materials
- Requires cold deposit process!
- Not suitable for CMOS production

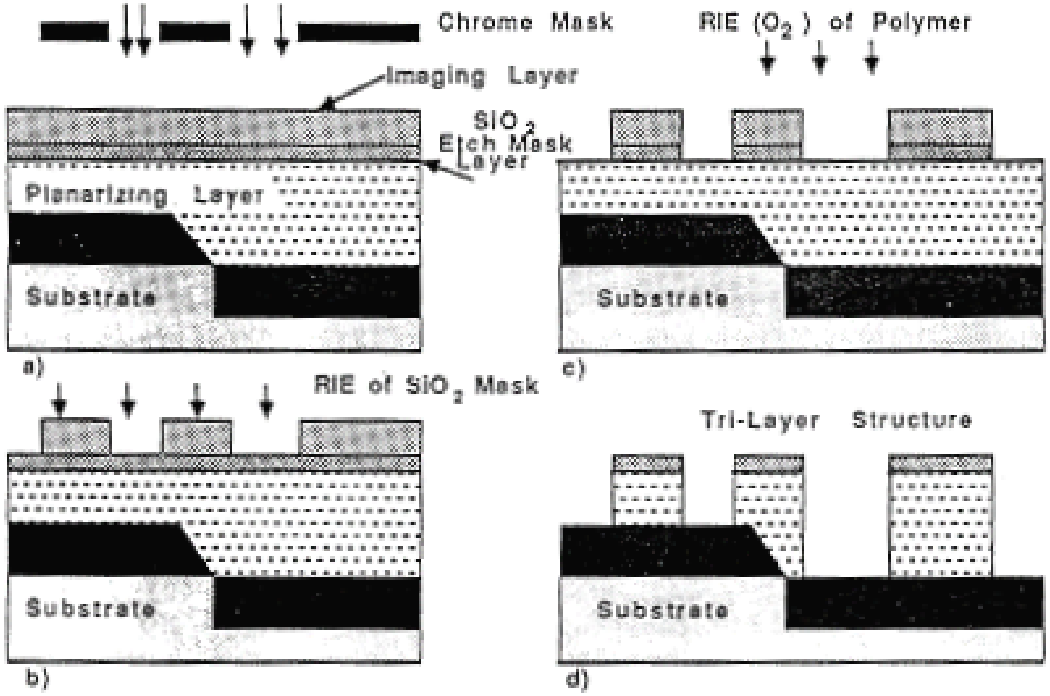


(Sze p. 441)

Resist Process Integration

2. Multilayer resist processing

- Under development for VLSI
- Example tri-layer resist:



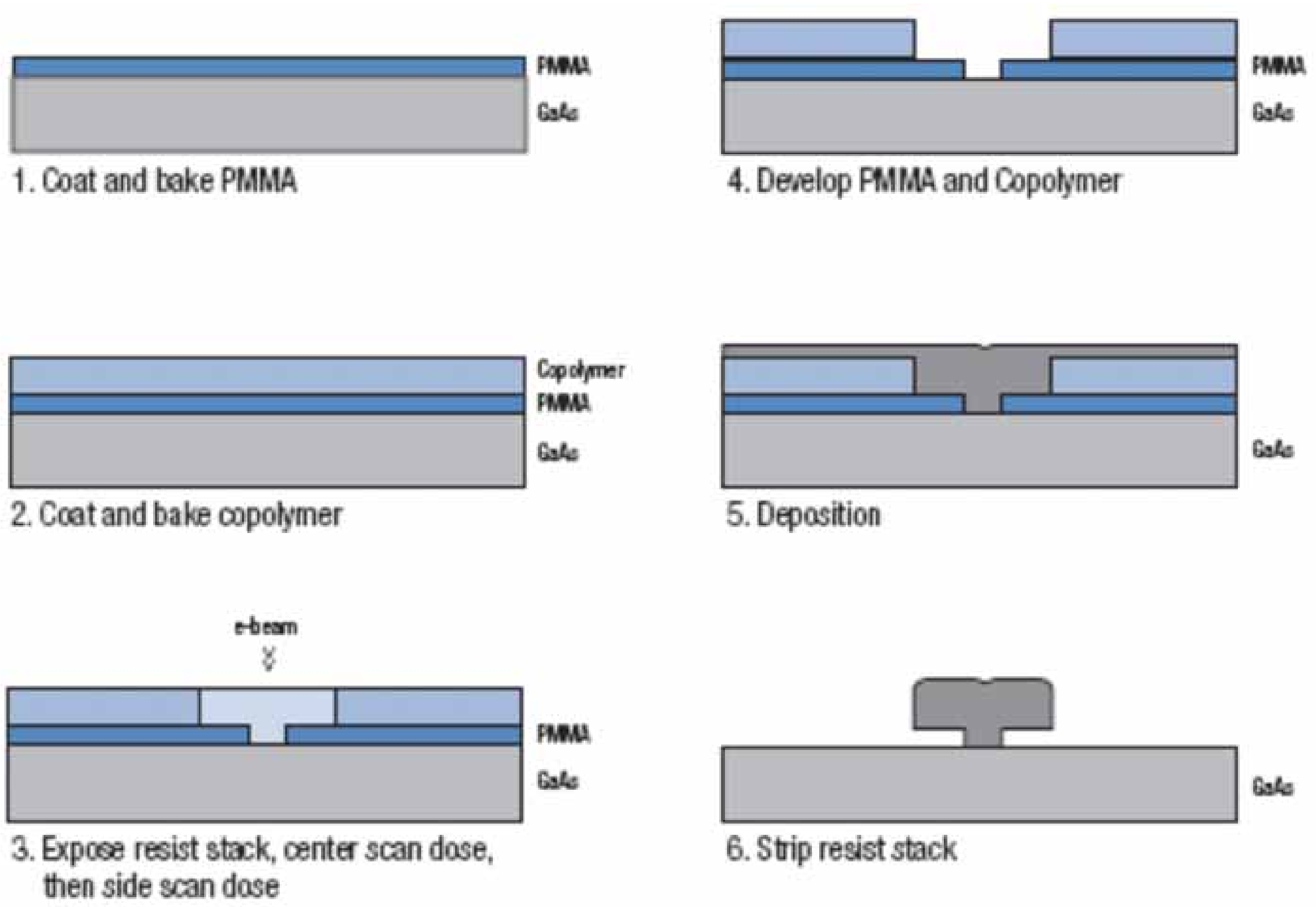
(Wolf p. 424)

- Patterning is made in upper layer. This is used as a contact mask for the lower layer
- RIE (O_2) of polymer in (c) can be replaced by flood exposure

Resist Process Integration

3. Bilayer Resist

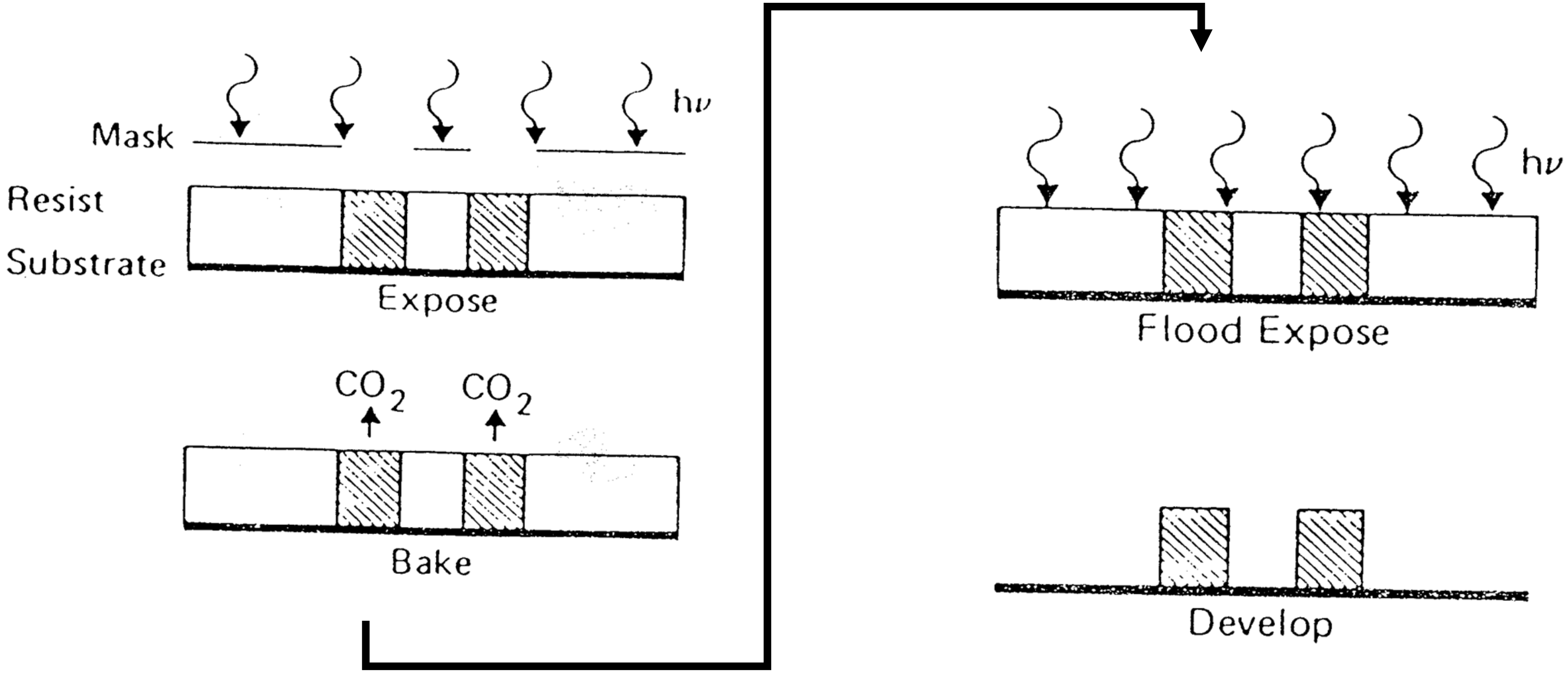
- Application: low-resistance gate electrodes for RF devices
- Mushroom or T-gates



Resist Process Integration

4. Image reversal of positive resist

- Exposed resist can be chemically altered by amine vapors to become non-dissolvable
- Flood exposure + development reverses image



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State of the art lithography

Current DUV generation (in ~2007):

DUV 193 nm
By combinations of phase-shift masks and off-axis illumination, 193 nm DUV can be extended beyond 100 nm, probably 70 nm!

25 nm!

DUV 157 nm
A solution for 50-70 nm but large absorption makes refractive systems extremely difficult to design. Further, no resist technology exists.

No!

Fraunhofer Diffraction: Improving Resolution

Resolution *R*

Practical resolution: $R = k_1 \frac{\lambda}{NA}$ where $0.6 < k_1 < 0.8$

Improve resolution by reducing λ or increasing NA:

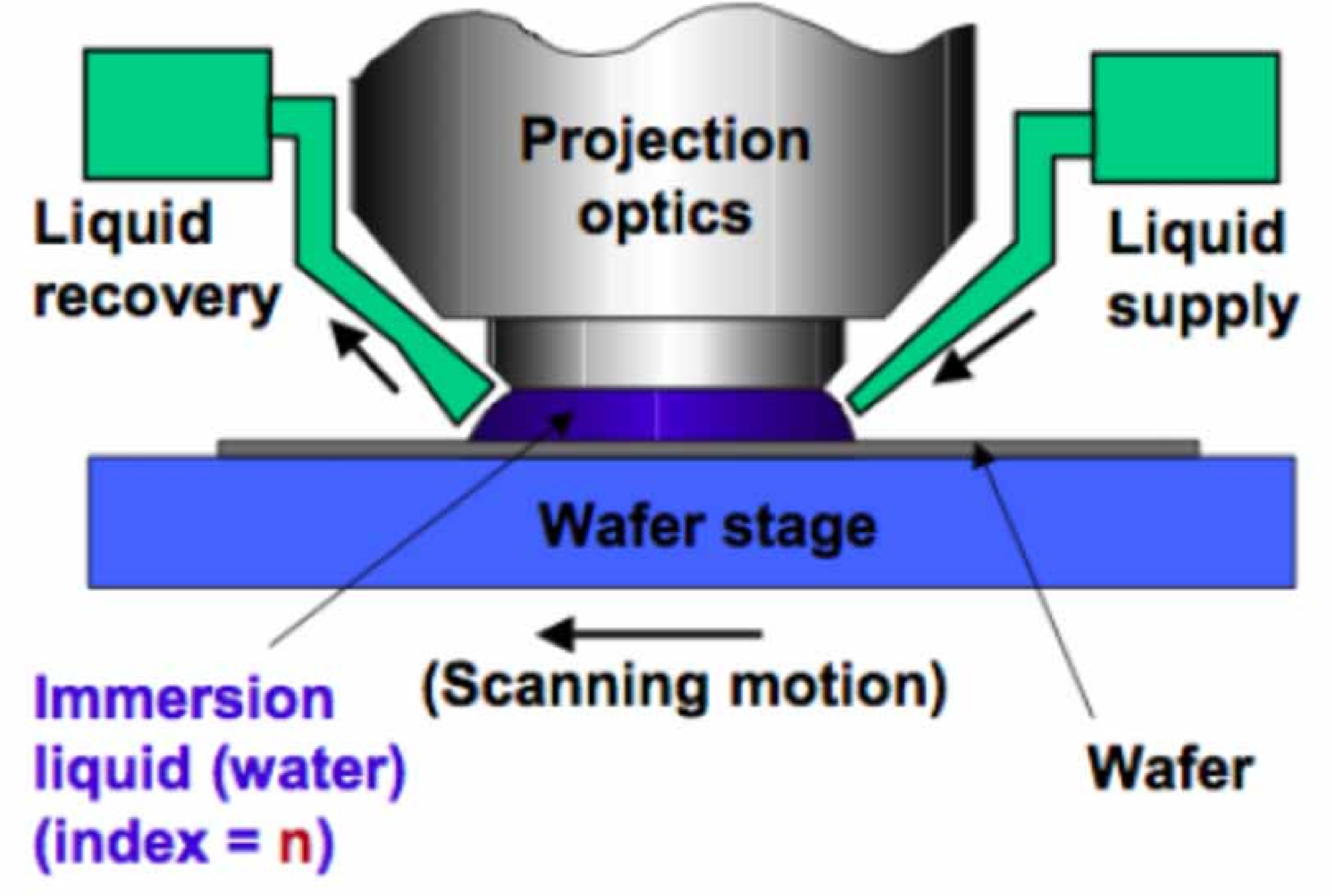
Higher NA lenses also decrease the depth of focus

$$NA = n \sin\alpha$$

***n* is index of refraction of the material between wafer and lens**

Can we replace air ($n = 1$)?

State-of-the-Art: Immersion Lithography



State-of-the-Art: Immersion Lithography

- Liquid immersion lithography:

- AMD, IBM: ***wet*** 193 nm for 65 nm
- Intel: ***dry*** 193 nm down to 45 nm, switching directly to EUV sources

- IBM demonstrated 22 nm with ***dry*** 193 nm

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Next Generation Lithography (NGL): 2012 and beyond

1. Extreme UV lithography (EUV)
2. E-beam projection lithography (EPL)
3. Ion projection lithography
4. X-ray lithography
5. Nano Imprint Lithography (NIL)

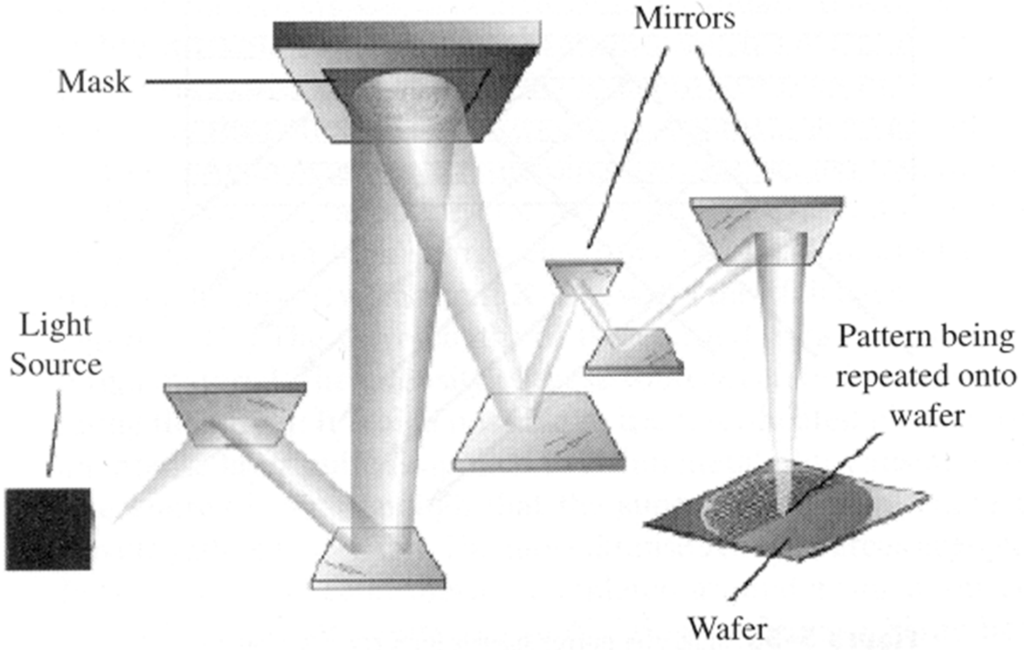
No consensus exists about the winner!
It is very likely that it will be either EUV or EPL.
Largest problem for all technologies is mask design!

Possibly, mix-and-match strategies will be used (different litho technologies in the same process)

In sharp contrast to 20 years common belief, it now appears that lithography will not act as "the show-stopper" for Moore's law!

1. Extreme UV lithography (EUV)

- Light source with λ = 13 nm
- Purely reflecting system including mask
- Each mirror consists of multilayers of Mo and Si and can both be used for reduction
- (usually 4x) and as mask
- Strong support from US and European manufactures
- ASML predicts one system will cost 30 MUSD



(Plummer p278)

2. E-beam projection lithography (EPL)

Electrons with λ < 0.1 nm. (Almost) no diffraction limit!

EPL is a variation of e-beam lithography (EBL) which traditionally is used for *direct writing* (i.e. mask-less): Reticles, prototype chips, research etc

Problem with EBL Throughput typically 50x lower than optical lithography. Beam size (shape) and scan schemes important:

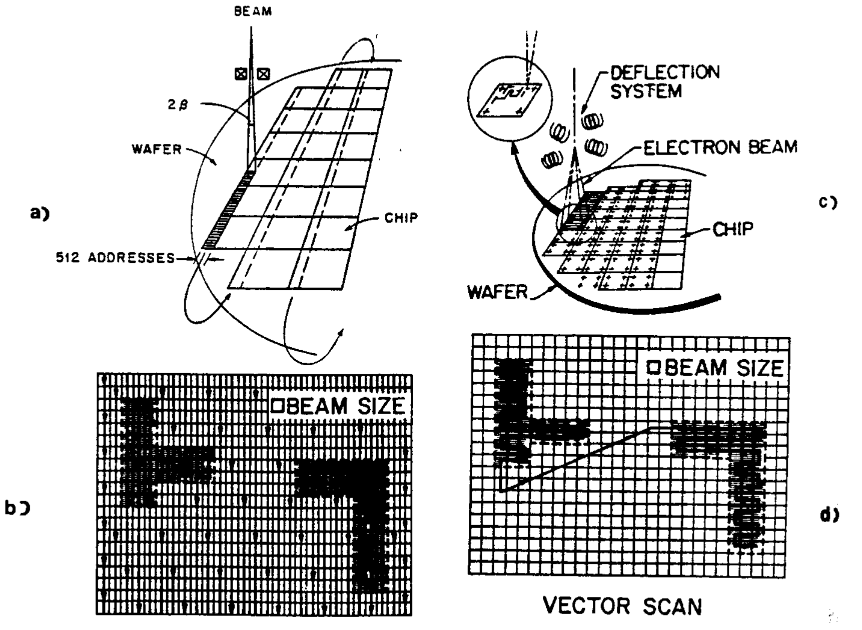


Fig. 5 (a) and (b) Raster scan exposure scheme. (c) and (d) Vector scan exposure scheme.

2. E-beam projection lithography (EPL)

SCALPEL (scattering with angular limitation e-beam lithography)

Invented by Bell 1989

Membrane mask design in SCALPEL based on the various amount of scattering experienced by incoming electrons: Widely scattered electrons do not expose resist

- Simpler mask than EUV
- 4:1 system
- Large DOF
- DUV resists
- 100 keV beam

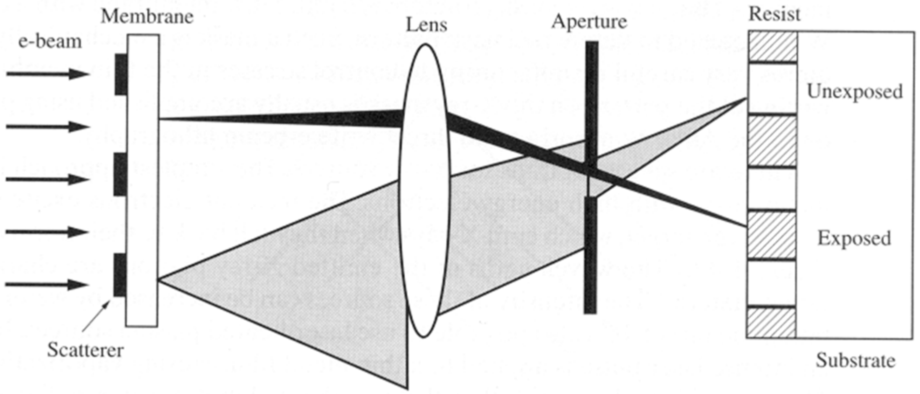


Figure 5–53 SCALPEL® e-beam projection lithography system. The resist is "exposed" in areas where the e-beam has not been widely scattered (mask areas where there is no scatterer). When the e-beam is widely scattered, the intensity reaching the resist is insufficient for exposure.

(Plummer p. 275)

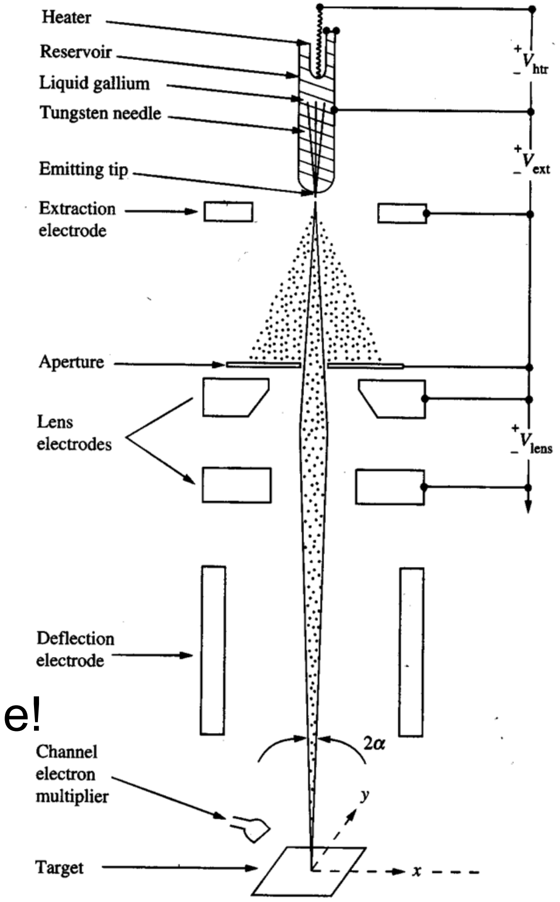
3. Ion projection lithography

Ions scatter much less than e- →
higher resolution and throughput than e-beam lithography

Problems:

- Ion beam source
- Beam forming
- Mask

Example on lithography system using Ga ions without mask:



(Chang p 322)

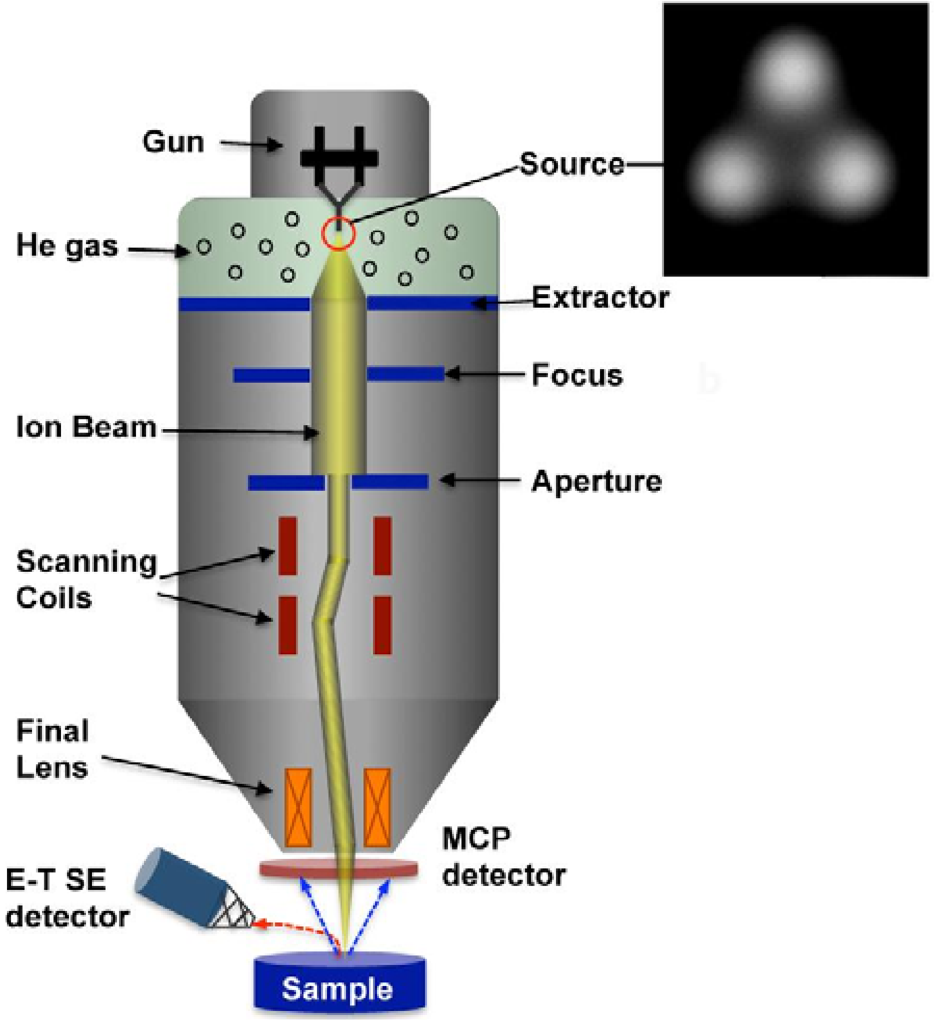
Reticle design based on a 0.5 μm thick stencil mask. Fragile!
Ion beam of protons or H_2.

A relatively immature technology compared to EPL.

3. Ion projection lithography (Example)

Helium Ion Microscope: A new Nano-Fabrication-Tool

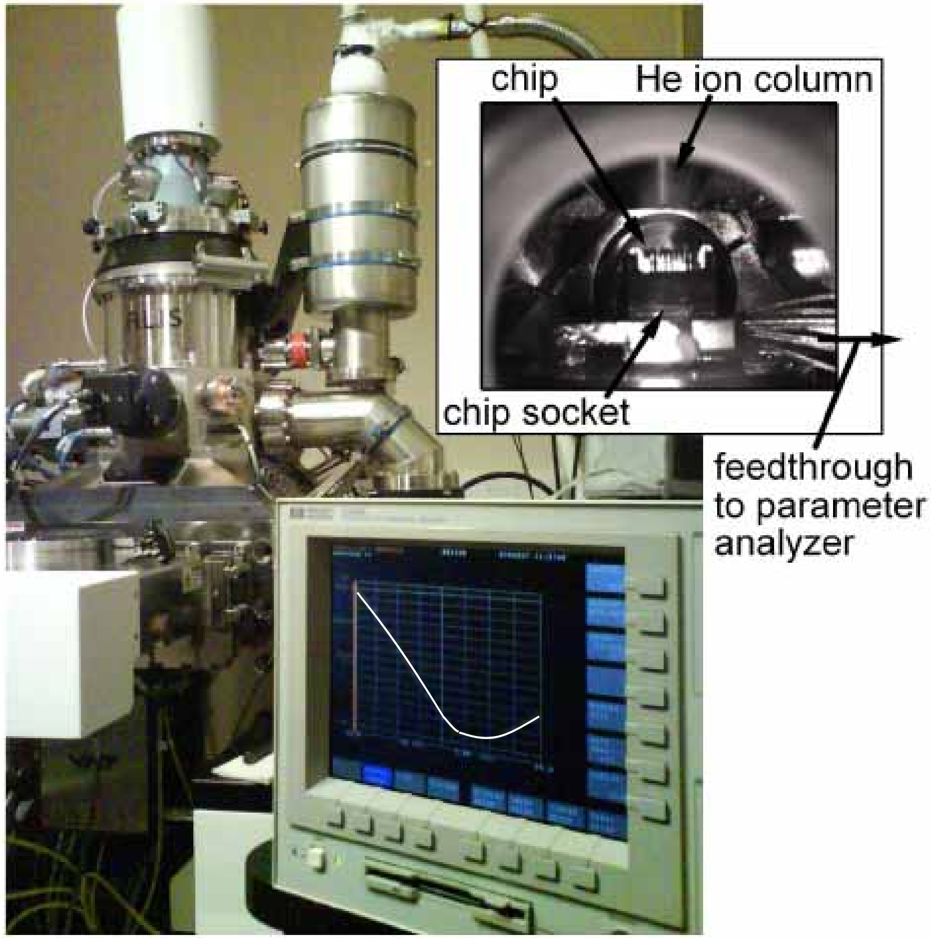
Zeiss Orion He Ion Microscope



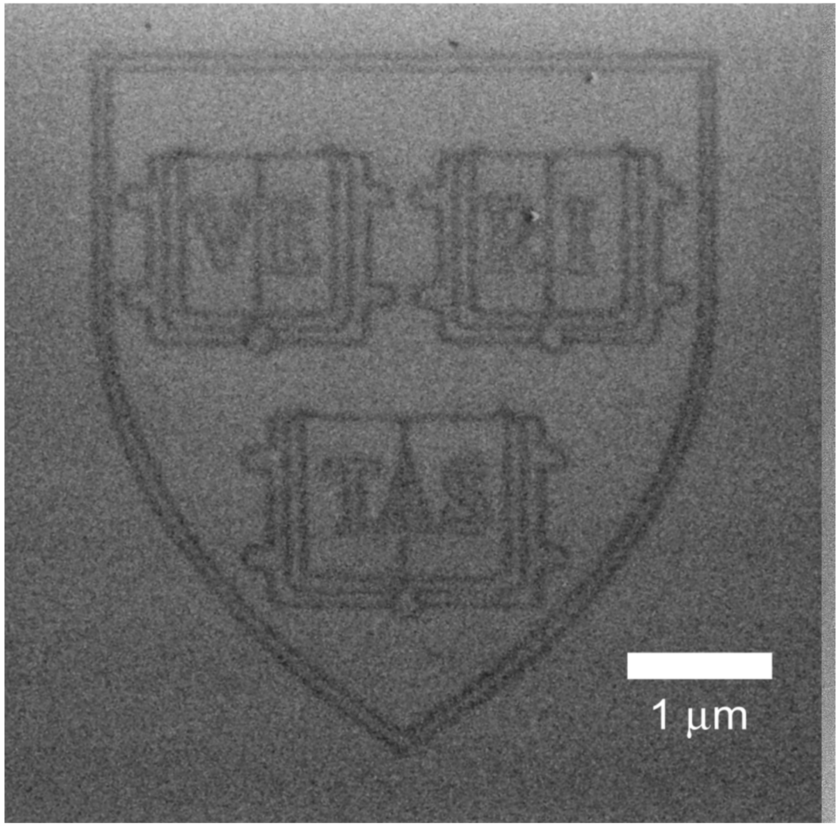
Spot size: d = 0.25nm @ 30 keV

3. Ion projection lithography (Example)

Helium Ion Microscope: A new Nano-Fabrication-Tool



Lemme et al., *ACS Nano,* 2009.



Harvard Logo in Graphene

Sub 10nm resolution

4. X-ray lithography

X-rays with λ ~1 nm

X-ray source usually a synchrotron connected to several X-ray steppers in litho area

Focusing x-rays very difficult →
Proximity printing combined with step- and repeat action

1:1 system
Very high resolution (no diffraction) and throughput

Mask design requires absorbent and
transparent regions.

This has turned out extremely
difficult for x-ray lithography

Despite huge efforts, X-ray lithography
now seems abandoned as NGL

(Chang p 314)

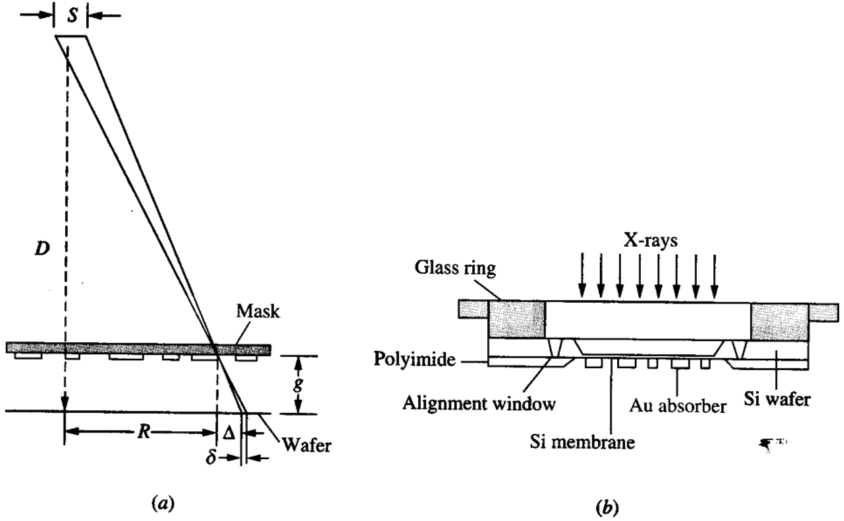
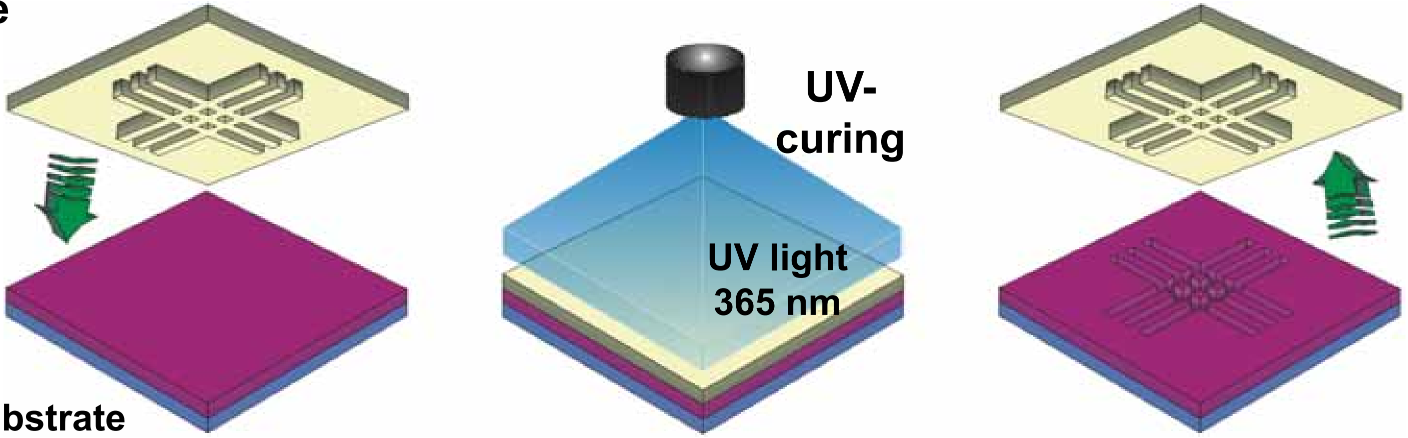


FIGURE 29
X-ray shadowing errors and x-ray mask structure. (*a*) X-ray proximity printing consideration. (*b*) X-ray mask structure example. (*After Fleming et al., Ref. 54.*)

5. Nanoimprint Lithography (NIL)

Here: UV-NIL, also: thermal NIL

Process



Etching of residual resist and structuring by RIE

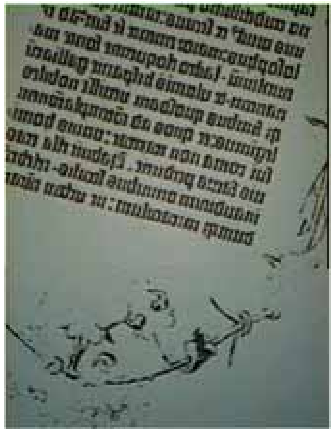
- \+ Low cost of ownership (COO)
- \+ Precision
- \+ Random patterns
- \- Reproducibility
- \- Tilting
- \- Contamination (contact with resist)

5. Nanoimprint Lithography

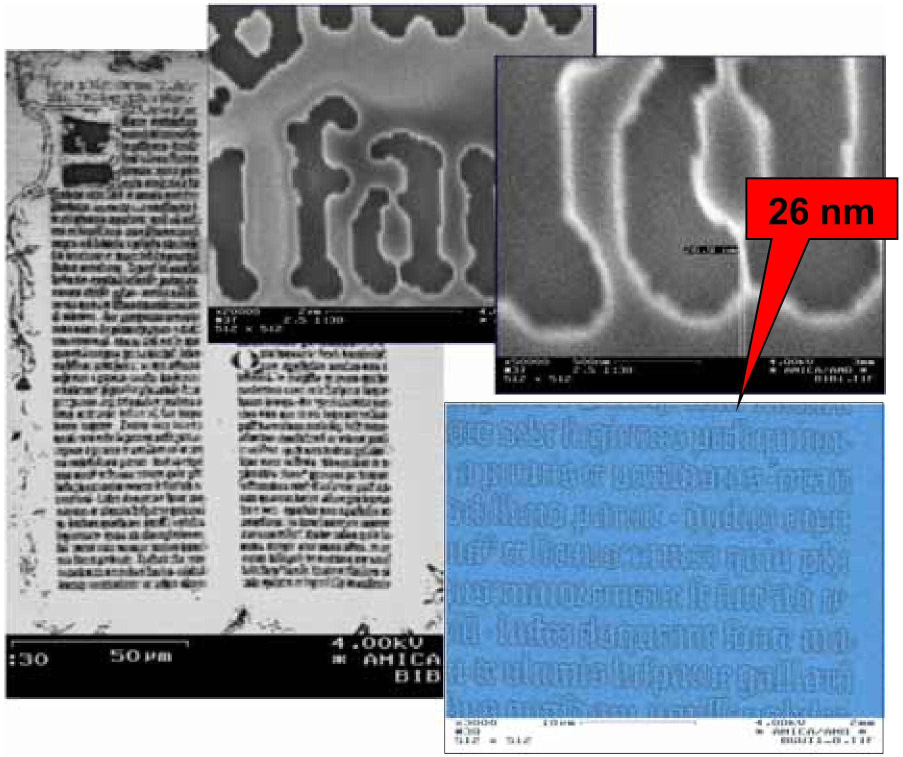
Example 1:

J. Gutenberg
1400-1468

1452: Printing of first page of the Bible („Gutenberg Bible“)



SiO_2
Template



550 years later in 2002:

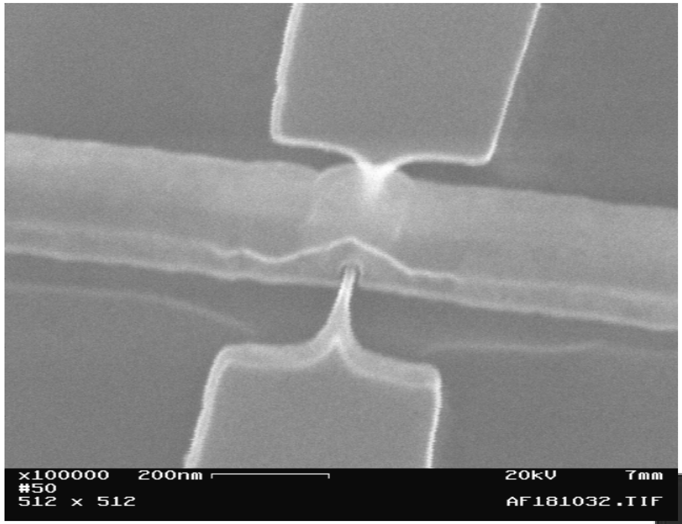
Gutenberg Bible page, printed and etched into silicon, minimim features ~25 nm.

Deutsches Museum, München, SEM images

5. Nanoimprint Lithography

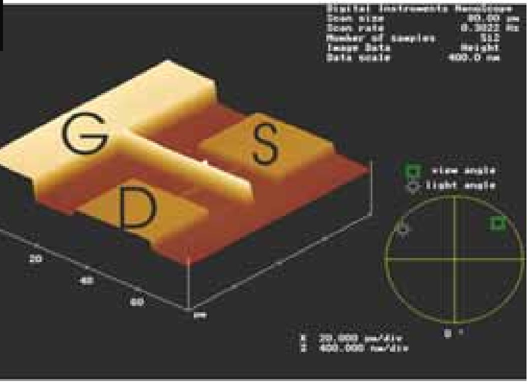
Example 2: Demonstration of UV-NIL in a MOSFET

Triple-Gate Transistor made using NIL

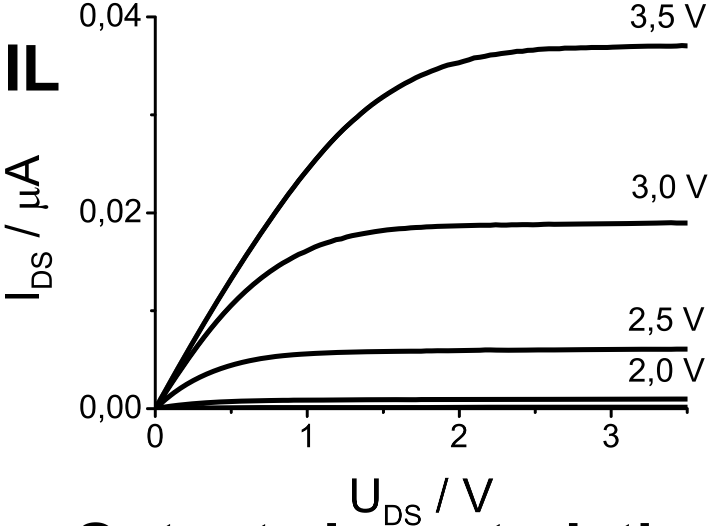


SEM image

- **Smallest features: <20nm**
- **Alignment: <20nm**



AFM image



Output characteristics

Fuchs et al., J. Vac. Sci. Technol. B, 24(6), 2006