Microcontrollers

-Definition, Basics and Trends

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Agenda

- Definition of a Microcontroller
- Blockdiagram of a generic MCU and Core
- Bus system
- Architecture
  - Cisc
  - Risc
- Production Technology
- ST Microcontrollers
  - How we think when we design a MCU
- Future
- Q & A

After the session you should have learnt..

- Know the difference between a MCU and a MPU and a CPU.
- Differences between a 8 bit and 32 bit MCU.
- Differences between Risc and Cisc architecture
- Differences between Harvard and Von Neuman Architecture
- Temporary production technologies

Definition of a Microcontroller

Definition of a Microcontroller

- What is the Definition of a Microcontroller?

- There is no absolut definition...

A **microcontroller** (sometimes abbreviated **µC**, **uC** or **MCU**) is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals. Program memory in the form of NOR flash or OTP ROM is also often included on chip, as well as a typically small amount of RAM. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications.

....from Wikipedia

Architecture

Cisc and Risc

Cisc vs Risc

CISC	RISC
Emphasis on hardware	Emphasis on software
Includes multi-clock complex instructions	Single-clock, reduced instruction only
Memory-to-memory: "LOAD" and "STORE" incorporated in instructions	Register to register: "LOAD" and "STORE" are independent instructions
Small code sizes, high cycles per second	Low cycles per second, large code sizes
Transistors used for storing complex instructions	Spends more transistors on memory registers

Example: Multiply (MULT) , considered as a complex instruction

Cisc:

MULT 2:3, 5:2

Risc:

LOAD A, 2:3
LOAD B, 5:2
PROD A, B
STORE 2:3, A

Block diagram and the Core

Essential block diagram of a MCU

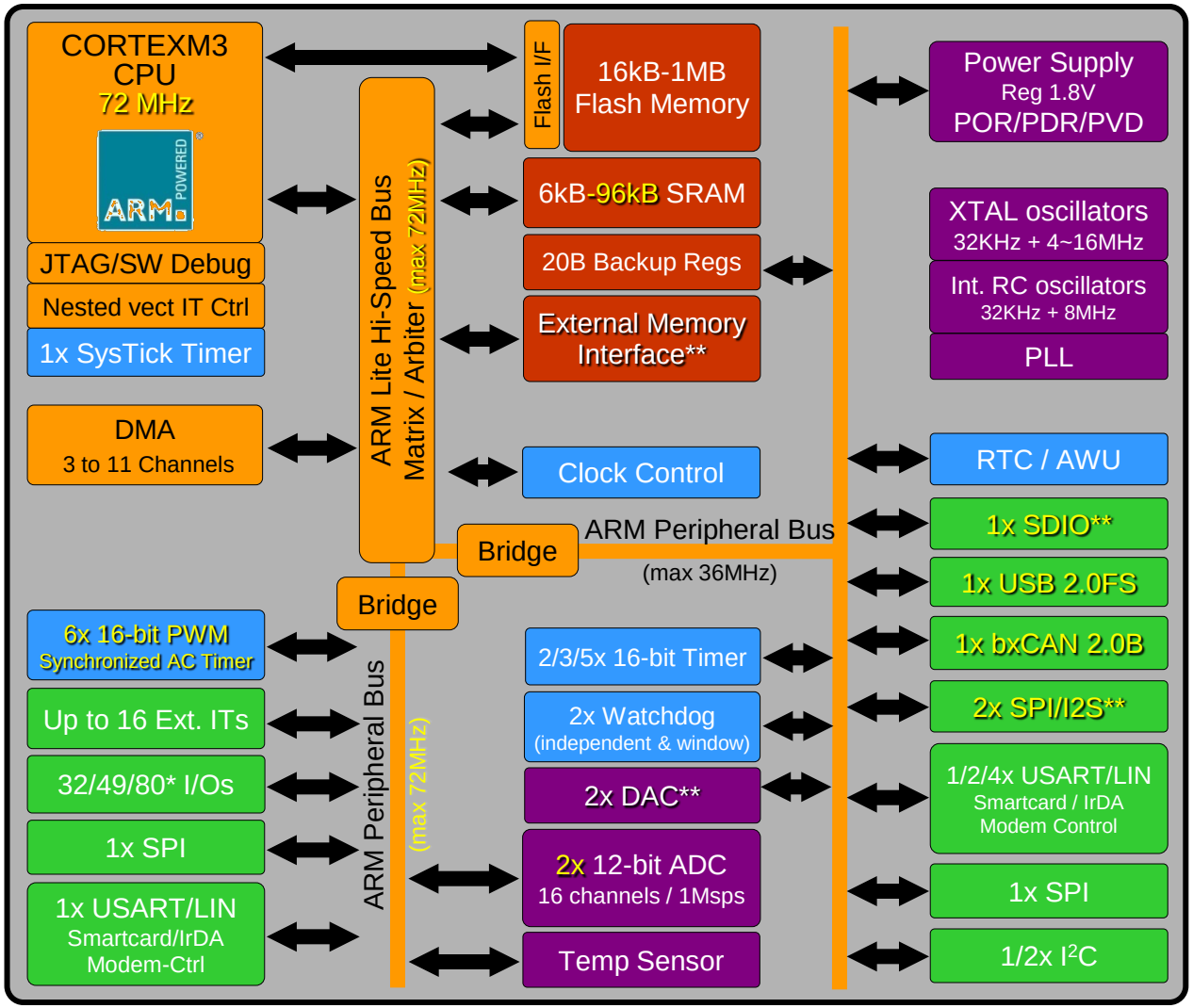
ROM (FLASH)

RAM

CPU

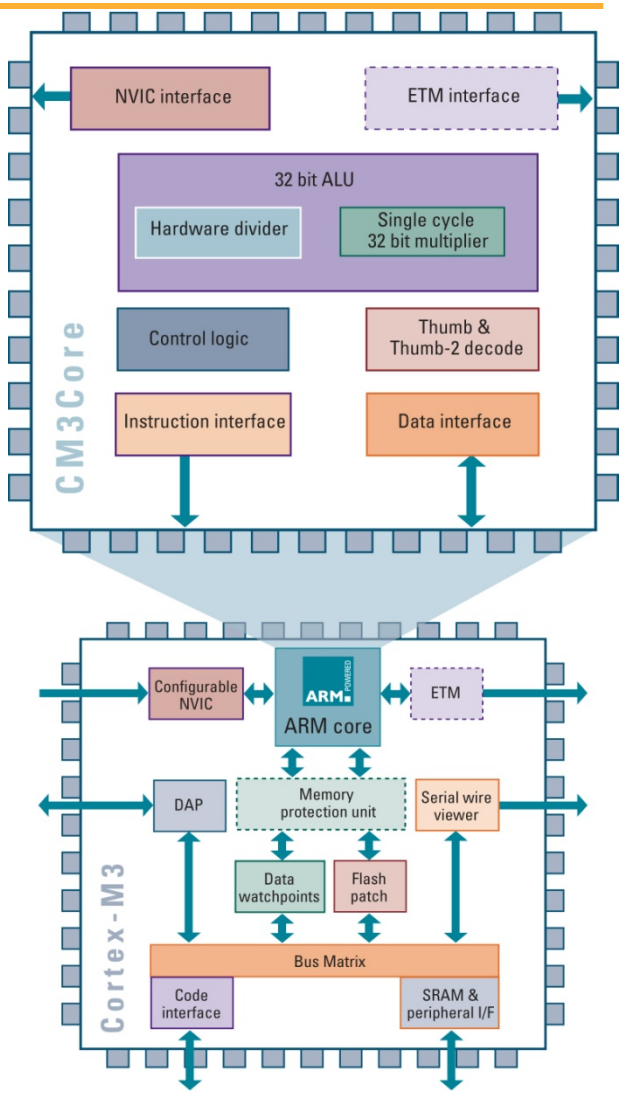
Clocks

Peripherals

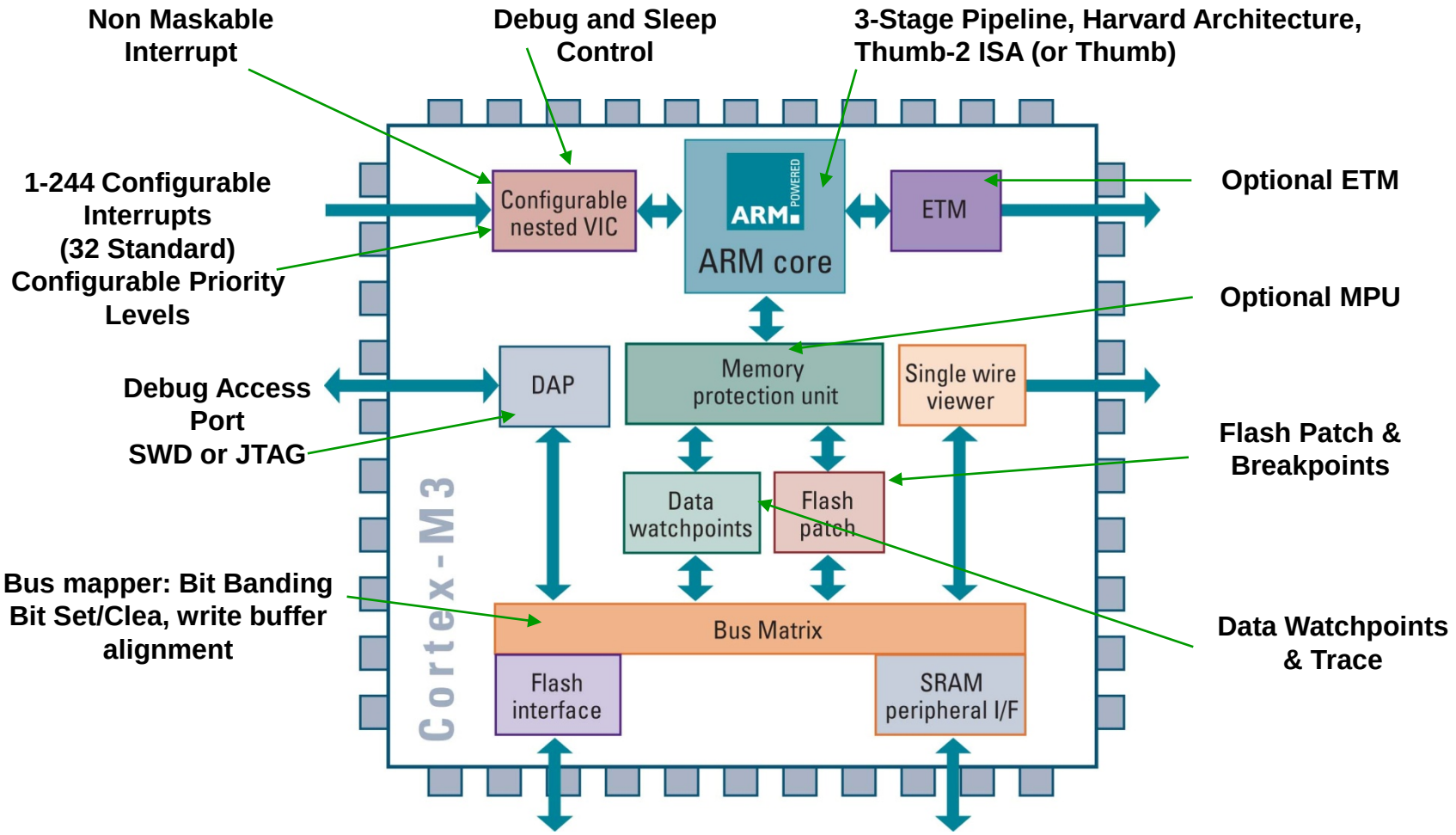


Cortex-M3 CPU

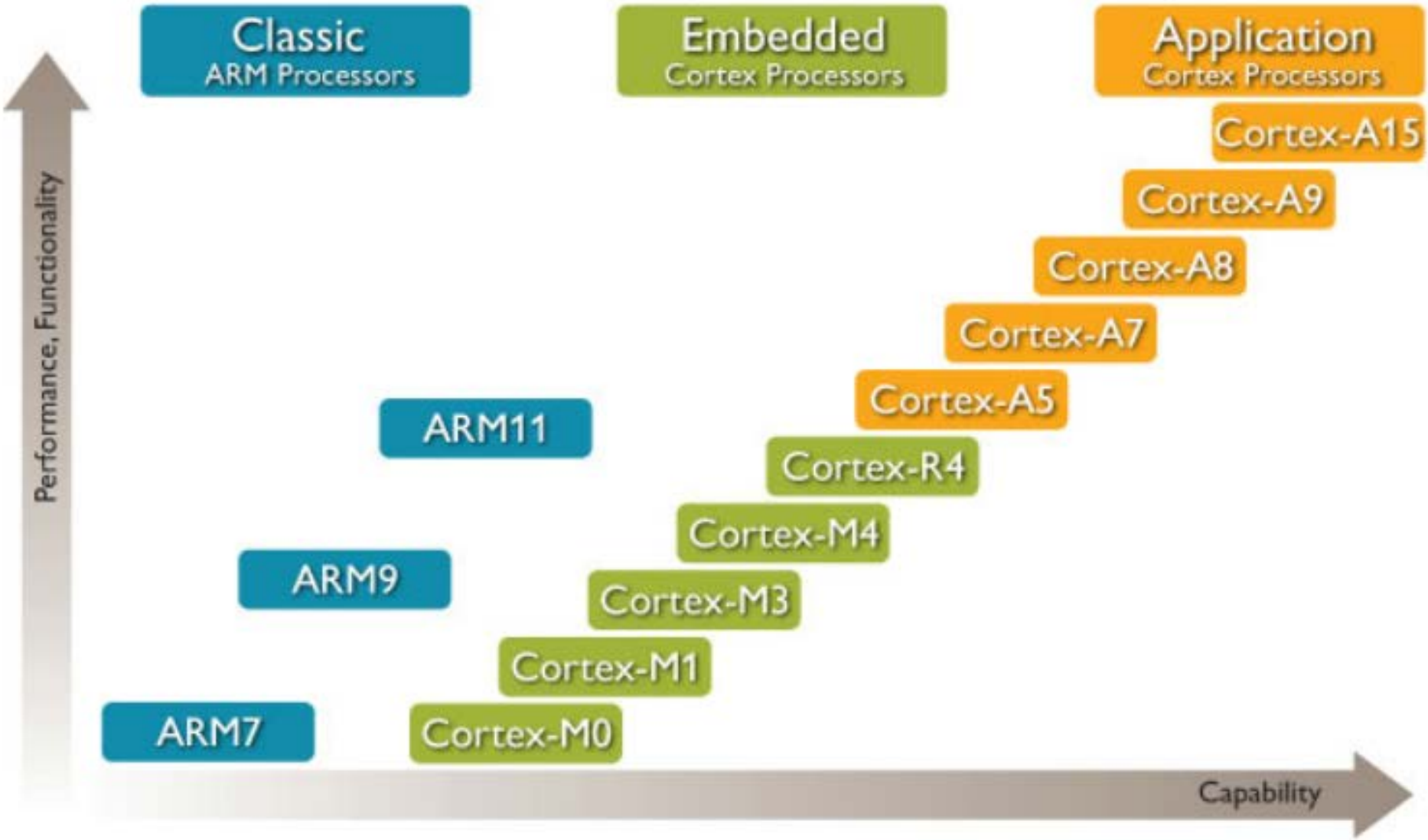
- Hierarchical processor integrating core and advanced system peripherals
- Cortex-M3 core
  - Harvard architecture
  - 3-stage pipeline w. branch speculation
  - Thumb®-2 and traditional Thumb
  - ALU w. H/W divide and single cycle multiply
- Cortex-M3 *Processor*
  - Cortex-M3 core
  - Configurable interrupt controller
  - Bus matrix
  - Advanced debug components
  - Optional MPU & ETM (Not available in STM32F10x)



Cortex-M3 Microprocessor



Processors for All Applications

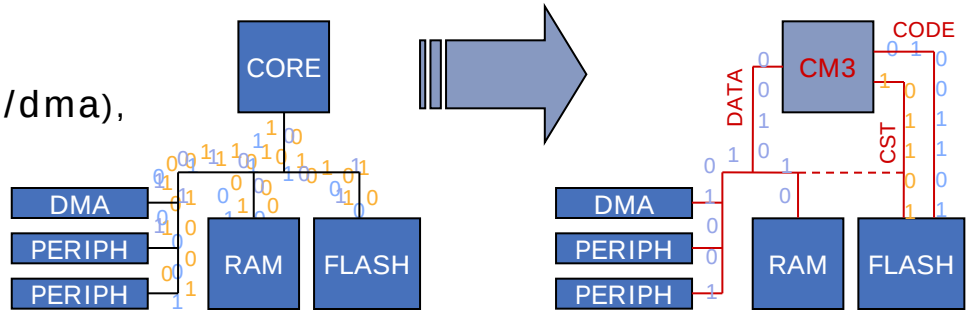


Bus system

Architecture of the bus

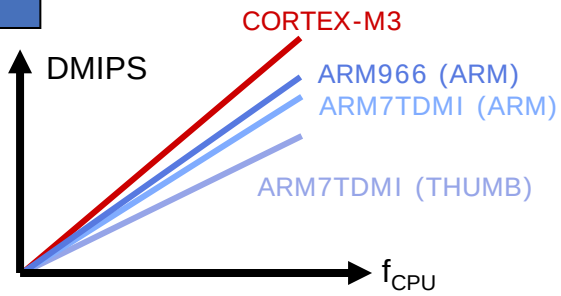
- Cortex M3 Architecture: Harvard benefits with Von Neumann single memory space

Von Neumann “bottleneck”
Single 32bit bus for:
- code execution,
- data transfer (core/dma),
- peripheral control



Three 32bit buses for a parallel
- code execution,
- data transfer (core/dma),
- peripheral control

- Outstanding efficiency of 1.25 DMIPS/MHz



- THUMB2 instruction set provides 32bit performance with 16bit code density

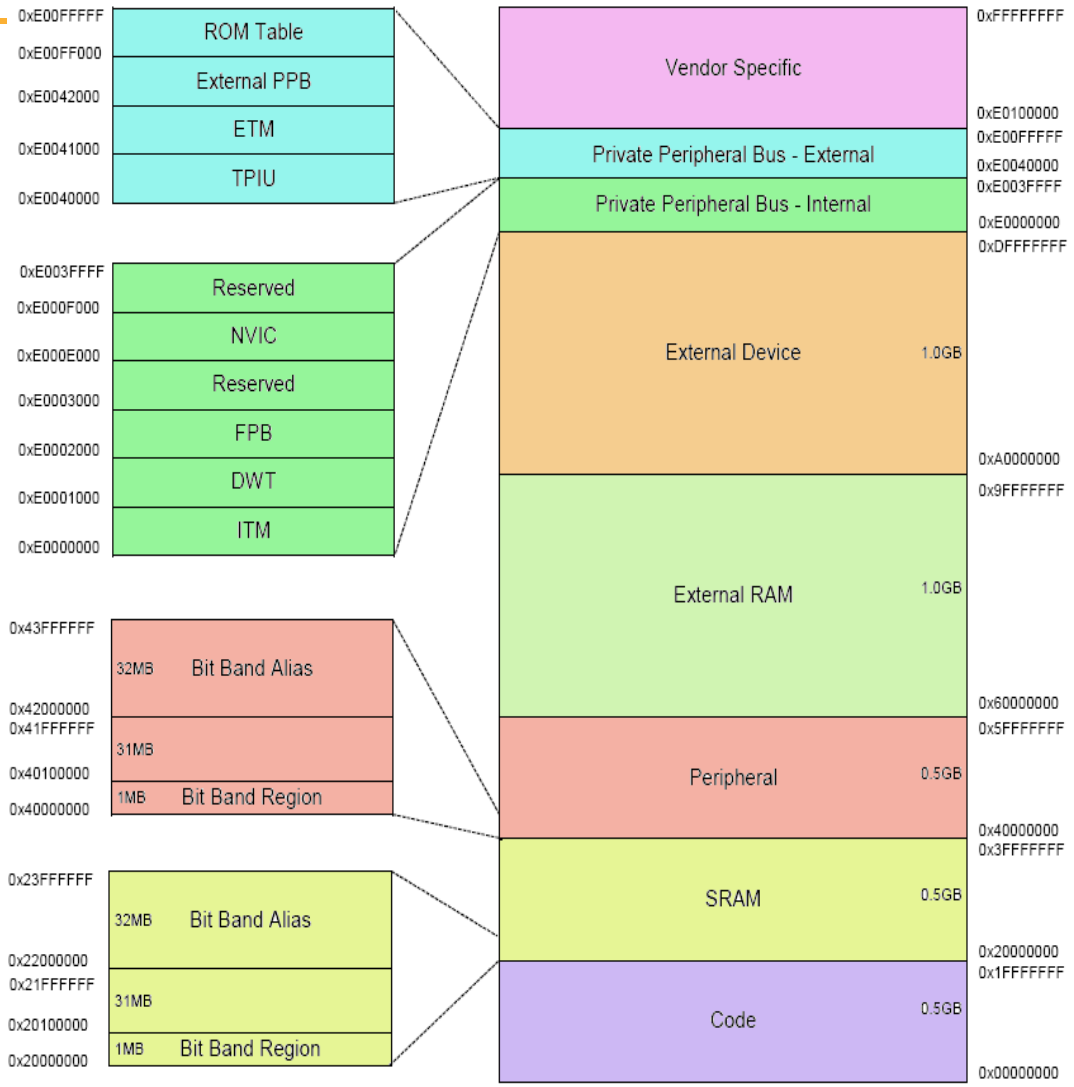
THUMB 16bit Instruction Set	Full THUMB compatibility
ARM 32bit Instruction Subset	Complete ARM instruction set for better performance
New 16/32bit Instructions	1 cycle MAC and Hardware Divide Unaligned data, Bit banding

THUMB-2

- Single POWERFUL instruction set
  → No more mode switching
- 25% smaller code
- 25% lower RAM requirement

Cortex-M3 Memory Map

- **Vendor Specific (0.5GB)**
  - **Set aside to enable vendors to implement peripheral compatibility with previous systems**
- **Private Peripheral Bus (1M)**
  - **Address space for system components (CoreSight, NVIC etc.)**
- **External Device (1GB).**
  - **Intended for external devices and/or shared memory that needs ordering/non-buffered**
- **External RAM (1GB)**
  - **Intended for off chip memory**
- **Peripheral (0.5G)**
  - **Intended for normal peripherals. The bottom 1MB of the 32MB peripheral address space (0x40000000 – 0x400FFFFF) is reserved for bit-band accesses. Accesses to the peripheral 32MB bit band alias region (0x42000000 – 0x43FFFFFF) are remapped to this 1MB**
- **SRAM (0.5GB)**
  - **Intended for on-chip SRAM. The bottom 1MB of the SRAM address space (0x20000000 - 0x200FFFFF) is reserved for bit-band accesses. Accesses to the SRAM 32MB bit band alias region (0x22000000 – 0x23FFFFFF) are remapped to this 1MB address space.**
- **Code(0.5GB)**
  - **Reserved for code memory (flash, SRAM). This region is accessed via the Cortex-M3 ICode and DCode busses.**

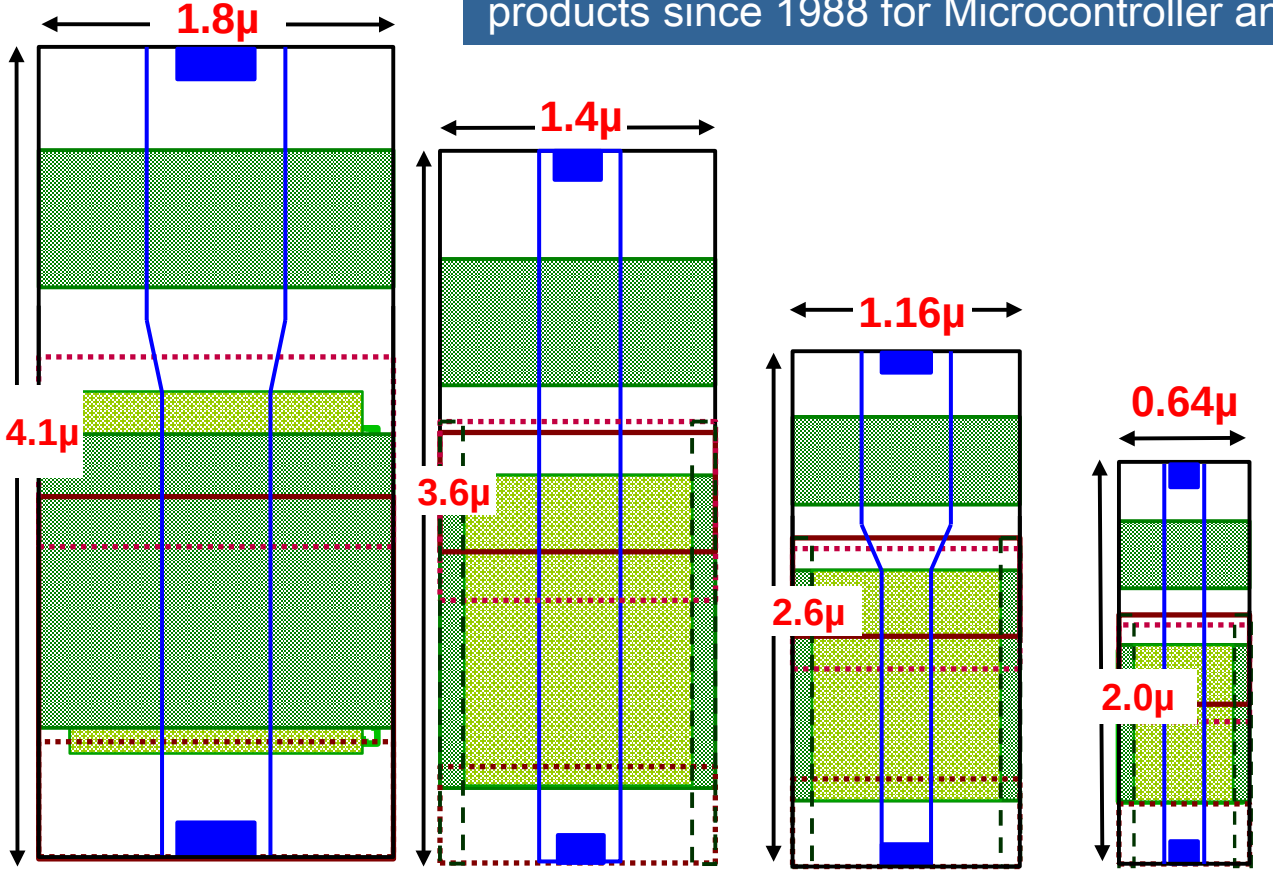


Production Technologies

The road to success...

CMOSF9 eEEPROM Technology History

STMicroelectronics designs and manufactures embedded EEPROM products since 1988 for Microcontroller and Smartcard applications.



0.35µ
F6Y s=7.4µ²

0.18µ
F8 s=5.04µ²

0.15µ
F8N s=3.02µ²

0.13µ
F9 1.28µ²

Beside embedded EEPROM each technology node contains also a sister technology with embedded flash.

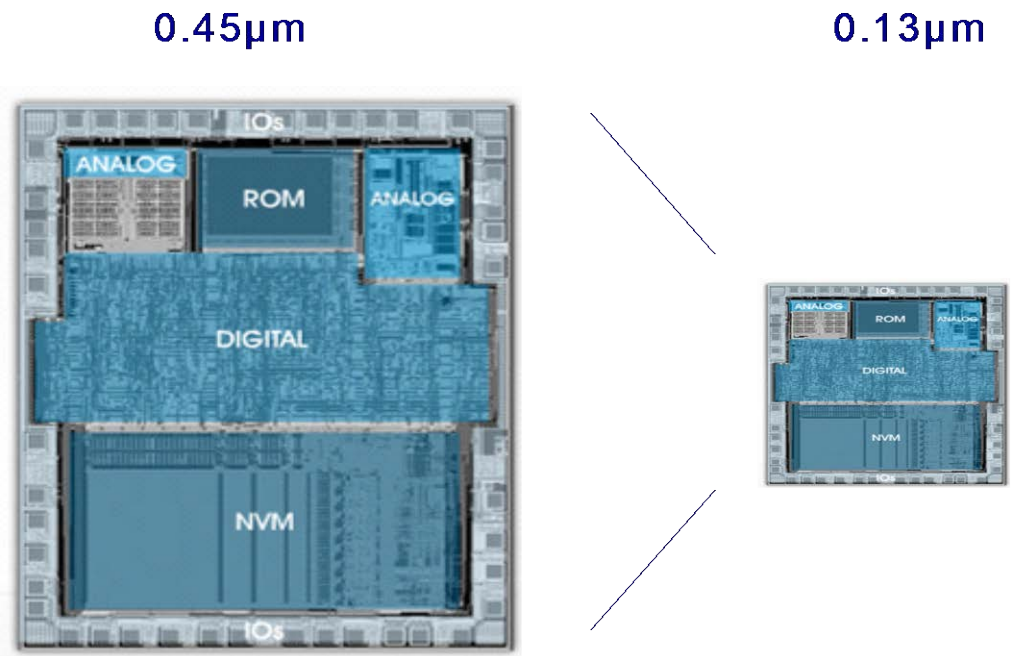
Today the 65nm node is being developed.

Technology to Break Price Barriers

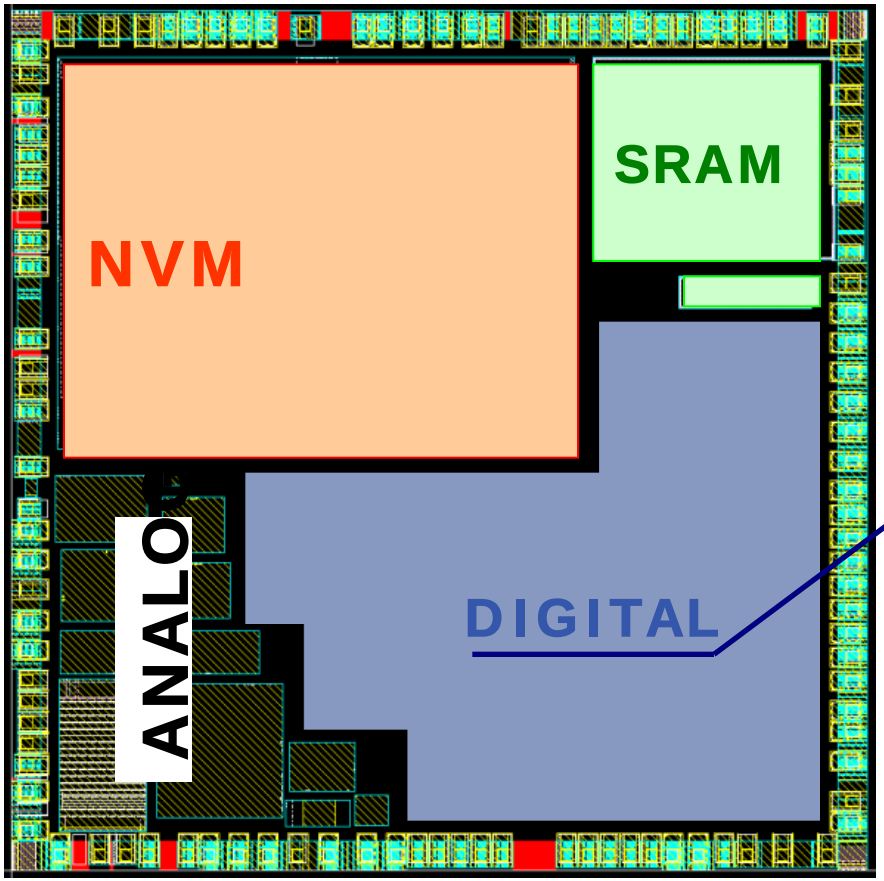
- Technology driving 8-bit evolution
- Breakthrough with 130nm lithography
- E² non-volatile memory, analog and digital peripherals

0,4µM

0,13µm



What part can be shrunk with production technologies?



Total digital bloc is **25% of the die size**

The CPU represents **30% of the digital area**

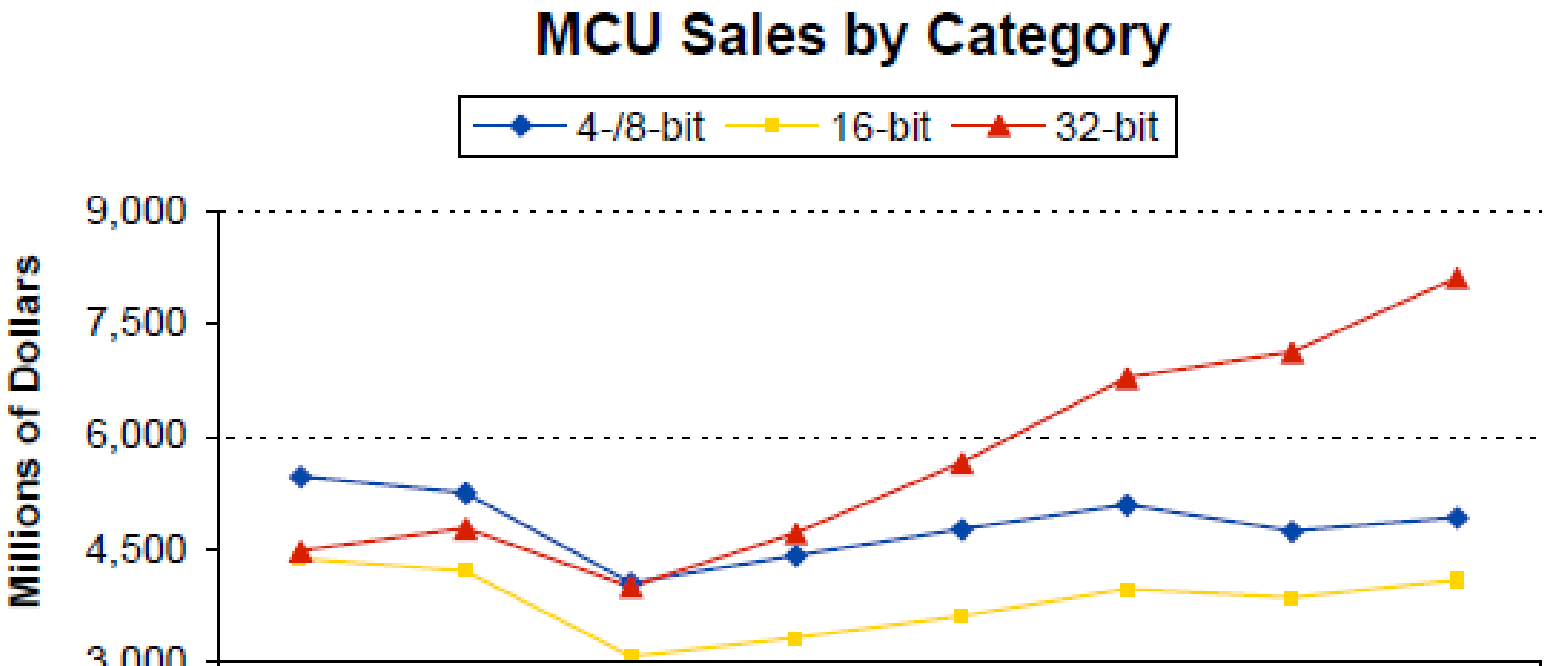
Cortex M0 is half gate count of M3 for the same configuration

Using M0 instead of M3 would lead to :

- **Less than 4% die area gain**
- **Less than 2% product cost gain**

How do we think when we design a MCU?

MCU total market trend



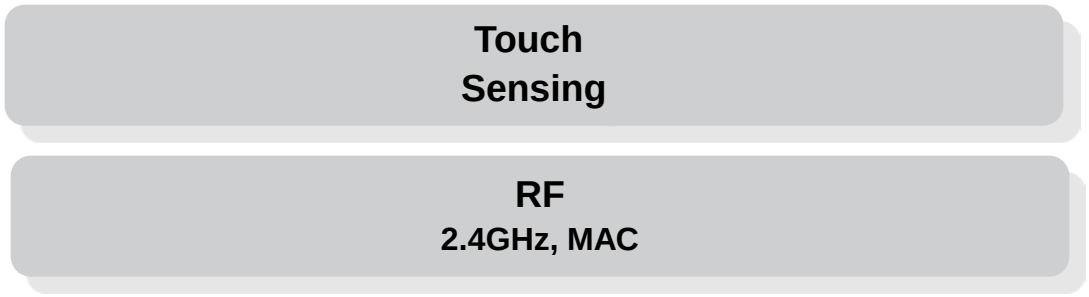
	07	08	09	10F	11F	12F	13F	14F
4-/8-bit	5,460	5,242	4,036	4,399	4,751	5,084	4,728	4,917
16-bit	4,370	4,195	3,062	3,307	3,605	3,966	3,847	4,078
32-bit	4,475	4,766	3,984	4,701	5,641	6,769	7,108	8,103

Source: IC Insights

Product Strategy – 5 Product families

General Purpose family
The foundation of our product portfolio

Application specific in key area of expertise



Minimal External Components

- **Built-in Supervisor reduces need for external components**
  - Filtered reset input, Power-On reset, Low-Voltage Detect, Brown-Out Detect, Watchdog Timer with independent clock
- **One main crystal drives entire system (with help from PLL)**
  - Inexpensive 4-16 MHz crystal drives CPU, USB, all peripherals
- **Embedded 8 MHz RC can be used as main clock**
  - Optional 32 kHz crystal needed additionally for RTC, can run on internal 40 kHz RC
- **Only 7 external passive components for base system on LQFP100 package!!**

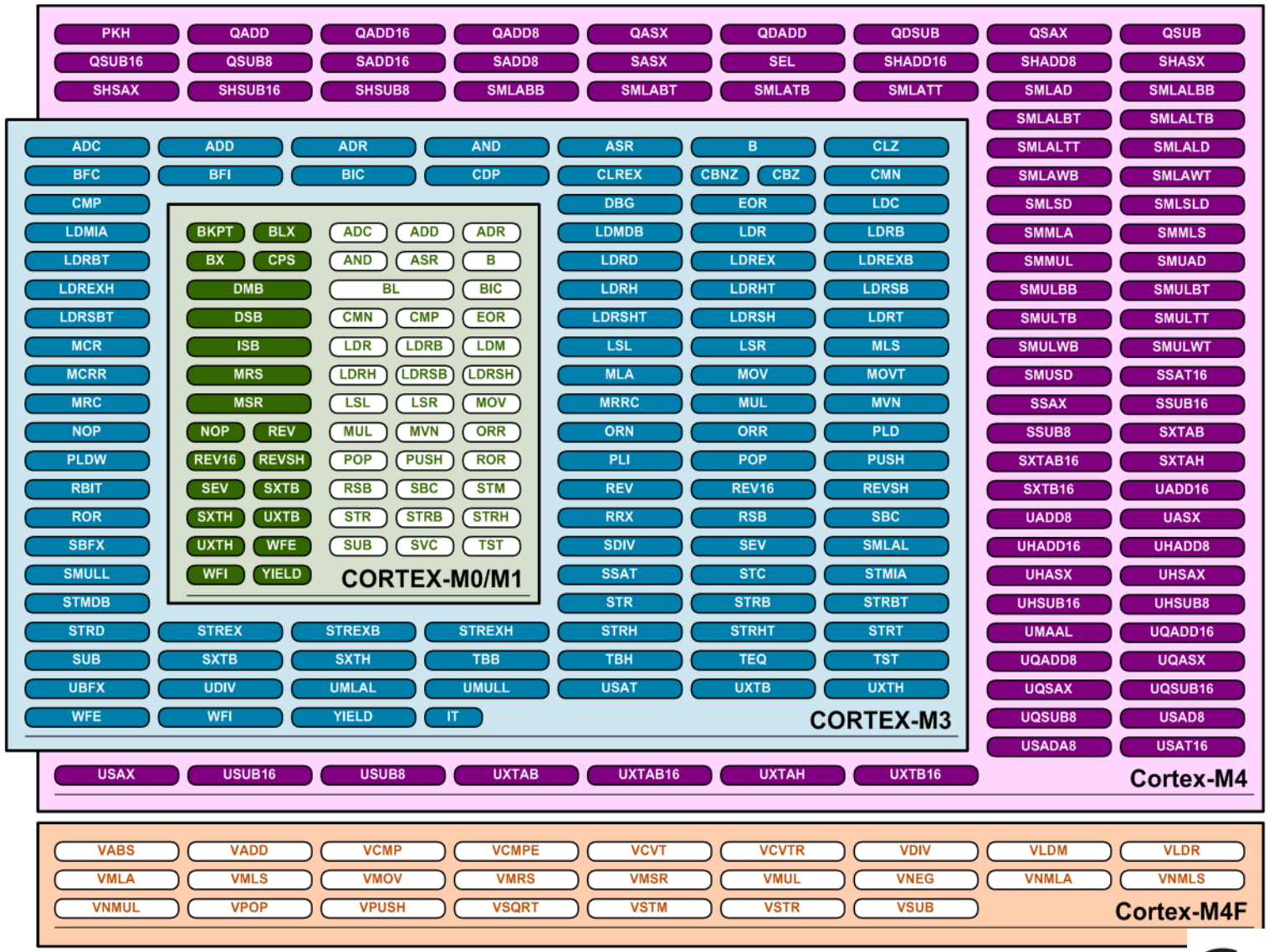
Cortex-M processors

- **Forget traditional 8/16/32-bit classifications**
  - Seamless architecture across all applications
  - Every product optimised for ultra low power and ease of use

Cortex-M0	Cortex-M3	Cortex-M4
“8/16-bit” applications	“16/32-bit” applications	“32-bit/DSC” applications

Binary and tool compatible

Cortex-M processors binary compatible



STM32 product series

4 product series

Common core peripherals and architecture:

- Communication peripherals: USART, SPI, I²C
- Multiple general-purpose timers
- Integrated reset and brown-out warning
- Multiple DMA
- 2x watchdogs Real-time clock
- Integrated regulator PLL and clock circuit
- External memory interface (FSMC)
- Dual 12-bit DAC
- Up to 3x 12-bit ADC (up to 0.41 µs)
- Main oscillator and 32 kHz oscillator
- Low-speed and high-speed internal RC oscillators
- -40 to +85 °C and up to 105 °C operating temperature range
- Low voltage 2.0 to 3.6 V or 1.65/1.7 to 3.6 V (depending on series) 5.0 V tolerant I/Os
- Temperature sensor

STM32 F4 series - High performance with DSP (STM32F405/415/407/417)

168 MHz Cortex-M4 with DSP and FPU	Up to 192-Kbyte SRAM	Up to 1-Mbyte Flash	2x USB 2.0 OTG FS/HS	3-phase MC timer	2x CAN 2.0B	SDIO 2x I²S audio Camera IF	Ethernet IEEE 1588	Crypto/hash processor and RNG

STM32 F2 series - High performance (STM32F205/215/207/217)

120 MHz Cortex-M3 CPU	Up to 128-Kbyte SRAM	Up to 1-Mbyte Flash	2x USB 2.0 OTG FS/HS	3-phase MC timer	2x CAN 2.0B	SDIO 2x I²S audio Camera IF	Ethernet IEEE 1588	Crypto/hash processor and RNG

STM32 F1 series - Connectivity line (STM32F105/107)

72 MHz Cortex-M3 CPU	Up to 64-Kbyte SRAM	Up to 256-Kbyte Flash	USB 2.0 OTG FS	3-phase MC timer	2x CAN 2.0B	2x I²S audio	Ethernet IEEE 1588

STM32 F1 series - Performance line (STM32F103)

72 MHz Cortex-M3 CPU	Up to 96-Kbyte SRAM	Up to 1-Mbyte Flash	USB FS device	3-phase MC timer	CAN 2.0B	SDIO 2x I²S

STM32 F1 series - USB Access line (STM32F102)

+

48 MHz Cortex-M3 CPU	Up to 16-Kbyte SRAM	Up to 128-Kbyte Flash	USB FS device

STM32 F1 series - Access line (STM32F101)

36 MHz Cortex-M3 CPU	Up to 80-Kbyte SRAM	Up to 1-Mbyte Flash

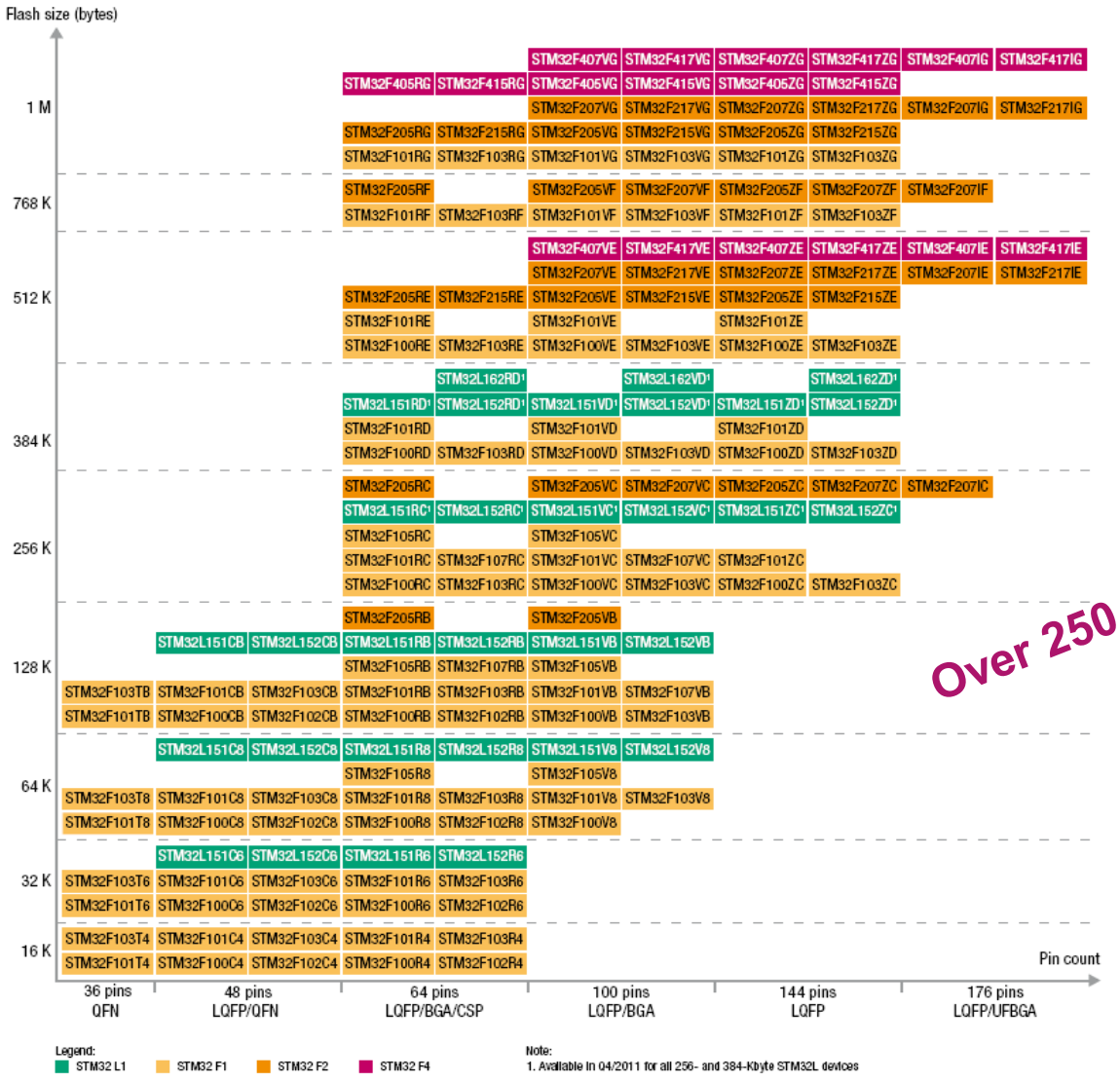
STM32 F1 series - Value line (STM32F100)

24 MHz Cortex-M3 CPU	Up to 32-Kbyte SRAM	Up to 512-Kbyte Flash	3-phase MC timer	CEC

STM32 L1 series - Ultra-low-power (STM32F151/152)

32 MHz Cortex-M3 CPU	Up to 48-Kbyte SRAM	Up to 384-Kbyte Flash	USB FS device	Data EEPROM up to 12 Kbytes	LCD 8x40 4x44	Comparator	BOR MSI VScal	AES 128-bit

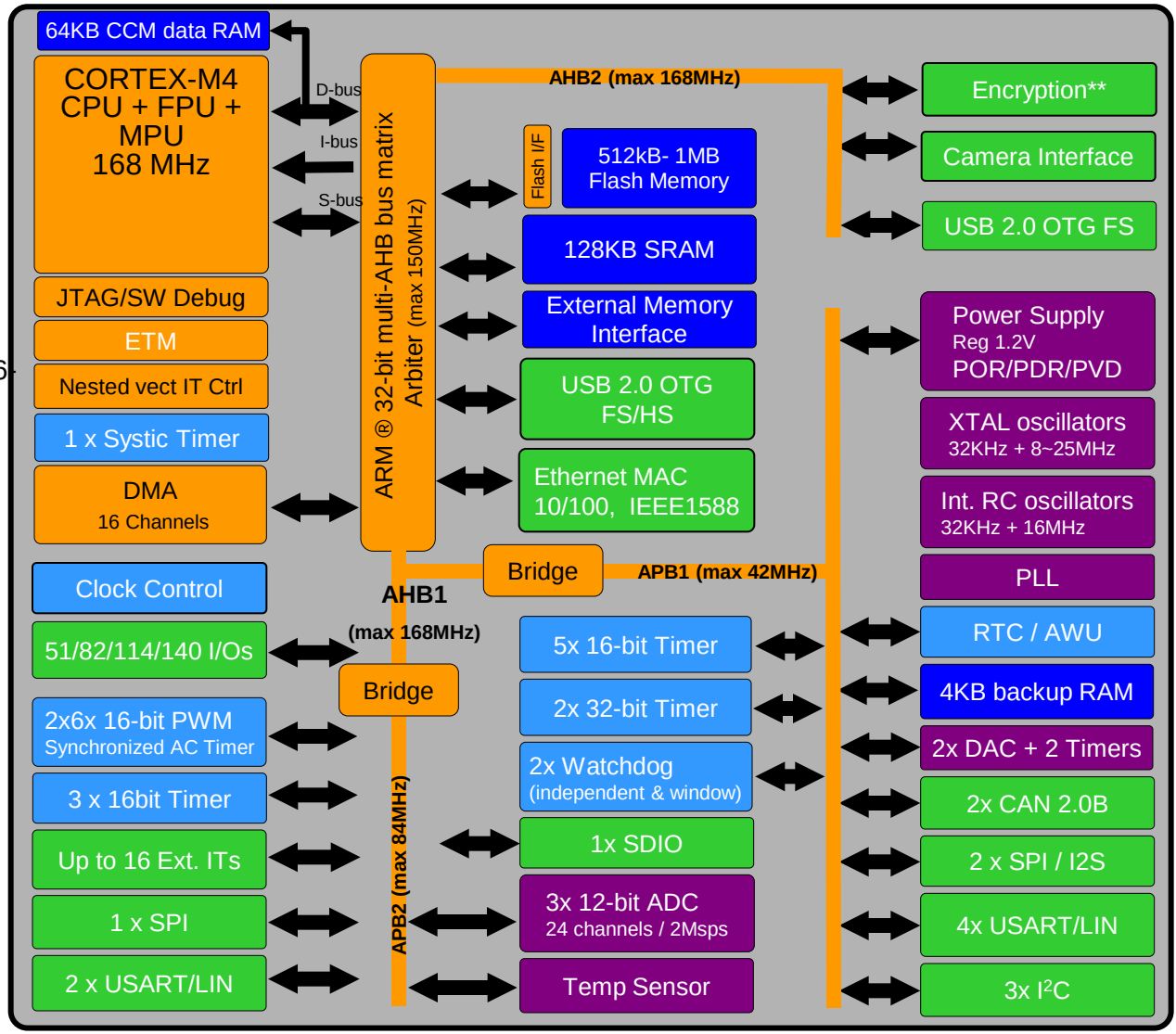
STM32 – leading Cortex-M portfolio



Over 250 pin-to-pin compatible part numbers

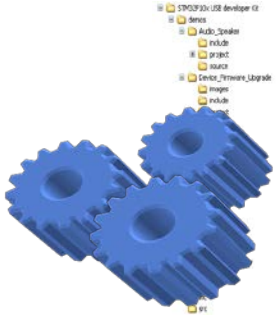
STM32F4xx Block Diagram

- **Cortex-M4 w/ FPU, MPU and ETM**
- **Memory**
  - Up to 1MB Flash memory
  - 192KB RAM including 64KB CCM data RAM
  - FSMC up to 60MHz
- **New application specific peripherals**
  - USB OTG HS w/ ULPI interface
  - Camera interface
  - HW Encryption**: DES, 3DES, AES 256-bit, SHA-1 hash, RNG.
- **Enhanced peripherals**
  - USB OTG Full speed
  - ADC: 0.416µs conversion/2.4Msps, up to 7.2Msps in interleaved triple mode
  - ADC/DAC working down to 1.8V
  - Dedicated PLL for I2S precision
  - Ethernet w/ HW IEEE1588 v2.0
  - 32-bit RTC with calendar
  - 4KB backup SRAM in VBAT domain
  - Pure 1% RC
  - 2 x 32bit and 8 x 16bit Timers
  - high speed USART up to 10.5Mb/s
  - high speed SPI up to 37.5Mb/s
- **RDP (JTAG fuse)**
- **More I/O:s in UFBGA 176 package**



HS requires an external PHY connected to ULPI interface,
** Encryption is only available on STM32F415 and STM32F417

Free software solutions from ST



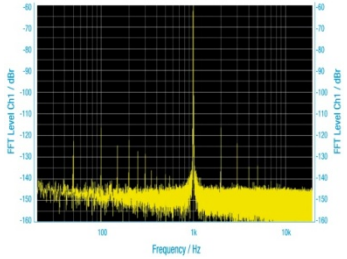
Standard Peripheral Library

USB device library

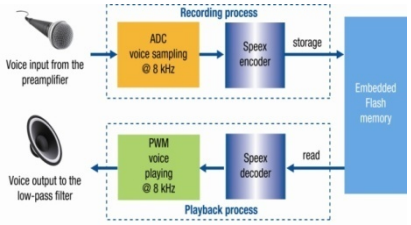
USB Host Library

Motor Control Library

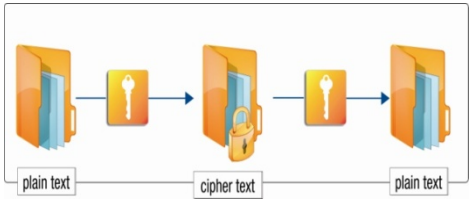
Self-test routines for EN/IEC 60335-1 Class B



DSP Library



SPEEX Codec



Encryption Library

STM32 Audio Engine

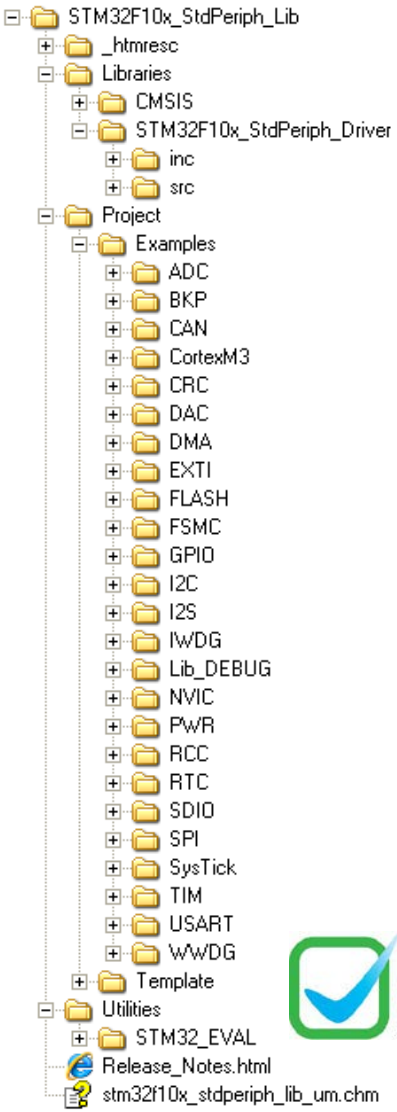
Software libraries – speed time to market

- **ST software libraries free at www.st.com/mcu**

  C source code for easy implementation of all STM32 peripherals in any application

  - **Standard library** – source code for implementation of all standard peripherals; code implemented in demos for STM32 evaluation board
  - **Motor control library –** sensorless vector control for 3-phase brushless motors
  - **USB Device Library** – Supporting HID,CDC, Audio, Mass Storage, DFU…)
  - **USB Host Library** – Supporting Mass Storage and HID
  - **DSP Library** – PID, IIR, FFT, FIR
  - **Graphics Library** – Drop down menus, radio buttons, sliders, …

- **Software Solutions for**
  - Ethernet TCP/IP
  - Bluetooth
  - SpeexCodec
  - And many others.

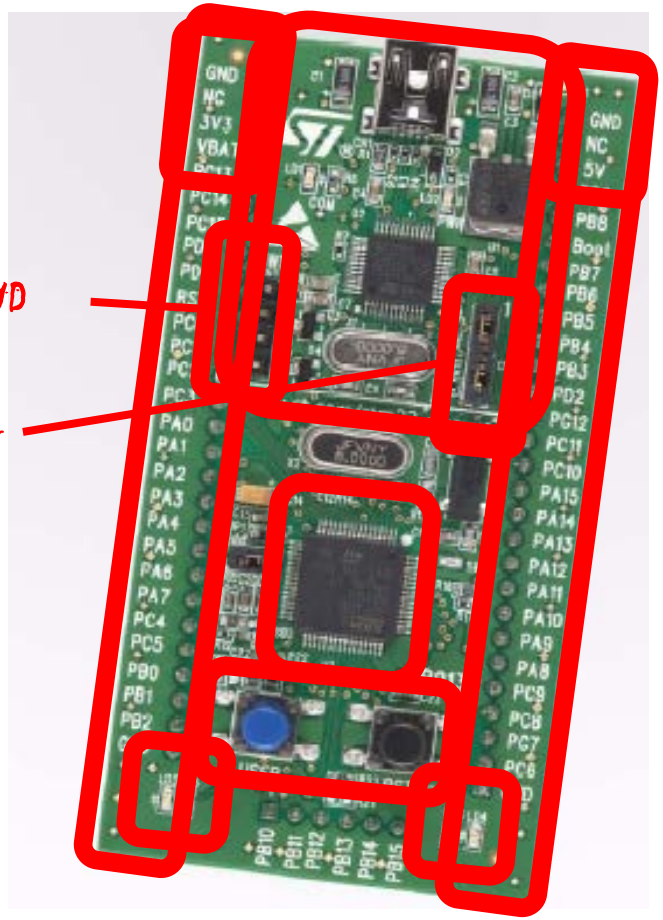


STM32 Evaluation Board

- Hardware Evaluation Platform for all interfaces
  - Boards available for ALL STM32 Families
- Possible connection to all I/Os and all peripherals
- Flash is loaded with self-test firmware, and demos for USB, CAN, SD Card etc.
- Firmware projects available from www.st.com/mcu
- Vendor neutral
  - works with any IDE or JTAG dongle

STM32 Discovery Kit

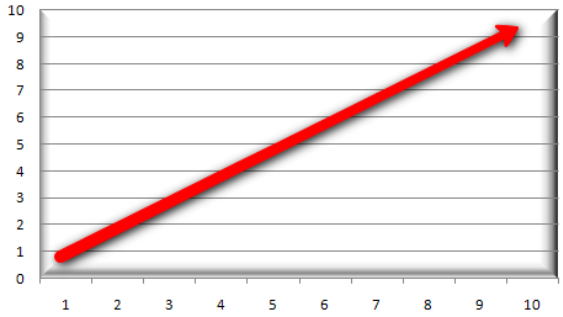
- STM32F100RBT6B microcontroller,
  - 128 KB Flash, 8 KB RAM in 64-pin LQFP
- On-board ST-Link
  - Can be used as standalone ST-Link with SWD for programming and debugging
- On-board / Standalone configurable
- Multiple Power Supply Options
  - USB
  - External 5 V
  - External 3.3 V
- Two user LEDs
  - LD3 (green)
  - LD4 (blue)
- Two push buttons (User and Reset)
  - User / application
  - Reset
- 2.54mm (0.1”) Extension header for all MCU pins
  - Quick connection to prototyping board
  - Easy probing

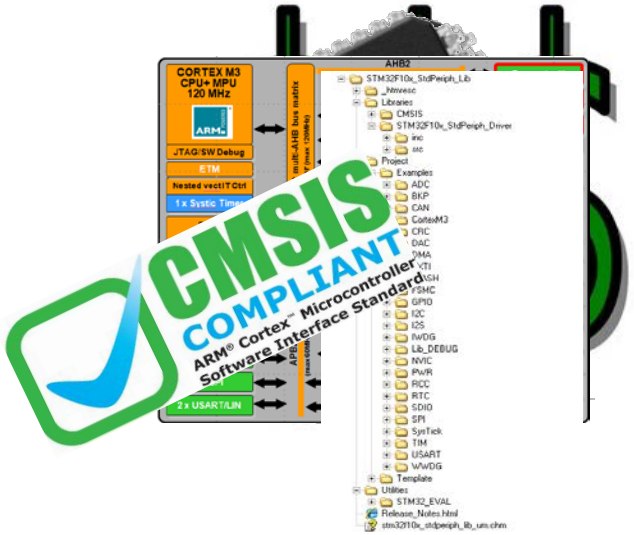


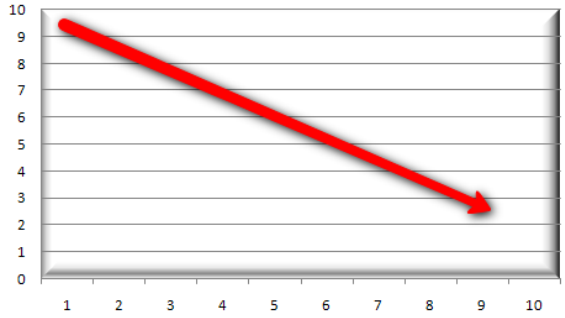
The easiest start to working with STM32!

Future

MCU Trends – a selection







MCU Trends – a selection of topics

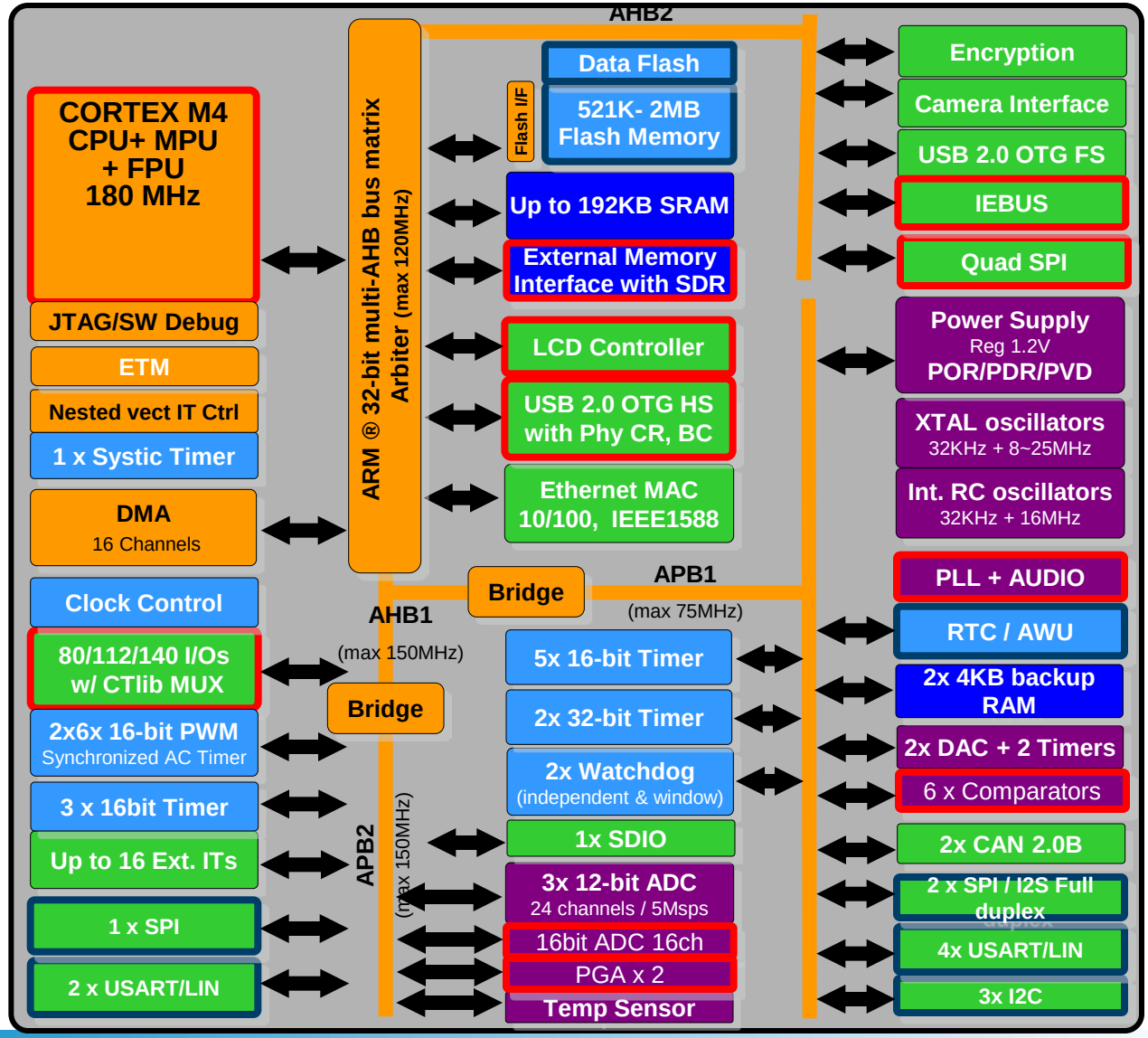
- Price → Technology
- Performance → Low Power and MIPS
- Memory size → Larger flash and RAM
- Peripheral Integration → analog, RF
- Industry standard cores → Cortex M
- Advanced Peripherals → USB Ethernet LCD
- Predefined Libraries + RTOS → Abstraction from the hardware

F-4 series STM32F47x

- 1.62V-3.6V Supply
- 180 MHz running M4 + FPU
- EMI with SDRAM Support
- LCD Controller
- Audio
  - PLL with streaming support
  - I2S full duplex
- Fast power-on reset
- Fast wakeup and recovery
- USB down to 1.62V
- Dual power IOs
- 64 pins to 176 pins
- -40/+105° C

Improvements

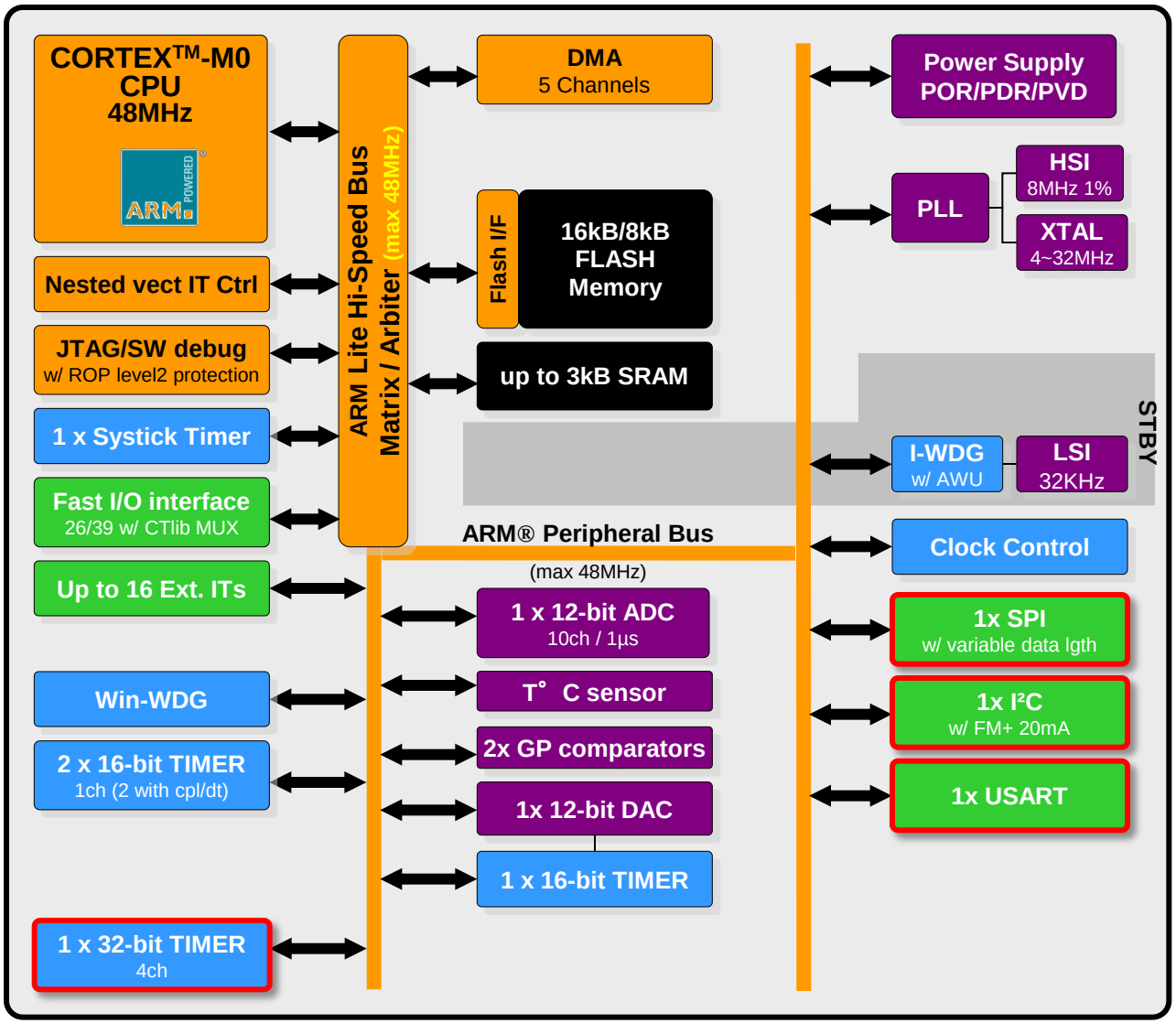
New



F-0 Series 16KB STM32F051

Key features

- 48MHz max CPU freq
- SRAM with hardware parity checking
- 2.0V-3.6V supply
  - 1.8V 10% with special bounding
- Package UFQFN 32, LQFP48
- Up to 39 fast IOs (AHB)
- 2x GP comparators
- Capacitive touch sensing
- I2C Fast Mode +
- SPI variable data length



Q & A

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