# Lecture 10

Metallization / Back-end technology (BEOL)

Lecture 9: Metallization and BEOL

- ## Metallization Technology
  - Evaporation
  - Sputtering
- ## Back End Of the Line (BEOL)
  - ITRS Requirements
  - Evolution of Metallization
  - Dielectrics
  - Integration
- ## Future Options

# Metallization: Two Main Deposition Methods
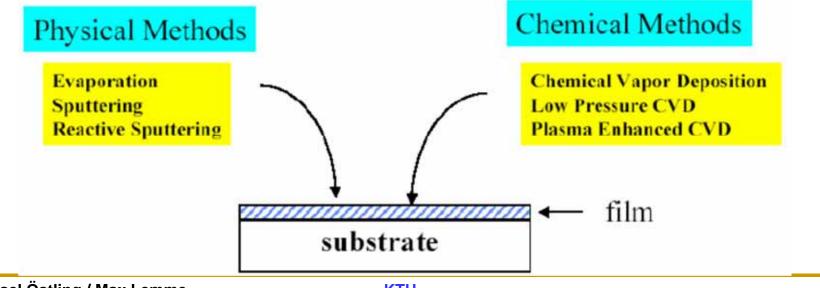
1) Chemical Vapor Deposition (CVD)
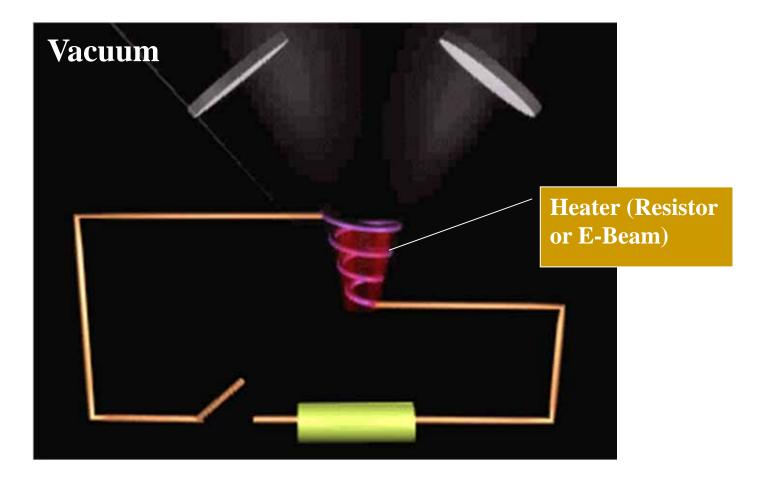
Gases are introduced into the deposition chamber that react and form the desired film on the substrate surface.

Such as APCVD, LPCVD, PECVD, HDPCVD, ALD

2) Physical Vapor Deposition (PVD)

Use a certain physical process to transfer materials, i.e., transfer atoms or molecules onto the substrate (Si) surface and deposit them into films.

Such as MBE, evaporation, sputtering

Physical Methods

Evaporation
Sputtering
Reactive Sputtering

Chemical Methods

Chemical Vapor Deposition
Low Pressure CVD
Plasma Enhanced CVD

film

substrate

Evaporation

Evaporation
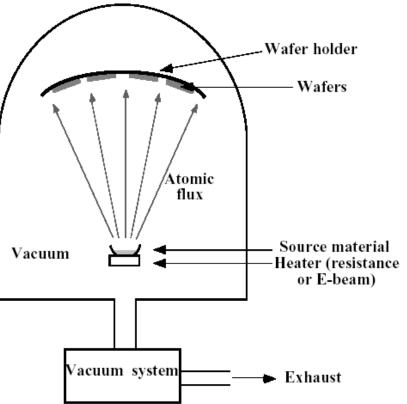
Physical Process

(a) The source material is heated up and evaporated from condensed phase (solid or liquid phase) to gas phase. The needed energy for the evaporation is Vaporization Heat ΔH_v

$$\log P_v = A - \frac{B}{T}$$

$$B = \frac{\Delta H_v}{2.3 R_0}$$

P_v is vapor pressure
A is integral constant
R_0 is Avogadro constant

(b) Evaporated atoms transport in the vacuum system

(c) Evaporated atoms are adsorbed onto the substrate wafers and nucleate and grow into films

Evaporation

Dependence of Vapor
Pressure on
Temperature for different
Elements

For the sake of suitable
deposition rate, the vapor
pressure should reduce to
less than 10 mTorr.

Ta, W, Mo and Pt have very
high melting points. For
example, in order for
10 mtorr vapor pressure, W
needs the temperature over
3000 ^{o}C.
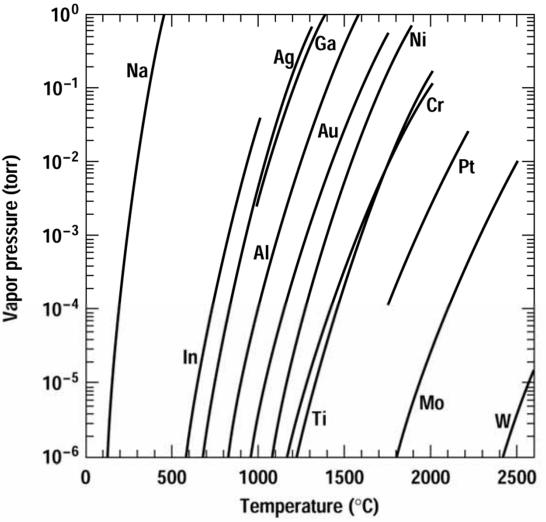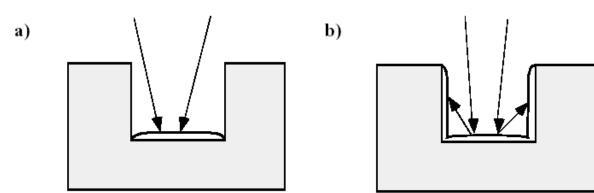
Figure 12.2   Vapor pressure curves for some commonly
evaporated materials (data adapted from Alcock et al.).

Evaporation

Properties:

• Can evaporate just about any element

• Deposition rate of some elements very slow

• Difficult to evaporate alloys and compounds

• Step coverage is poor (line of sight and $S_c \sim$ 1)

• Not applicable for mass production

Superiority of Sputtering:

✓**Better step coverage than evaporation**
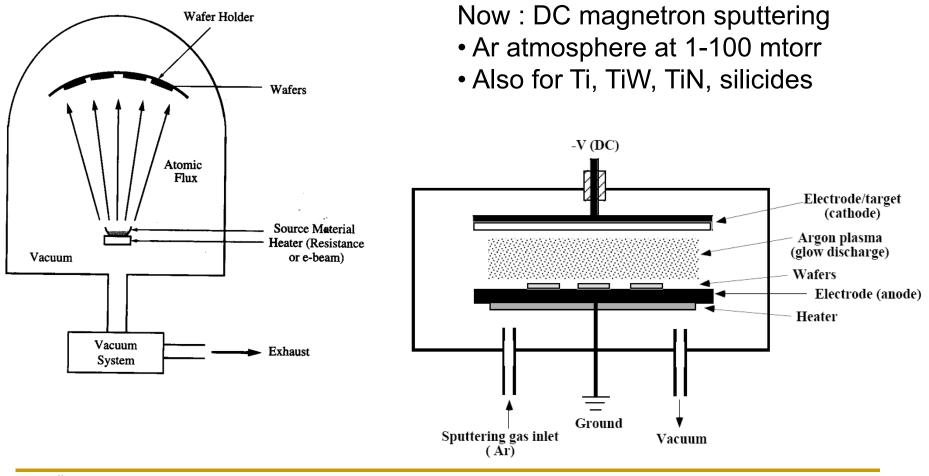
✓**Less radiation-caused defects than e-beam evaporation**

✓**Better performance for the fabricated compound materials and alloys**
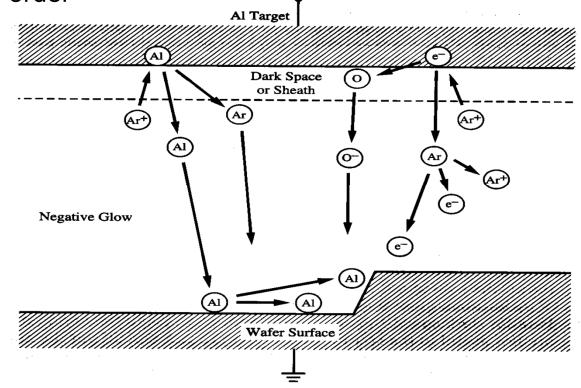
✓**Applicable for dielectric deposition**

a)

b)

Evaporation

Past: Evaporation

- Step coverage and deposition of alloys
- No Al CVD in production

Now : DC magnetron sputtering
• Ar atmosphere at 1-100 mtorr
• Also for Ti, TiW, TiN, silicides

Sputtering

Sputtering tools are similar to RIE and PECVD tools – only work in "reverse order"
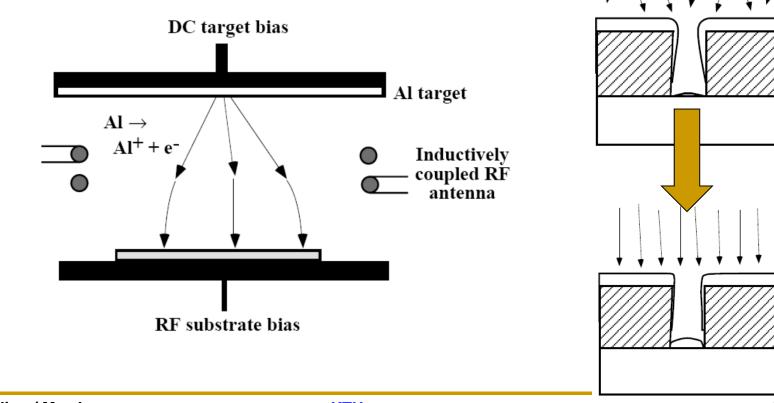

Step coverage:
Sputtering targets are generally large and provide a wide range of arrival angles in contrast to a point source
Higher temperature may enhance ion mobility on surface
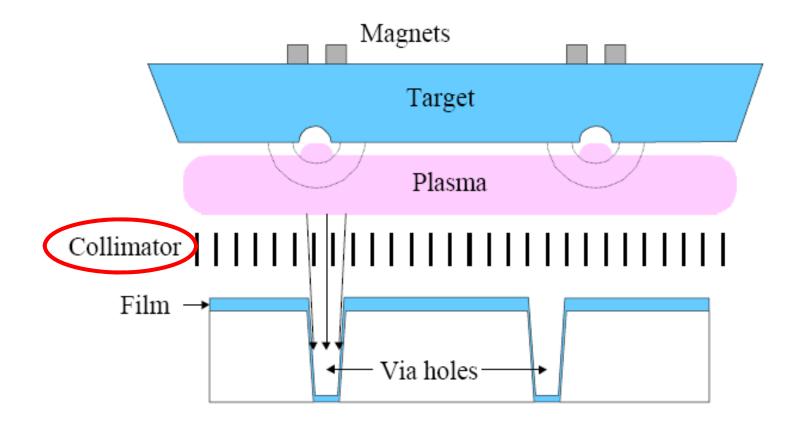
Sputtering
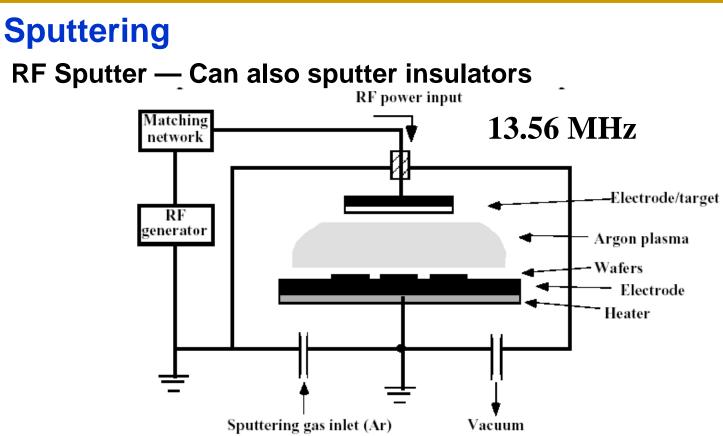
New sputter deposition technique: Ionized sputtering

RF coil around the plasma induces collisions in the plasma creating the ions

Ionizing field will direct ion flux perpendicular to wafer

→ narrow distribution of arrival angles improves filling or coating the bottom of deep contact holes

Sputtering

Collimated Sputtering

- Enhancing directionality

Sputtering

RF Sputter — Can also sputter insulators

RF power input

Matching network

13.56 MHz

RF generator

Electrode/target

Argon plasma

Wafers

Electrode

Heater

Sputtering gas inlet (Ar)   Vacuum
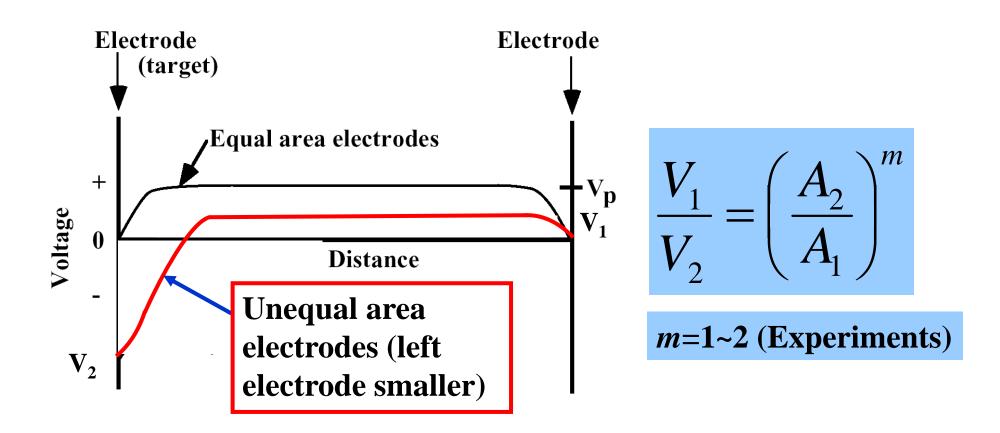
Reactive Sputter

Introduce reactive gases, such as O_2 or N_2, into the chamber to change or control the properties of the sputtered films.

Examples:
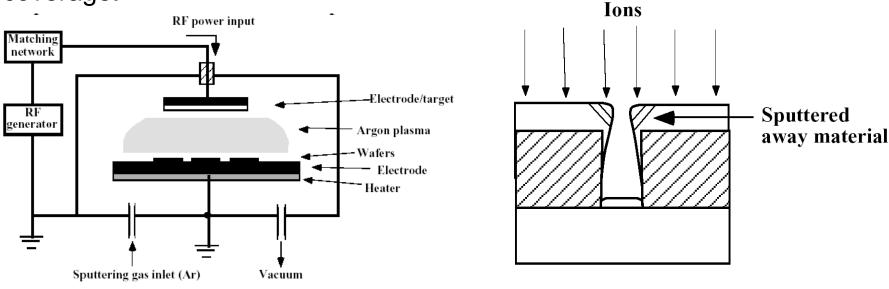
- Low-temperature fabrication of SiO_x and SiN_x passivation films
- Multilayer intermetal dielectrics
- Conductive films or diffusion barrier layers of TiN, TaN, etc.

Sputtering

Steady-state Voltage Distribution in RF Sputtering Systems

$$\frac{V_1}{V_2} = \left(\frac{A_2}{A_1}\right)^{m}$$

m=1~2 (Experiments)

Sputtering

Usually small-area target electrode is used to make most voltage difference apply on the target and let sputtering happen there. The wafer electrode can be connected with the chamber to increase the voltage difference ratio.

The wafer electrode can also be applied with RF bias separately for precleaning the wafer before actual deposition, or "sputter etching".

Another application is in "bias-sputtering", where deposition and sputtering of the wafer are done simultaneously. It can improve step coverage.

Sputtering

In both conventional DC and RF sputtering, the efficiency of ionization from energetic collisions between the electrons and gas atoms is rather low. Most electrons lose their energy in non-ionizing collisions or are collected by the anode. Magnetron sputtering can improve such efficiency.

- ✓ Can sputter alloys and refractory metals and unlike evaporation, do not change the alloy component
- ✓ Secondary electrons emitted from the cathode do not bombard the wafers due to the restriction from magnetic field and the temperature increase of wafers can be prevented.
- ✓ Good uniformity, reproducibility, and step coverage
- ✓ High efficiency

CVD versus PVD (coarse comparison)

	CVD	**PVD**
Flexibility	Poor	Good
Deposition temperature	High	Low
Deposition pressure	High	Low
Step coverage (conformality)	Good	Poor
Thickness uniformity	Good	Good
Composition control	Good	Poor
Film purity	High	Low
Dielectric	Preferred	-
Metal	-	Preferred

Preferred Deposition Methods by Metal

Al	Magnetron sputter deposition		25-300°C (standard deposition) 440-550°C (hot Al for in-situ reflow) CVD difficult for alloys (Al-Cu-Si)
Ti and Ti-W	Magnetron sputter deposition (standard, ionized or collimated)		CVD difficult Nitrogen can be added to Ti-W to stuff grain boundaries.
W	LPCVD	$2WF_6 + 3SiH_4 \rightarrow$ $2W + 3SiF_4 + 6H_2$ $WF_6 + 3H_2 \rightarrow$ $W + 6HF$	250-500°C Blanket deposition with two step process using both reactions is common.
$TiSi_2$	Sputter and surface reaction Co-sputtering or CVD	$Ti(sputtered) +$ $Si(exposed) \rightarrow TiSi_2$	Sputter/reaction give self-aligned silicide Two step anneal process required (600/800°C)
TiN	Reactive sputter deposition	$Ti + N_2(in\ plasma) \rightarrow TiN$	Organometallic source possible for MOCVD deposition

Concept Test 10.1

When writing the lab reports, I can

A.   use text passages from online sources like Wikipedia without referencing them, because Wikipedia is a free resource accessible for anyone.

B.   use text passages from non-copyrighted web sources without referencing them.

C.   quote any source I like, even when it is copyrighted.

D.   use sentences from Journal publications like "Nature" or "Electron Device Letters", because they are so well written that there is no need to change them.

E.   use facts from journal publications without a reference – they are facts after all.

Lecture 9: Metallization and BEOL

- # Metallization Technology
  - ## Evaporation
  - ## Sputtering
- # Back End Of the Line (BEOL)
  - ## ITRS Requirements
  - ## Evolution of Metallization
 - ## Dielectrics
  - ## Integration
- # Future Options
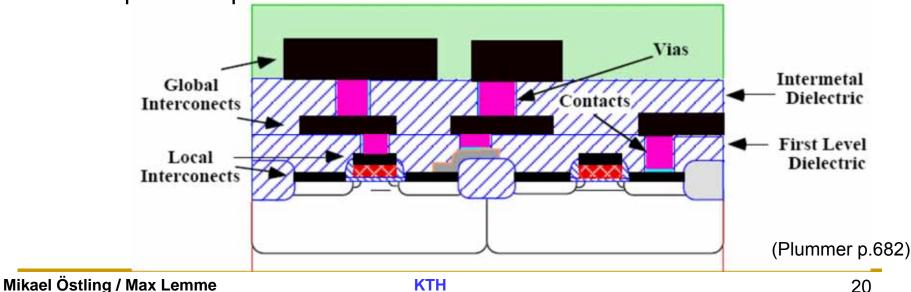
BEOL in VLSI: Interconnects and Dielectrics

Local interconnects: 1st level of metallization
• On device level
• In the past: Al
• Now: Heavily doped polysilicon and/or silicides
• Must withstand high temperatures ~800°C
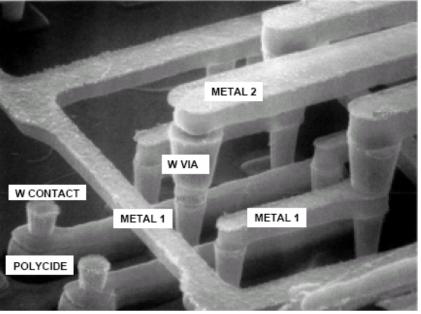
Global interconnects: 2nd level of metallization and up
• On chip level with length ~ µm
• Al and Cu used
• Low-temperature processes

(Plummer p.682)
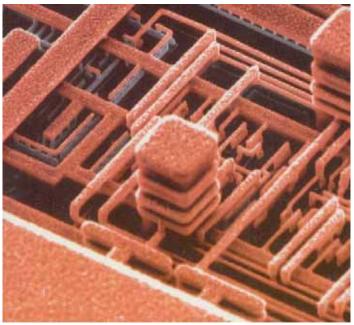
BEOL in VLSI: Interconnects and Dielectrics

• More metal interconnect levels increases circuit functionality and speed.

• Interconnects are separated into local interconnects (polysilicon, silicides, TiN) and global interconnects (usually Al, Cu).

• Backend processing is becoming more important.

• Larger fraction of total structure and processing.

• Increasingly dominates total speed of circuit.

(Photo courtest of Integrated Circuit Engineering.)

Cu metallization with etched off dielectrics, IBM 1997
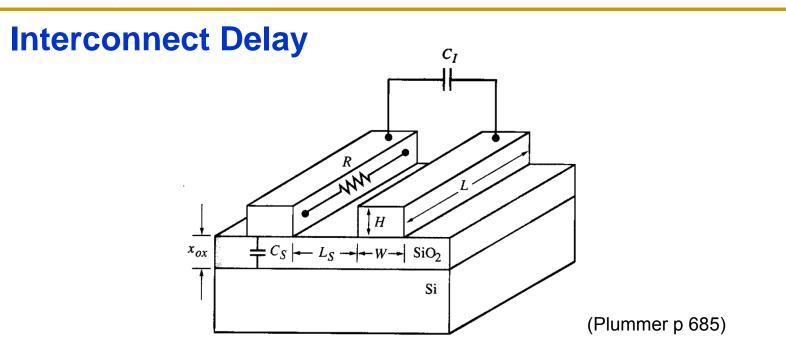
Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
Number of metal levels	11	11	11	12	12	12	12	12	13
Metal 1 wiring pitch (nm)	180	156	136	118	104	90	80	72	64
Metal 1 A/R (for Cu)	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9
Intermediate wiring dual damascene A/R (Cu wire/via)	1.7/1.5	1.7/1.6	1.8/1.6	1.8/1.6	1.8/1.6	1.8/1.6	1.8/1.6	1.9/1.7	1.9/1.7
Conductor effective resistivity ($\mu\Omega$–cm) Cu wiring, assumes no scattering	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Interlevel metal insulator – effective dielectric constant (κ)	3.1–3.4	3.1–3.4	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.1–2.4	2.1–2.4
J_{max} (A/cm^2) – intermediate wire (at 105°C)	8.91E+05	1.37E+06	2.08E+06	3.08E+06	3.88E+06	5.15E+06	6.18E+06	6.46E+06	8.08E+06

ITRS 2006

➢ **Circuit feature size continuously decreases, and current density increases**
➢ **The number and length of internal connections increase rapidly (with chip size)**
➢ **The number of metal levels and the metal aspect ratio (AR) increase**

Interconnect Delay

(Plummer p 685)

Line resistance, interconnect coupling and substrate coupling all contribute to an RC delay

$$\tau_L = 0.89\varepsilon \; \rho \frac{A}{(F_{min})^2}$$
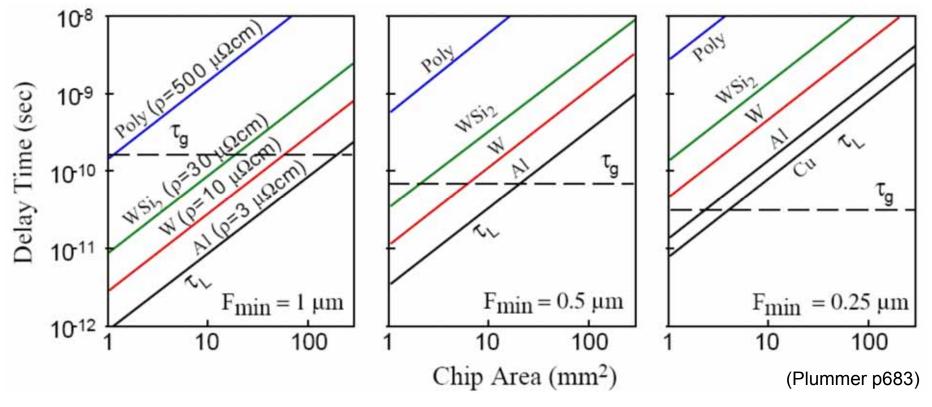
where A = chip area, F_{min} = minimum feature size, ρ = interconnect resitivity and ε = dielectric constant

0.18 μm CMOS: 30-40% of delay due to interconnects!
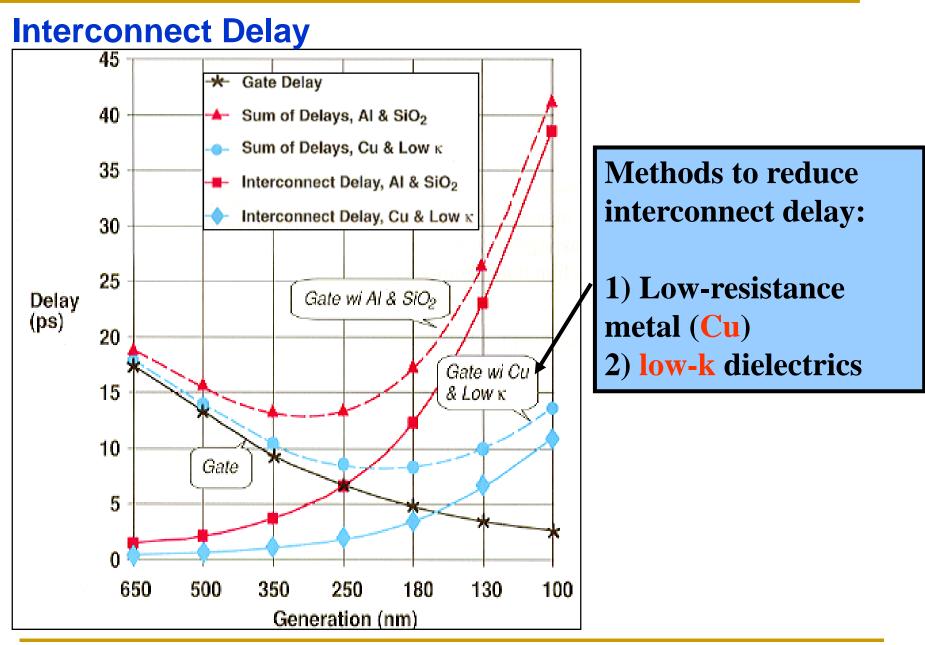
Interconnect Delay

**Interconnect and gate delay time versus chip area.**

(Plummer p683)

τ_g: gate delay in CMOS ring oscillator

Interconnect RC crisis partly postponed by increased dimensions and spacing of the highest level of interconnects ("fat wiring")

Interconnect Delay

Methods to reduce interconnect delay:

1) **Low-resistance metal (Cu)**
2) **low-k dielectrics**
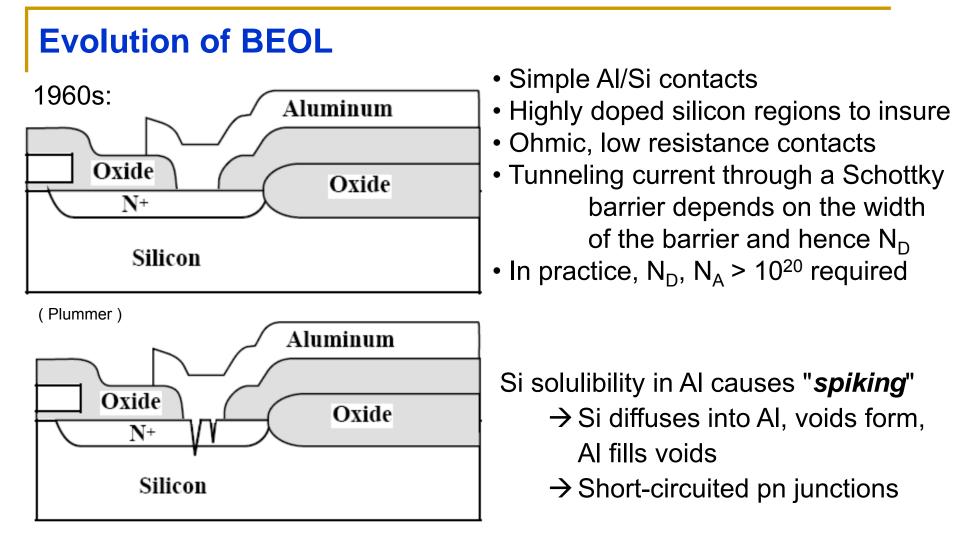
Requirements in IC Metallization

Electronics, Mechanics, Thermodynamics and Chemistry

1) Low-resistance metal-semiconductor contacts
2) Low-resistance interconnects
3) Good adhesion with underneath oxide (dielectric) layers
4) Good step coverage
5) Stable structure, no electromigration or corrosion
6) Easy to etch
7) Simple fabrication process

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Evolution of BEOL

1960s:

(Plummer)

- Simple Al/Si contacts
- Highly doped silicon regions to insure
- Ohmic, low resistance contacts
- Tunneling current through a Schottky barrier depends on the width of the barrier and hence N_D
- In practice, N_D, $N_A > 10^{20}$ required

Si solulibility in Al causes "*spiking*"
  → Si diffuses into Al, voids form, Al fills voids
  → Short-circuited pn junctions

Solution: Add 1-2% Si in Al to satisfy solubility
- Widely used, but Si can precipitate when cooling down and increase ρ_c

Contact Resistivity

Metal-Si contact must be ohmic,
i.e. a tunneling contact

Low contact resistance $R_C = \rho_c/A_c$ where ρ_c is
contact resistivity [Ωcm^2] and A_c contact area
High doping in Si required (>6x1019 cm-3)

Aluminum:
• Low resistivity ρ~2.7 $\mu\Omega cm$
• Low contact resistivity ρ_C~1-10 $\mu\Omega cm^2$ since Al
reduces native oxide on Si
• Excellent adhesion

Avoid degradation during subsequent processing:
Al-Si system: Eutectic temperature of 577°C
Forming gas anneal (FGA) or post-metal anneal
("alloying") at ~450°C
Barrier layers, e.g. TiN, TiW or silicides
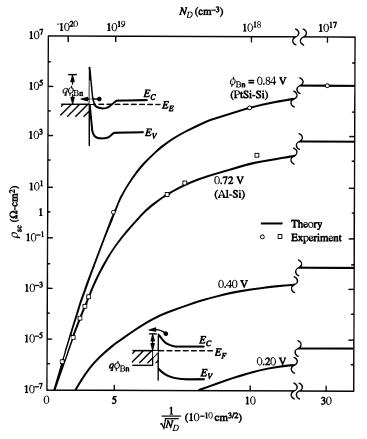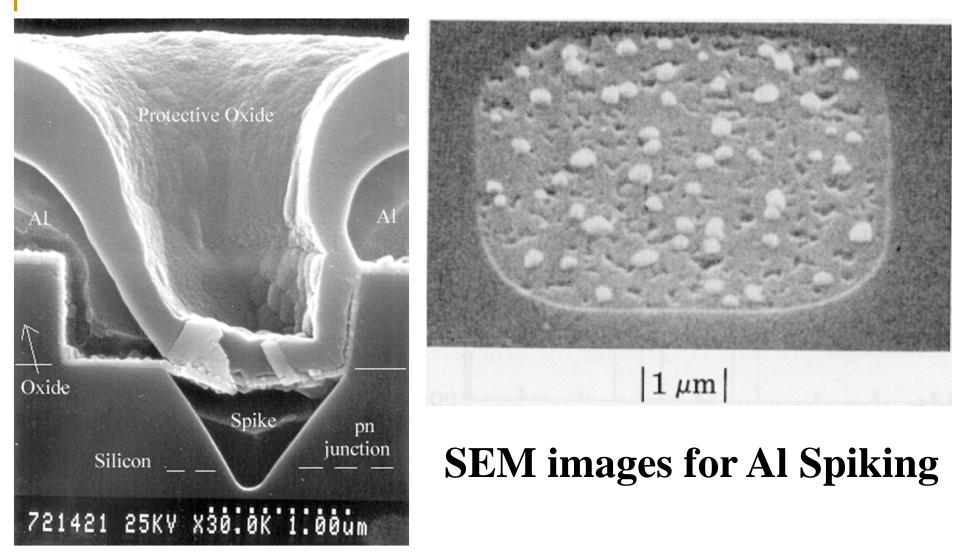
FIGURE 4
Specific contact resistance to Si. (*From Ref. 2 with permission.*)

(Sze p 376)
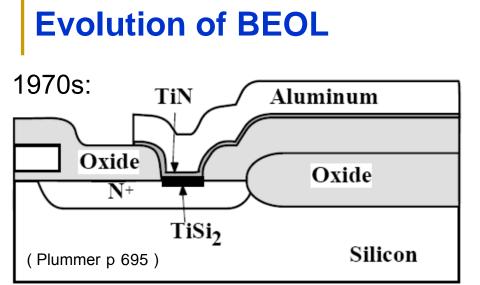
Evolution of BEOL: Spiking

SEM images for Al Spiking

Alloying

➢ **Alloying is to form low-resistance Ohmic contact between metal and Si and improve the adhesion between metal and SiO$_2$.**

➢ **Above 300 ^{o}C, Si can dissolve in Al by a certain percentage. Keeping such temperature for enough time may form a very thin layer of Al-Si alloy at the Al/Si interface. Al contacts the underneath heavily-doped semiconductor through this Al-Si alloy, resulting in Ohmic contact.**

➢ **Alloying temperature for Al-Si system is usually 450-500 ˚C.**

Evolution of BEOL

1970s:

(Plummer p 695)

Spiking can be up to 2μm
$\rightarrow$ Barrier layer(s)

- Ti or TiSi$_2$ for good contact and adhesion
- TiN for barrier (See Table 11.3 in text for various barrier options.)

Aluminum has been the dominant material for interconnects
- low resistivity
- adheres well to Si and SiO$_2$
- can reduce other oxides (= ohmic contacts)
- can be etched and deposited easily
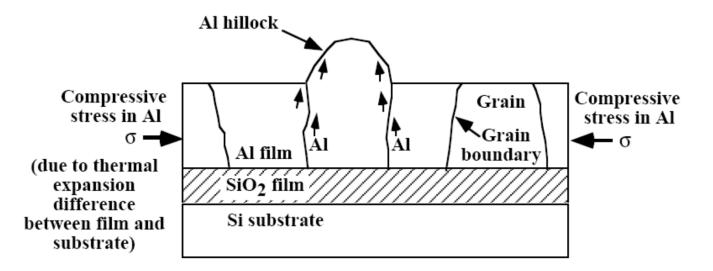
Problems:
- relatively low melting point and soft $\rightarrow$ need a higher melting point material for gate electrode and local interconnect $\rightarrow$ polysilicon
- hillocks and voids easily formed in Al

Evolution of BEOL: Hillocks and Voids

Compressive stress in Al during thermal cycling

Al grains pushed up forming hillocks and/or voids
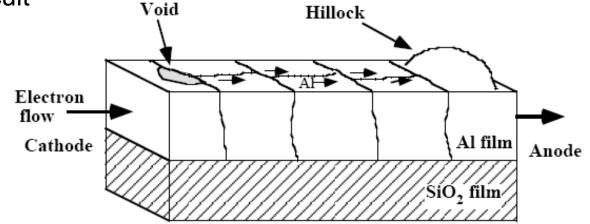
Depends much upon grain structure of Al connectors

Adding a few % Cu stabilizes grain boundaries and minimizes hillock formation

Evolution of BEOL: Electromigration

Broken interconnects occur at high current densities
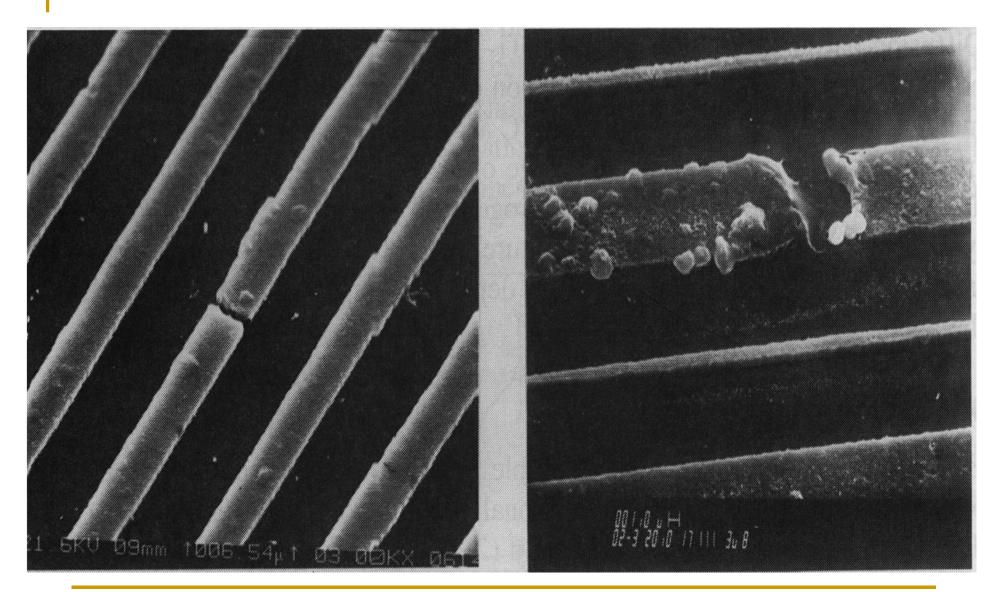
- Caused by "electromigration"
- High current density (0.1-0.5 MA/cm^2) causes diffusion of Al atoms in direction of electron flow by momentum transfer (e$^-$ $\rightarrow$ Al)
- Can cause hillocks and voids, leading to shorts or opens in the circuit

Adding Cu (0.5-4 weight %) can also inhibit electromigration

$\rightarrow$ Al is commonly deposited with 1-2 wt % Si and 0.5-4 wt % Cu

$\rightarrow$ Reliability tests ("accelerated" tests at high J_c and T_{op})

Evolution of BEOL: Electromigration
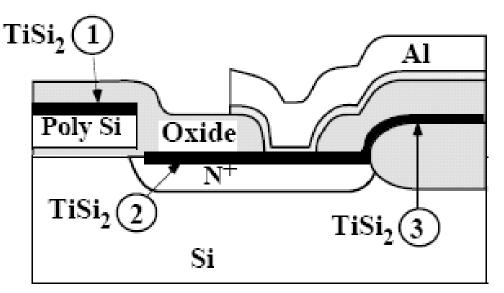
Evolution of BEOL: Silicides

Next development:

Use of other materials with lower resistivity as local interconnects, like TiN and *silicides*

Silicides used to

1. Strap polysilicon
2. Strap junctions
3. As a local interconnect

Evolution of BEOL: Silicides

Silicide must be thermally stable, exhibit low resistance and allow thin pn-junctions
(~500 Å between silicide and pn junctions)

Most common in production: $TiSi_2$:
Two RTP steps at 700°C and 800°C:
(1) $Ti + 2Si \rightarrow TiSi_2$ (C-49)   60-70 $\mu\Omega$cm
(2) $TiSi_2$(C-49) $\rightarrow TiSi_2$ (C-54)   15-20 $\mu\Omega$cm

Problem to perform C-49 transformation on thin poly-lines!

Cobalt disilicide for 0.18 µm CMOS:
$Co + Si \rightarrow CoSi$ (450 °C)
$CoSi + Si \rightarrow CoSi_2$ (700 °C)
For 0.1 μm:

Other silicides in production: MoSi2, TaSi2, WSi2, (PtSi)
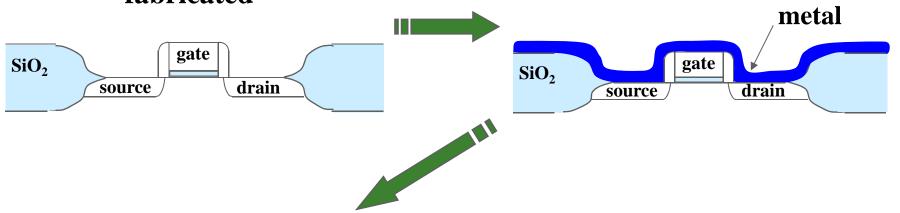
Maybe NiSi is used provided thermal stability can be solved
Minor Si consumption $\rightarrow$ Ni dominant moving species

Silicide Integration

Polycide = polysilicon-silicide
Salicide = Selfaligned silicide (shown here)
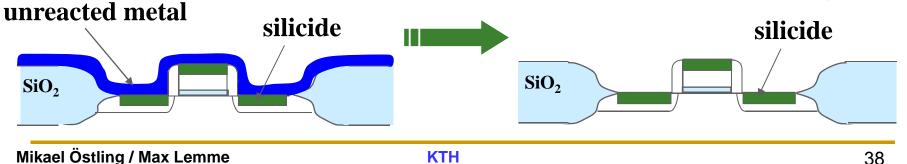
(a) Basic MOSFET structure fabricated

(b) Metal deposition

metal

SiO$_2$ gate   source   drain

SiO$_2$ gate   source   drain

(c) 1st anneal in N$_2$ at 300-700 ° C

unreacted metal   silicide

SiO$_2$

(d) Selective removal of unreacted metal + 2nd anneal at 500-850 ºC

silicide

SiO$_2$

Silicide Integration

Bridging problem in salicide

- Si atoms moves to form $TiSi_2$
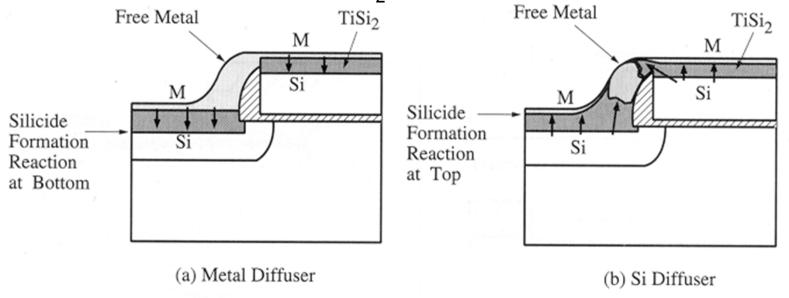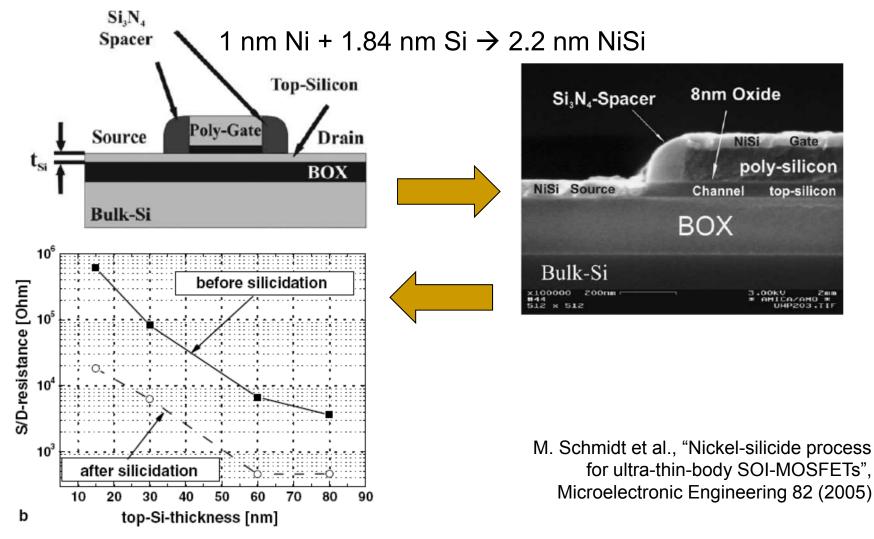
Figure 11-15 Schematic illustration of silicide formation for a silicide that forms by (a) diffusion of metal species and by (b) diffusion of silicon. In the latter case, lateral encroachment of the silicide over the oxide spacer can occur.

(Plummer p 702)

Remedy: Use N_2 during RTA $\rightarrow$ TiN formation suppresses bridging
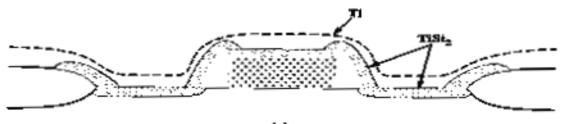
Silicide Integration
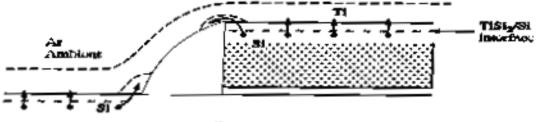
Example: Salicide process for Ultra-Thin-Body (UTB) SOI MOSFETs

1 nm Ni + 1.84 nm Si → 2.2 nm NiSi

M. Schmidt et al., "Nickel-silicide process for ultra-thin-body SOI-MOSFETs", Microelectronic Engineering 82 (2005)

Remedy: Use N_2 during RTA,. TiN formation suppresses bridging
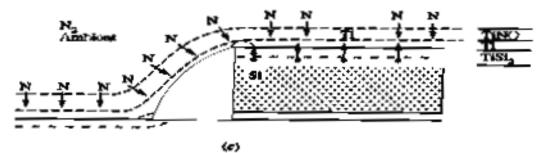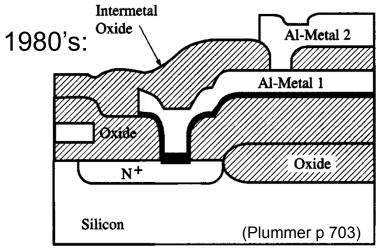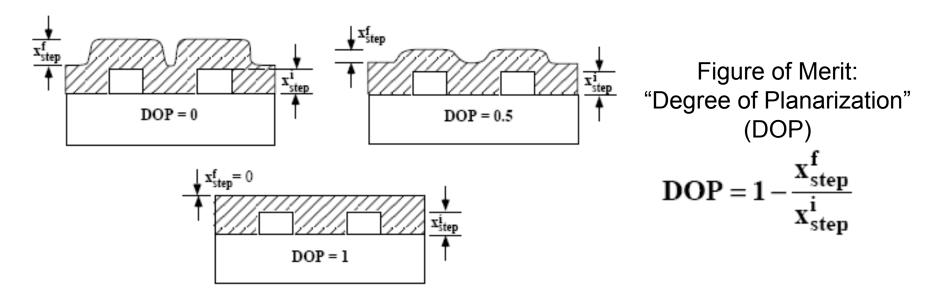
FIGURE 13
"Bridging" during the formation of Ti silicide: (a) TiSi₂ bridges over sidewall spacer and a short circuit is formed between S/G and D/G; (b) during TiSi₂ formation, Si diffuses into Ti to form TiSi₂; under favorable conditions Si can diffuse a long distance and form TiSi₂ on the sidewall spacer; (c) in a nitrogen atmosphere, nitrogen diffuses into Ti and blocks the diffusion of Si, reducing or eliminating bridging; TiN and/or Ti-O-N are formed on top of TiSi₂.

Evolution of BEOL

1980's:

Intermetal Oxide

Al-Metal 2

Al-Metal 1

Oxide

Oxide

N+

Silicon

(Plummer p 703)
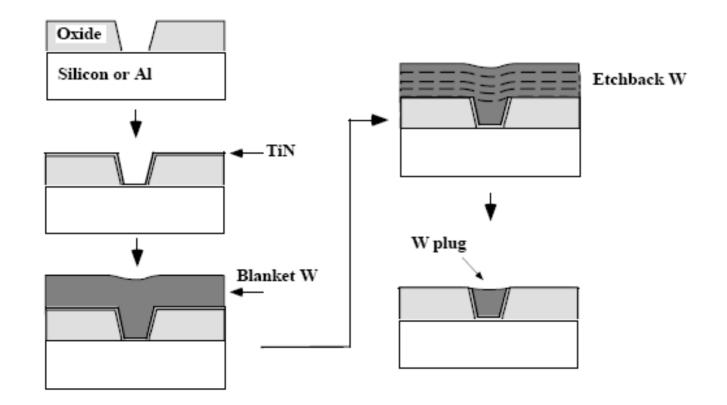
Early two-level metal structure
Nonplanar topography leads to
lithography, deposition, filling issues.
These issues get worse with additional
levels of interconnect
→Further change in structure
→Planarization!

x^f_{step}

x^i_{step}

DOP = 0

x^f_{step}

x^i_{step}

DOP = 0.5

$x^f_{step} = 0$

x^i_{step}

DOP = 1

Figure of Merit:
"Degree of Planarization"
(DOP)

$$DOP = 1 - \frac{x^f_{step}}{x^i_{step}}$$
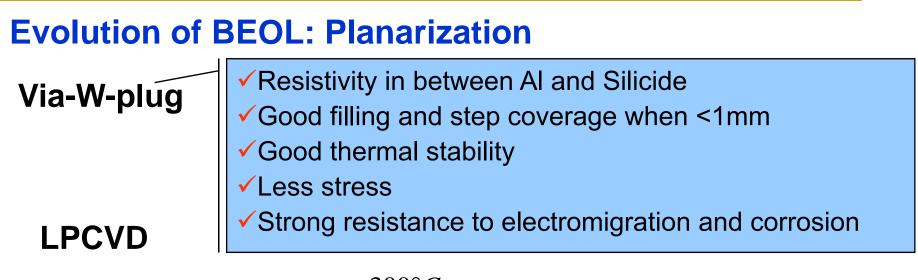
Evolution of BEOL: Planarization

Damascene Process

- Early approach to planarization incorporated tungsten (W) plugs and a simple etchback process

Evolution of BEOL: Planarization

Via-W-plug

> ✓Resistivity in between Al and Silicide
> ✓Good filling and step coverage when <1mm
> ✓Good thermal stability
> ✓Less stress
> ✓Strong resistance to electromigration and corrosion

LPCVD

$$2WF_6(g) + 3SiH_4(g) \xrightarrow{300°C} 2W(g) + 3SiF_4(g) + 6H_2(g)$$
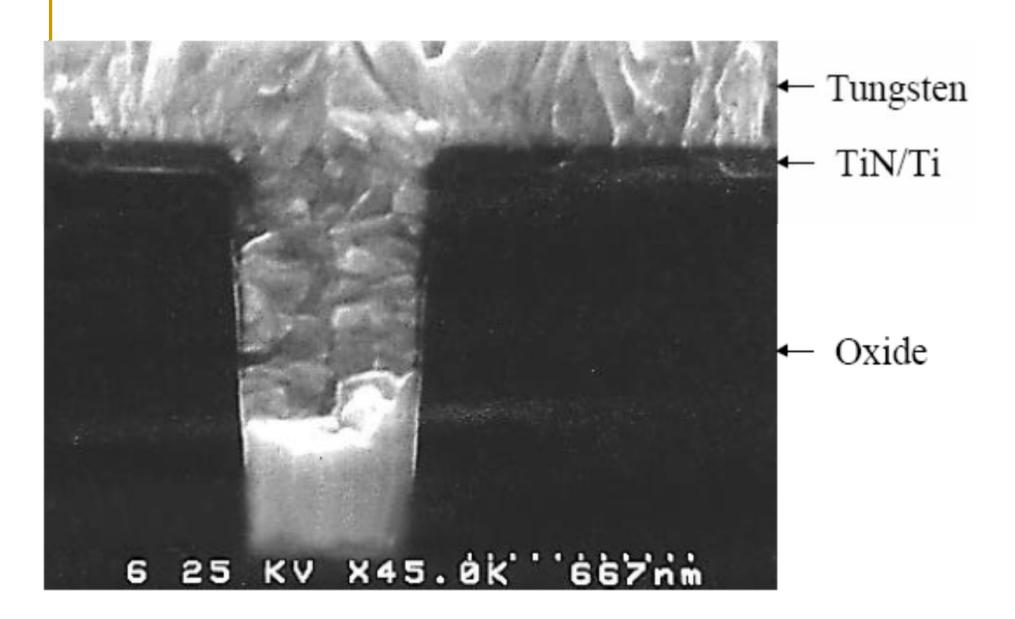
$$WF_6(g) + 3H_2(g) \xrightarrow{<450°C} W(g) + 6HF(g)$$
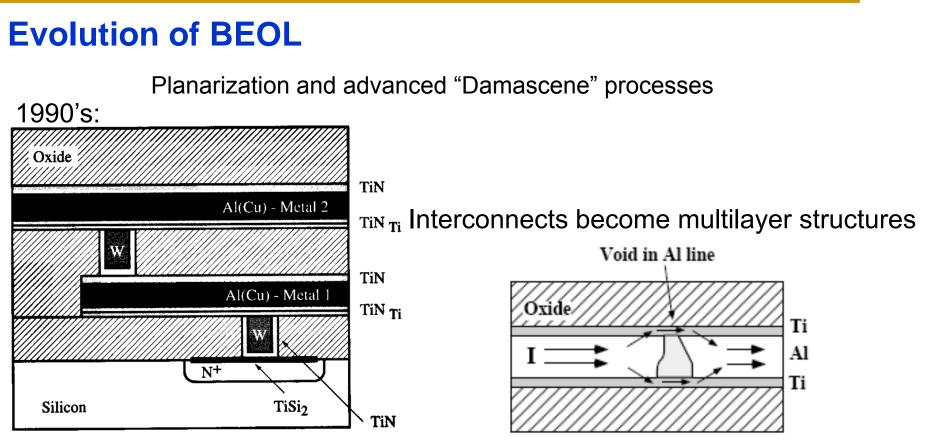
W/TiN/Ti/Si   W does not adhere well to SiO_2. TiN is needed as adhesion layer. To reduce contact resistance, Ti is added as contact layer for Si and TiN

Two-Step W-stud Filling: Silane for low-pressure nuclear growth + H_2 for complete and fast filling

Evolution of BEOL

Planarization and advanced "Damascene" processes

1990's:

Interconnects become multilayer structures

(Plummer p. 707)

- Shunting the Al helps mitigate electromigration and can provide mechanical strength, better adhesion and barriers in multi-level structures
- TiN on top also acts as antireflection coating for lithography

Summary: Properties of Interconnect Materials

Material	Thin film resistivity ($\mu\Omega$cm)	Melting point (^{o}C)
Al	2.7-3.0	660
W	8-15	3410
Cu	1.7-2.0	1084
Ti	40-70	1670
PtSi	28-35	1229
C54 TiSi$_2$	13-16	1540
WSi$_2$	30-70	2165
CoSi$_2$	15-20	1326
NiSi	12-20	992
TiN	50-150	2950
Ti$_{30}$W$_{70}$	75-200	2200
Heavily doped poly-Si	450-10000	1417

Concept Test 10.2

9.2: We have discussed several metallization technologies. Which of the following statements are true?

A. Sputtering uses a plasma to ionize a gas which contains the material to be deposited.

B. Evaporation of compounds (i.e. two or more materials mixed together) is not ideal because compounds typically have a high melting point.

C. CVD is used for dielectrics, but not for metallization.

D. Evaporation is more directional than CVD and CVD is more directional than sputtering.

E. None of the above.

Lecture 9: Metallization and BEOL

- # Metallization Technology
  - ## Evaporation
  - ## Sputtering

- # Back End Of the Line (BEOL)
  - ## ITRS Requirements
  - ## Evolution of Metallization
  - ## Dielectrics
  - ## Integration

- # Future Options

BEOL: Dielectrics

SiO$_2$ CVD (SiH$_4$ Source), PECVD SiO$_2$ (TEOS), SOG…

…but: SiO2 only a starting point ➡ $\tau_L = 0.89\varepsilon\ \rho\dfrac{A}{(F_{min})^2}$

Low-k dielectric material must meet many requirements:
- ✓Sufficient mechanical strength to support multi-interconnects
- ✓High Young's modulus
- ✓High breakdown voltage (> 4 MV / cm)
- ✓Low-leakage (<10^{-9} A/cm^2 at 1 MV / cm)
- ✓Thermal stability (> 450 ^{o}C)
- ✓Good adhesive strength
- ✓Low water absorption
- ✓Low film stress
- ✓Low thermal expansion
- ✓Easy for planarization
- ✓CMP compatibility
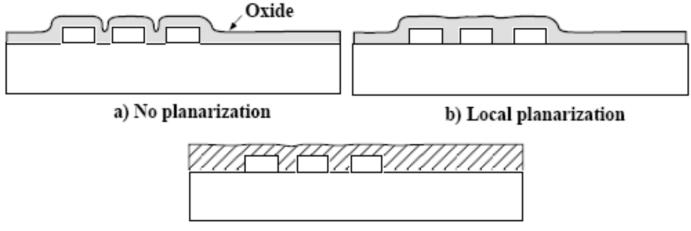
➡ **Low-k integration**

BEOL: Dielectrics

Global planarization required!

Past: Spin-on-glass (SOG)
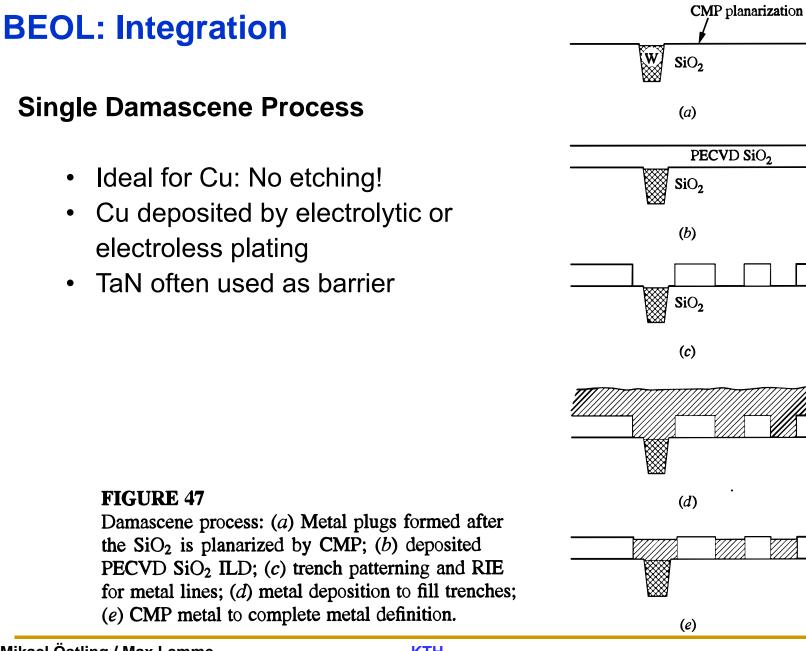
- Fills like liquid photoresist, but becomes SiO_2 after bake and cure
- Done with or without etchback
- Can also use low-K SOD's (spin-on-dielectrics)
- SOG oxides not as good quality as thermal or CVD oxides

Now: Chemical Mechanical Polishing (CMP)

BEOL: Dielectrics

Chemical Mechanical Polishing (CMP)

Both for inter metal dielectrics (IMDs) and metals (Al or Cu)

Plasma etch vs. CMP

Lecture 9: Metallization and BEOL

- # Metallization Technology
  - ## Evaporation
  - ## Sputtering

- # Back End Of the Line (BEOL)
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  - ## Integration

- # Future Options

BEOL: Integration

Single Damascene Process

- Ideal for Cu: No etching!
- Cu deposited by electrolytic or electroless plating
- TaN often used as barrier

FIGURE 47

Damascene process: (*a*) Metal plugs formed after the SiO_2 is planarized by CMP; (*b*) deposited PECVD SiO_2 ILD; (*c*) trench patterning and RIE for metal lines; (*d*) metal deposition to fill trenches; (*e*) CMP metal to complete metal definition.

BEOL: Integration
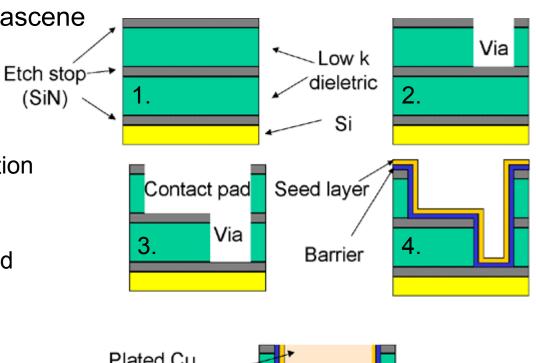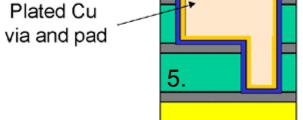
Dual damascene process

- Vias and global interconnects of same material
- Less complex than single damascene
- Etch stop needed in IMD

Process sequence:

1. Dielectric and etch stop deposition
2. Via definition by etch
3. Pad definition by etch
4. Barrier (e.g., tantalum) and seed copper (Cu) physical vapor deposition
5. Copper plating and chemical mechanical polishing (CMP)
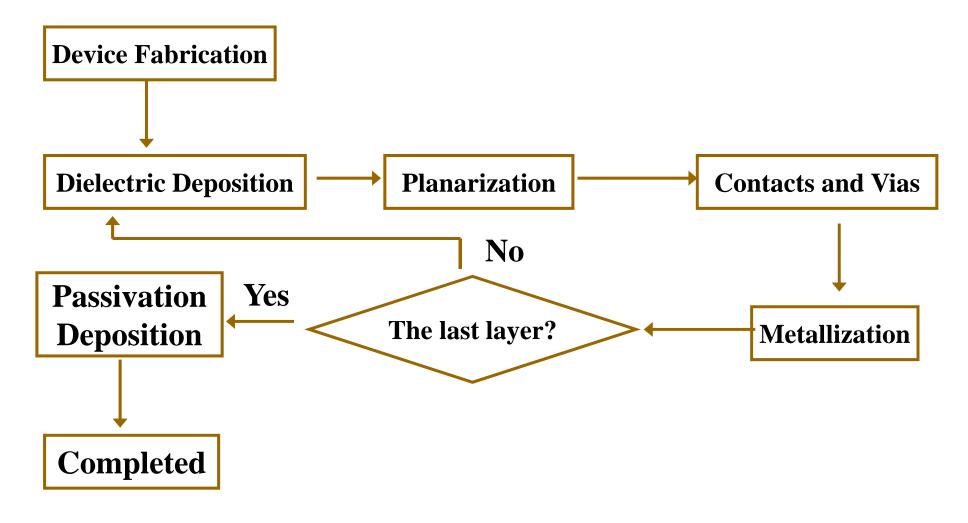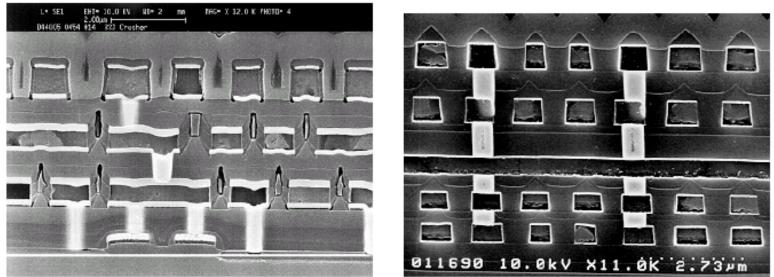
C.-K. Hu and J.M.E. Harper, *Mater. Chem. Phys.,* 52 (1998), p. 5

BEOL: Integration

Multilevel-Multilayer Metallization

```
┌──────────────────┐
│ Device Fabrication│
└──────────────────┘
         │
         ▼
┌──────────────────┐      ┌──────────────┐      ┌──────────────────┐
│Dielectric Deposition│──▶│ Planarization│──▶│ Contacts and Vias│
└──────────────────┘      └──────────────┘      └──────────────────┘
```

No

Yes

The last layer?

Passivation Deposition

Metallization

Completed

BEOL: Integration

Examples
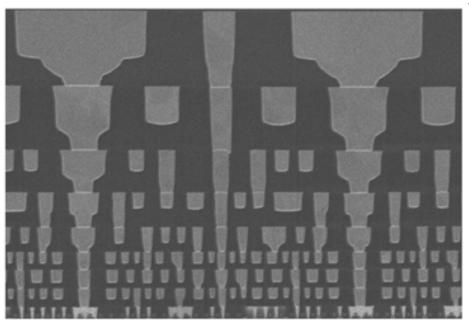
(Photos courtesy of VLSI Technology.)

Left: three metal levels and encapsulated BPSG for the first level dielectric; SOG (encapsulated top and bottom with PECVD oxide) and CMP in the intermetal dielectrics. The multilayer metal layers and W plugs are also clearly seen.

Right:five metal levels, HDP oxide (with PECVD oxide on top) and CMP in the intermetal dielectrics.

BEOL: Integration

Examples

SEM image of interconnect stack up to MT8
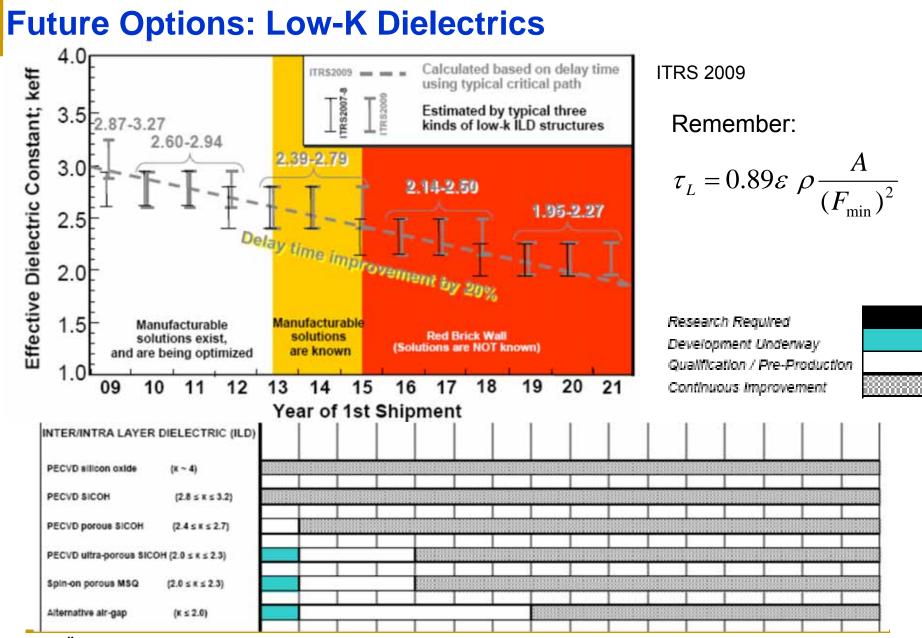
Layer	Dielectric Material	Pitch (nm)	Thick (nm)	Aspect Ratio
Metal 1	Low k	160	144	1.8
Metal 2	Low k	160	144	1.8
Metal 3	Low k	160	144	1.8
Metal 4	Low k	240	216	1.8
Metal 5	Low k	280	252	1.8
Metal 6	Low k	360	324	1.8
Metal 7	Low k	560	504	1.8
Metal 8	SiO_2	810	720	1.8
Metal 9	Polymer	30.5μm	7μm	0.4

P. Moon et al. "Intel's 45nm CMOS Technology", Intel Technology Journal, 12(02), 2008

Lecture 9: Metallization and BEOL
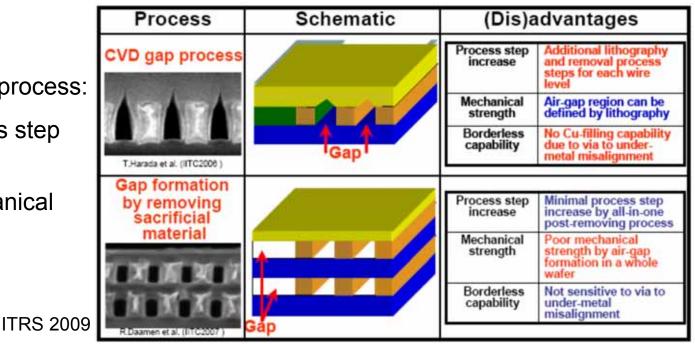
- # Metallization Technology
  - Evaporation
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  - Integration

- # Future Options

Future Options: Low-K Dielectrics

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Remember:

$$\tau_L = 0.89\varepsilon\ \rho\ \frac{A}{(F_{min})^2}$$

Future Options: Low-K Dielectrics

- Porous low-κ materials
  - Poor mechanical integrity
  - Substantial damage from plasma etching
  - Integration of porous low-κ materials with κ ≤ 2.0 extremely difficult
- Air gaps
  - Gradual transition from ultra low-κ materials to air-gaps considered
  - Hybrid of low-κ materials and air-gaps most realistic solution

Realistic air gap process:

• Minimal process step increase

• Maintain mechanical stability

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Future Options: Low-K Dielectrics

Material class	Material	Dielectric constant	Deposition technique
Inorganic	SiO_2 (including PSG and BPSG)	3.9-5.0	CVD/Thermal ox./Bias-sputtering/HDP
	Spin-on-glass (SiO_2) (including PSG, BPSG)	3.9-5.0	SOD
	Modified SiO_2 (e.g. fluorinated SiO_2 or hydrogen silsesquioxane - HSQ)	2.8-3.8	CVD/SOD
	BN (Si)	>2.9	CVD
	Si_3N_4 (only used in multilayer structure)	5.8-6.1	CVD
Organic	Polyimides	2.9-3.9	SOD/CVD
	Fluorinated polyimides	2.3-2.8	SOD/CVD
	Fluoro-polymers	1.8-2.2	SOD/CVD
	F-doped amorphous C	2.0-2.5	CVD
Inorganic/Organic Hybrids	Si-O-C hybrid polymers based on organo-silsesquioxanes (e.g. MSQ)	2.0-3.8	SOD
Aerogels (Microporous)	Porous SiO_2 (with tiny free space regions)	1.2-1.8	SOD
Air bridge		1.0-1.2	
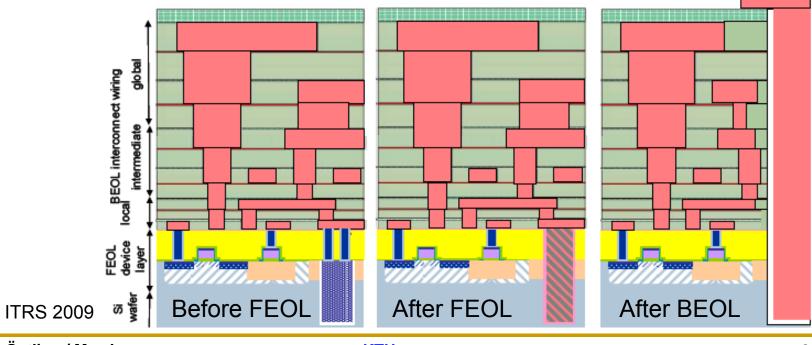
Future Options: Interconnects

Application	Option	Potential Advantages	Primary Concerns
Cu Extensions:	Airgaps	Lower latency and power, mature technology	Reliability, cost, integration issues
	3D	Form factor, heterogeneous integration, reduced power and latency	3D design tools and standards, reliability of TSVs, extreme thinning, high aspect ratio TSV, thermal heat extraction
	LC Transmission Lines	Mature technology, reduced power and latency for long lines	Limited bandwidth due to wide pitch
Cu Replacements:	Other metals (Ag, silicides, stacks)	Potential lower resistance in fine geometries	Grain boundary scattering, integration issues, reliability
	Nanowires	Ballistic conduction in narrow lines	Quantum contact resistance, controlled placement, low density, substrate interactions
	Carbon Nanotubes	Ballistic conduction in narrow lines, electromigration resistance	Quantum contact resistance, controlled placement, low density, chirality control, substrate interactions
	Graphene Nanoribbons	Ballistic conduction in narrow films, planar growth, electromigration resistance	Quantum contact resistance, control of edges, deposition and stacking, substrate interactions
	Optical (interchip)	High bandwidth, low power and latency, noise immunity	Connection and alignment between die and package, optical /electrical conversions
	Optical (intrachip)	Latency and power reduction for long lines, high bandwidth with WDM	Benefits only for long lines, need compact components, integration issues, need WDM
	Wireless	Available with current technology, parallel transport medium, high fan out capability	Very limited bandwidth, intra-die communication difficult, large area and power overhead
	Superconductors	Zero resistance interconnect, high Q passives	Cryogenic cooling, frequency dependent resistance, defects, low critical current density, inductive noise and crosstalk
Native Device Interconnects:	Nanowires	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, substrate interactions, fan out/branching and placement control
	Carbon Nanotubes	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, fan out/branching and placement control
	Graphene Nanoribbons	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, deposition and patterning processes.
	Spin Conductors- Si(Mn), Ga(Mn)As	Long diffusion length for spin excitons	Low T requirements, low speed, surface magnetic interactions

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Future Options: 3D-Through-Si-Via (TSV) Technology

- *Through Silicon Via (TSV)* connections
    - Galvanic connection between the two sides of a Si wafer
    - Electrically isolated from the substrate and from other TSV connections
- Isolation layer surrounding the TSV conductor is called the *TSV liner:*
    - Electrically isolate the TSVs from the substrate and from each other
    - This layer determines the TSV parasitic capacitance
- *Barrier layer* between the liner and the TSV metal:
    - Avoid diffusion of metal from the TSV into the Si-substrate

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Before FEOL   After FEOL   After BEOL

Summary of Key Ideas

• Backend processing (interconnects and dielectrics) have taken on increased importance in recent years.

• Interconnect delays now contribute a significant component to overall circuit performance in many applications.

• Early backend structures utilized simple Al to silicon contacts and are now replaced by advanced material stacks.

• Reliability issues, the need for many levels of interconnect and planarization issues have led to much more complex structures today involving multilayer metals and dielectrics.

• CMP is the most common planarization technique today.

• Copper and low-K dielectrics are now found in advanced chips and have become common features.

• Beyond these changes, interconnect options in the future include architectural (design) approaches to minimizing wire lengths, optical interconnects, carbon nanotubes, graphene, electrical repeaters and RF circuitry.