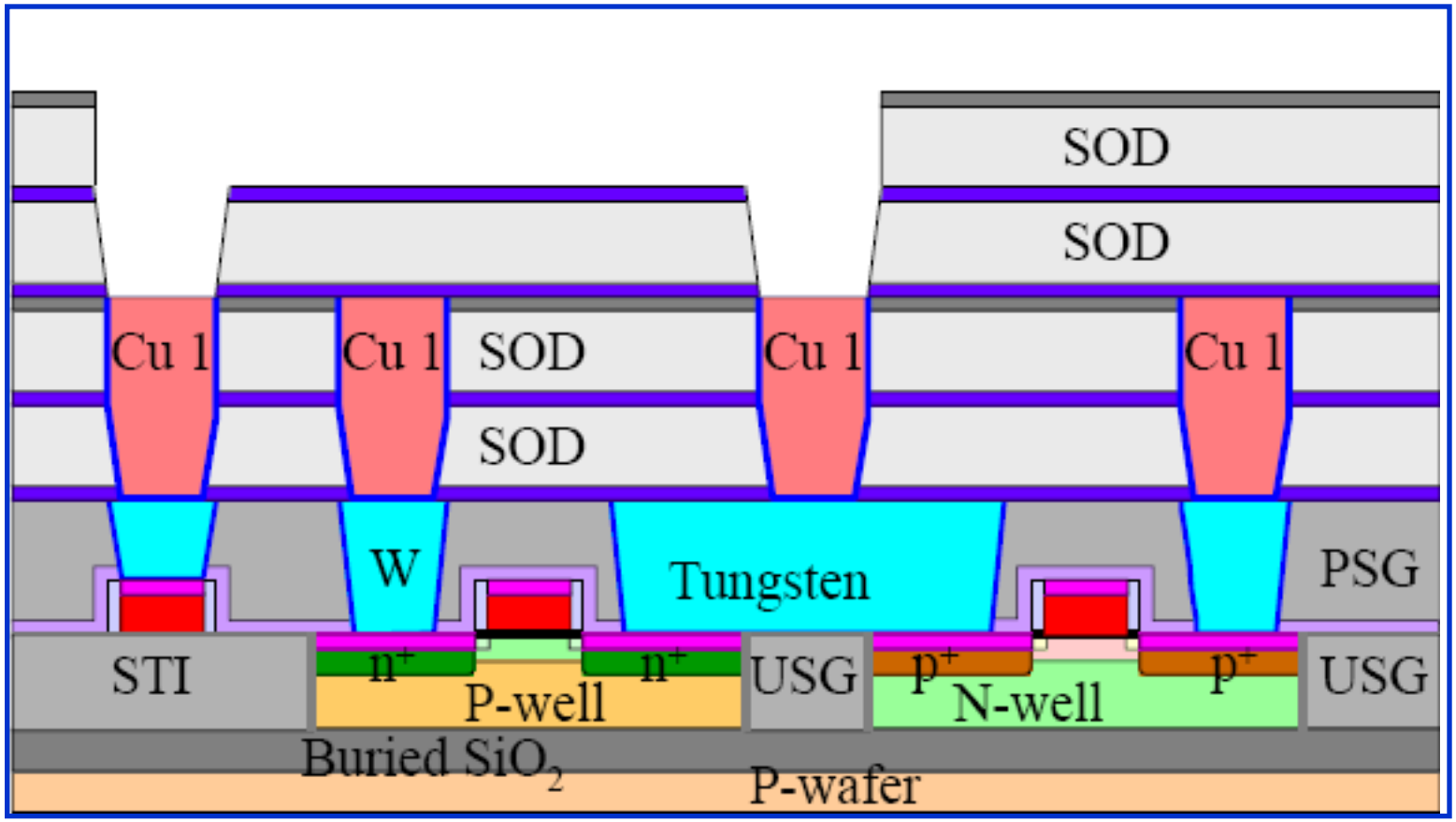
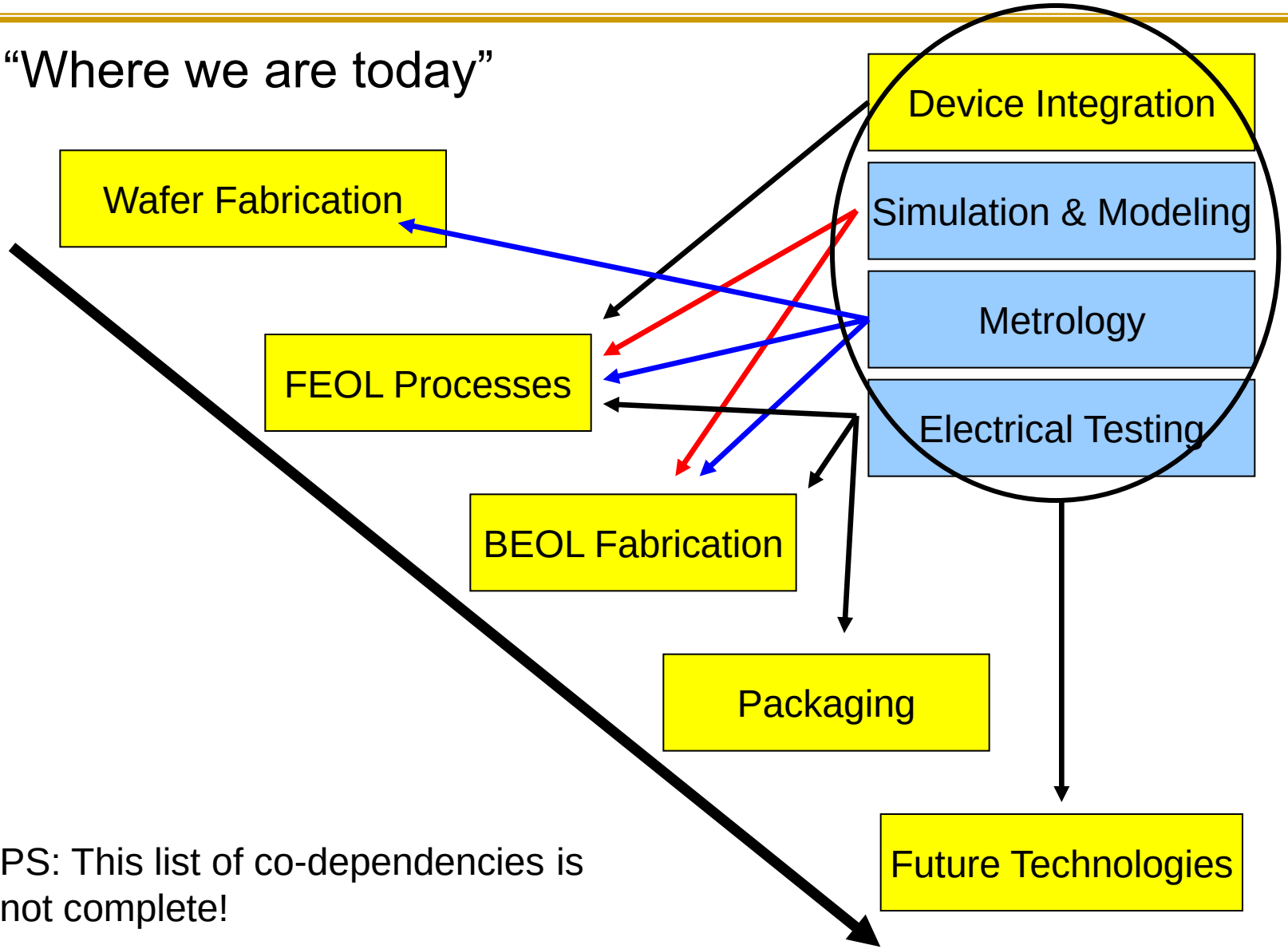
Lecture 11

Process Integration



Lecture 11: Process Integration

"Where we are today"



PS: This list of co-dependencies is not complete!

Process Integration: Overview

Pattern

- **Lithography**

Laser (Steppers), EUV, E-Beam, …

- **Thin Film deposition**

CVD – LPCVD, PECVD, ALD …
PVD – Sputtering (DC, RF, …), Evaporation (Resistance, E-Beam), …
Epitaxy – CVD, MBE, SPE
Spin-coating
Inkjet Printing

- **Etching**

Wet etching
Dry etching

- **Doping**

Ion implantation
Diffusion

- **Surface engineering**

Thermal oxidation
Metal silicide（SALICIDE）

Process Integration - Overview

- **Isolation Technology**
  - **LOCOS**
  - **STI**
- **Gate Stack Options**
- **Advanced CMOS Integration**

MOS-Basic Isolation in Ics

MOS transistors are self-isolated. Compared to bipolar devices, MOSFETs may have higher density, but they will suffer from parasitic effects from the adjacent devices.

✓High threshold voltage at the field region V_{TF} is preferred. V_{TF} must be 3-4 V higher (depending on CMOS generation) than the supply voltage to ensure that the current from parasitic MOSFET is less than 1 pA.

✓V_{TF} decreases with decreasing device distance or increasing temperature T. When T increases from 25 ^{o}C to 125 ^{o}C, V_{TF} will decrease by 2 V.

$$V_T = V_{FB} + 2\phi_{MS} + \frac{\sqrt{2\varepsilon_S q N_A (2\phi_{MS})}}{C_{ox}}$$

Methods to Increase Field Threshold Voltage V_{TF}

- **Increase field oxide to be 7~10 times thicker than gate oxide**
- **Increase the doping concentration under field oxide (Channel-stop implantation)**

LOCOS Isolation Technology

Wafer clean

Grow pad oxide (40nm)

LPCVD nitride (a) (80nm)

Mask 1, LOCOS

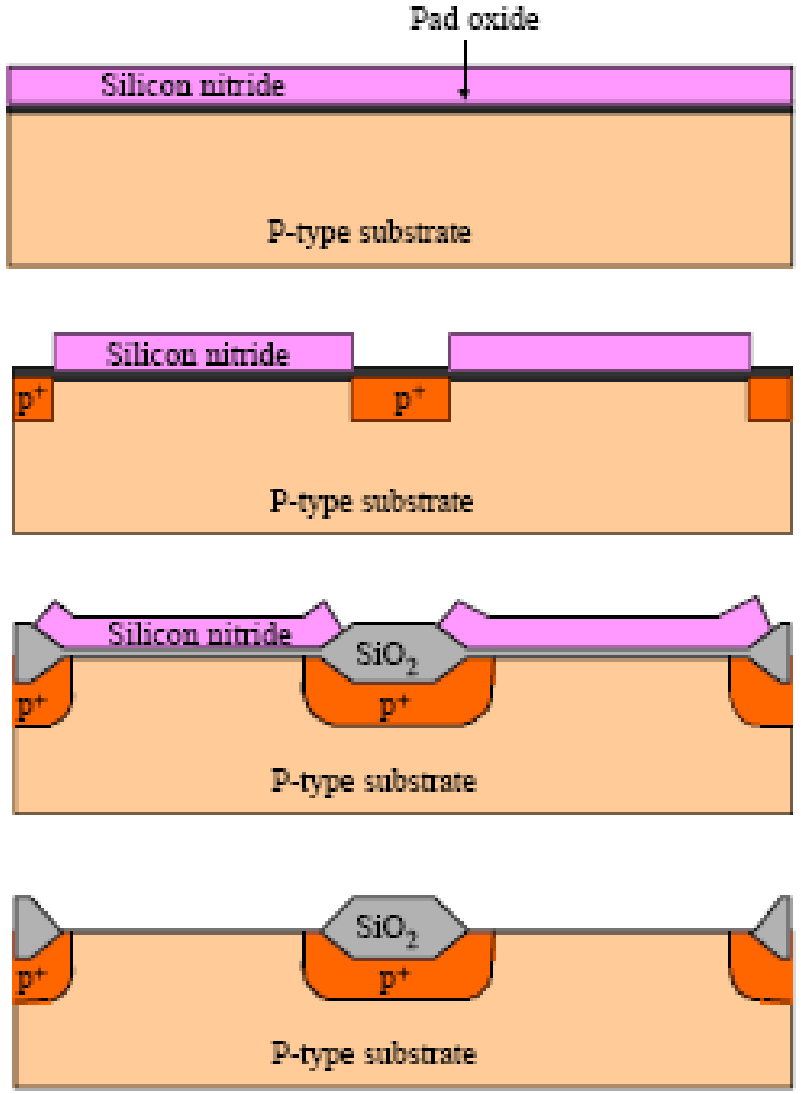
Etch nitride

Strip photoresist

Isolation implantation, boron (b)
50 keV , 1×10^{13} cm^{-2}

Wet oxidation, LOCOS formation (c)

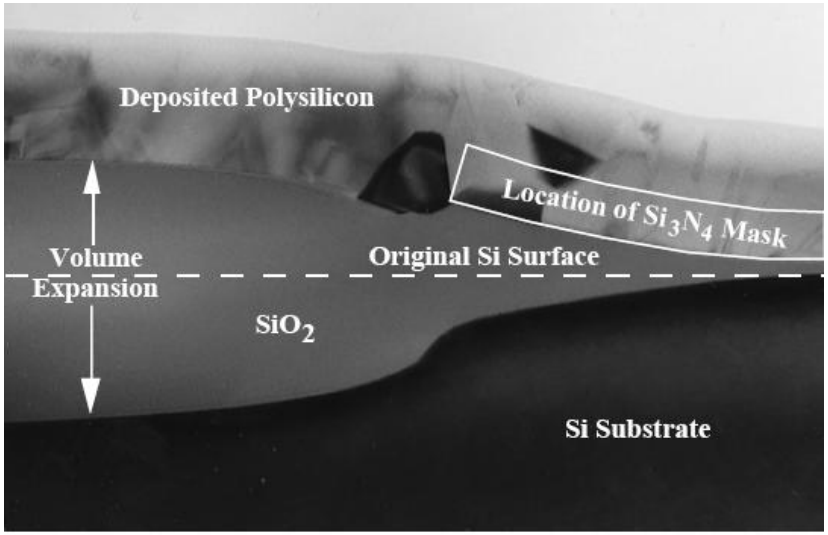
Strip nitride and pad oxide (d)



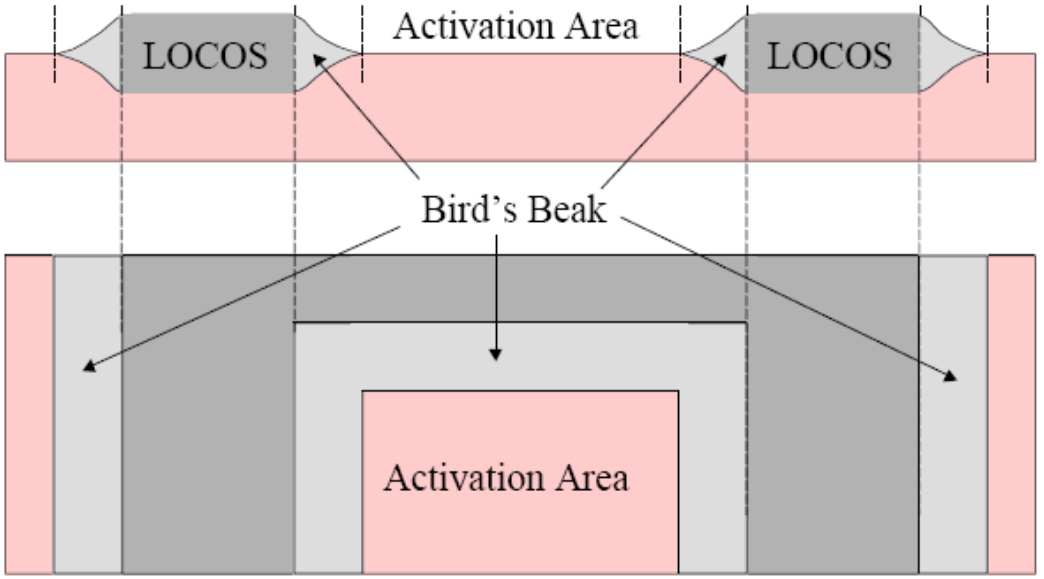
Problems in LOCOS Technology

1) Bird's Beak Effect
— limits integration improvement

2) Rough Surface
— limits Lithography (DOF)

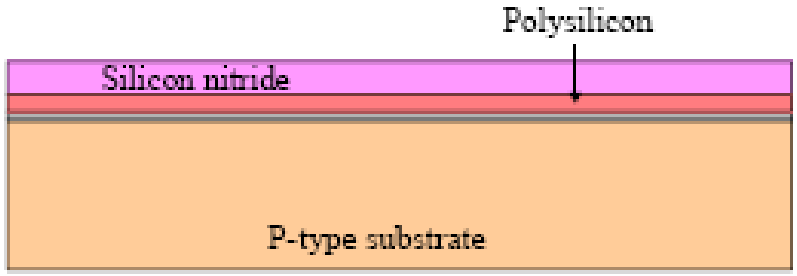


(Photo courtesy of J. Bravman.)

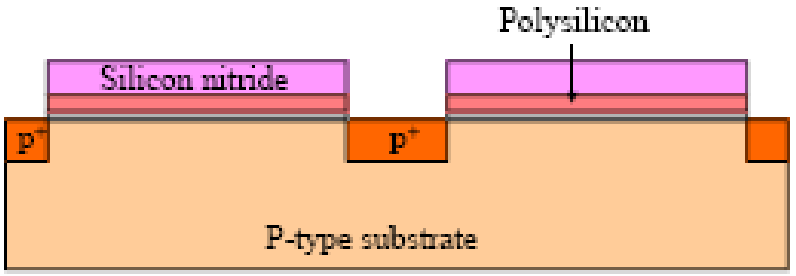


Improved LOCOS — PBL (Poly-Buffered LOCOS)

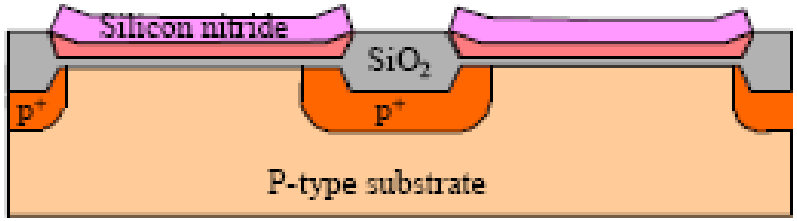
Deposit a layer of polysilicon before LPCVD Si_3N_4. Polysilicon consumes the oxygen diffused laterally during field oxidation. The bird's beak can reduce to 0.1-0.2 μm.



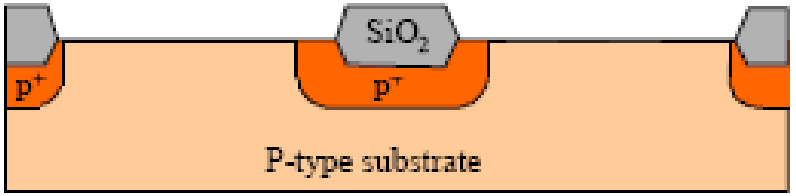
Pad oxidation, poly and nitride LPCVD



Nitride, poly, and oxide etch, B implantation

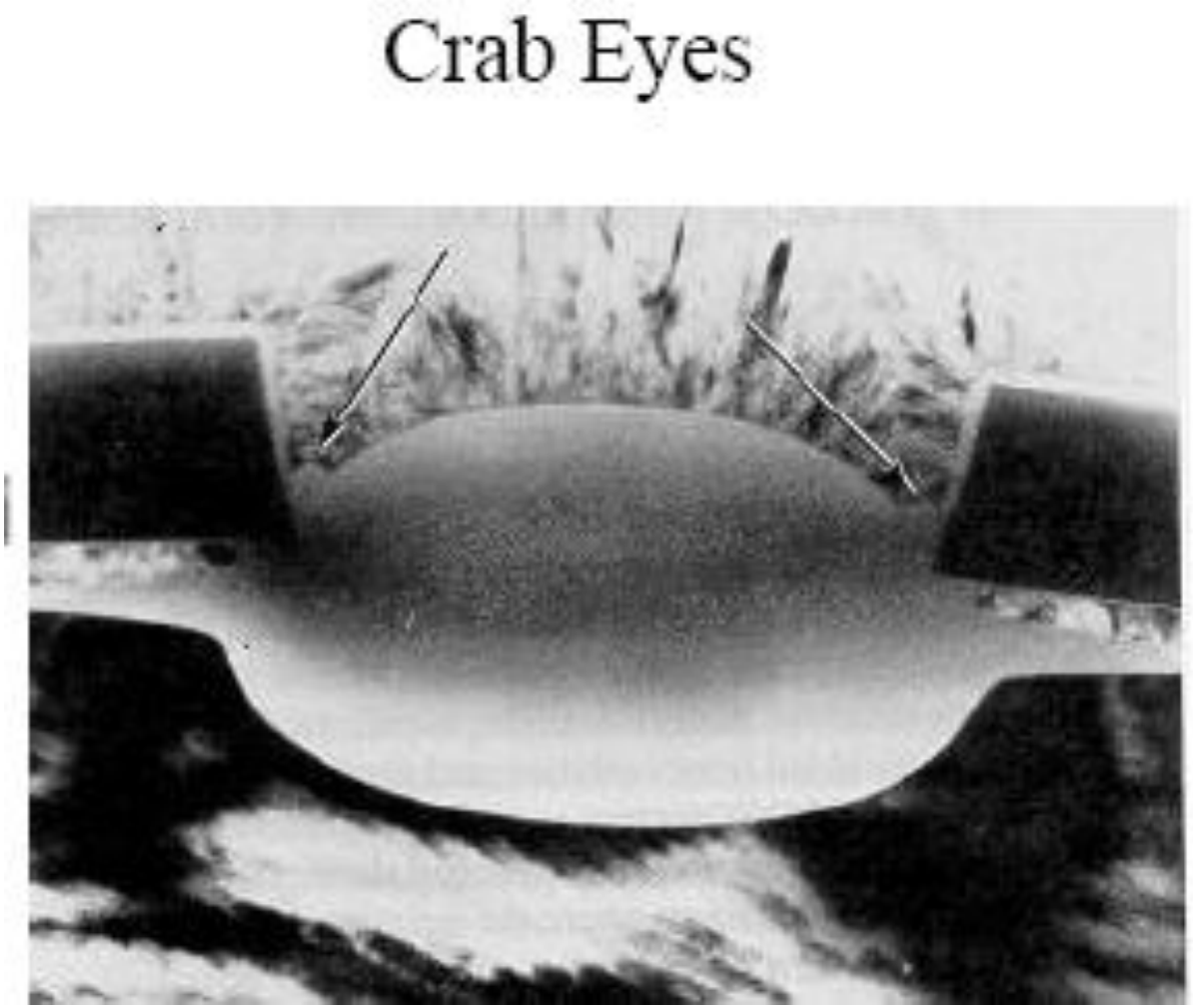


Oxidation



Strip pad oxidation, poly and nitride

Improved LOCOS — PBL (Poly-Buffered LOCOS)

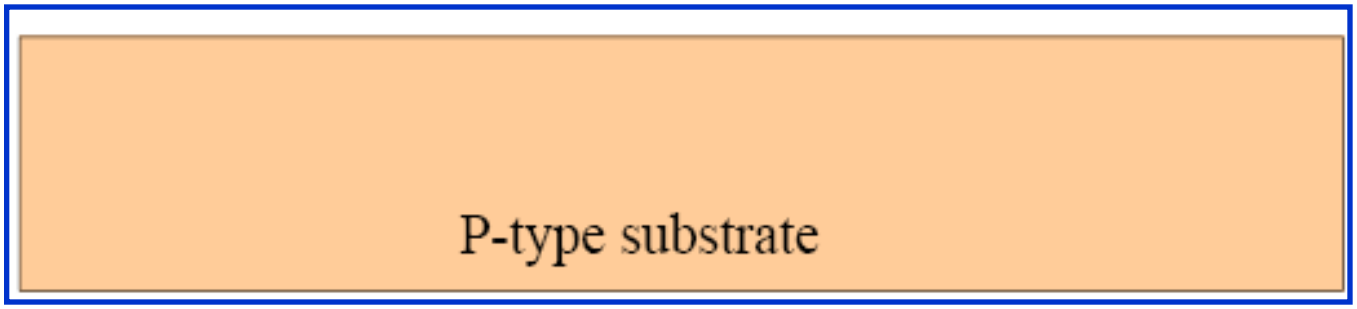


Helpful to integration improvement

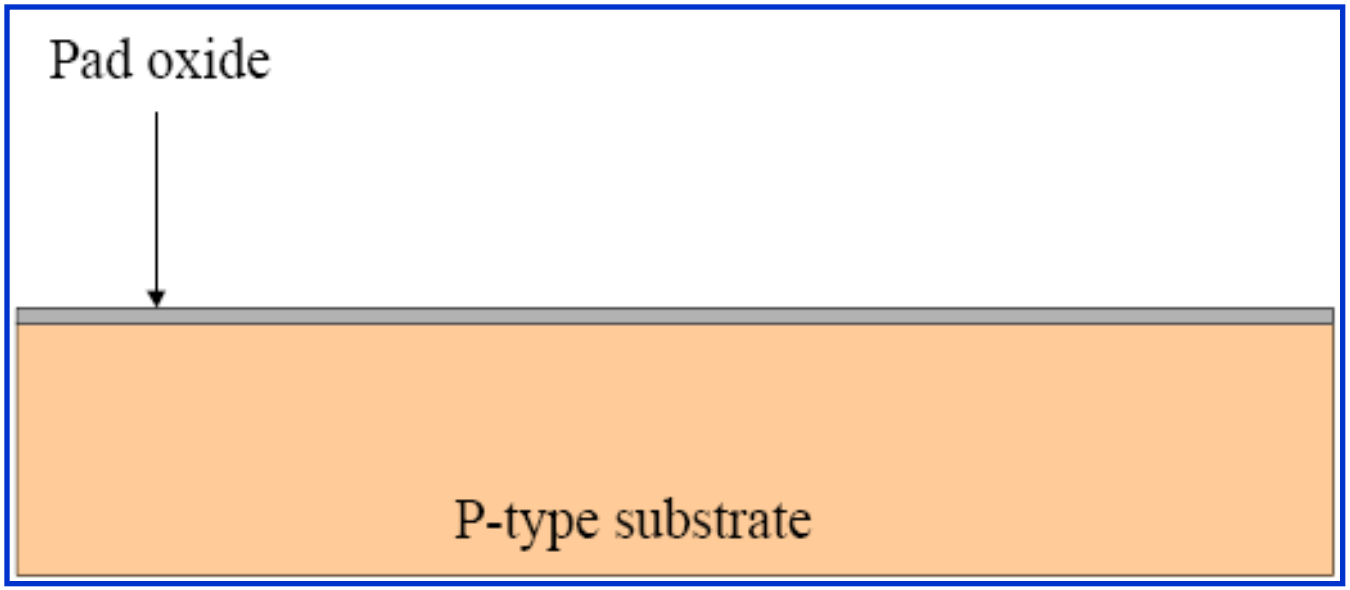
Shallow Trench Isolation (STI) 1/5

LOCOS, PBL applicable for technology node≥0.35-0.5 mm.
For technology node <0.35 mm, STI must be used.

1) Wafer Cleaning

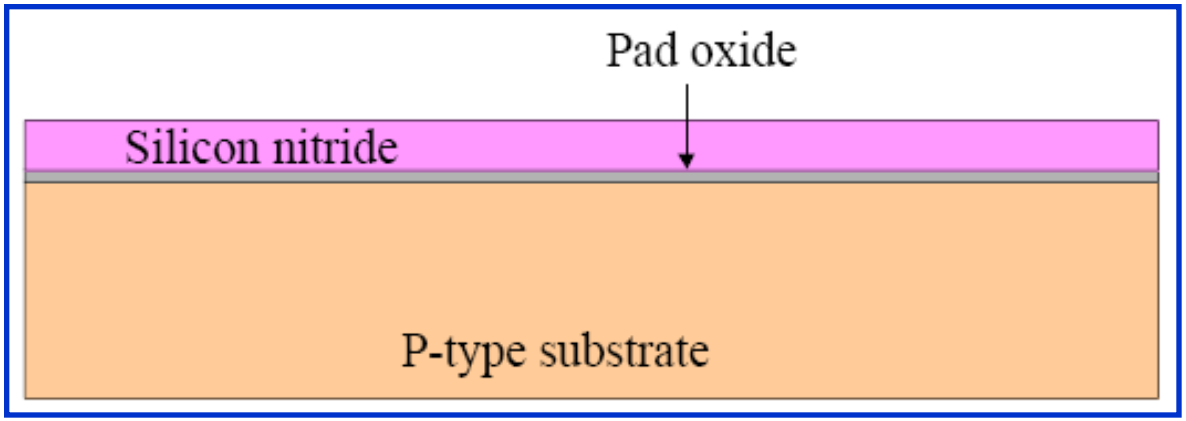


2) Substrate Oxidation (20 nm)

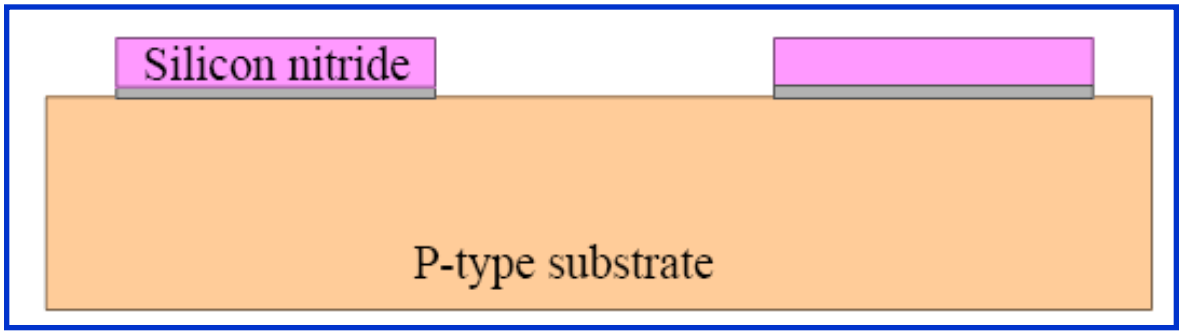


Shallow Trench Isolation (STI) 2/5

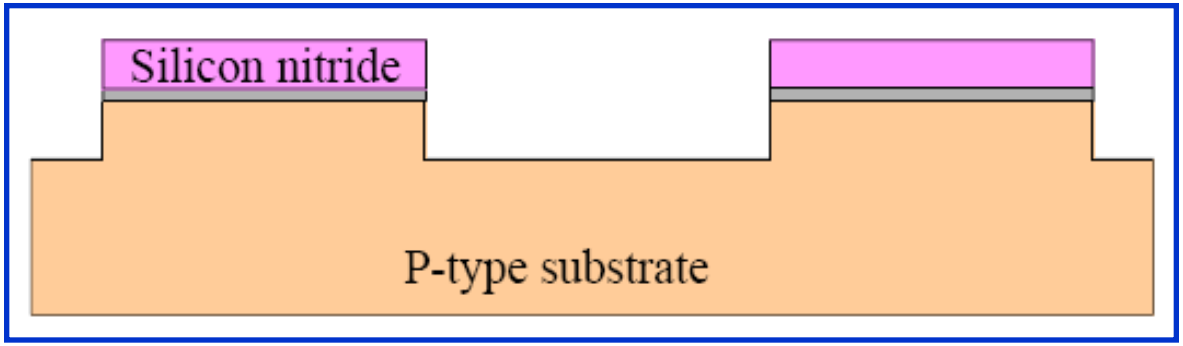
3) LPCVD Si_3N_4 (100 nm)



4) Isolation Lithography

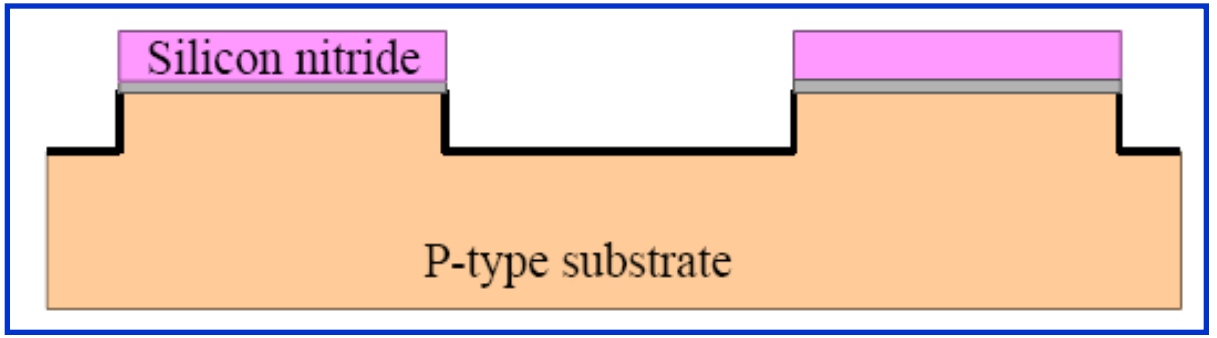


5) Shallow Trench Etching (0.5 mm)

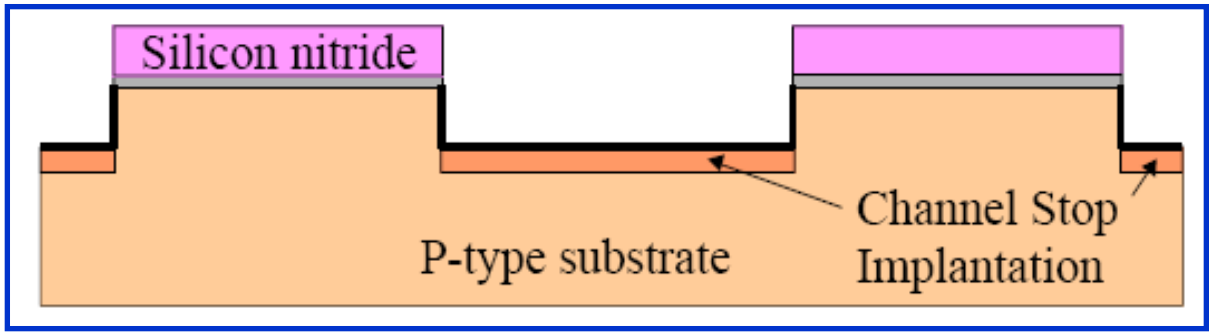


Shallow Trench Isolation (STI) 3/5

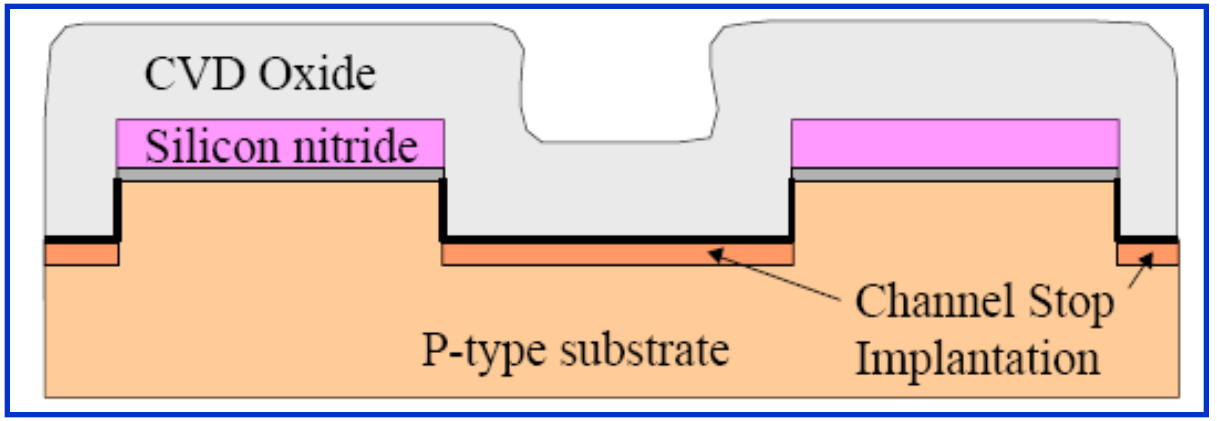
6) Thermal Growth of Oxide Stop (20 nm)



7) Channel Stop Implantation

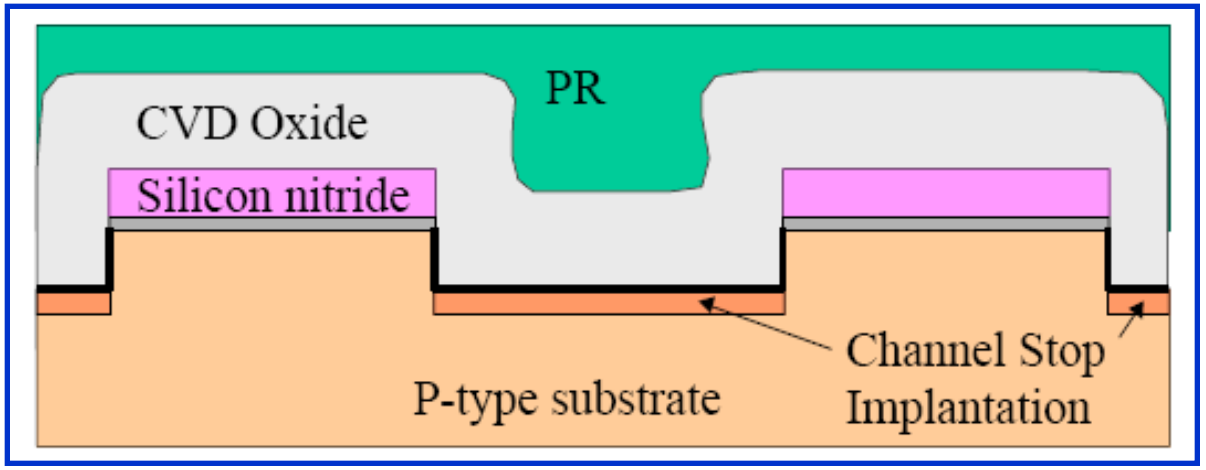


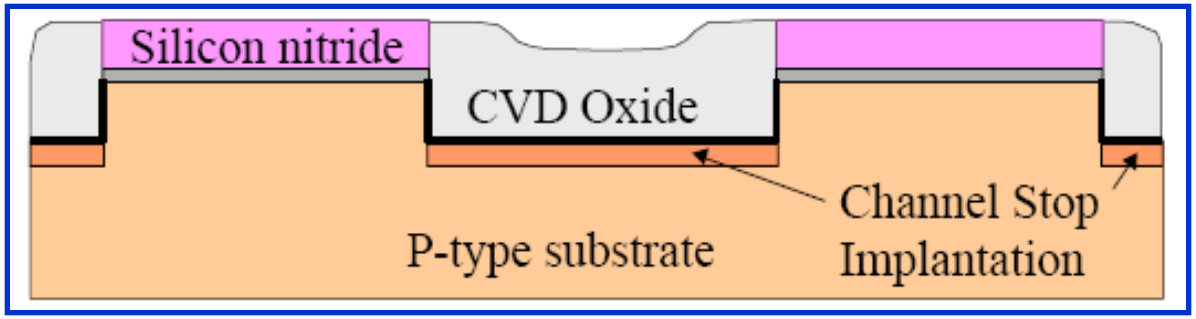
8) Trench Filling by CVD Oxide



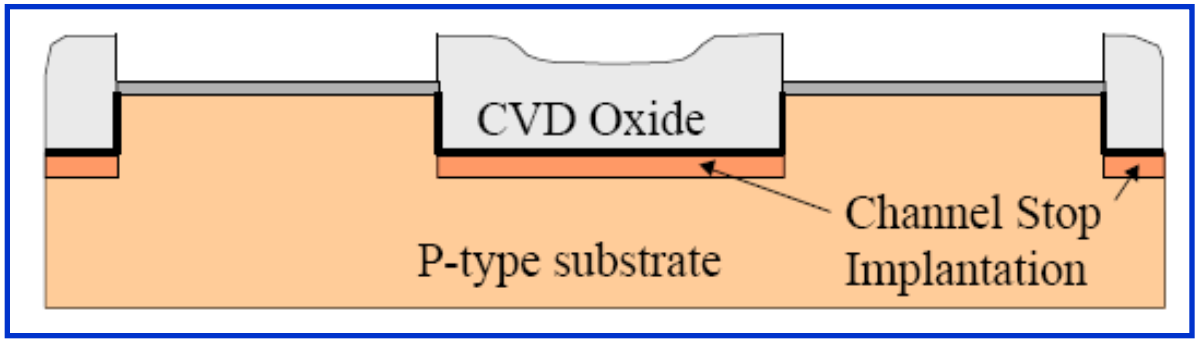
Shallow Trench Isolation (STI) 4/5

9) Etching-back Planarization



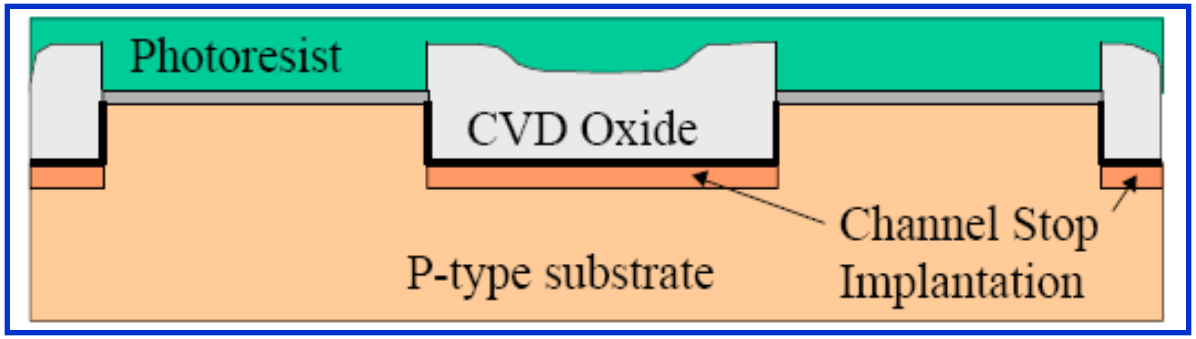


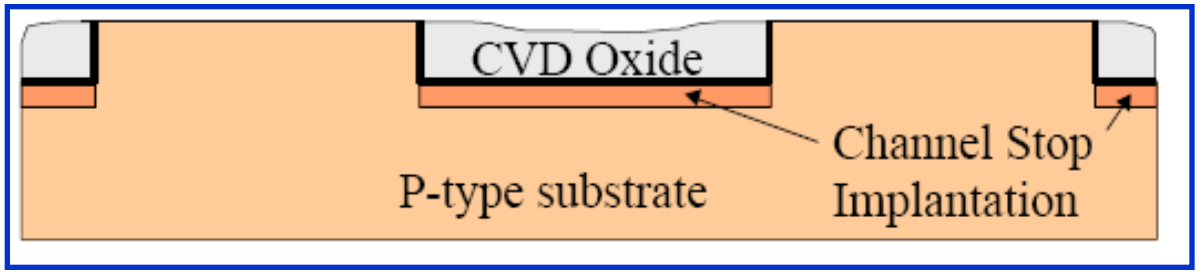
10) Si_3N_4 Etching



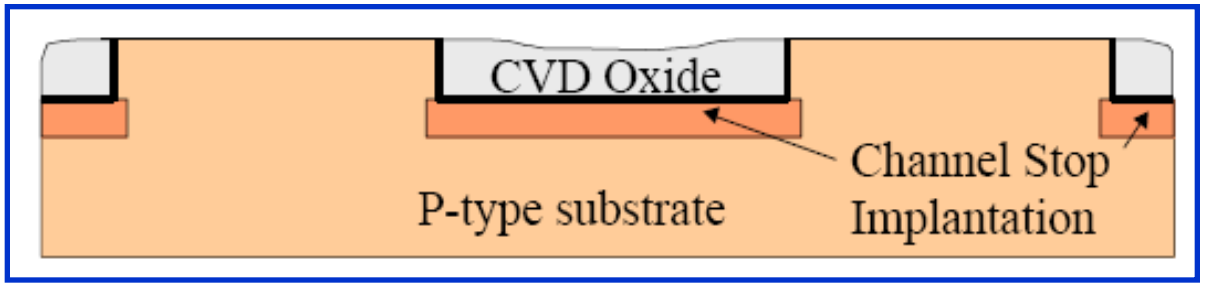
Shallow Trench Isolation (STI) 5/5

11) Re-Etching-back Planarization



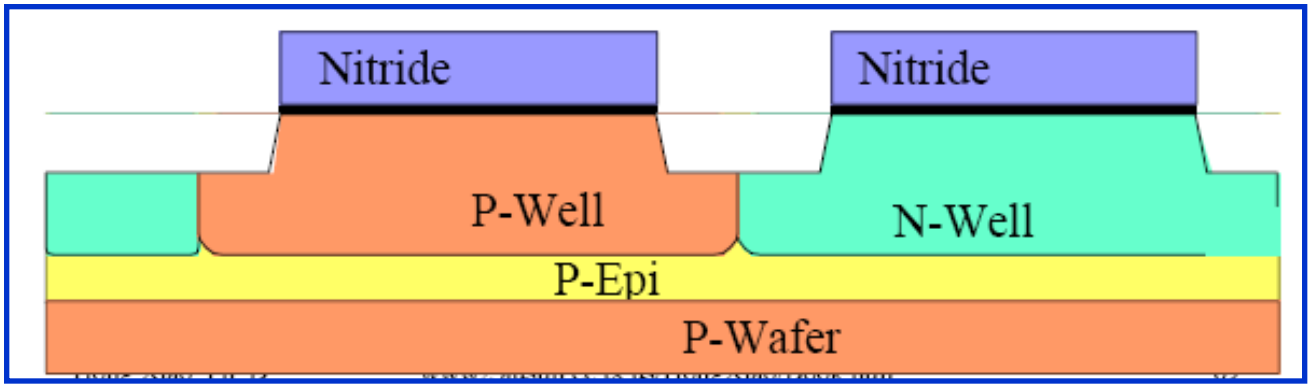


12) Densification Annealing of CVD Oxide



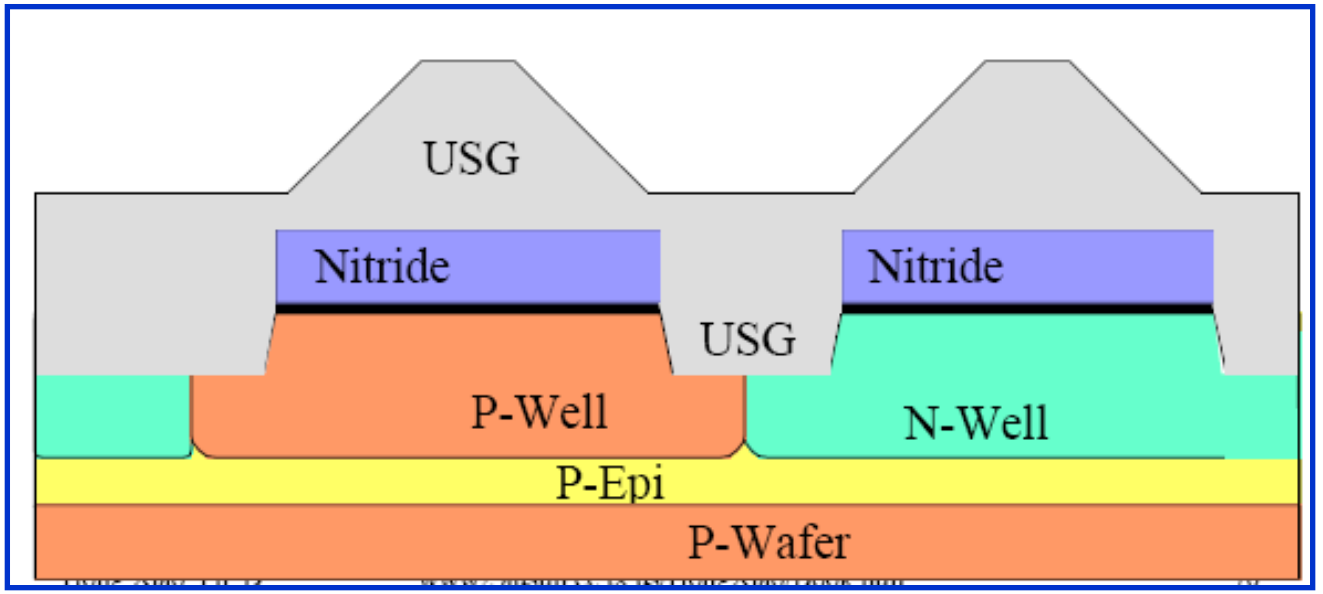
Modern STI Technology (CMOS) 1/2

1) No Channel Stop Implantation



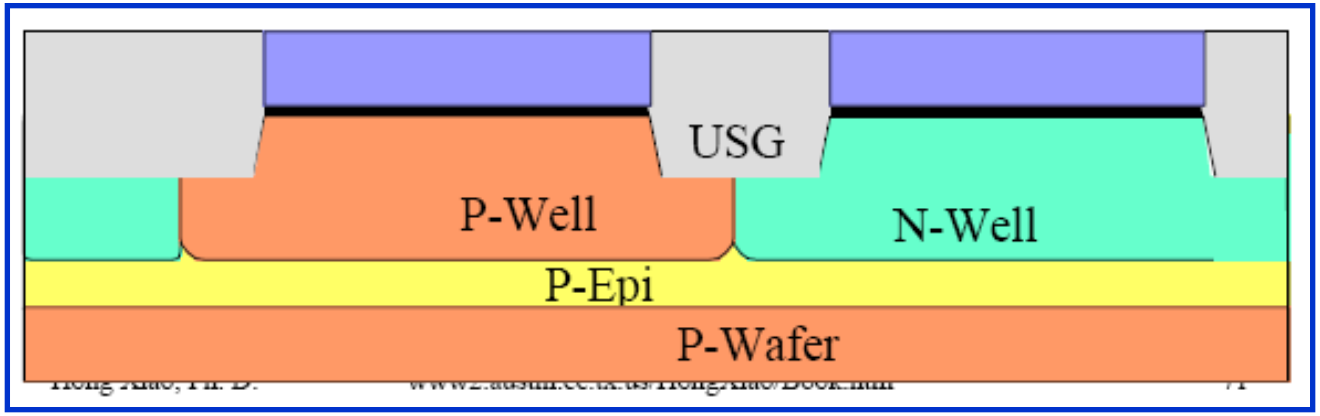
USG (Un-doped Silicate Glass): $SiH_4+O_2+Ar \rightarrow$USG + volatiles↑

2) HDPCVD: No Densification Annealing

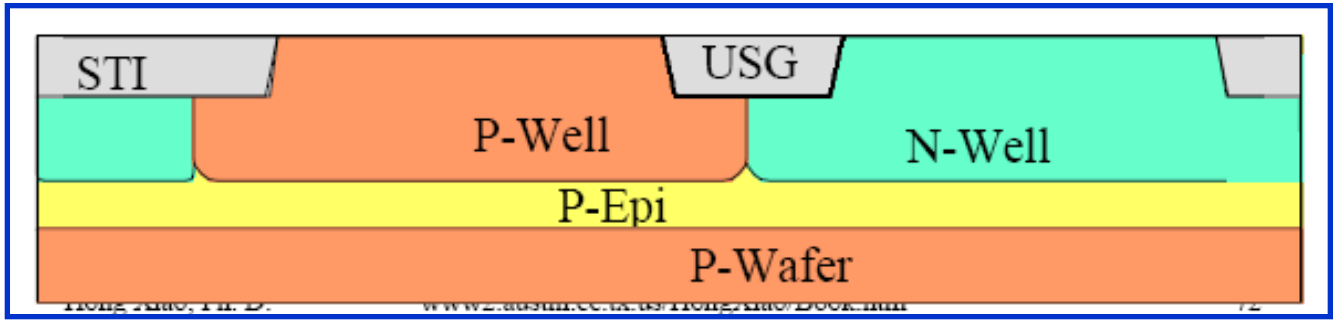


Modern STI Technology (CMOS) 2/2

3) CMP Planarization



4) Si_3N_4 Etching-back and USG



Process Integration - Overview

- Isolation Technology
- Gate Stack Options
  - Self Aligned Structures
  - Replacement Gate Technology
  - Fully Silicided Gates
- Advanced CMOS Integration

Gate Structure

Early gate structure is SiO_2 - Metal Gate (Al Gate).
With increased integration, low V_T is required.

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_F)}}{C_{ox}}; \phi_F = V_T \ln\left(\frac{N_D}{n_i}\right)$$

Moreover, Al is incompatible to high-temperature process, such as ion implantation annealing.
Al gate not feasible when reducing source-drain series resistance is required.

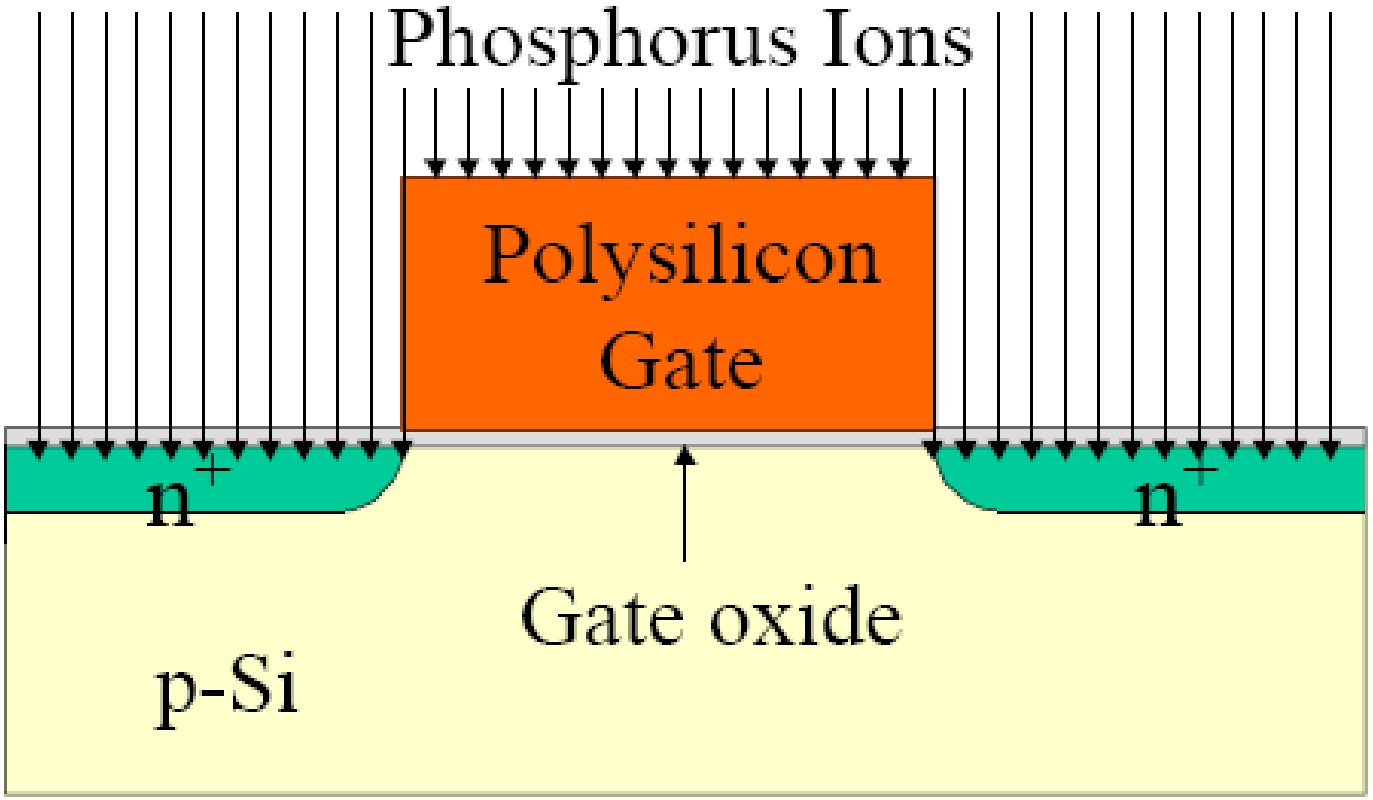
→ **Poly-Gate (Interconnect)**

Using poly-gate, V_T can decrease by 1.2~1.4 V

Other Advantages of Poly-Gate:

- **ϕ_{MS} can be changed by doping. For example, n-poly may reduce V_T by 1.1 V, i.e., the dual-poly (n & p) technology commonly used in industry.**
- **Poly-Gate self-alignment technology can further improve integration.**

Poly-Gate Self-Alignment Technology

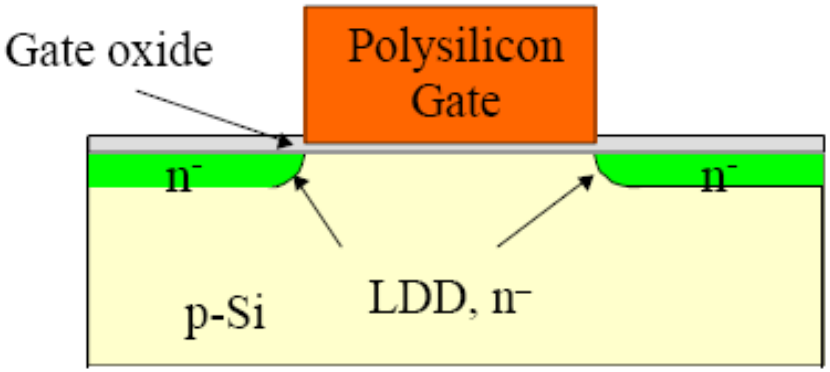


“Hot” electron effects are considerable in small devices !!

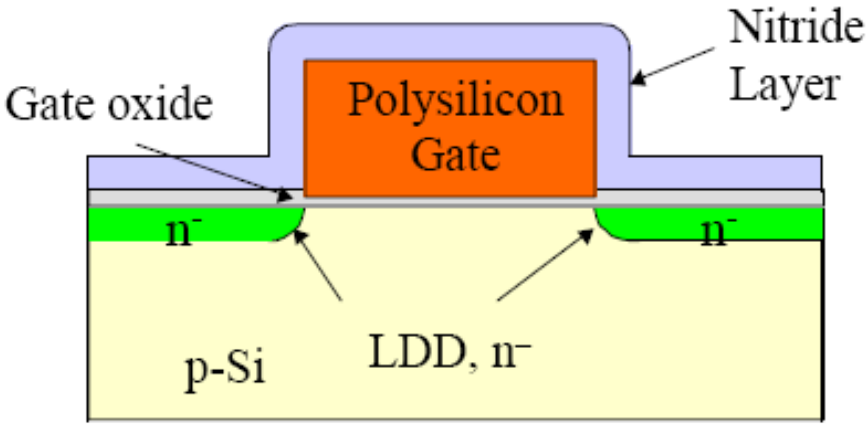
Lighly Doped Drain (LDD) + Spacer

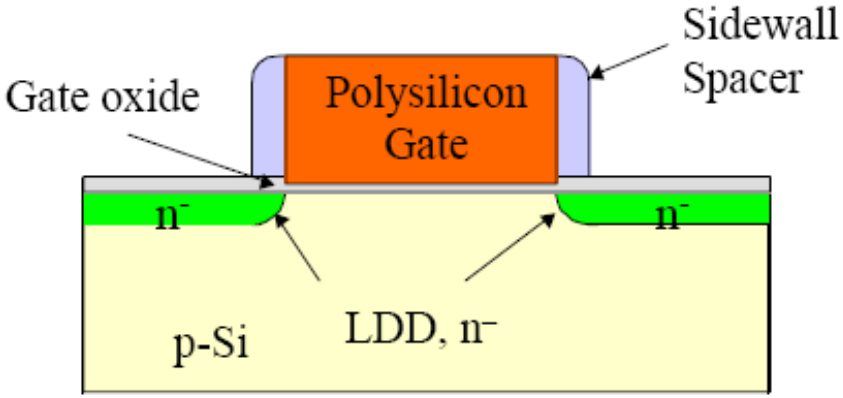
LDD + Spacer Polysilicon Self-Alignment

1) LDD Implant



2) Sidewall Formation

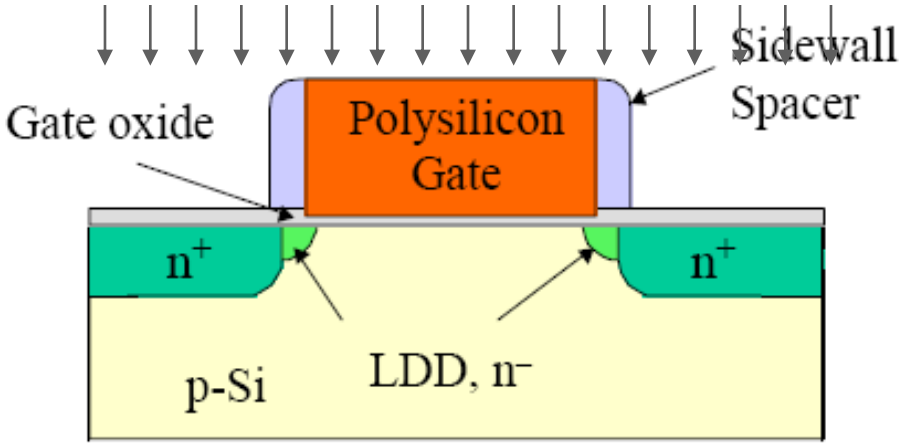




LDD + Spacer Polysilicon Self-Alignment

3) Ion Implantation
+Annealing

Self-Aligned Ion Implantation



Self-Aligned Silicide

SALICIDE

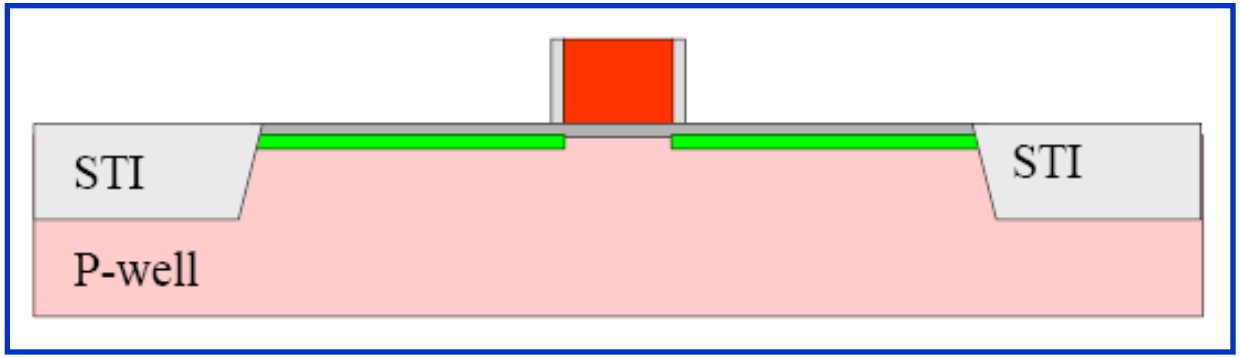
Maximize contact area, reduce contact resistance and make contacts much closer to the channel (see also Lecture 9)

$TiSi_2$, $CoSi_2$, NiSi

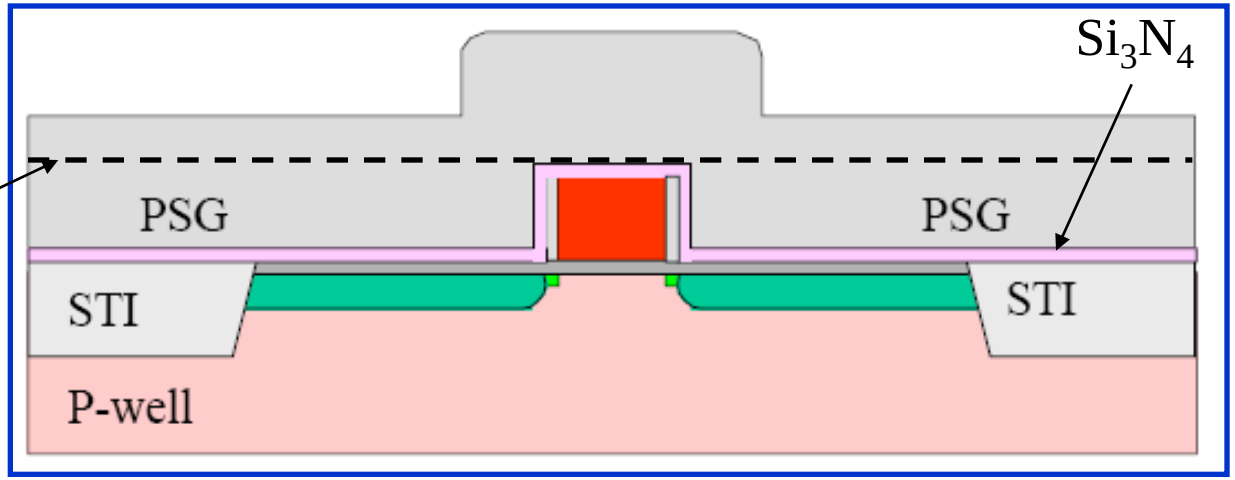
High k/Metal Gate: Replacement of Poly-Gate

Problem: High-k / Metal Gate stacks are not compatible with CMOS FEOL temperature requirements.

1) LDD and Sidewall

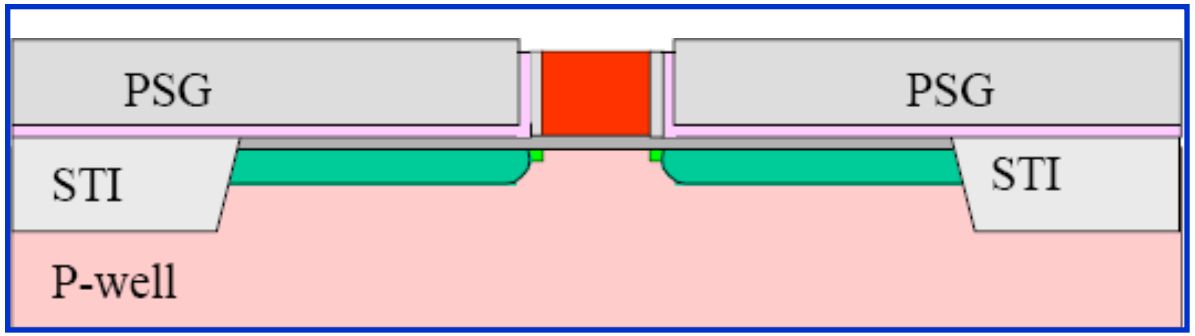


2) LPCVD Si_3N_4
+ CVD PSG
+ CMP

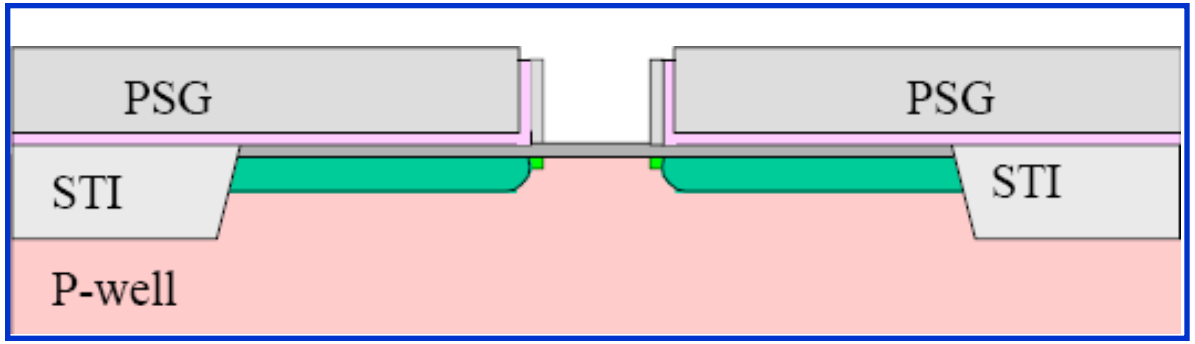


High k/Metal Gate: Replacement of Poly-Gate

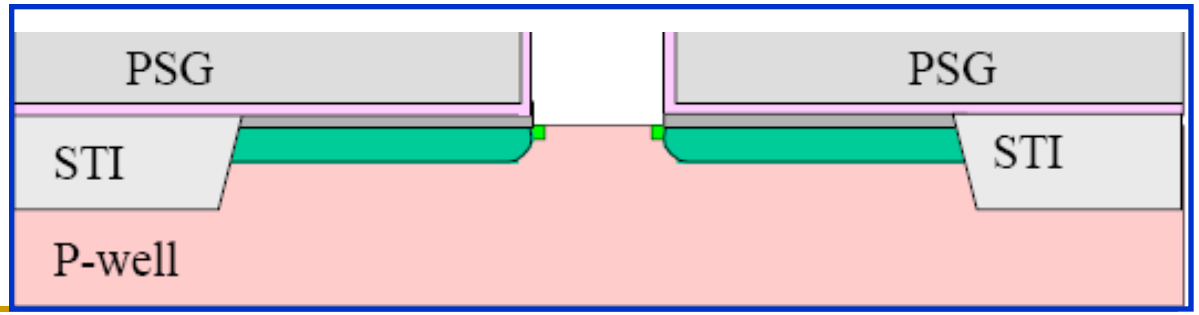
3) Si_3N_4 Etching



4) Poly-Si Etching



5) Oxide Etching

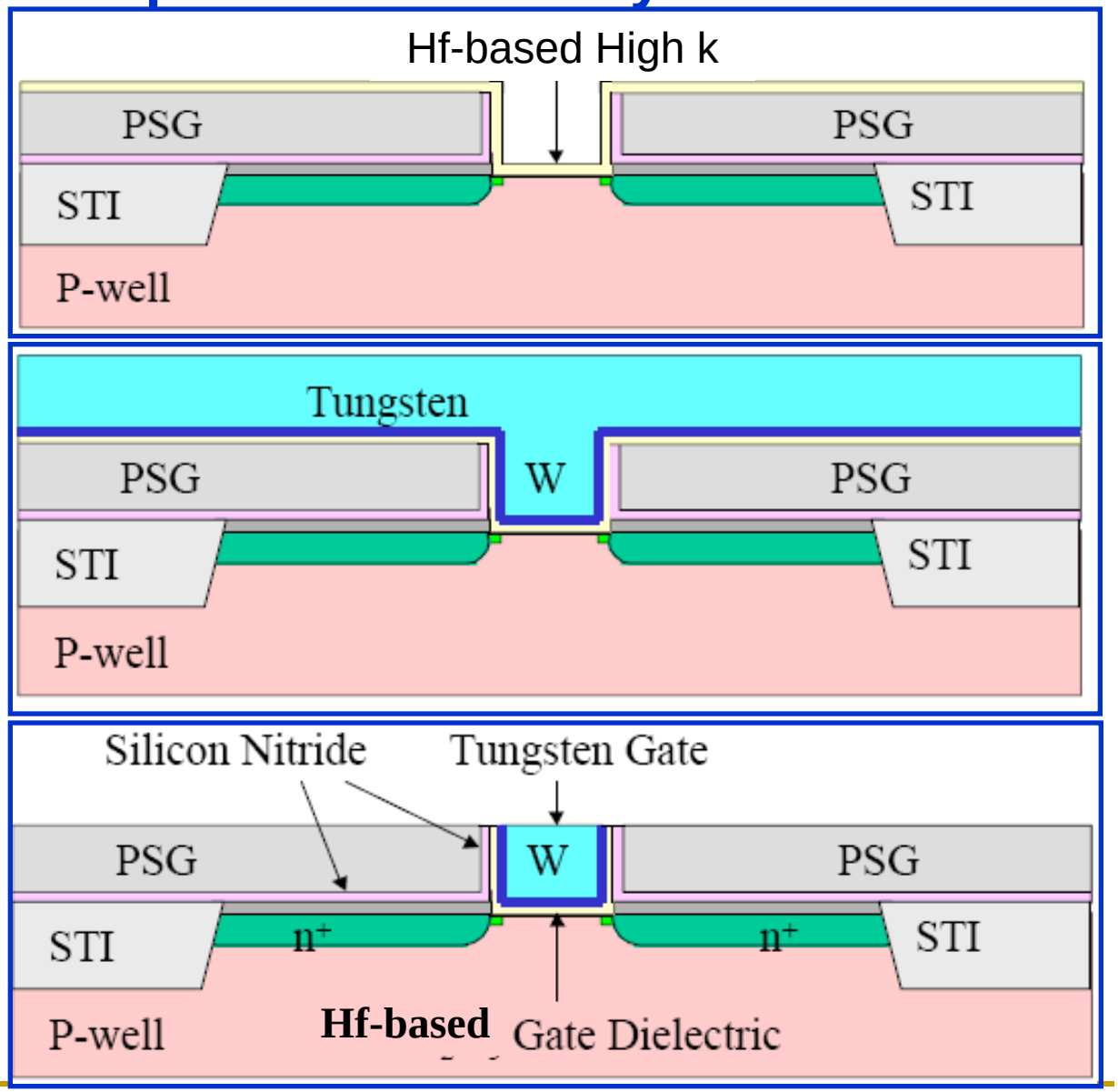


High k/Metal Gate: Replacement of Poly-Gate

6) High-k Deposition
Today: Hafnium-based; ALD process

7) Metal Gate

8) CMP



Fully-Silicided (FUSI) Gate

Metal silicide directly on gate oxide without poly-Si in-between

Example: nickel silicide (1 nm Ni + 1.84 nm Si → 2.2 nm NiSi)

Nickel Silicide FUSI Gates

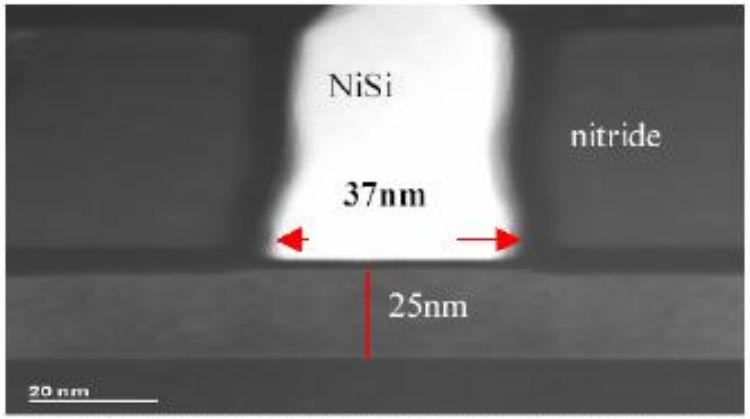
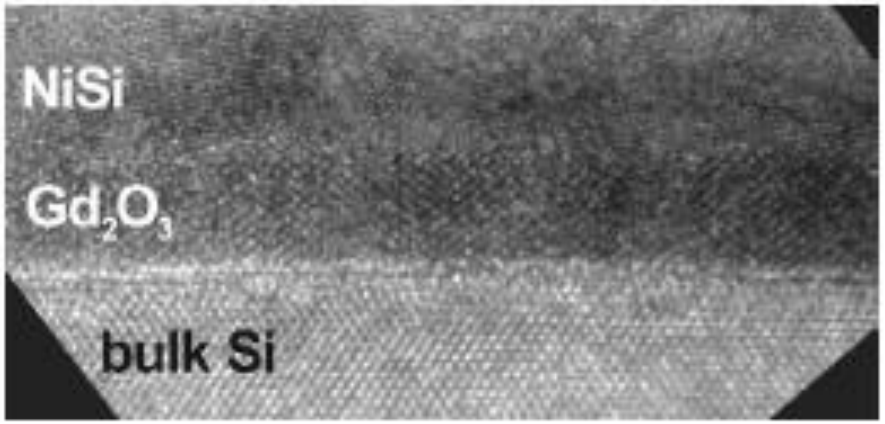
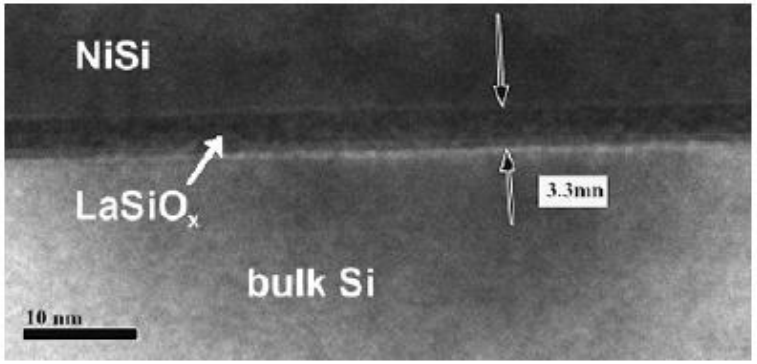


Fig. 3: Scanning tunneling electron micrograph with a Z-contrast shows that nickel is present only in the gate.



Gottlob et al., "0.86-nm CET Gate Stacks With Epitaxial Gd_2O_3 High-*k* Dielectrics and FUSI NiSi Metal Electrodes", IEEE El. Dev. Lett., 27(10), 2006.



Gottlob et al., "Gentle FUSI NiSi metal gate process for high-k dielectric screening", Microelectronic Engineering 85 (2008) 2019–2021

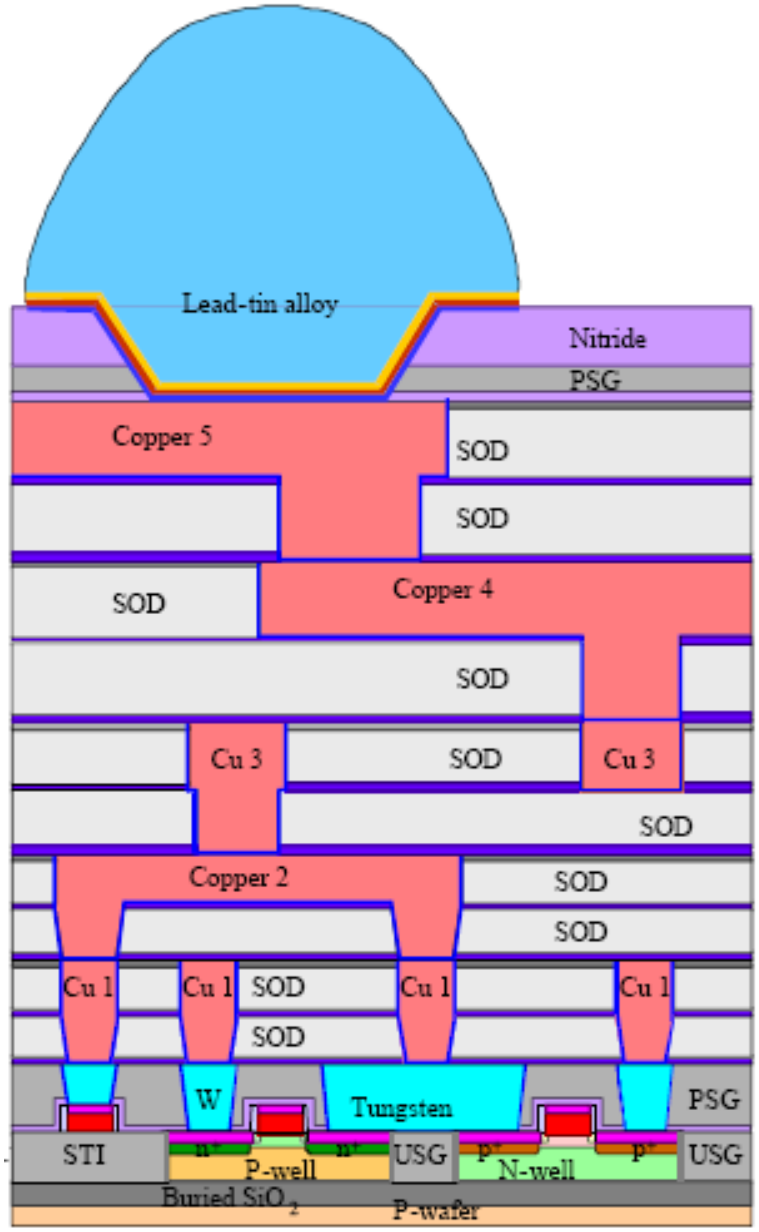
Process Integration - Overview

- Isolation Technology
- Gate Stack Options
- Advanced CMOS Integration
  - Full SOI CMOS Process
  - Flip Chip Packaging
  - Current Technology

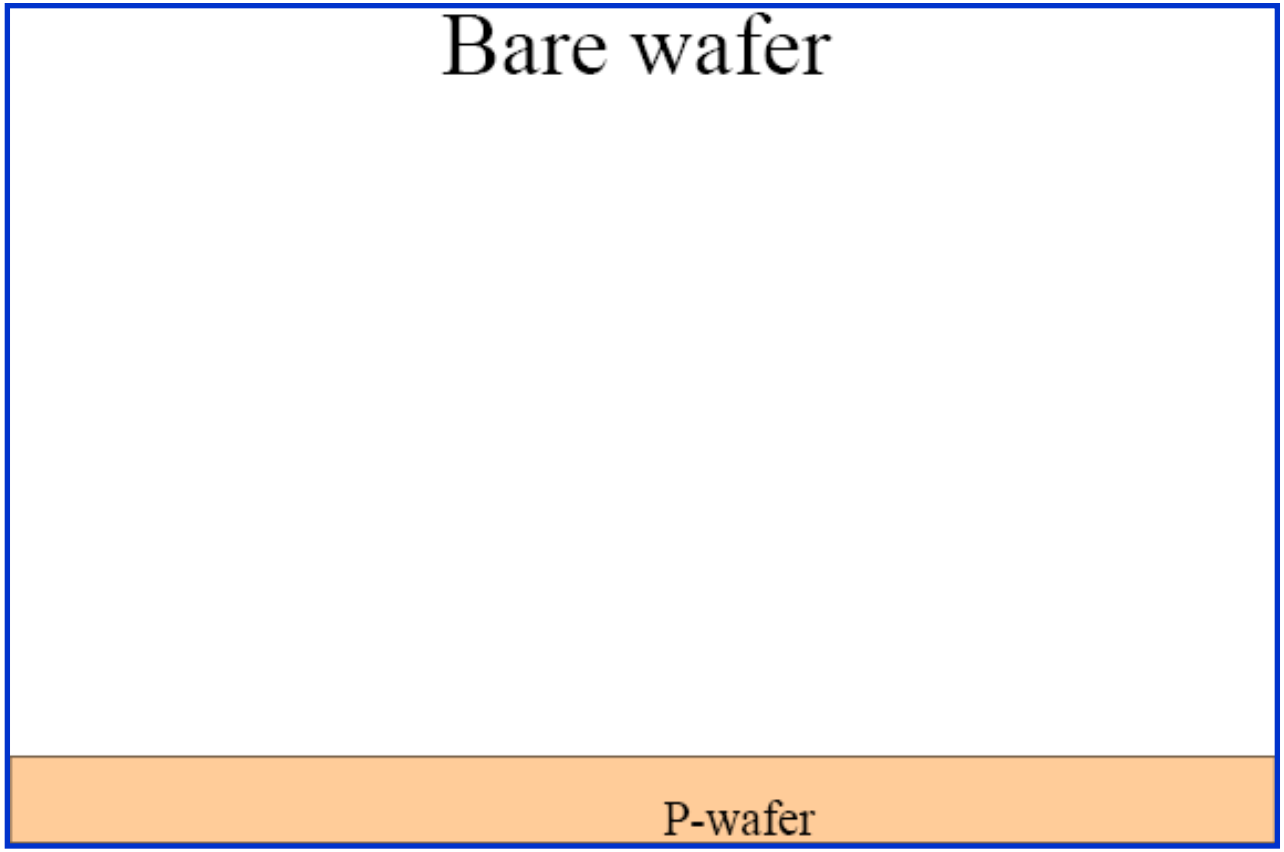
Modern SOI CMOS Integration Technology

Example:
SOI + Five-level
Cu Interconnect

Next Slides
21 mask process

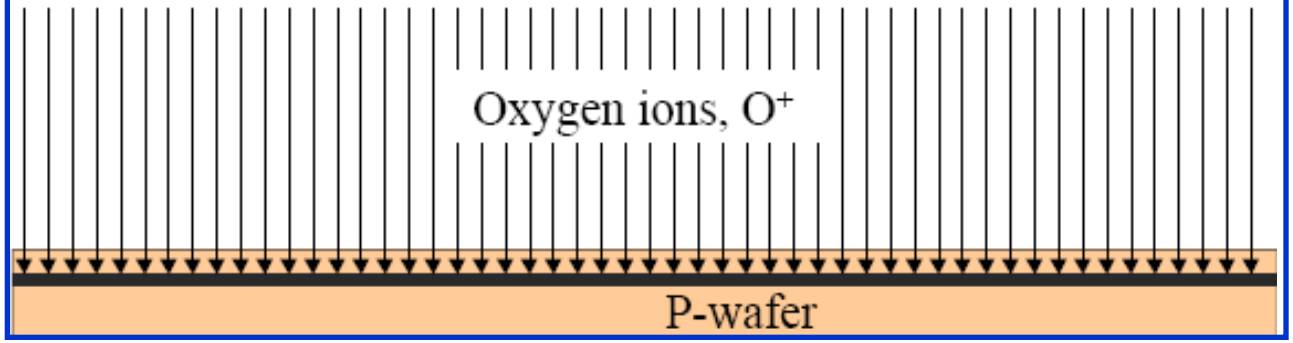


CMOS Integration



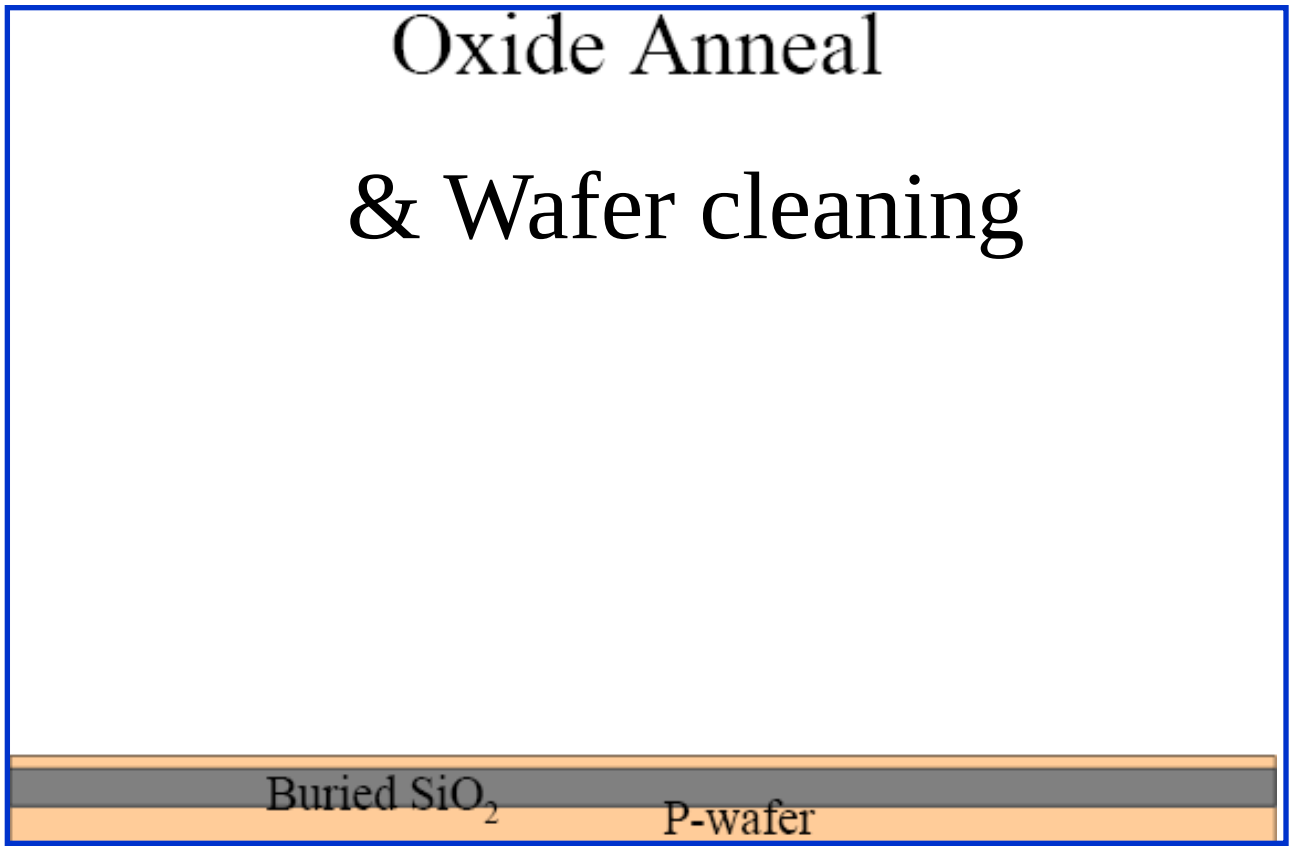
High Current Oxygen Ion Implantation

SIMOX = Separation by Ion Implantation of Oxygen



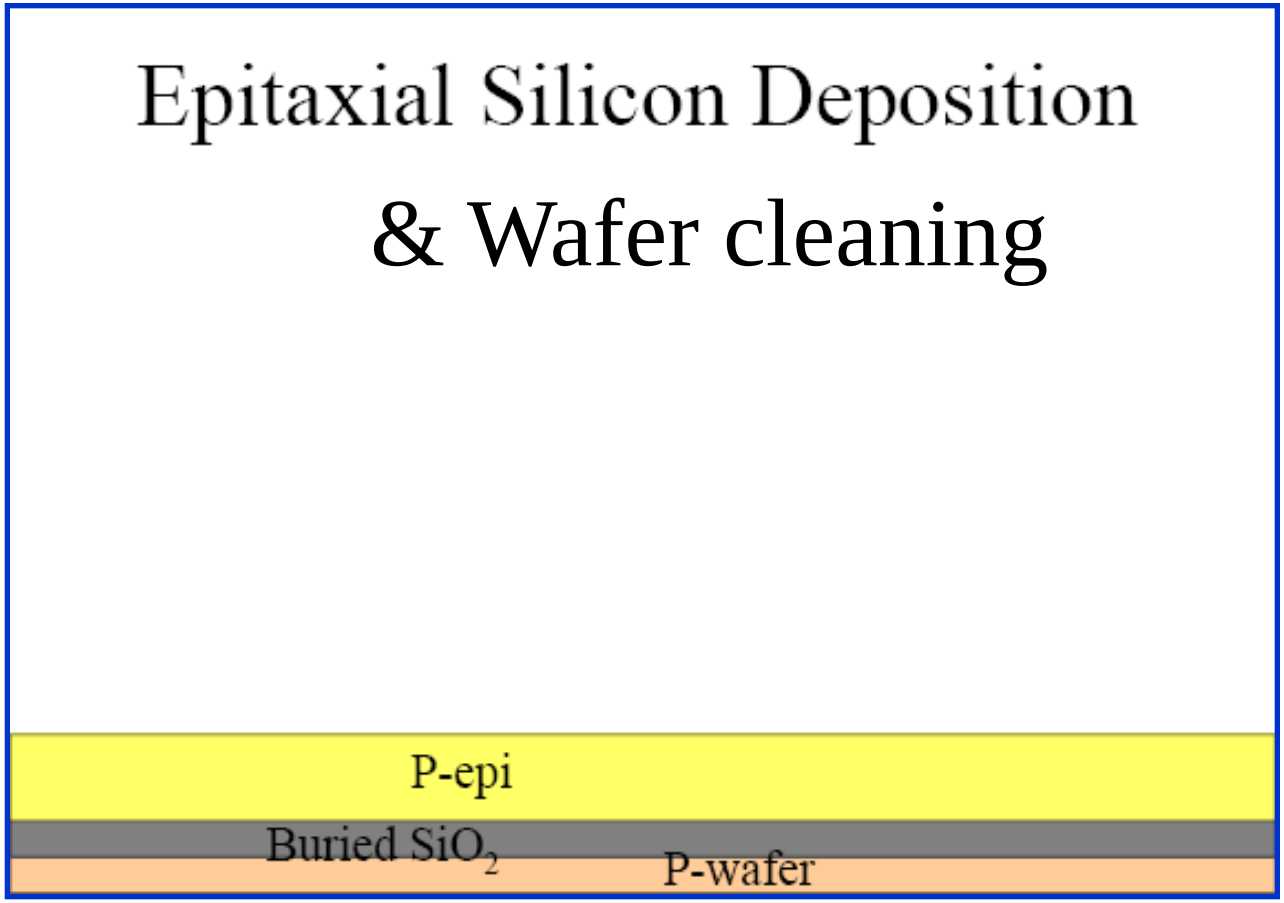
Oxide Anneal

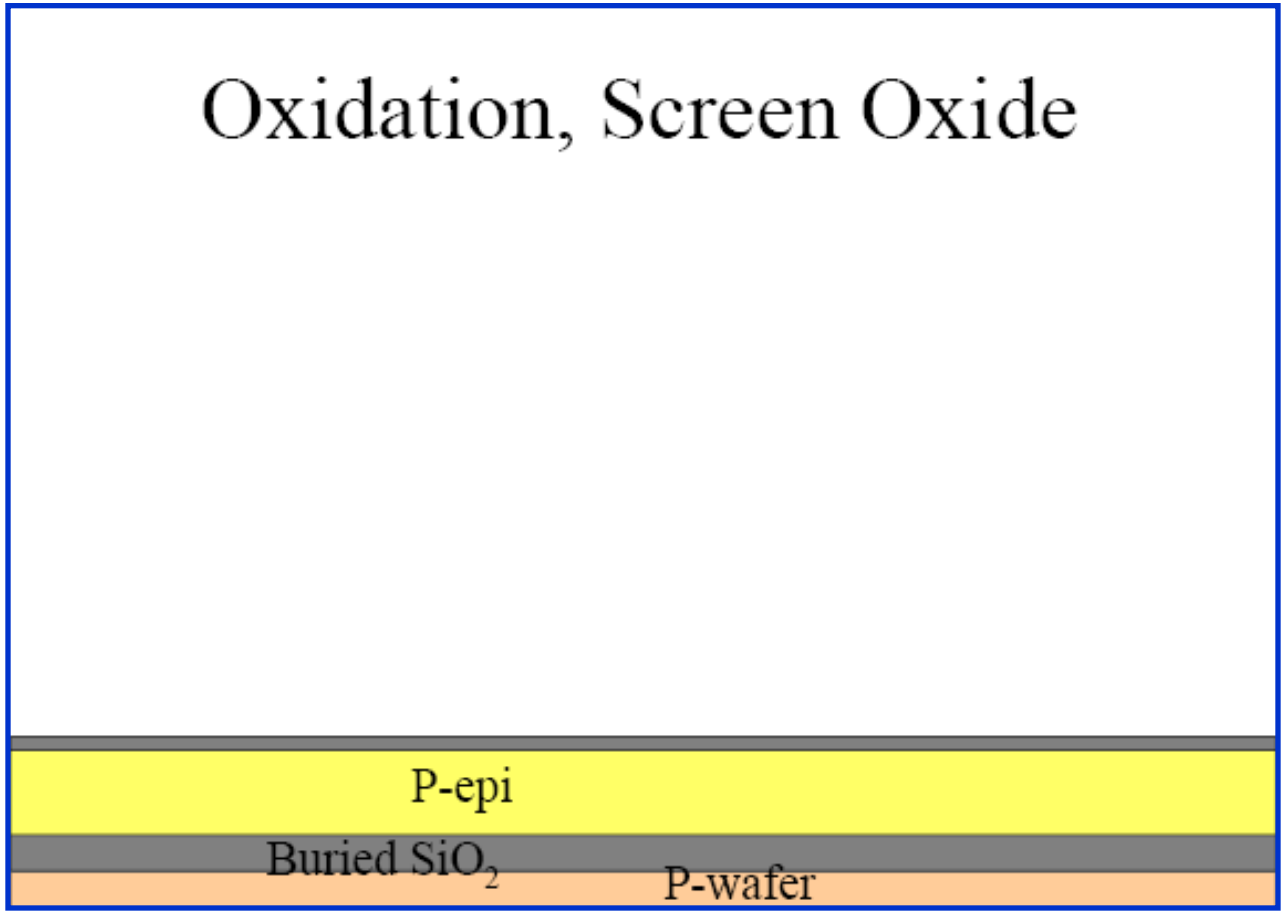
& Wafer cleaning



Epitaxial Silicon Deposition

& Wafer cleaning

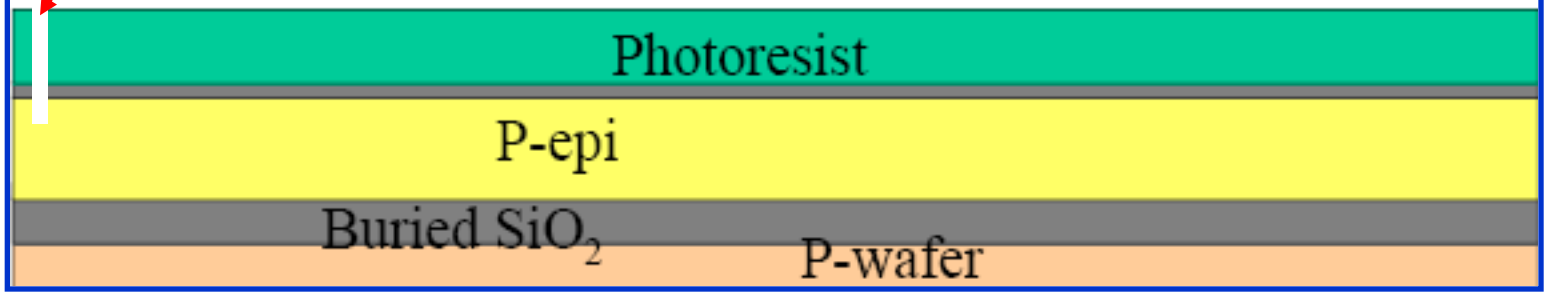



Oxidation, Screen Oxide
P-epi
Buried SiO_2
P-wafer

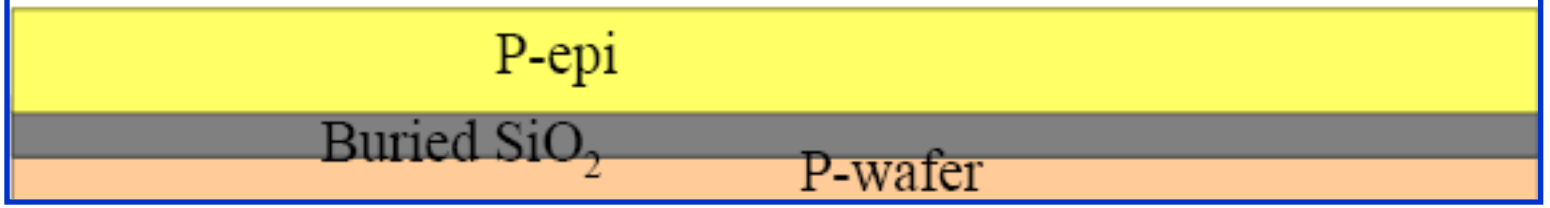
Photoresist Coating and Baking & alignment, exposure, PEB, development and inspection

Etch oxide & Si as alignment marks

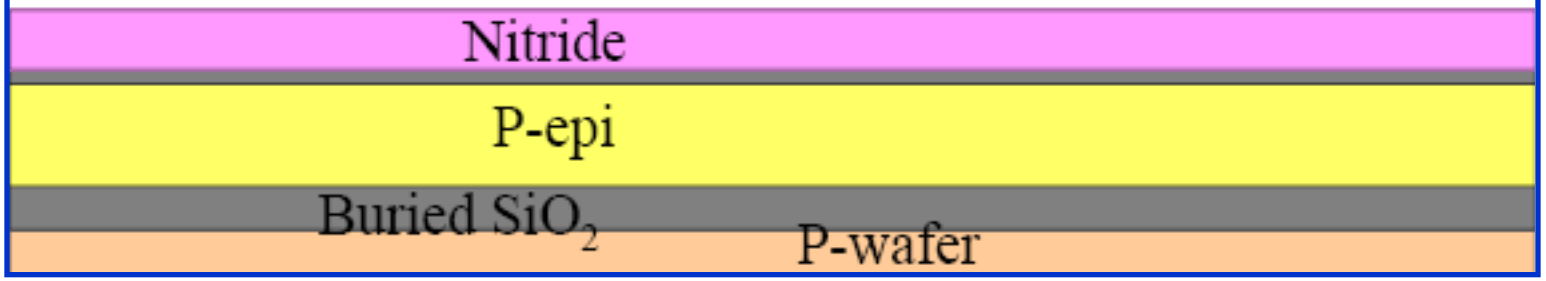
mask0



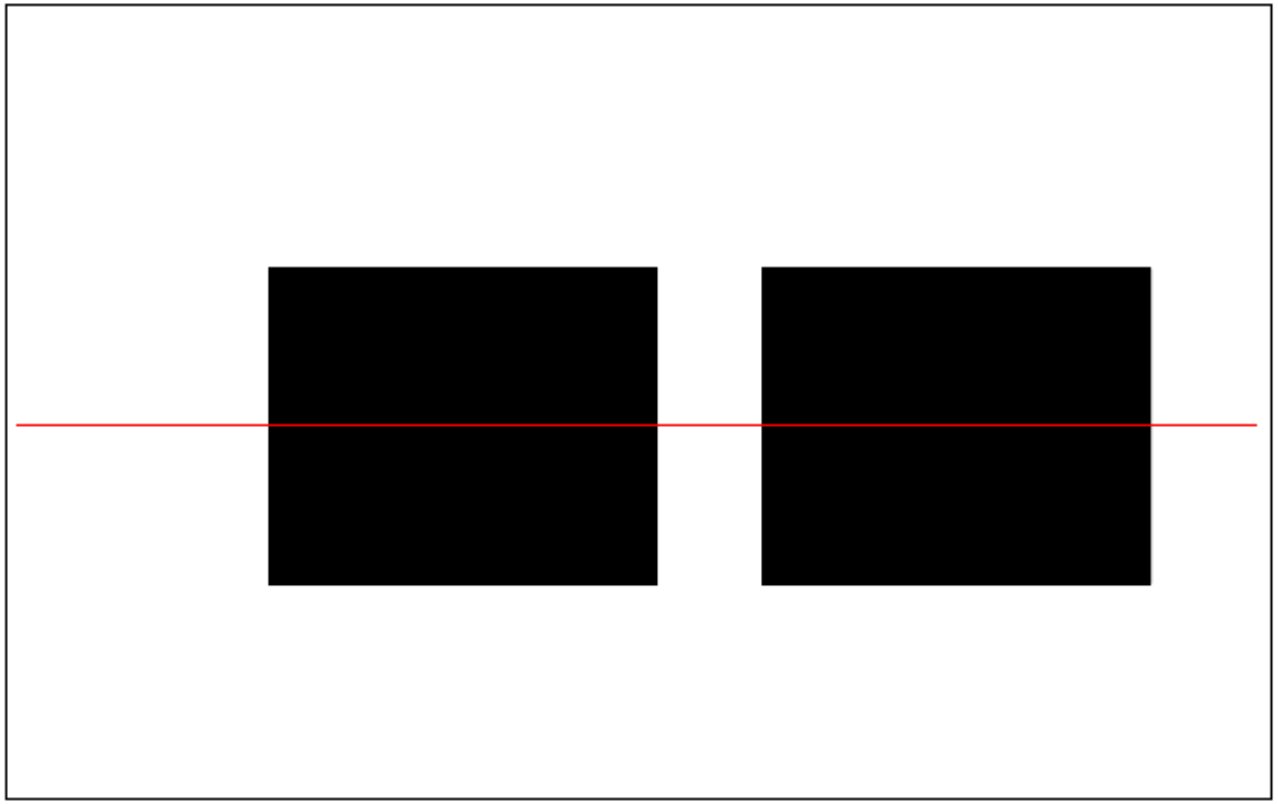
Strip PR and Screen Oxide Wafer cleaning



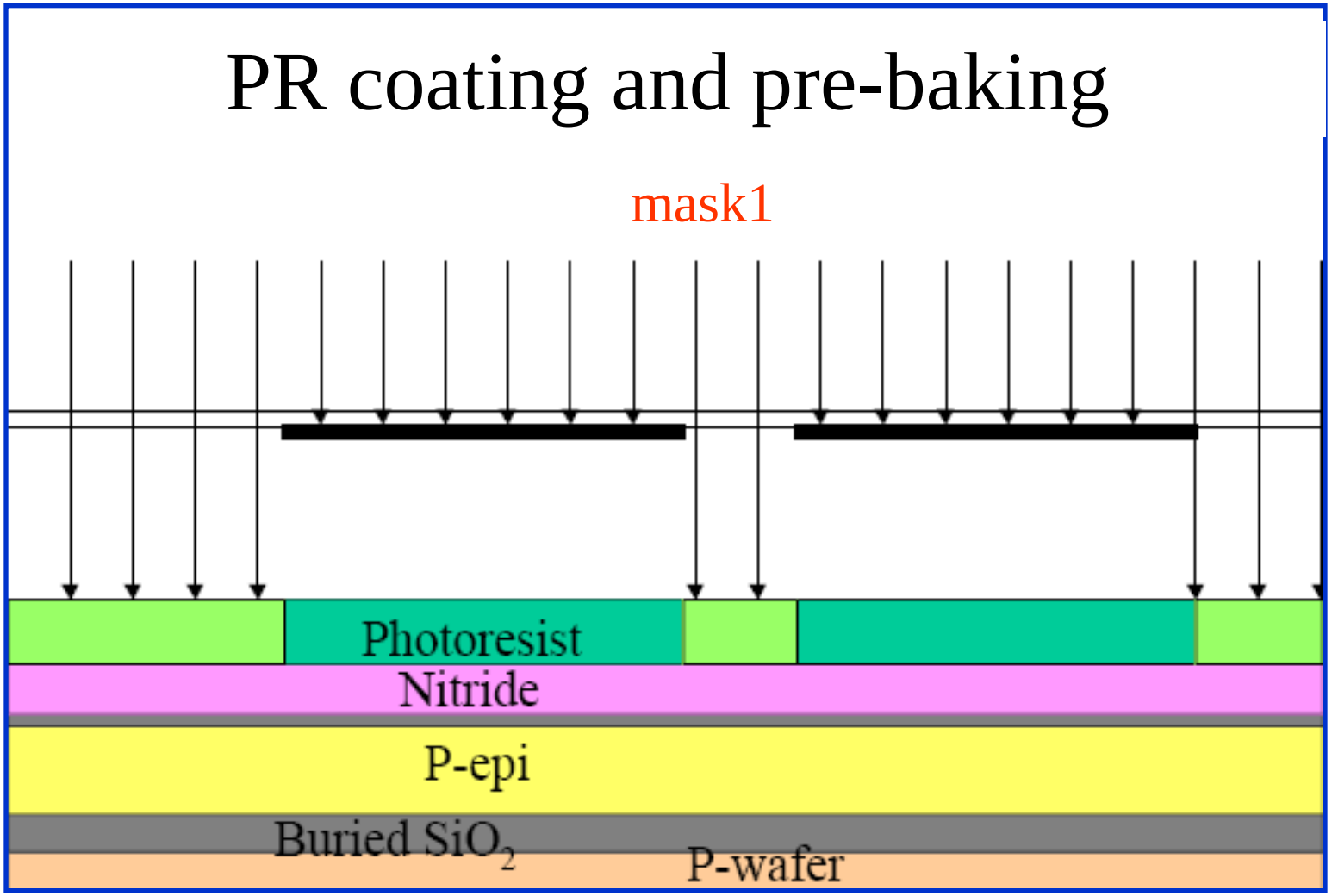
Pad thermal oxidation
LPCVD Nitride



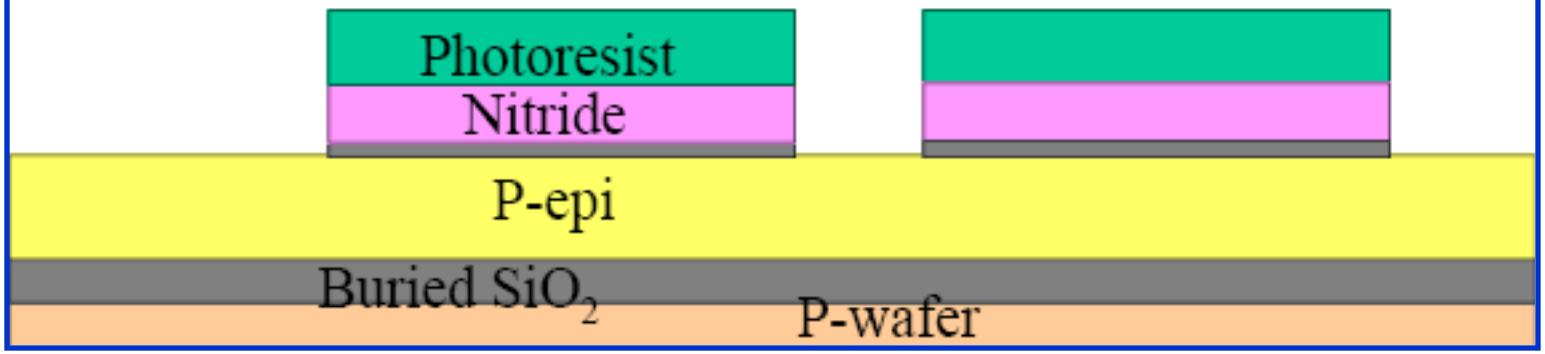
Mask 1: Shallow Trench Isolation



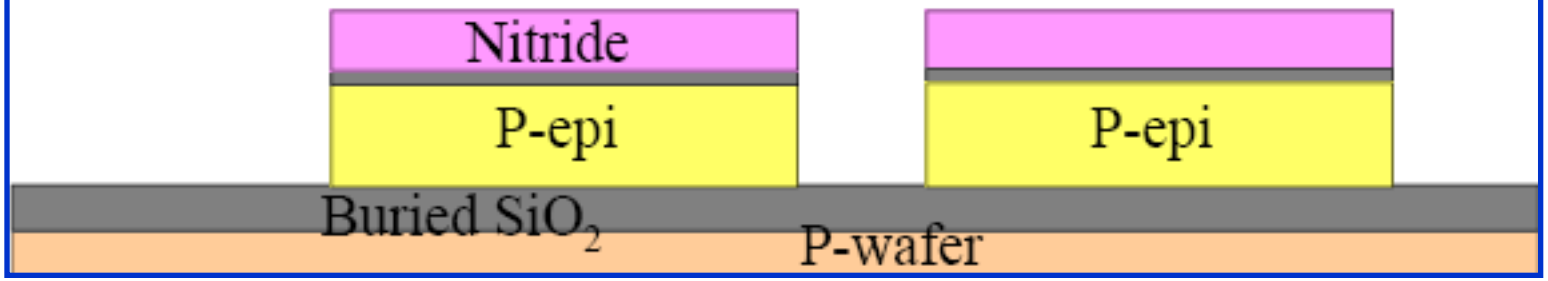
PR coating and pre-baking

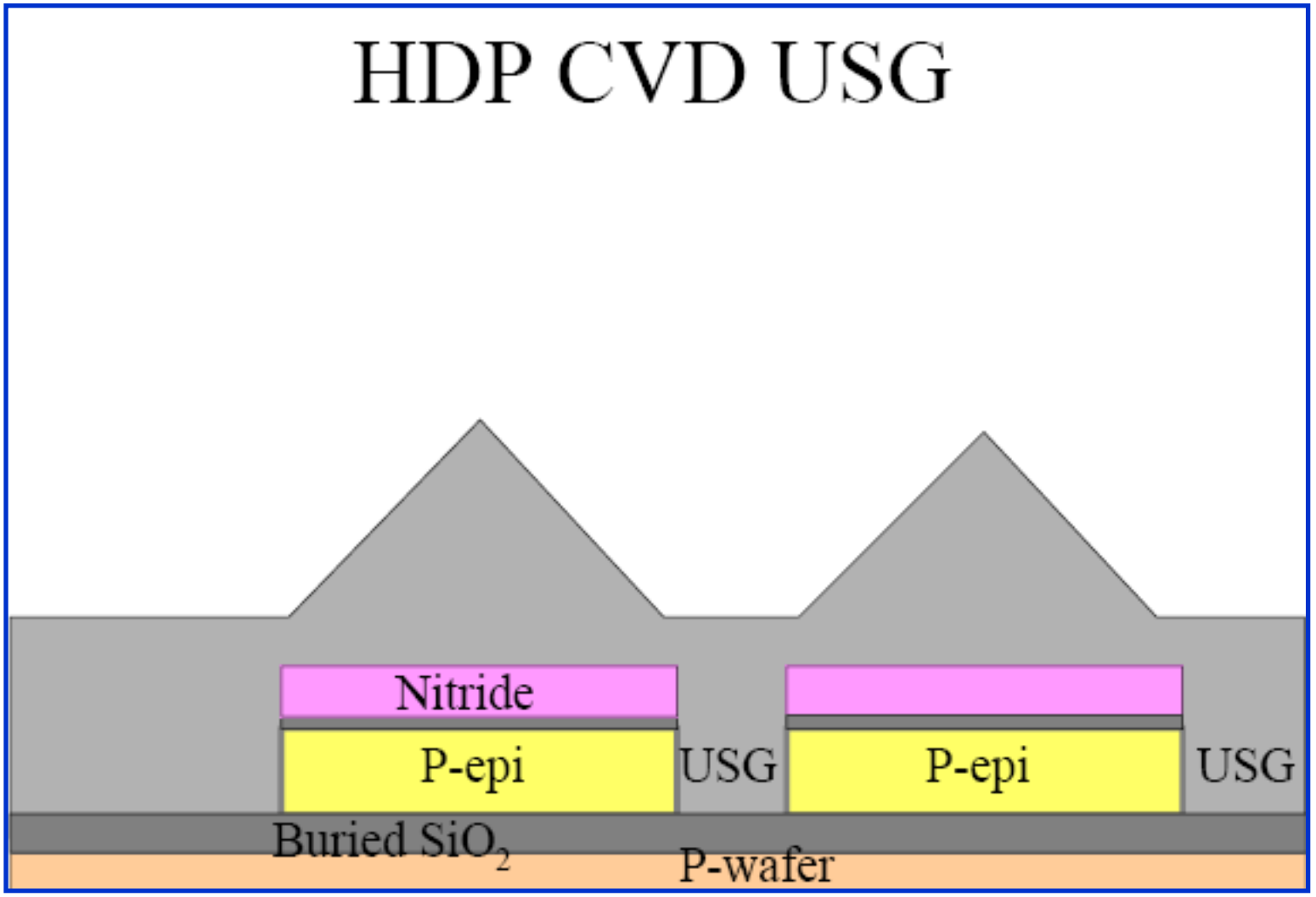


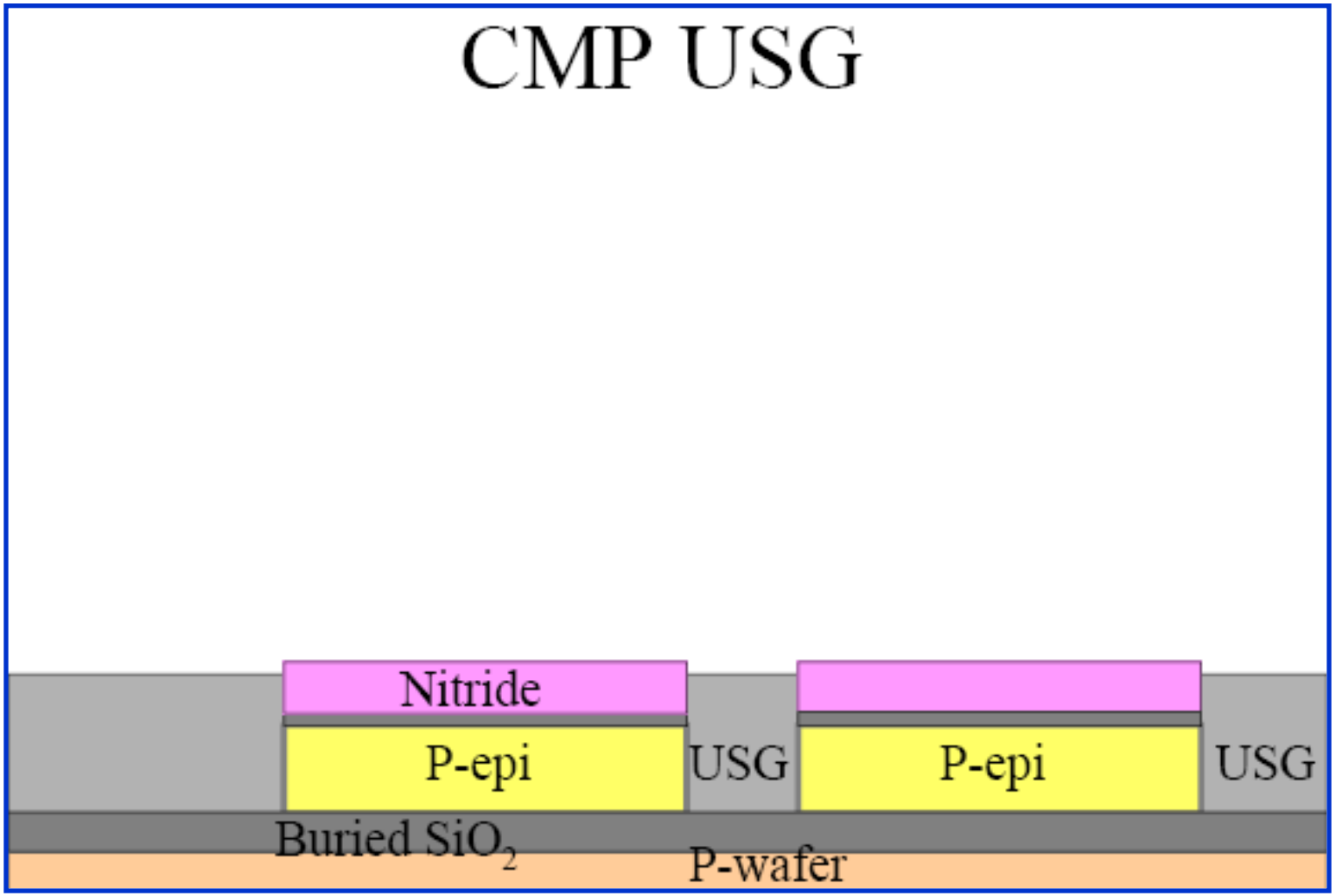
PEB, development & inspection
Etch pad oxide and nitride



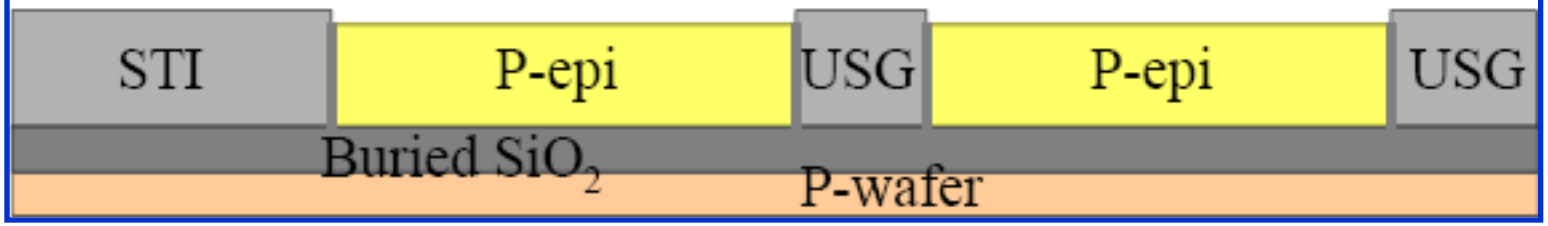
Strip PR & etch Si



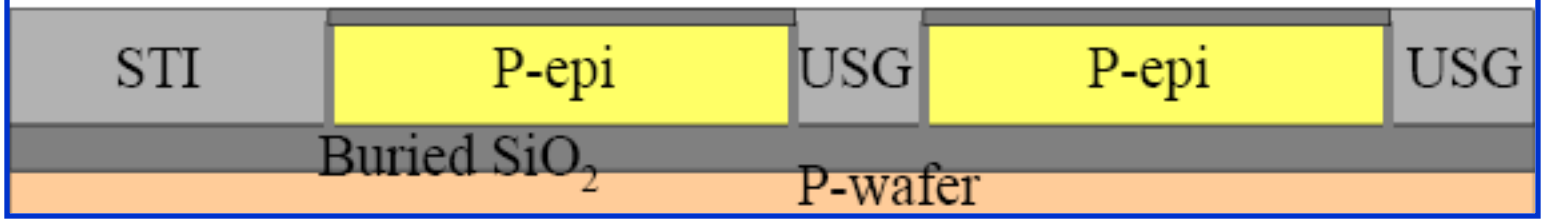

HDP CVD USG
Nitride
P-epi
USG
P-epi
USG
Buried SiO_2
P-wafer


CMP USG
Nitride
P-epi
USG
P-epi
USG
Buried SiO_2
P-wafer

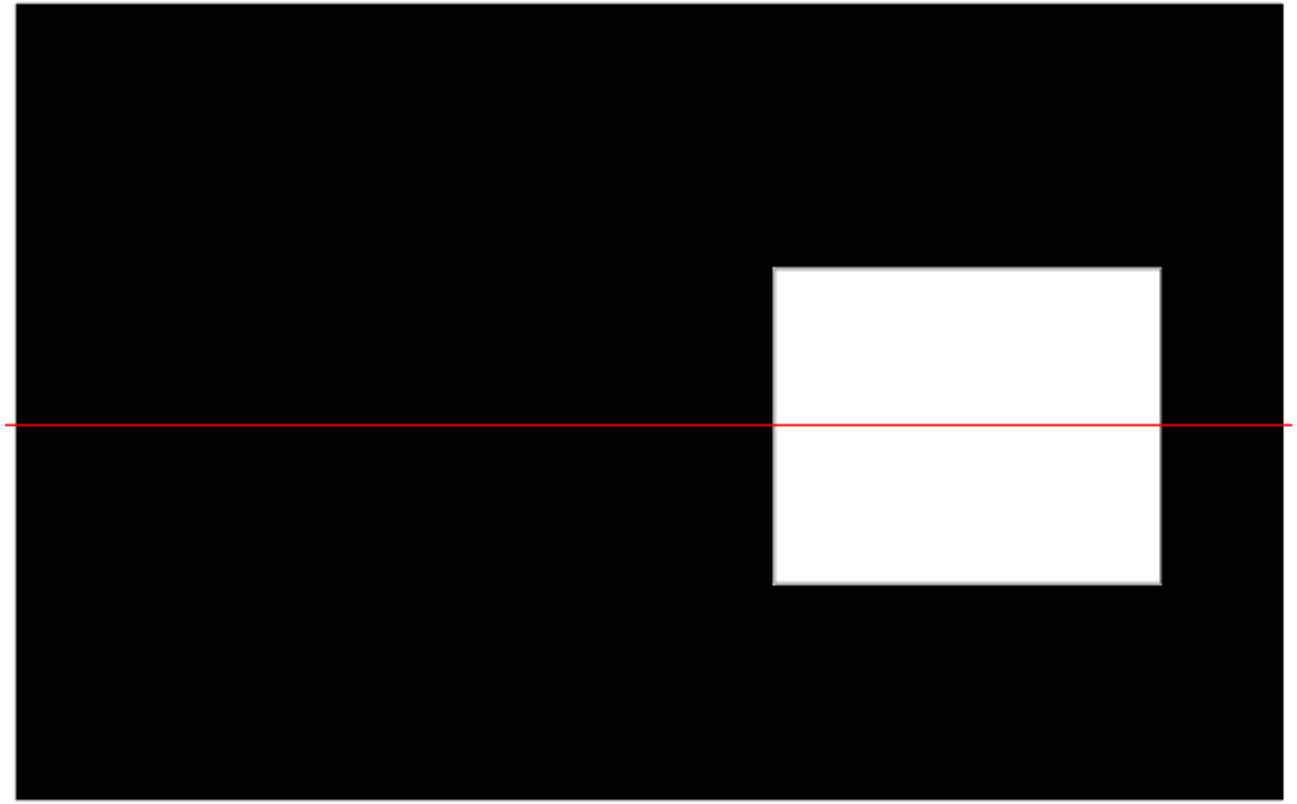
Strip nitride & oxide
Wafer cleaning



Oxidation, Sacrificial Oxide

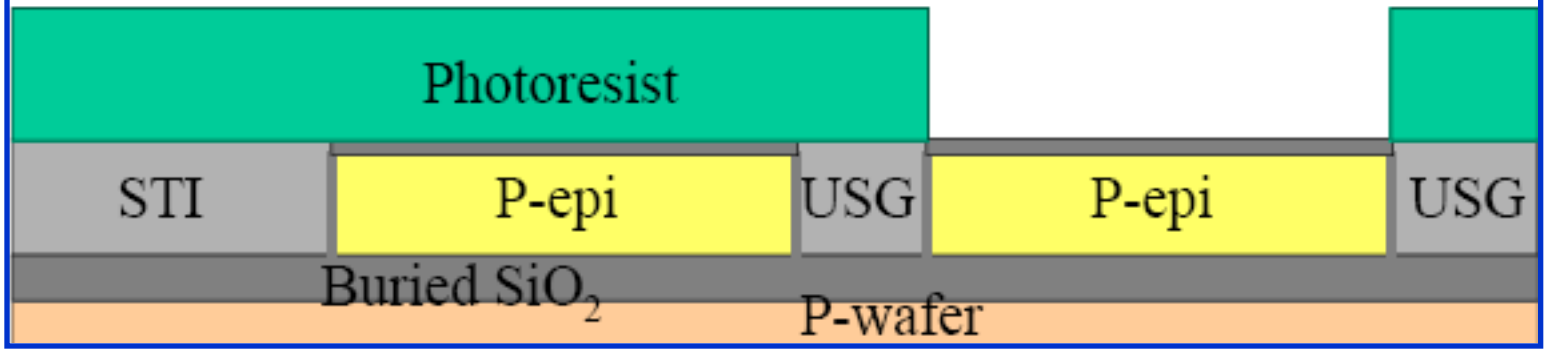


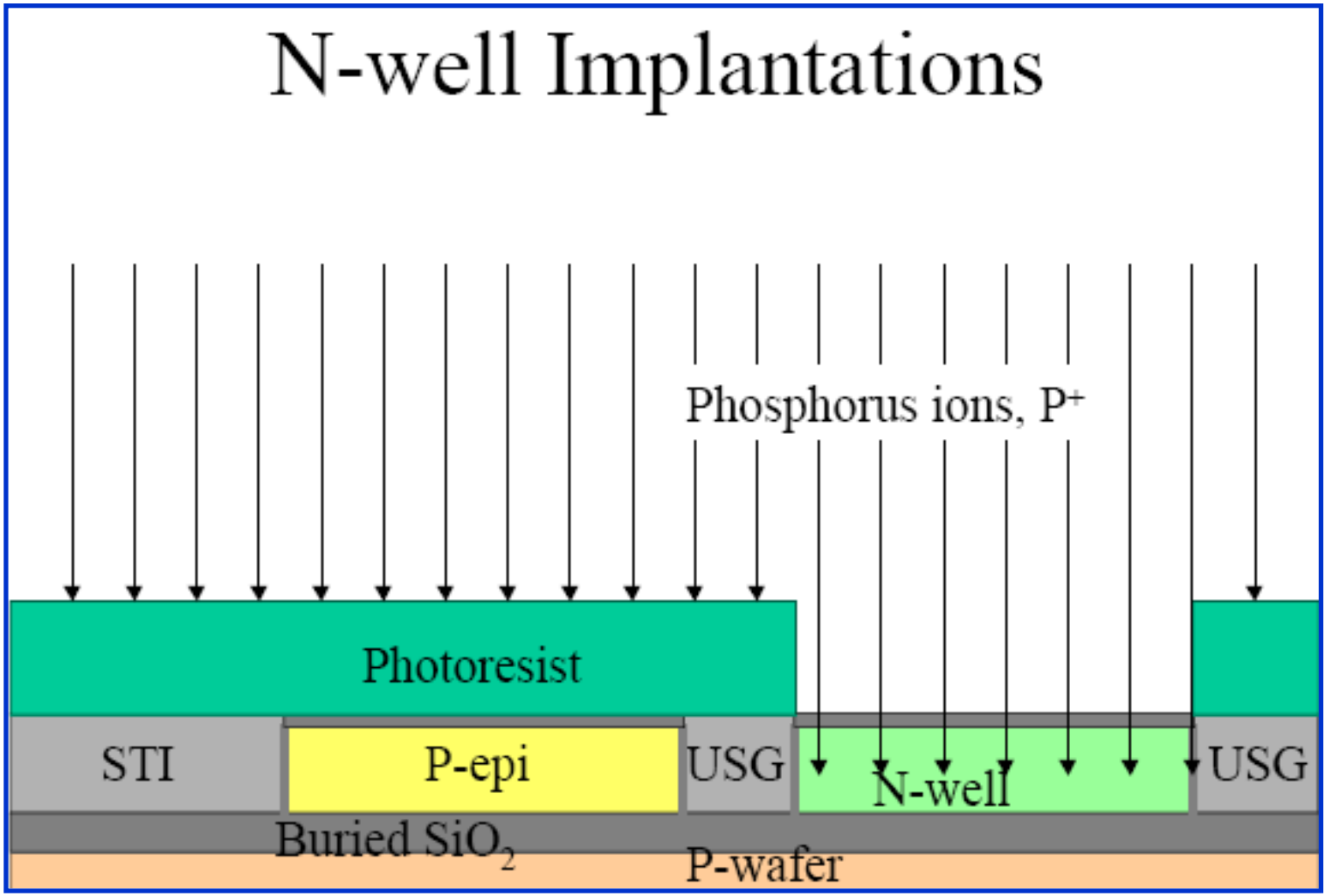
Mask 2: N-well



PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

mask2

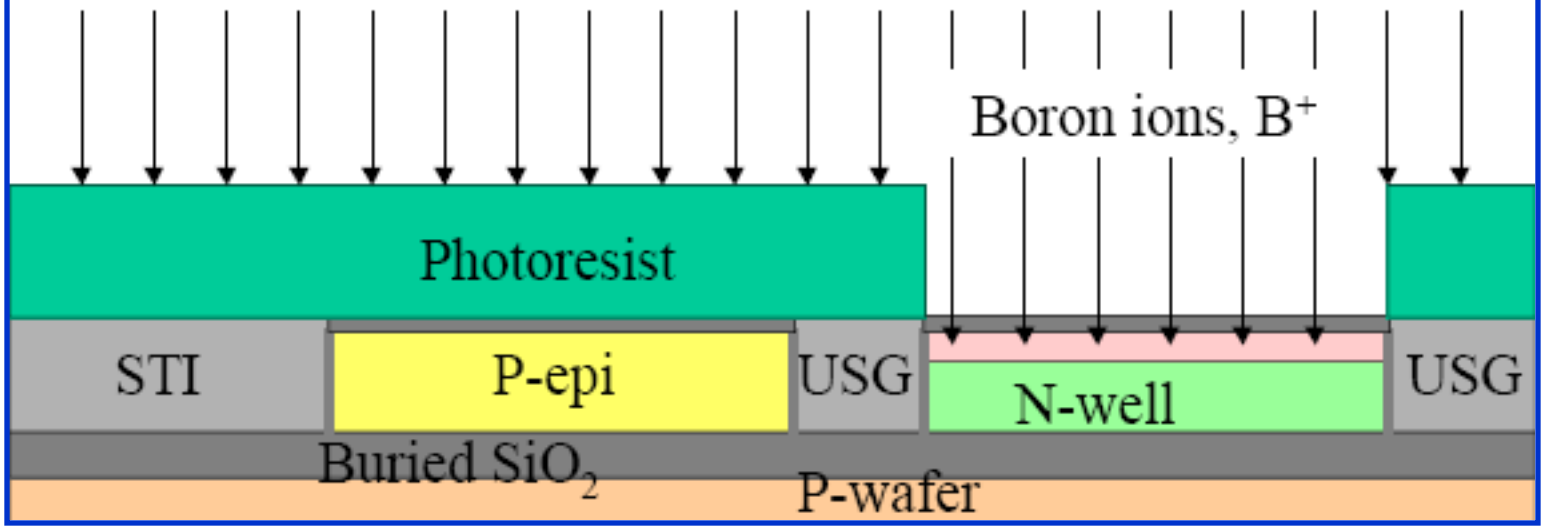



N-well Implantations
Phosphorus ions, P+
Photoresist
STI
P-epi
USG
N-well
USG
Buried SiO2
P-wafer

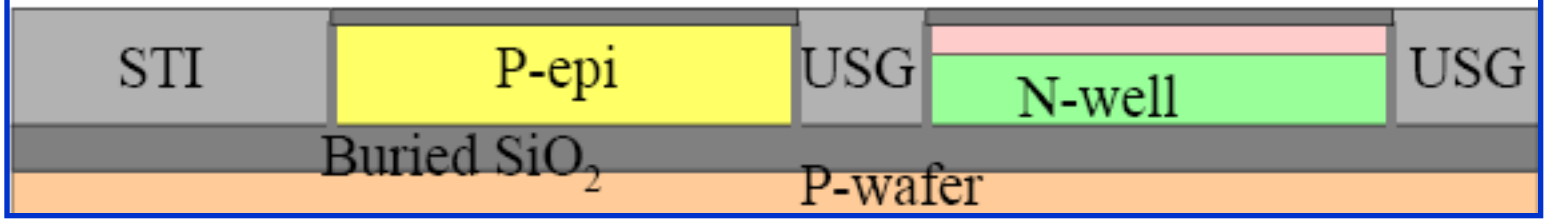
PMOS V_T Adjust Implantation

$$V_{th} = V_{FB} + 2\Phi_F + \frac{\sqrt{2\varepsilon_S q N_A (2\Phi_F)}}{C_{Ox}} + \frac{2Q_I}{C_{Ox}}$$

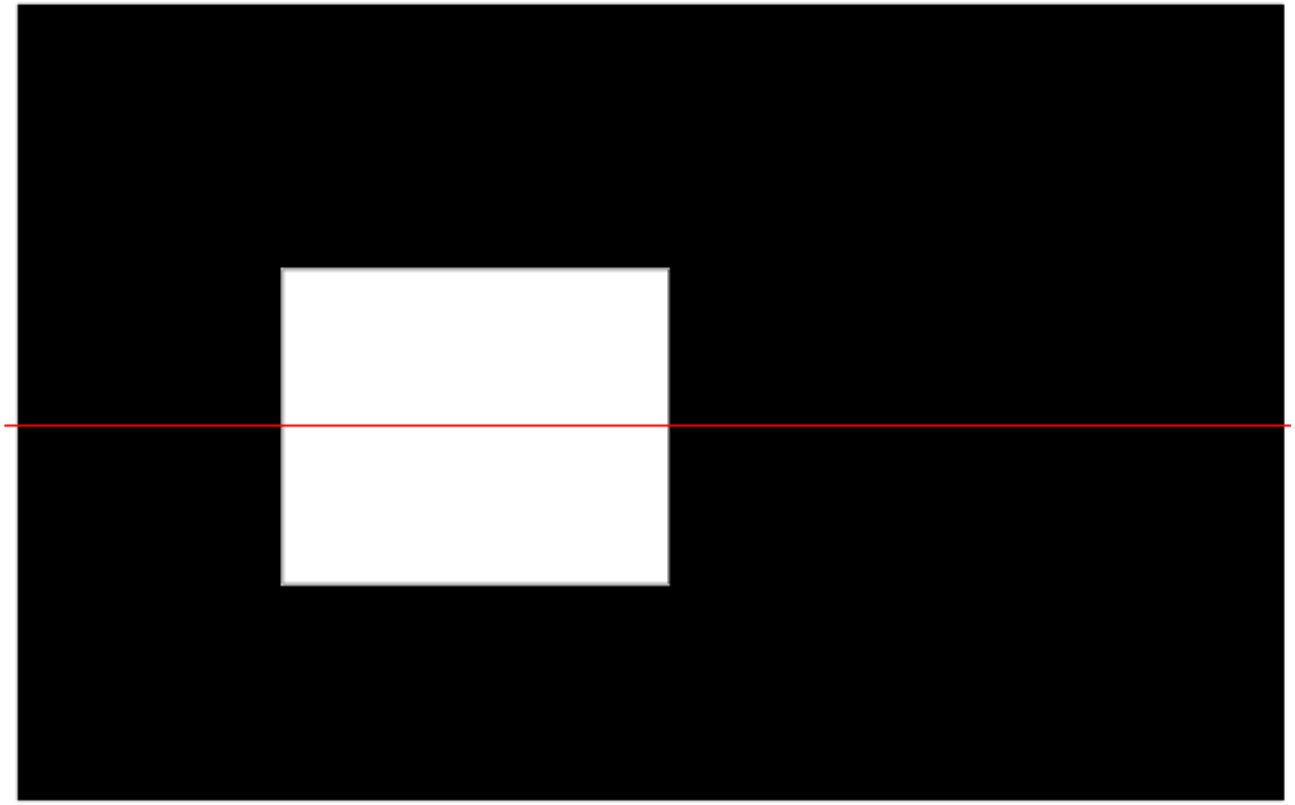
Q_I ion implantation dose (typical dose 10^{11}-10^{12})



Strip Photoresist

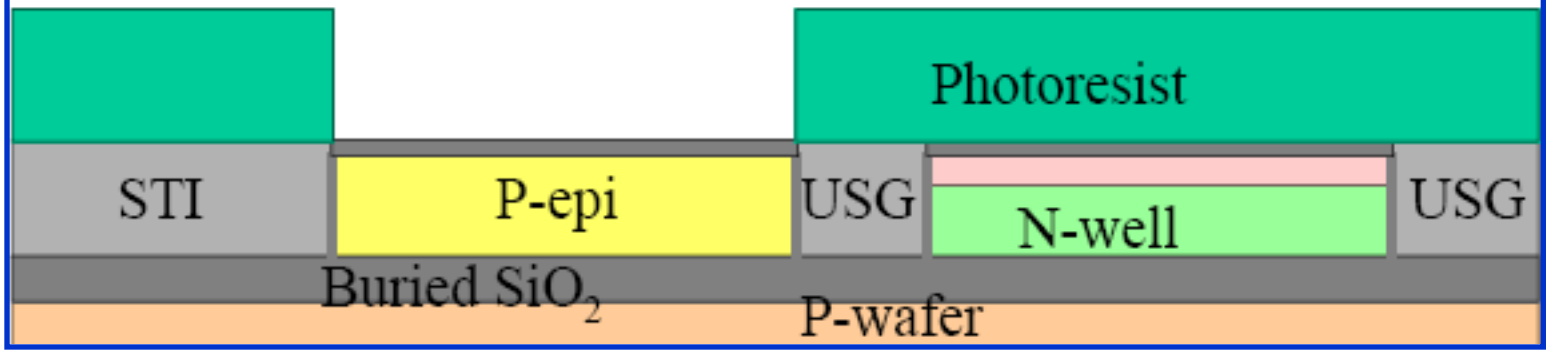


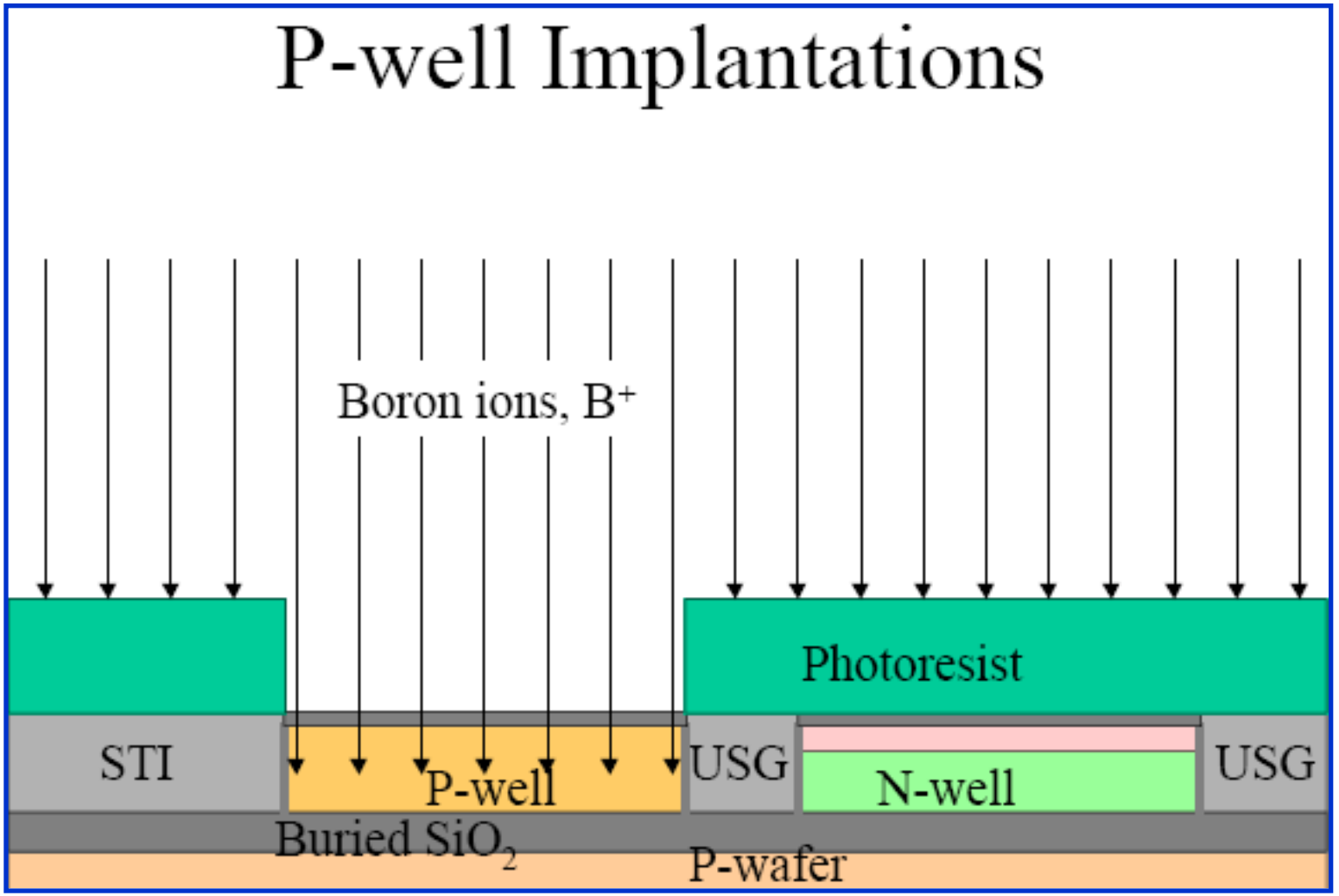
Mask 3: P-well



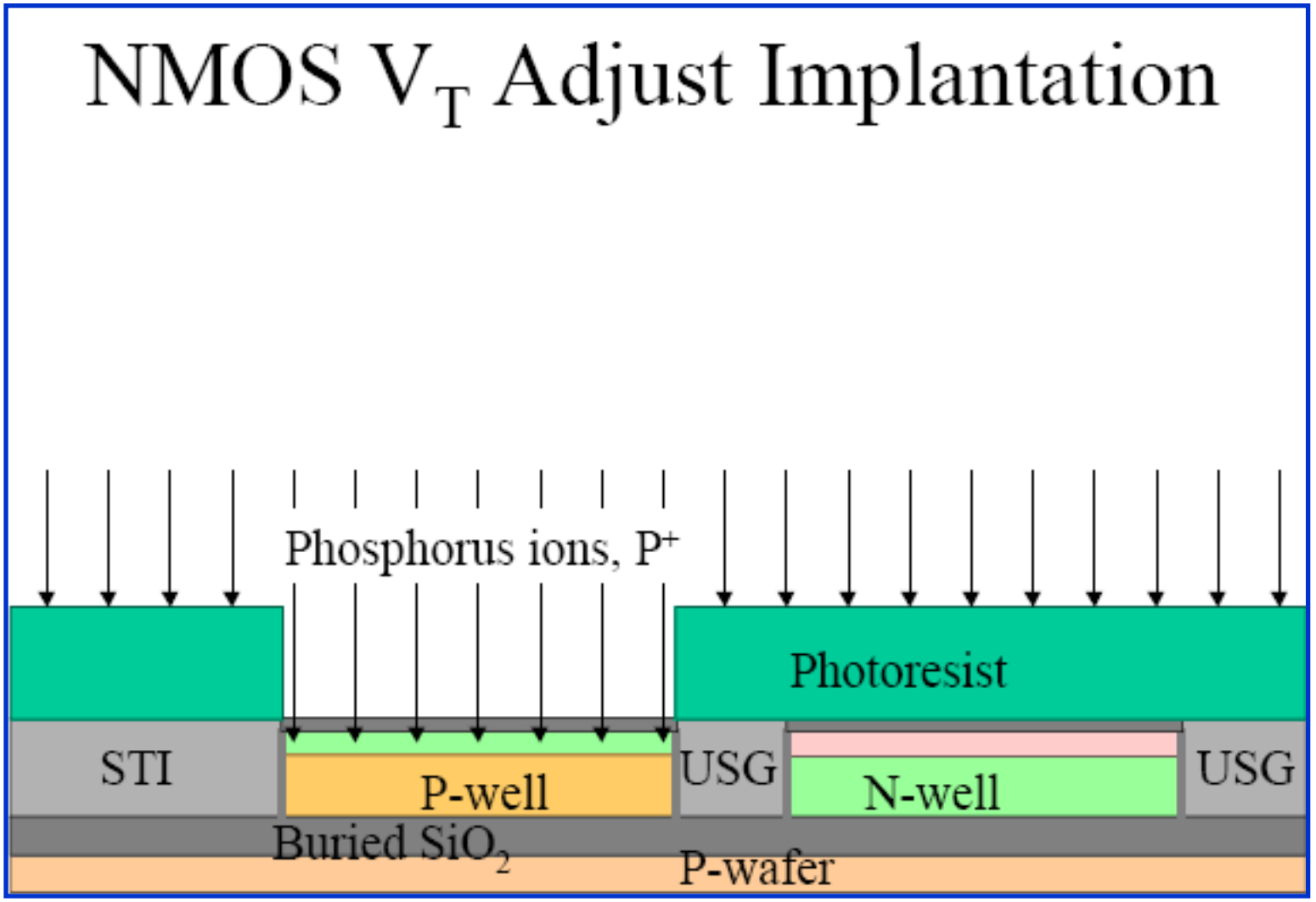
PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

mask3




P-well Implantations
Boron ions, B+
Photoresist
STI
P-well
USG
N-well
USG
Buried SiO2
P-wafer

NMOS V_T Adjust Implantation

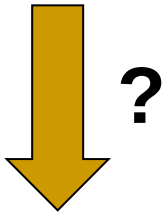


Strip PR & sacrificial oxide
Wafer cleaning

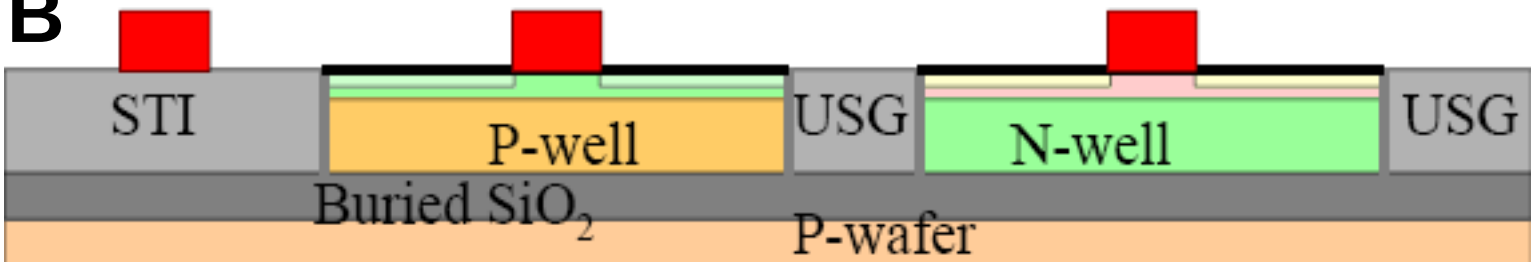
Group Activity 1

How to get from A to B?

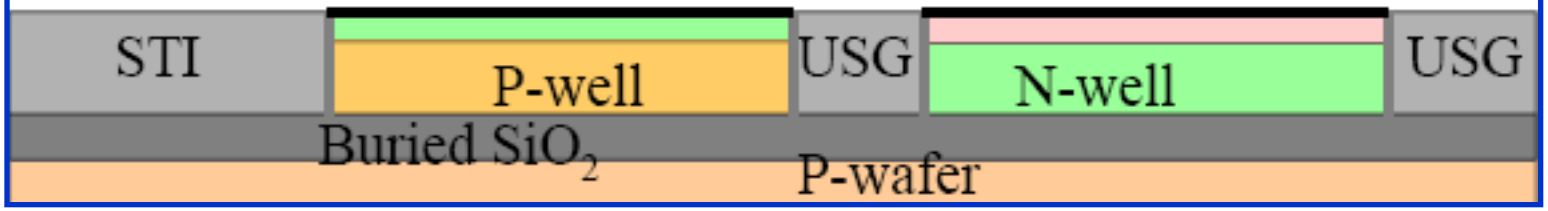
A



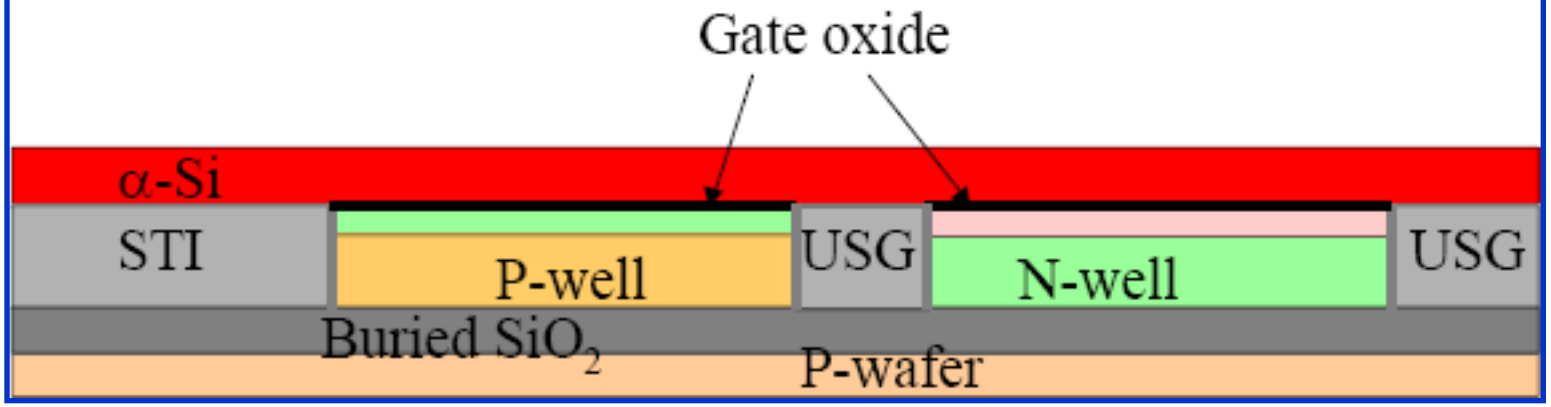
B



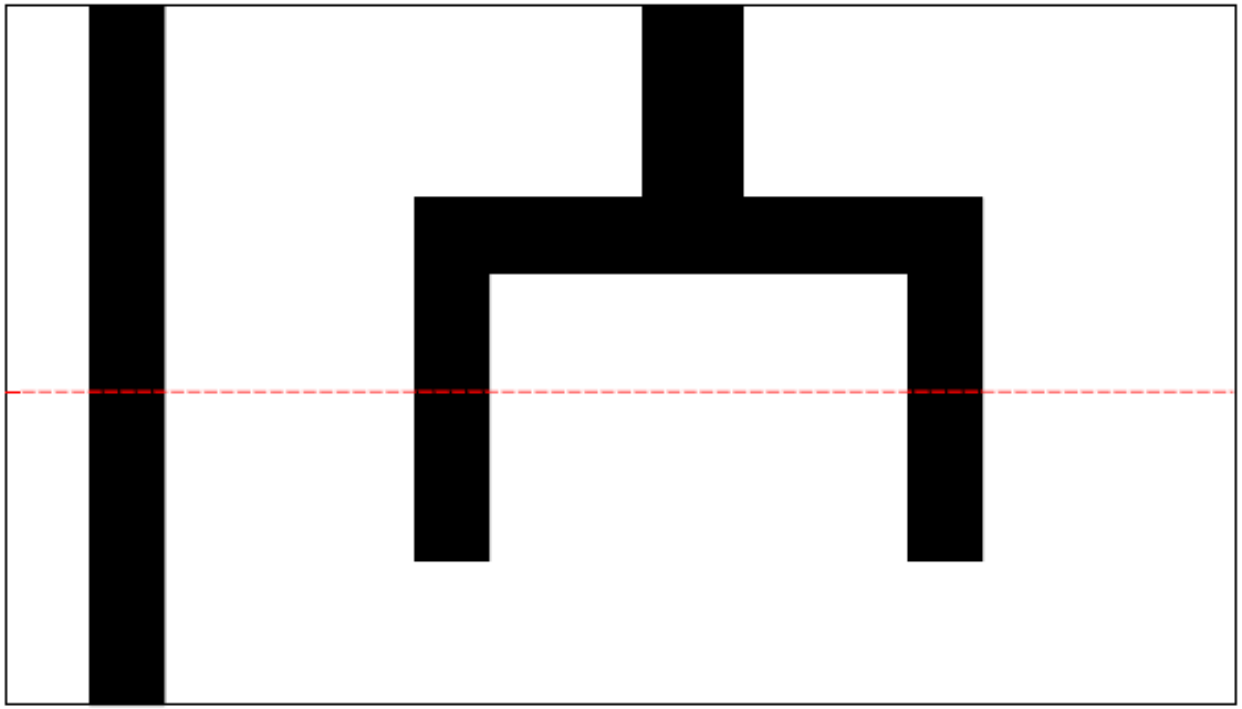
Gate Oxidation



LPCVD Amorphous Silicon



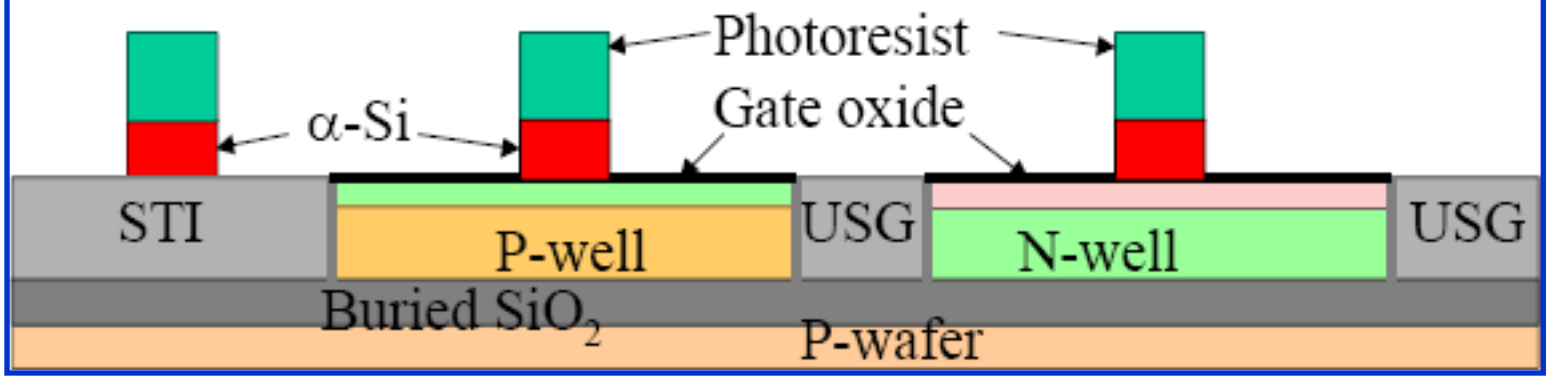
Mask 4, Gate and Local Interconnection



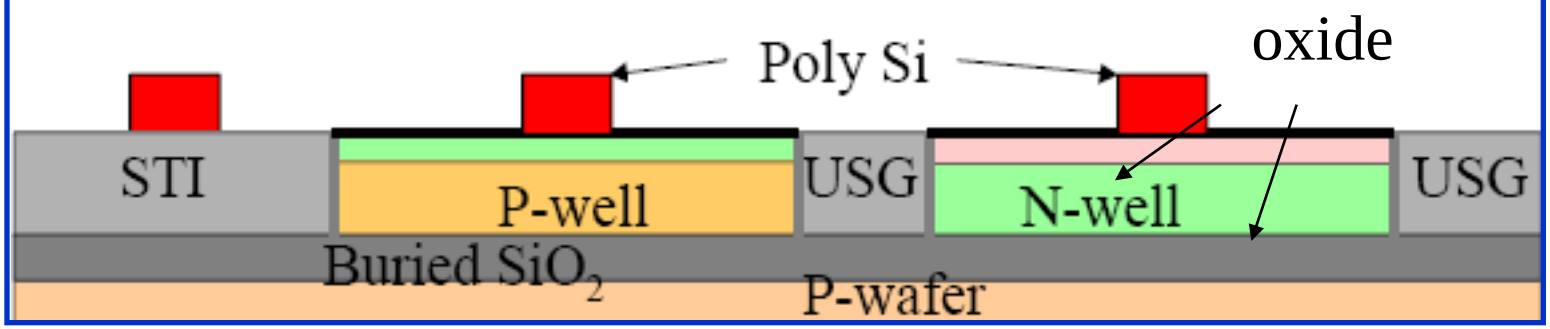
PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

α-Si etching

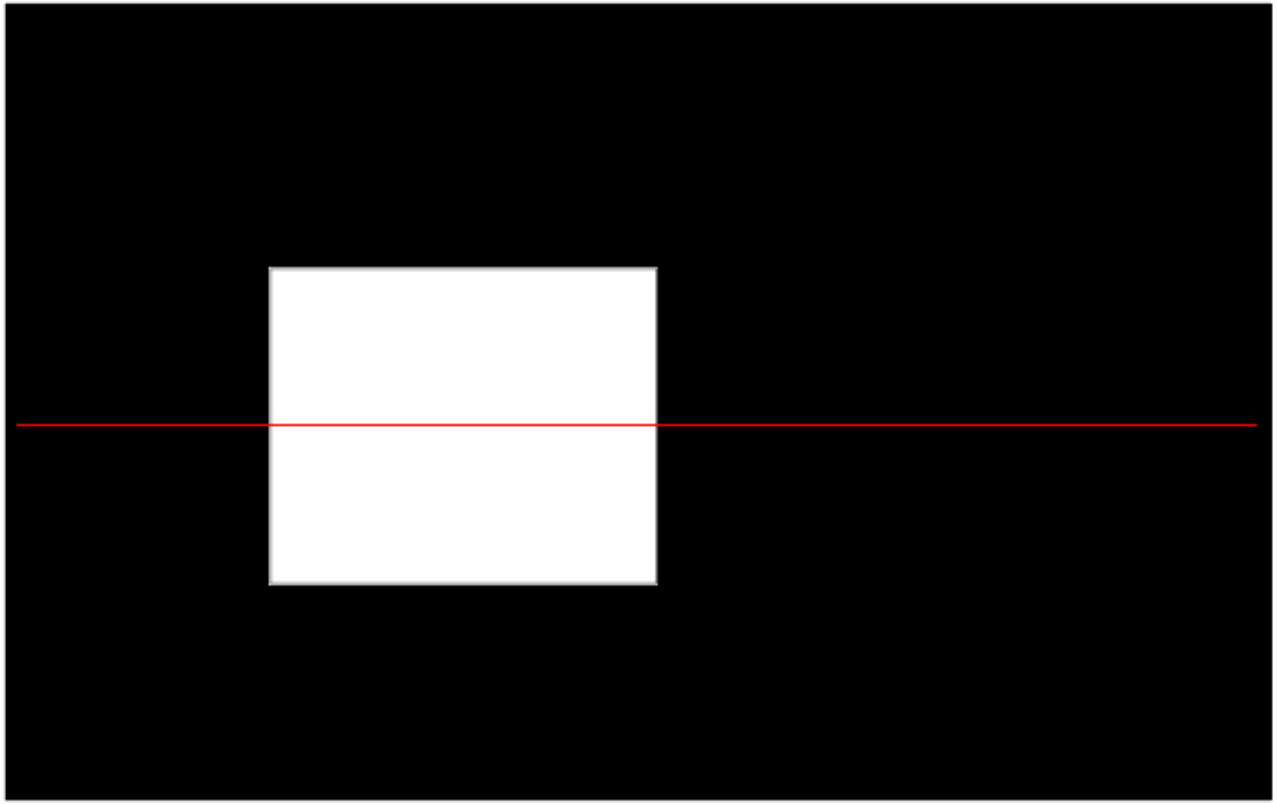
mask4



Strip PR, wafer cleaning, α-Si annealing and oxidation

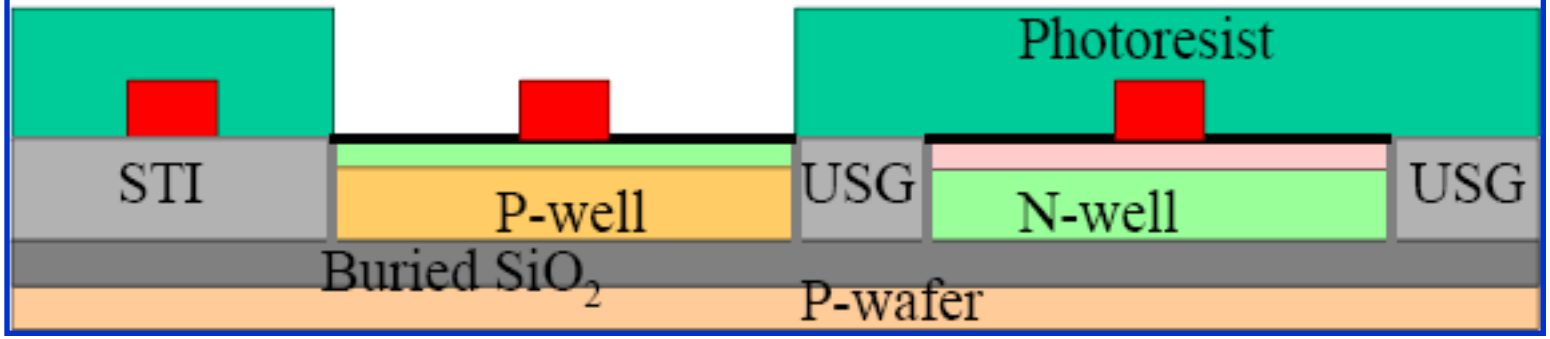


Mask 5, NMOS LDD Implantation

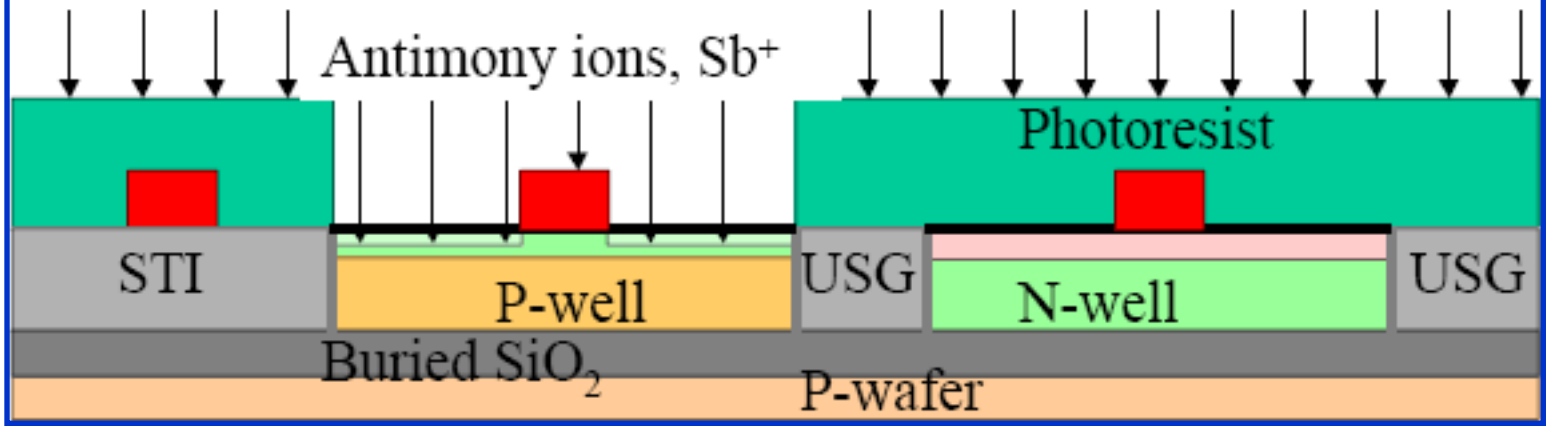


PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

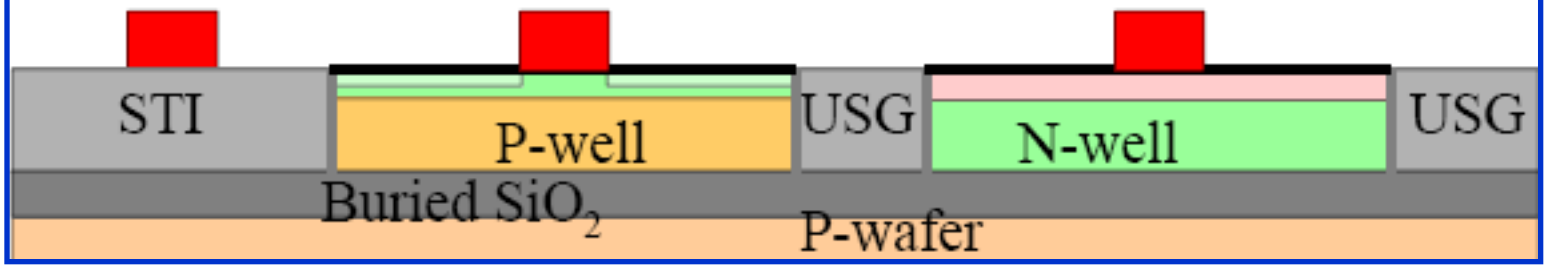
mask5



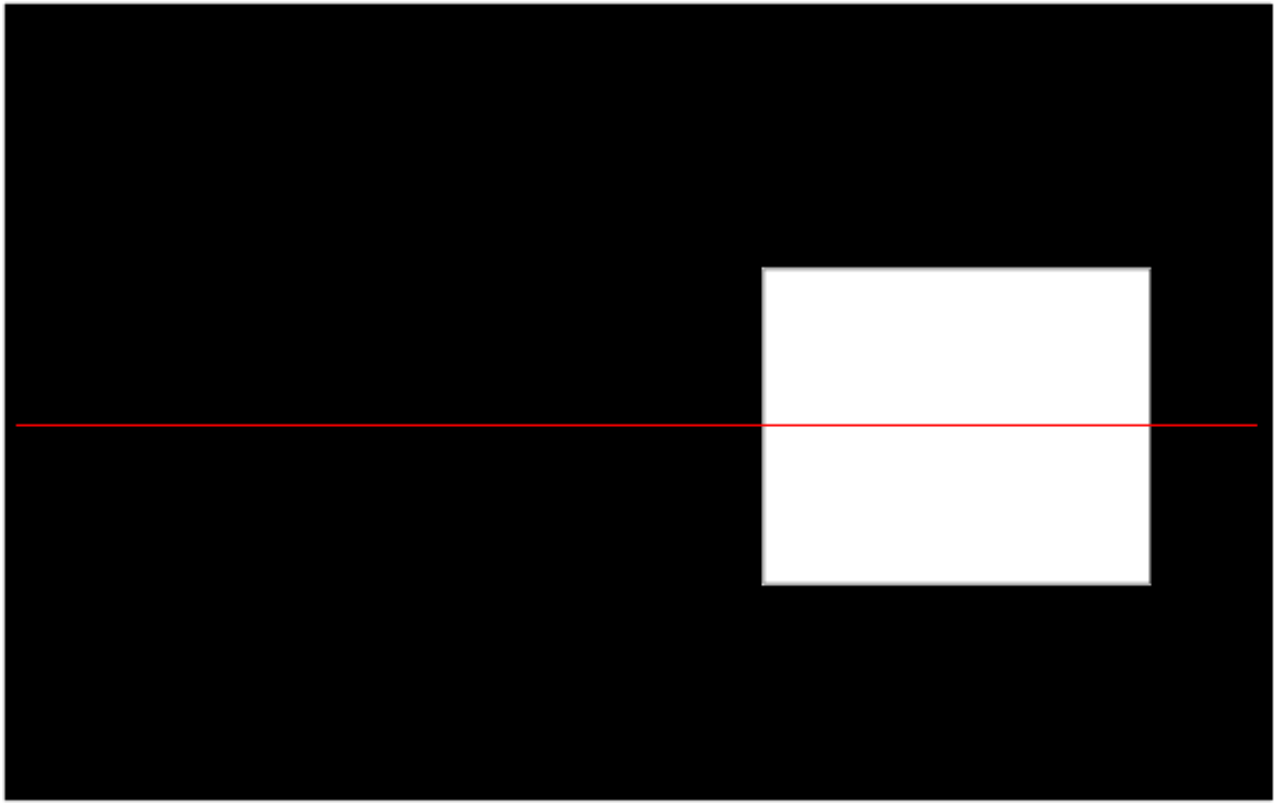
NMOS LDD Implantation



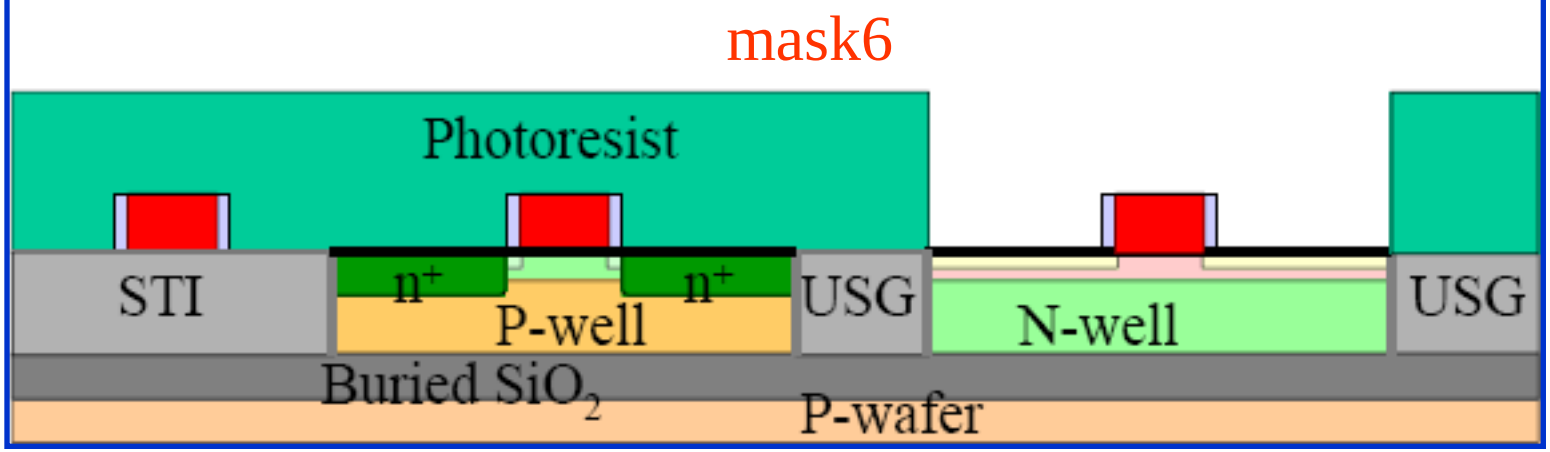
Strip Photoresist

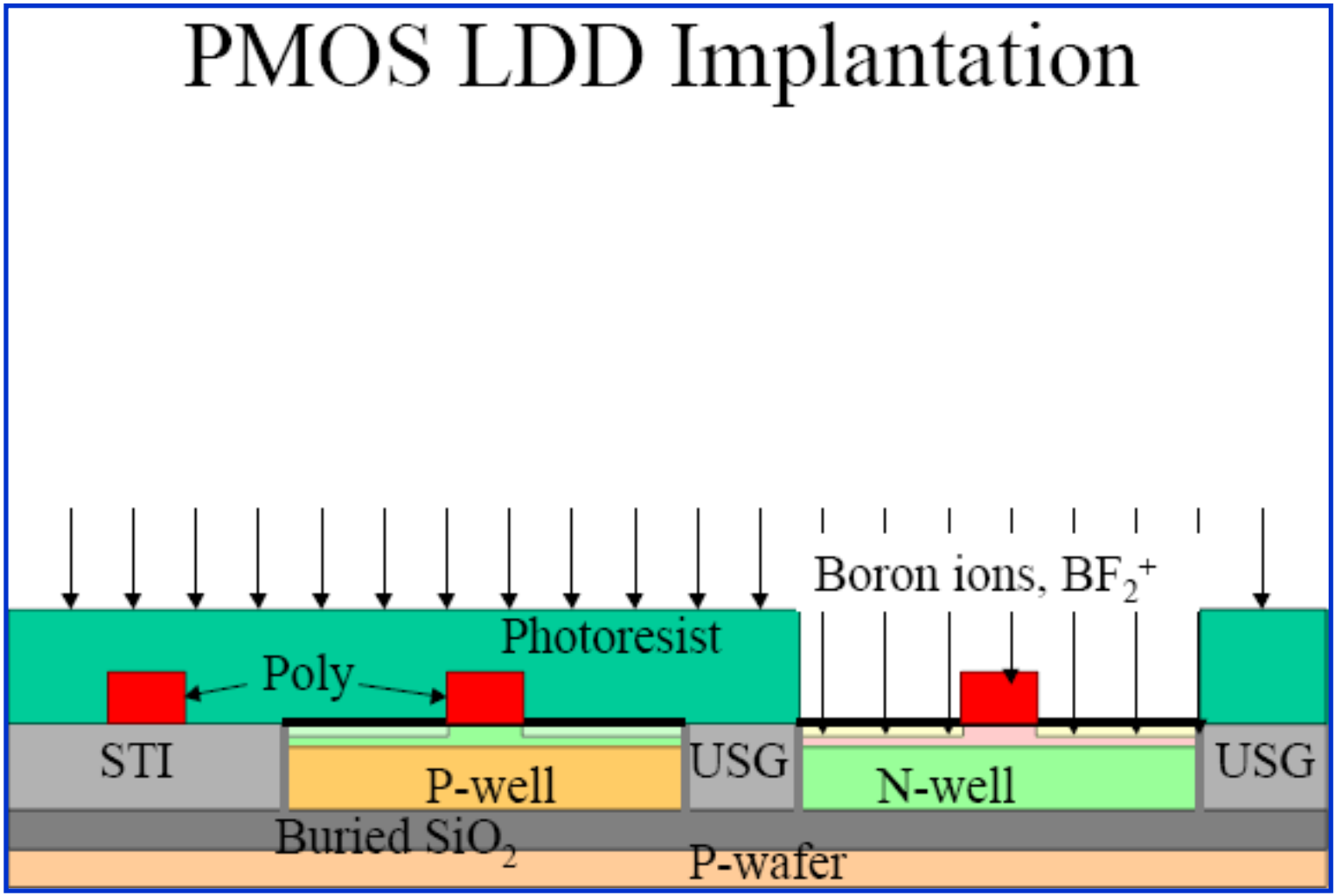


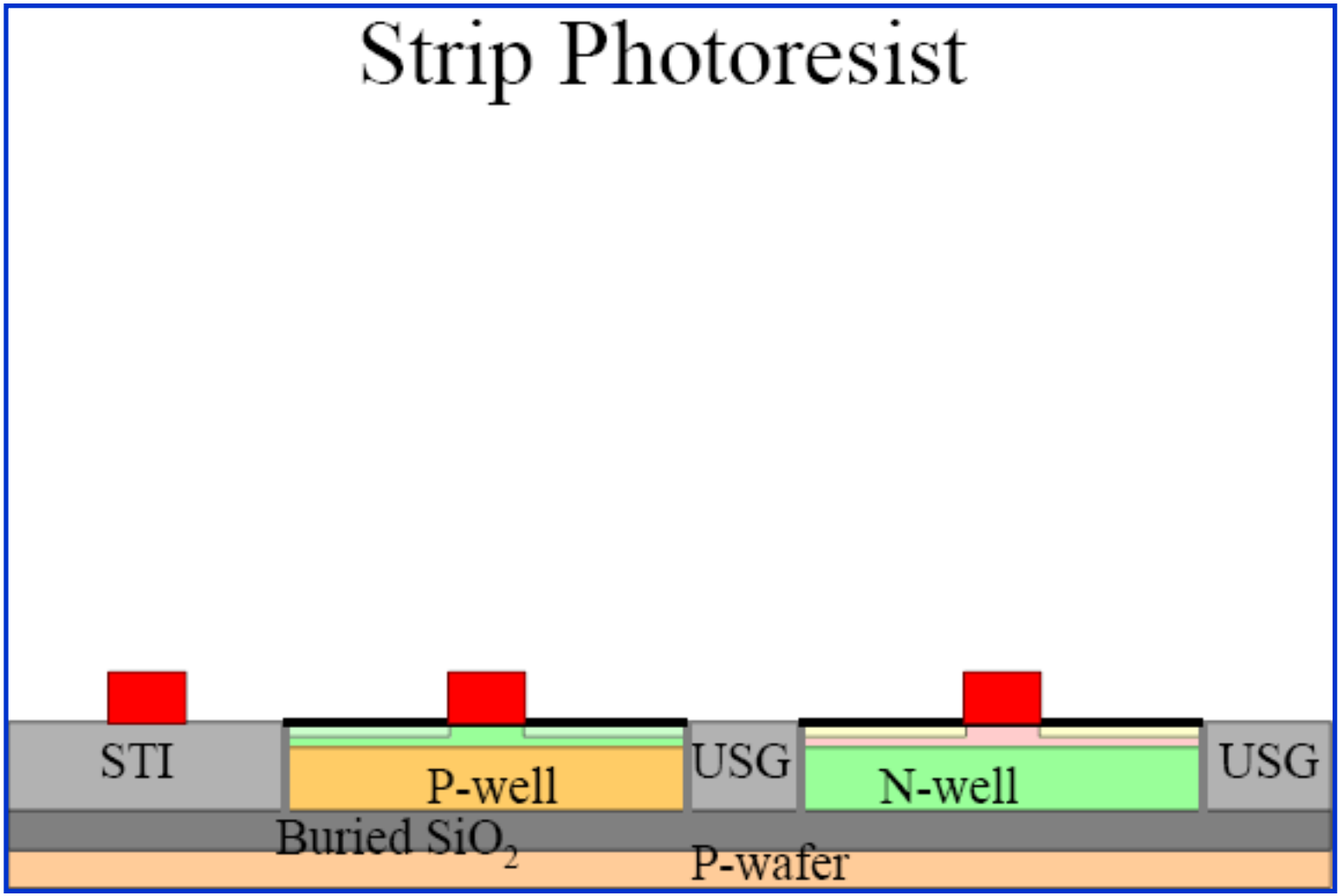
Mask 6: PMOS LDD Implantation



PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

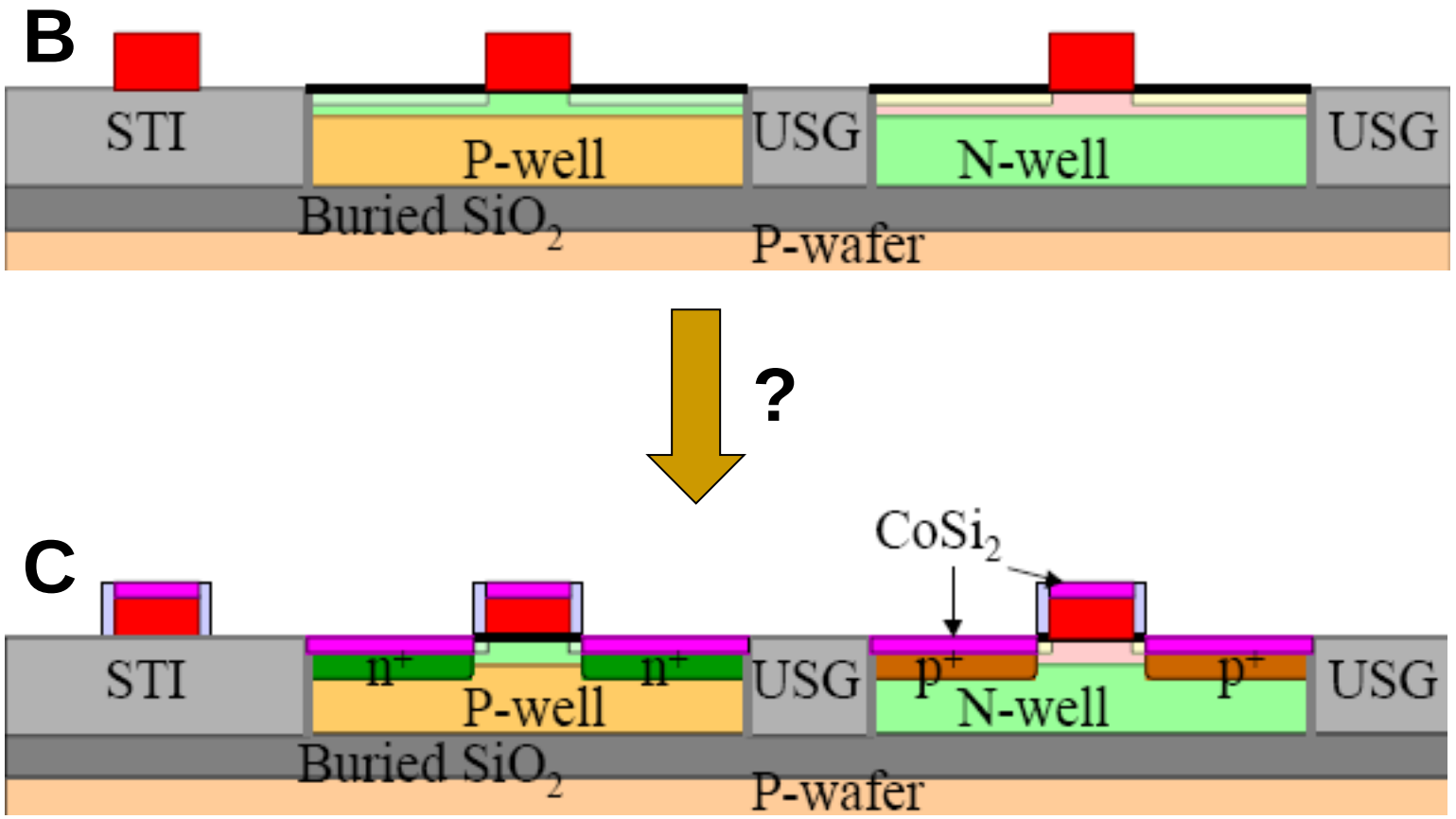



PMOS LDD Implantation
Boron ions, BF_2^+
Photoresist
Poly
STI
P-well
USG
N-well
USG
Buried SiO_2
P-wafer

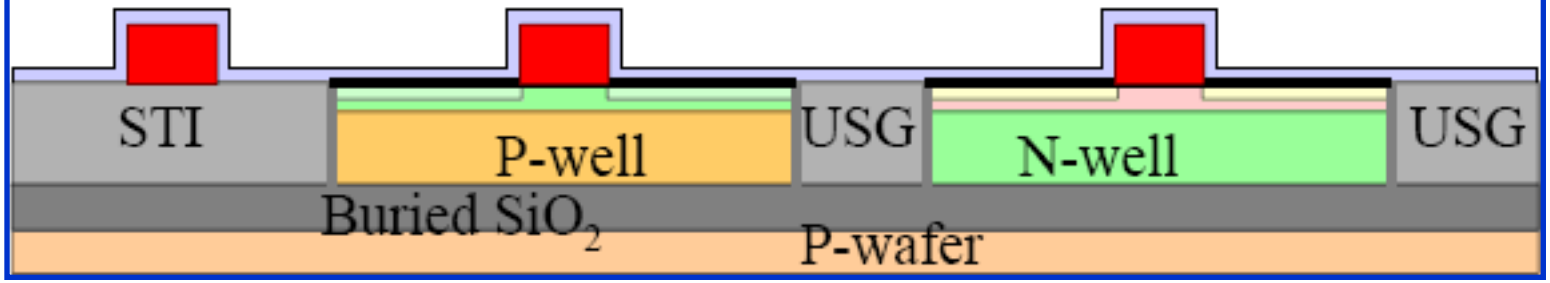

Strip Photoresist
STI
P-well
USG
N-well
USG
Buried SiO2
P-wafer

Group Activity 2

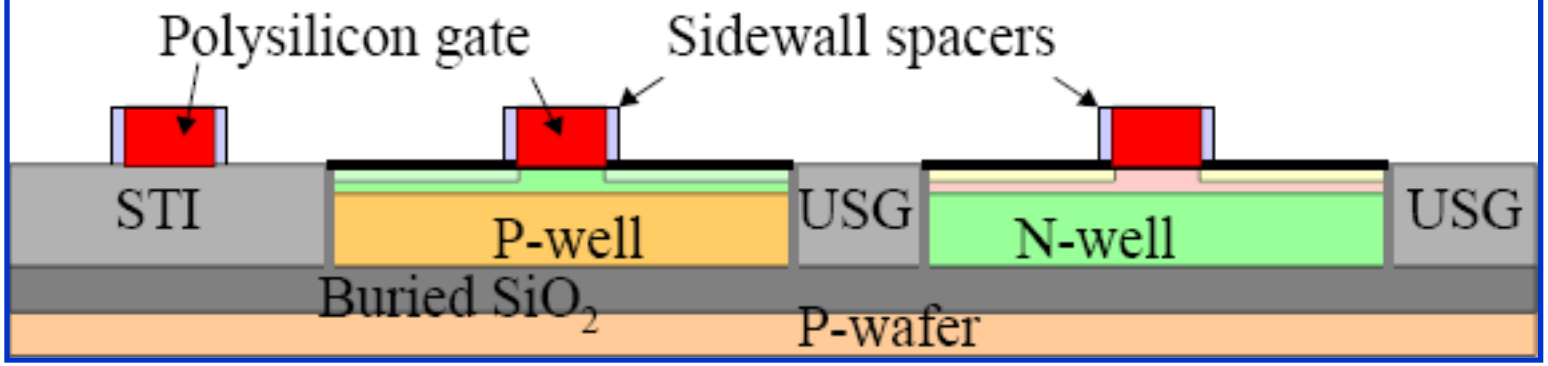
How to get from B to C?



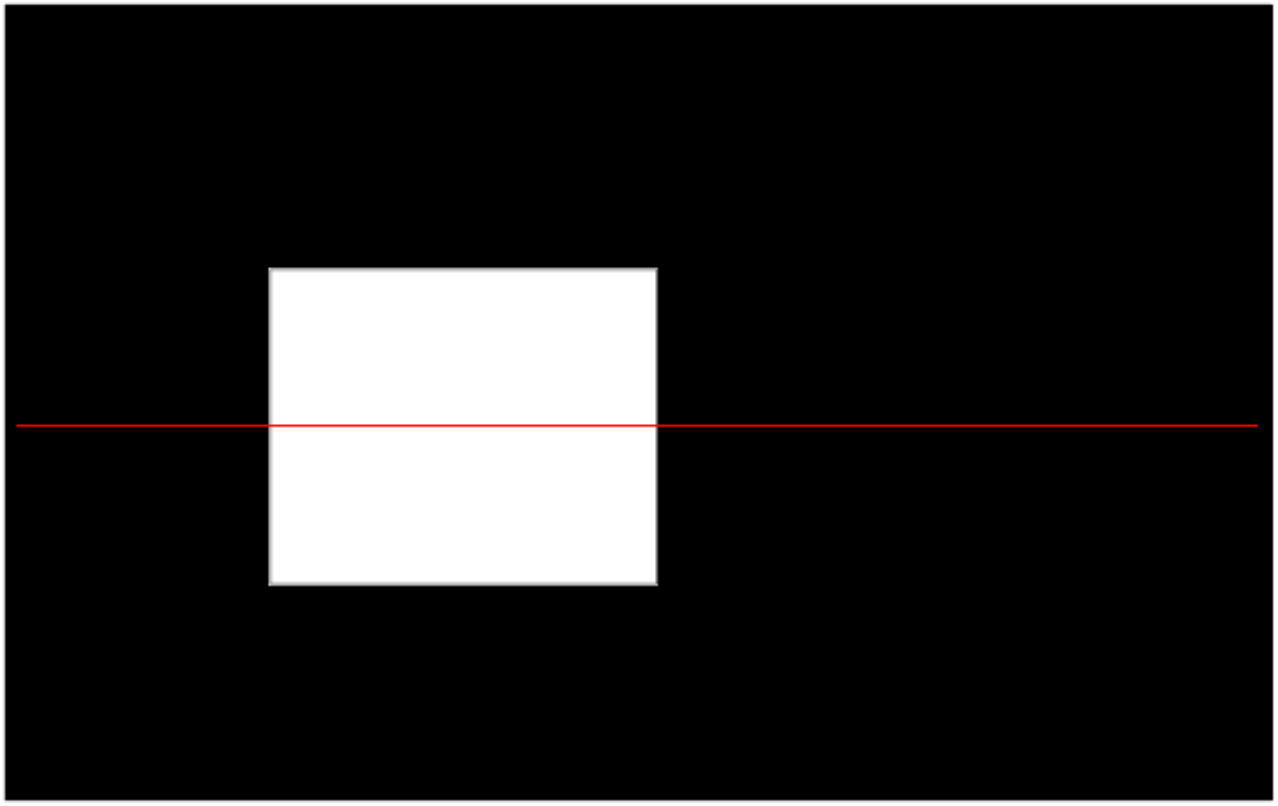
CVD USG, CVD Nitride



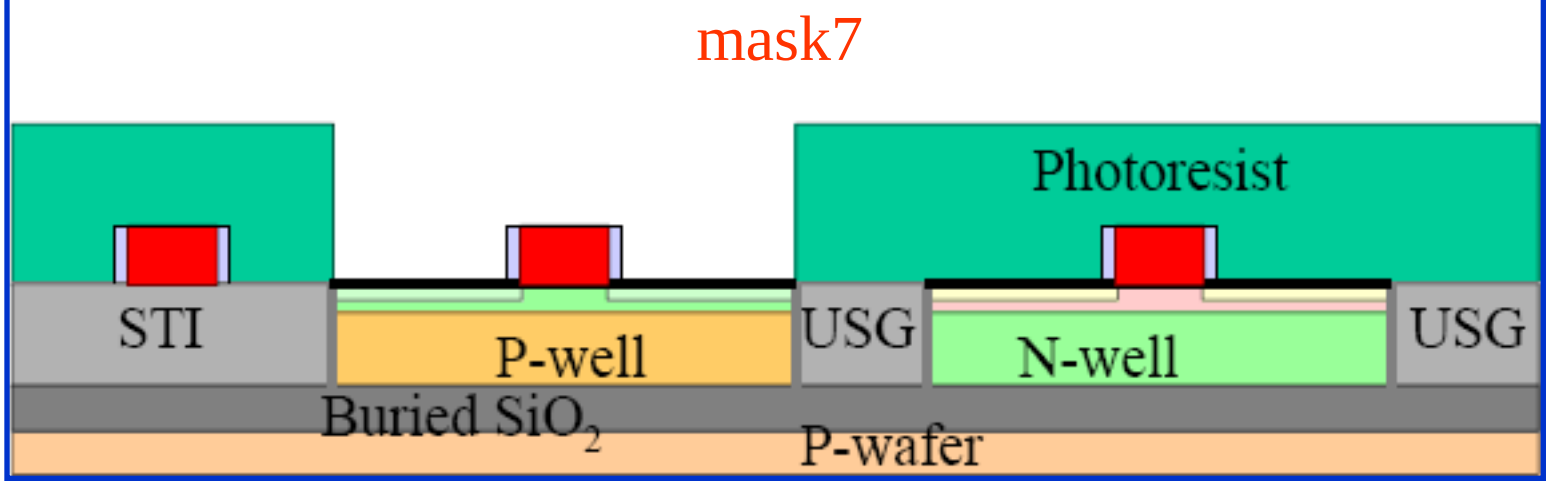
Nitride and USG Etchback



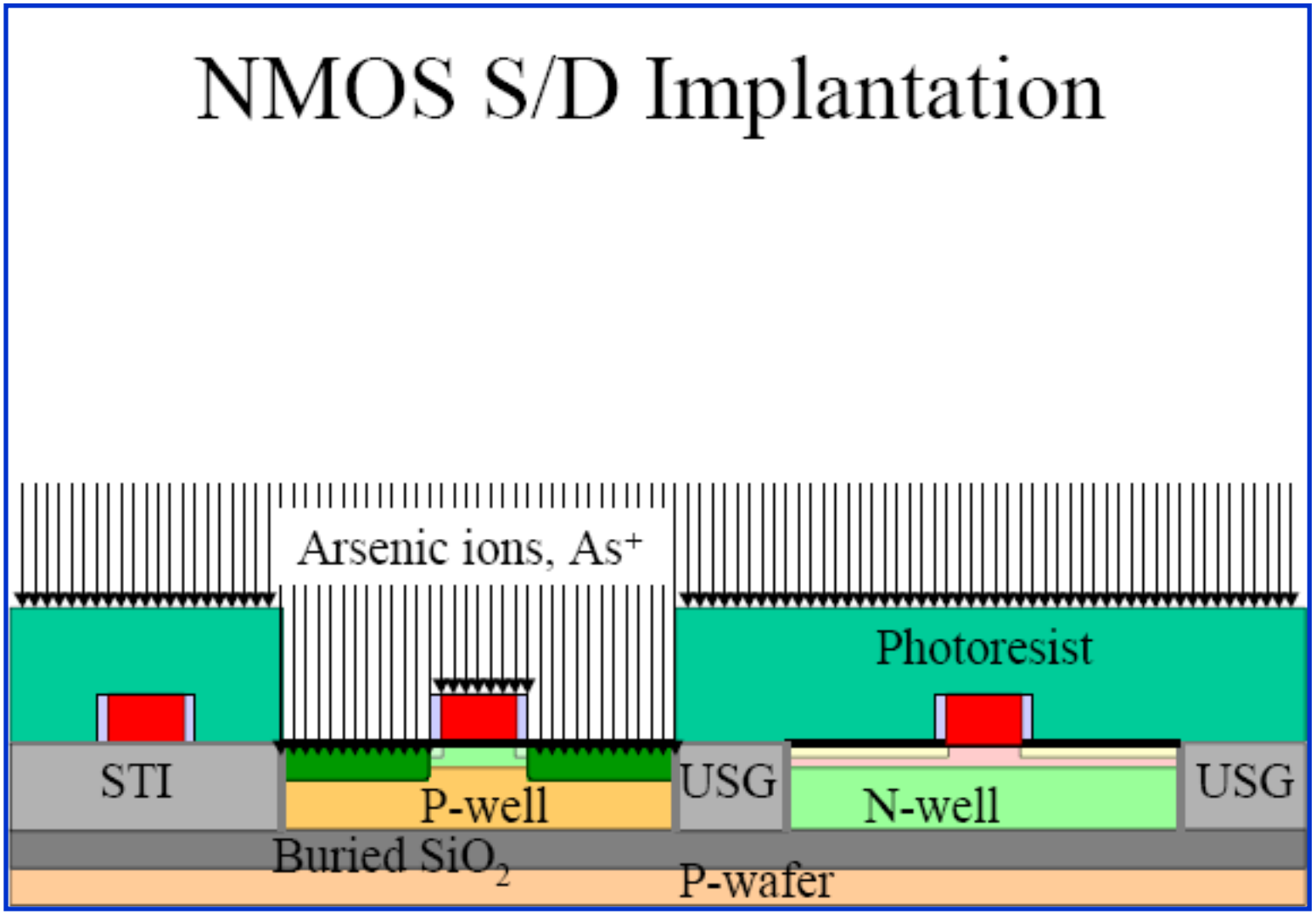
Mask 7, NMOS S/D Implantation

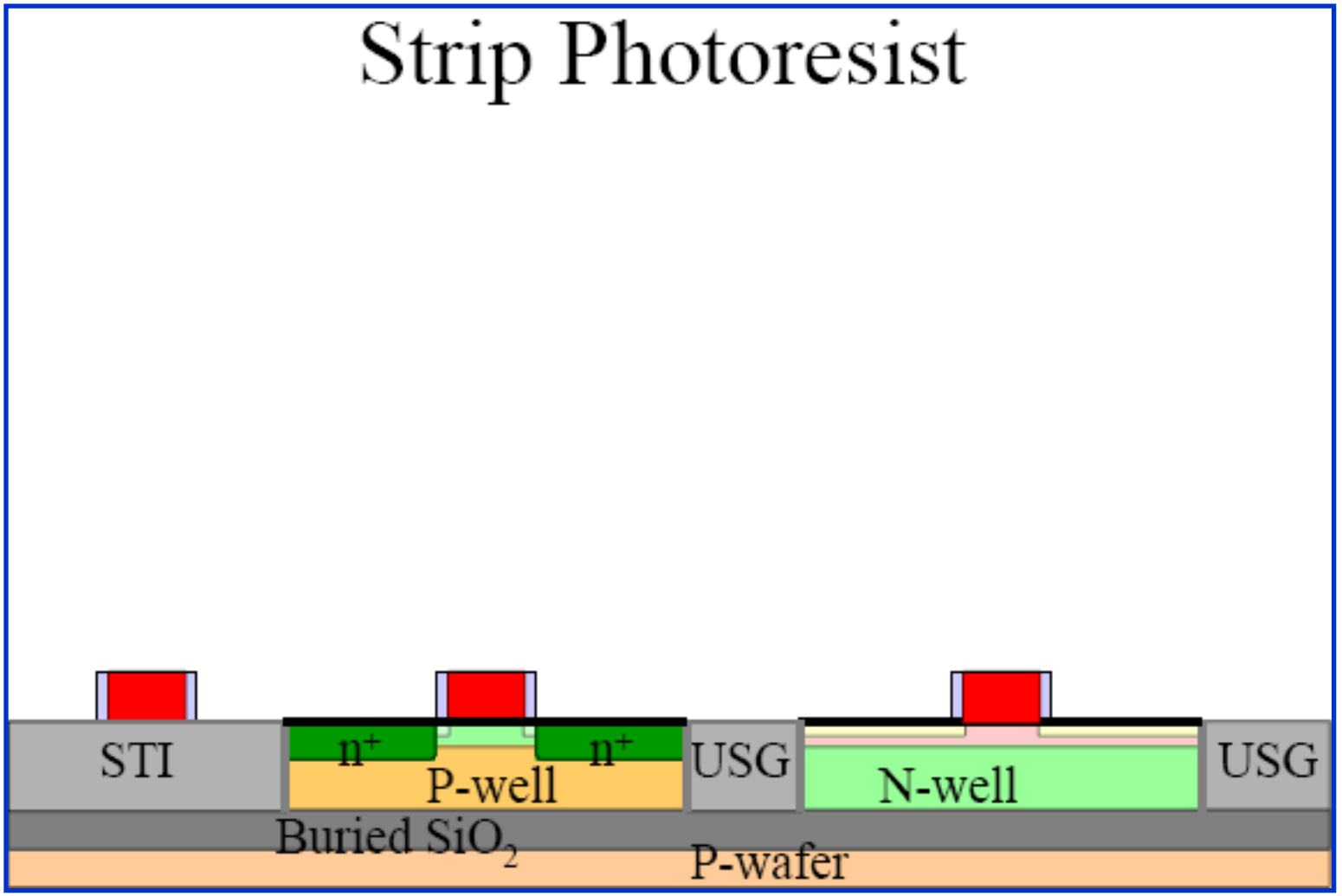


PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

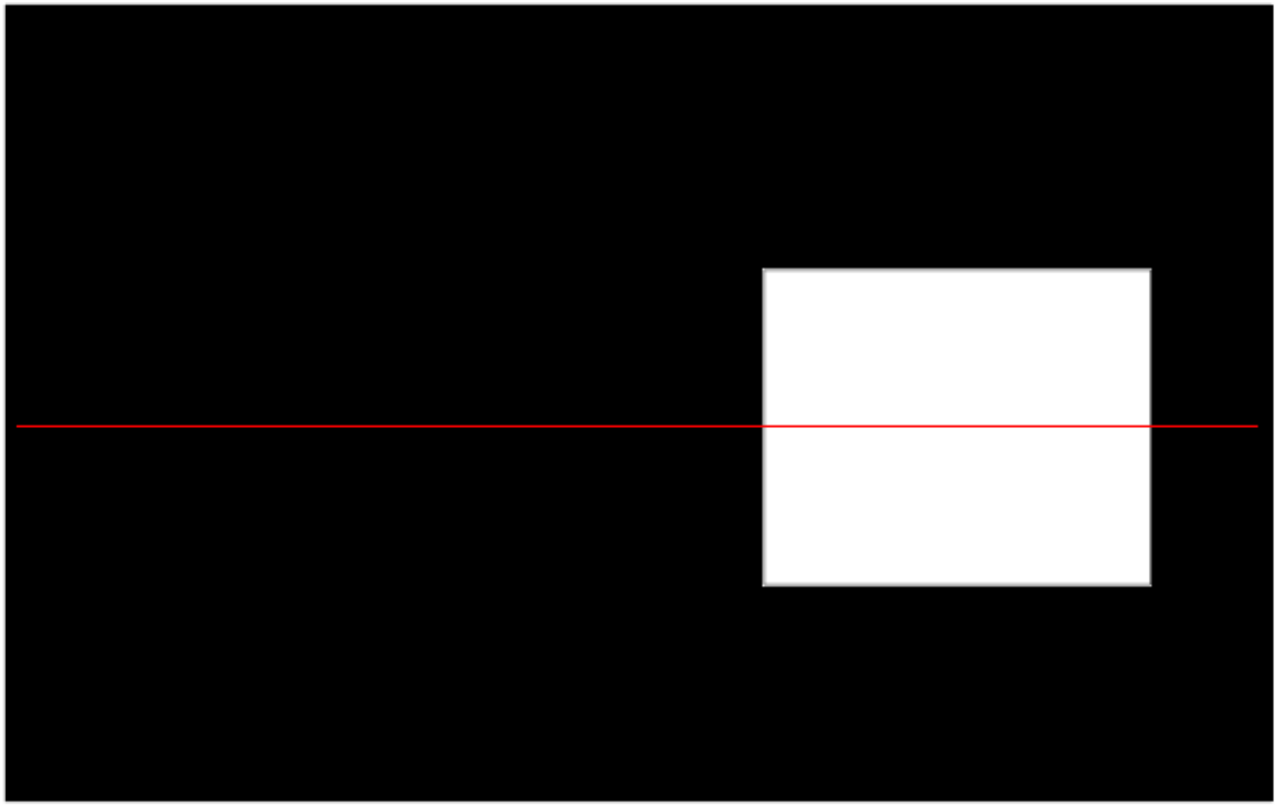


NMOS S/D Implantation



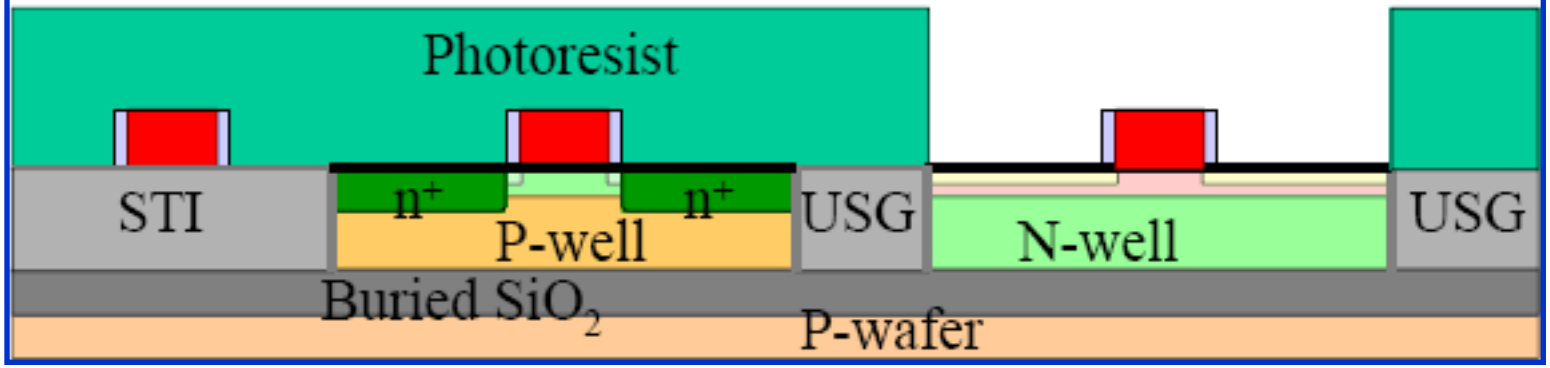

Strip Photoresist
STI
n+
n+
P-well
USG
N-well
USG
Buried SiO2
P-wafer

Mask 8, PMOS S/D Implantation

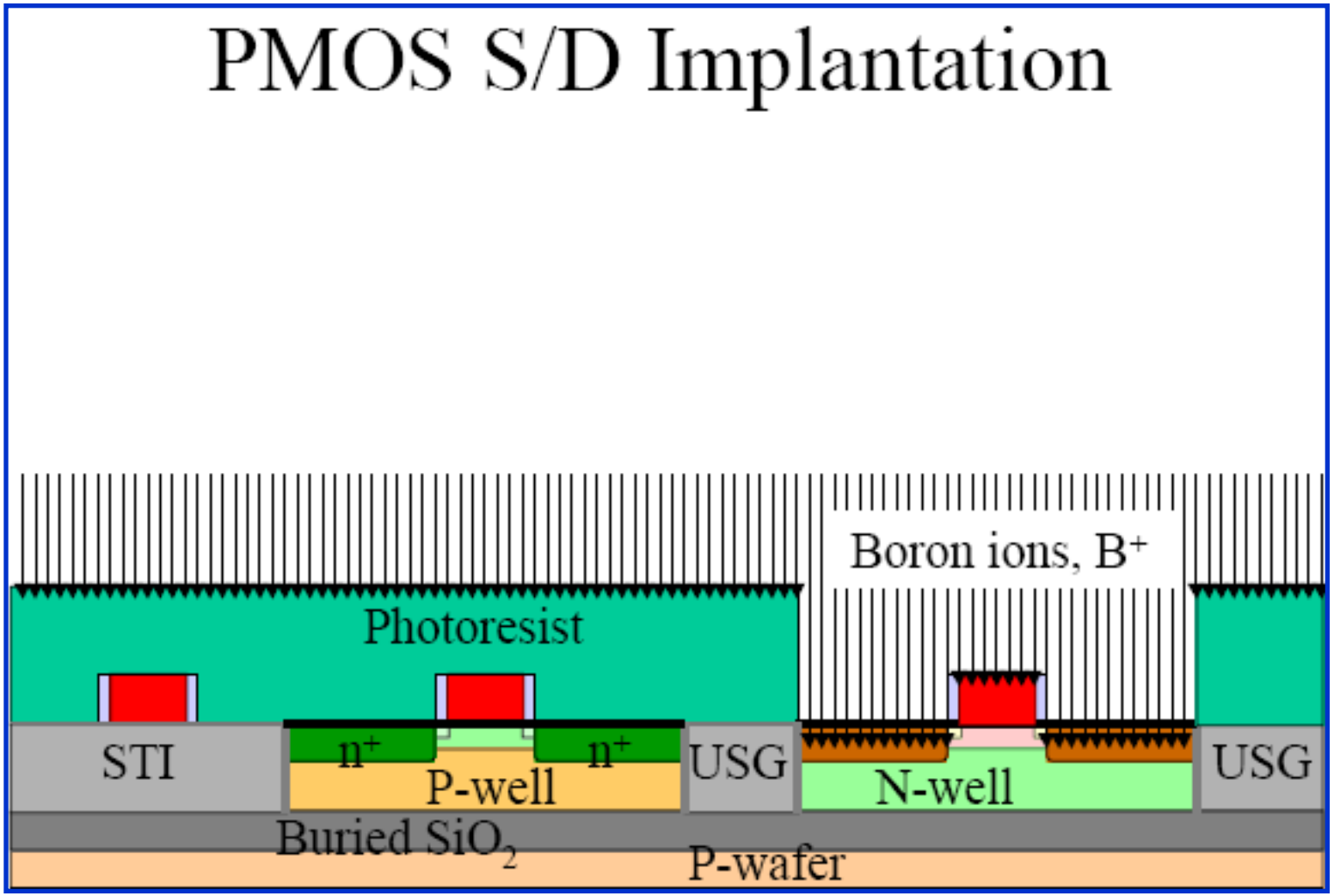


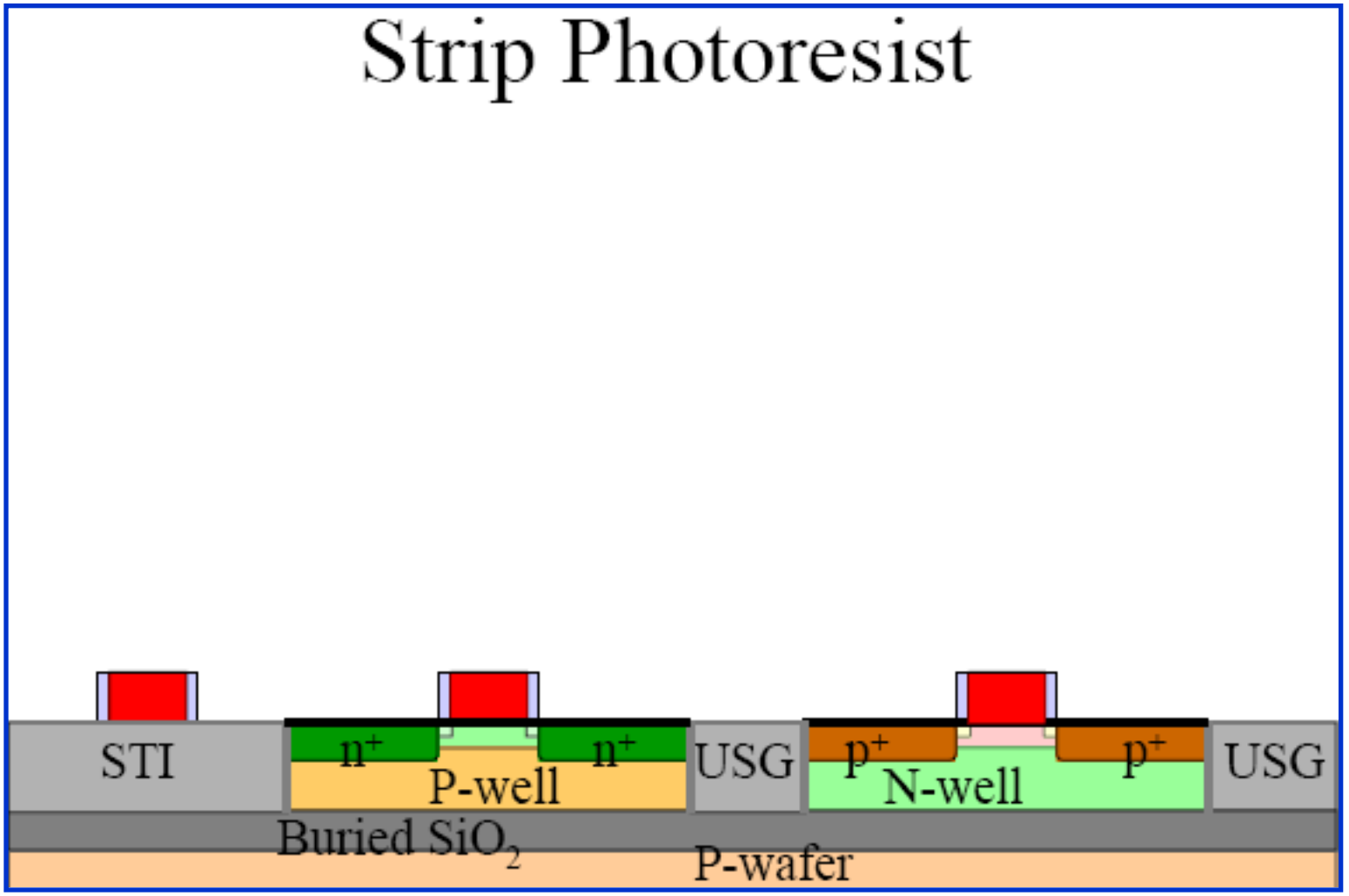
PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

mask8

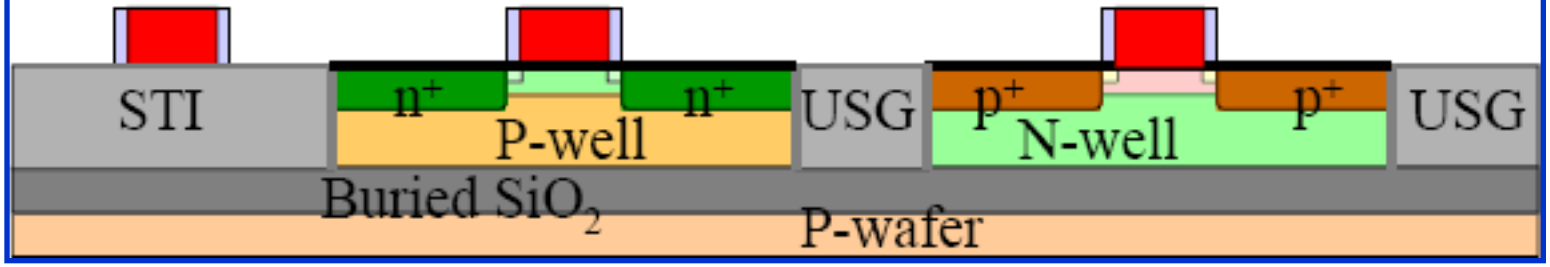


PMOS S/D Implantation

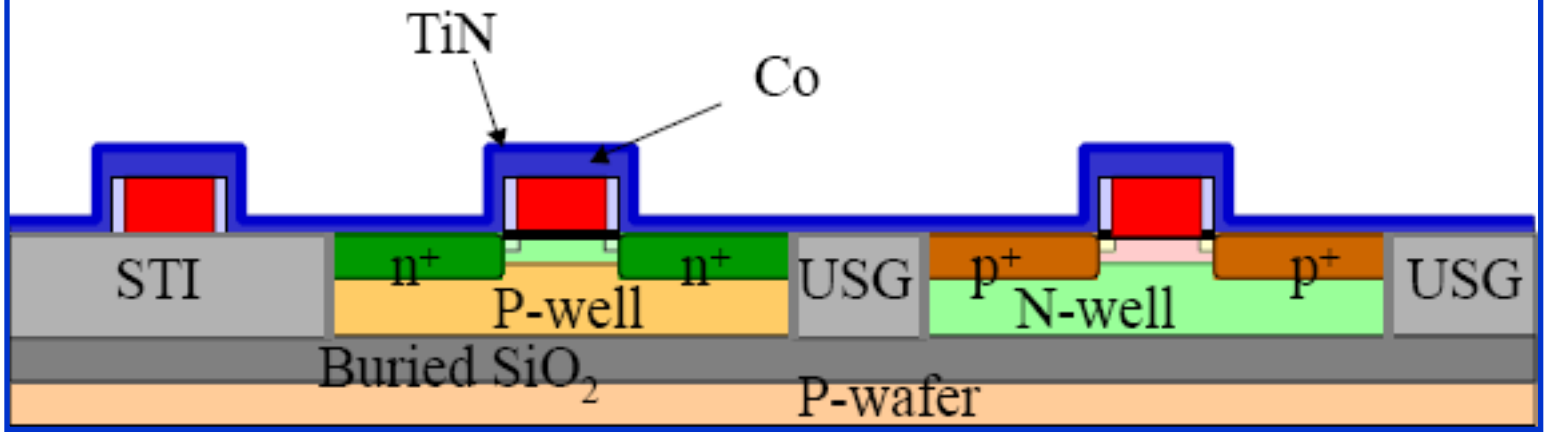



Strip Photoresist
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer

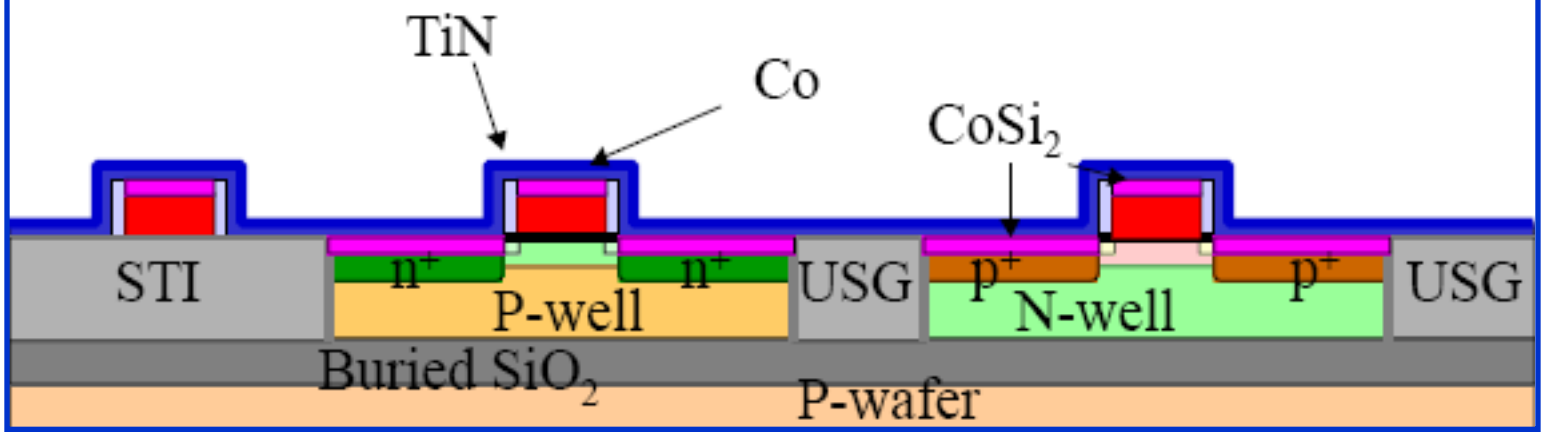
Rapid Thermal Annealing



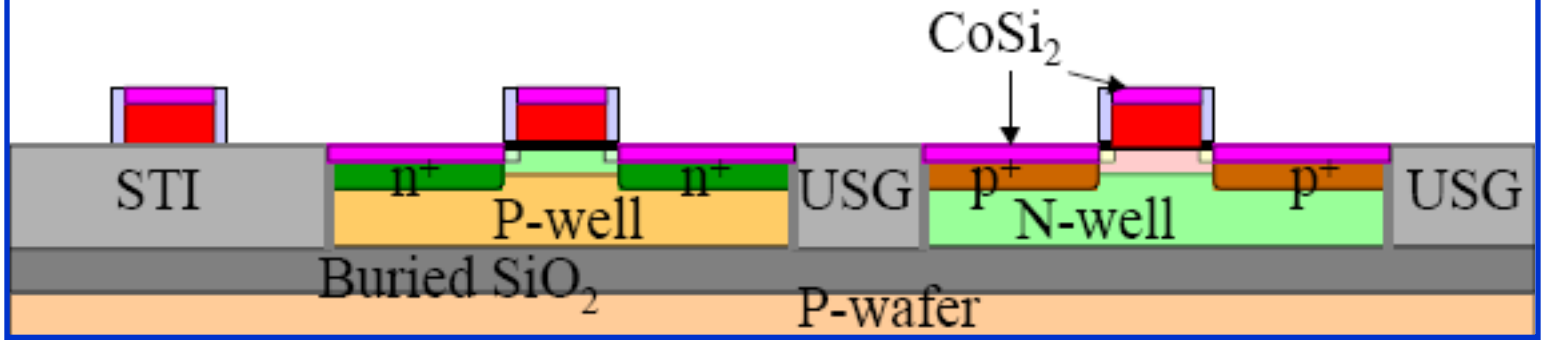
Ar Sputtering etching (SiO_2 and Cleaning)
Co and TiN Sputtering Deposition

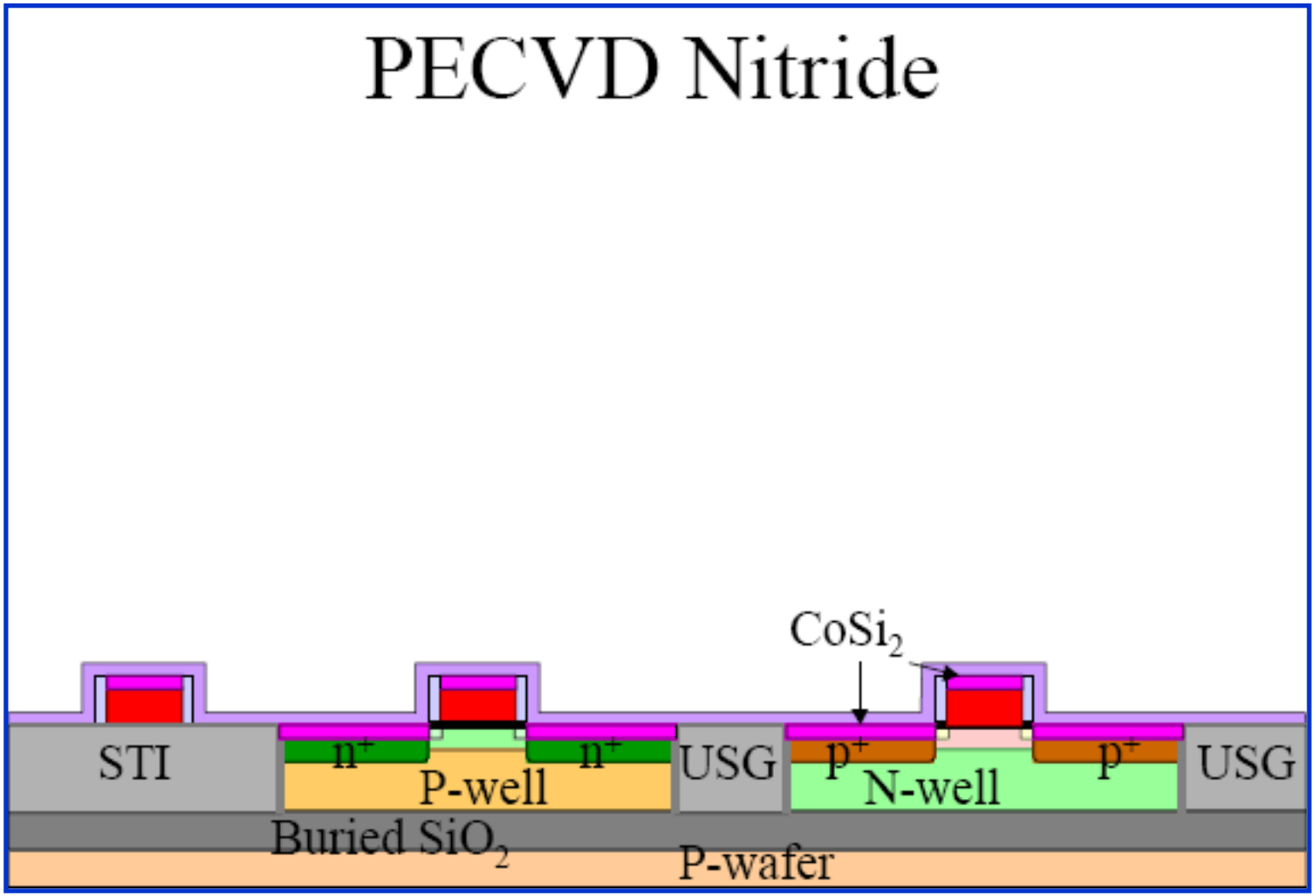


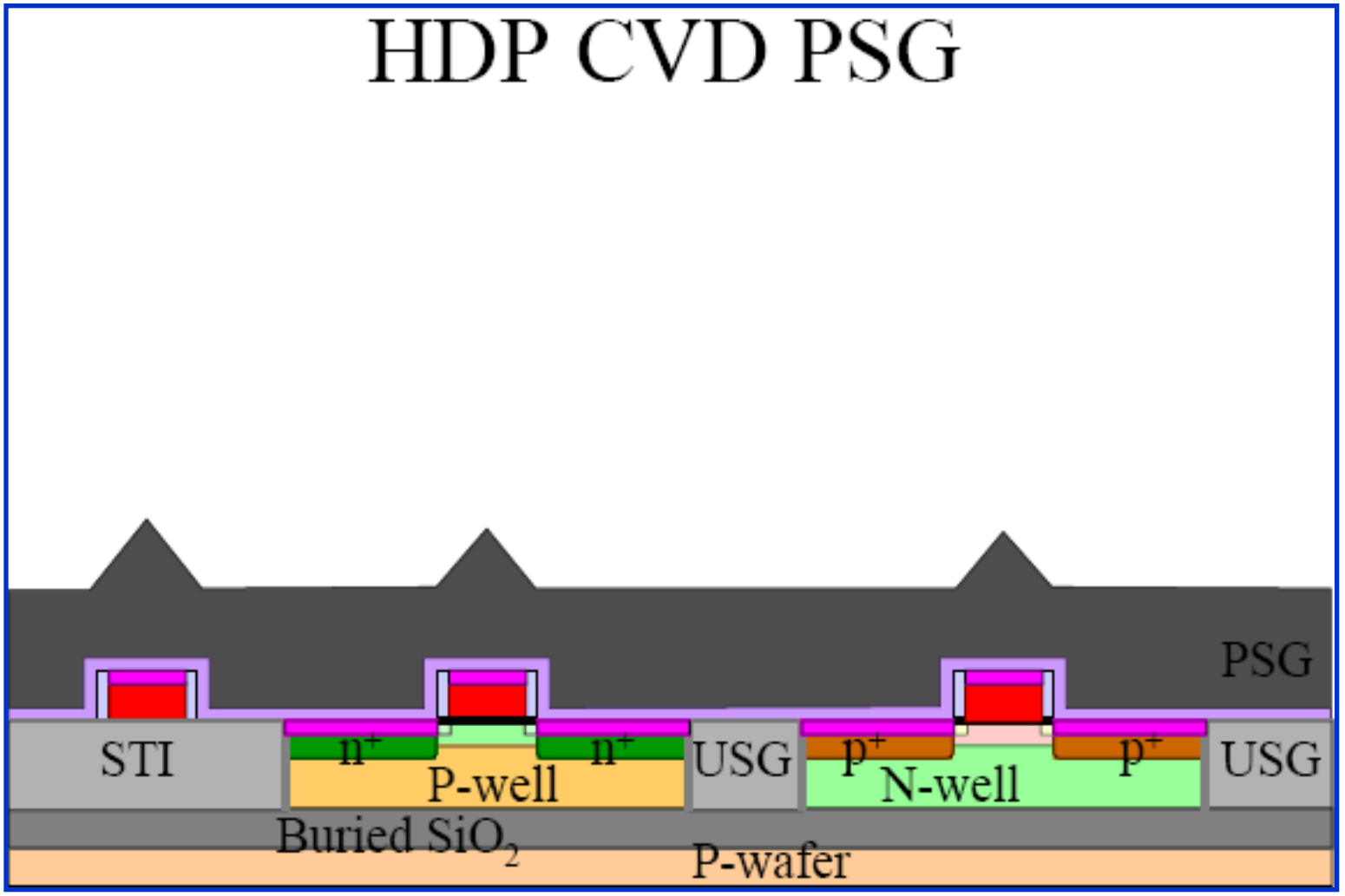
Rapid Thermal Annealing

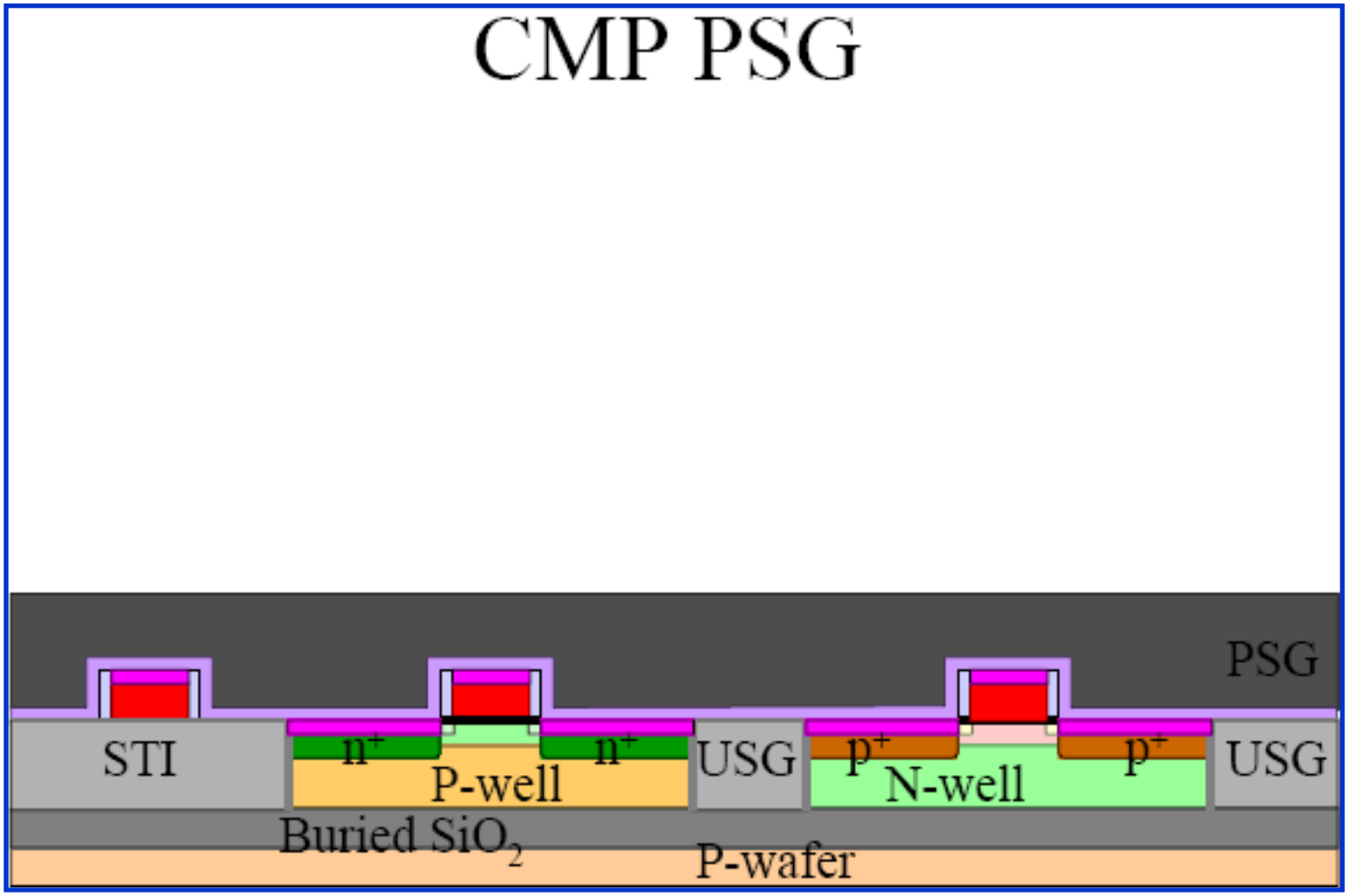


Strip Titanium Nitride and Cobalt

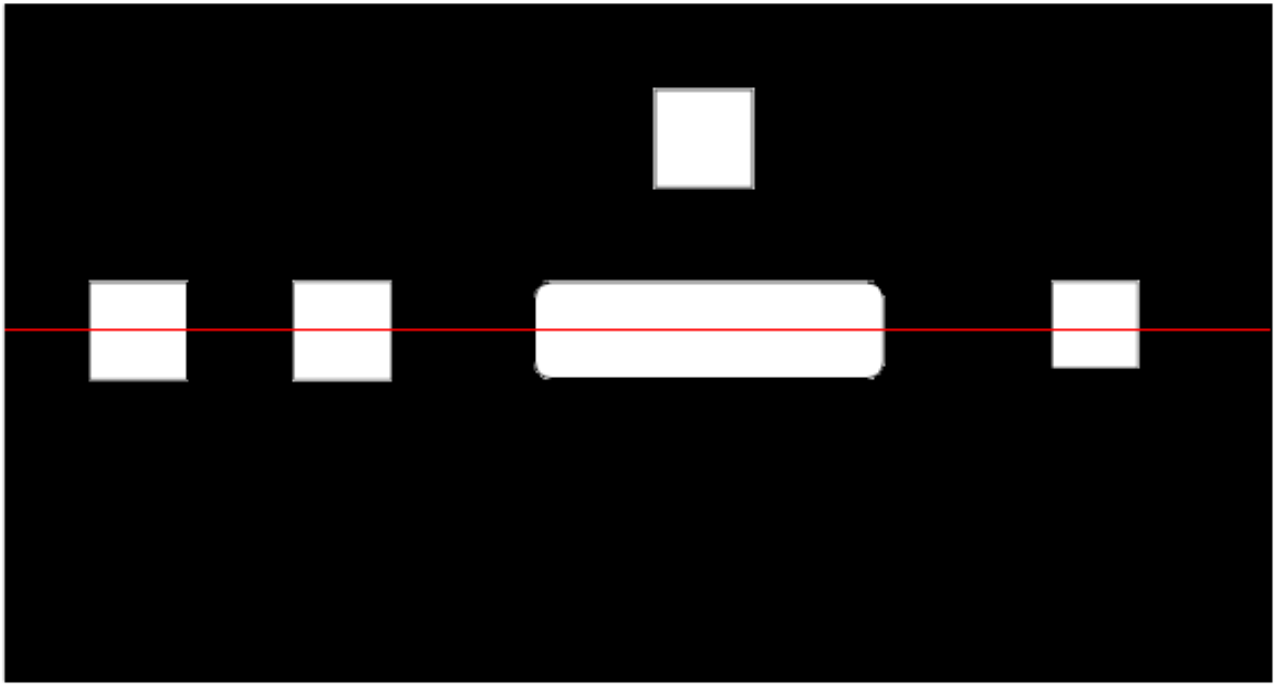



PECVD Nitride
CoSi2
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer


HDP CVD PSG
PSG
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer

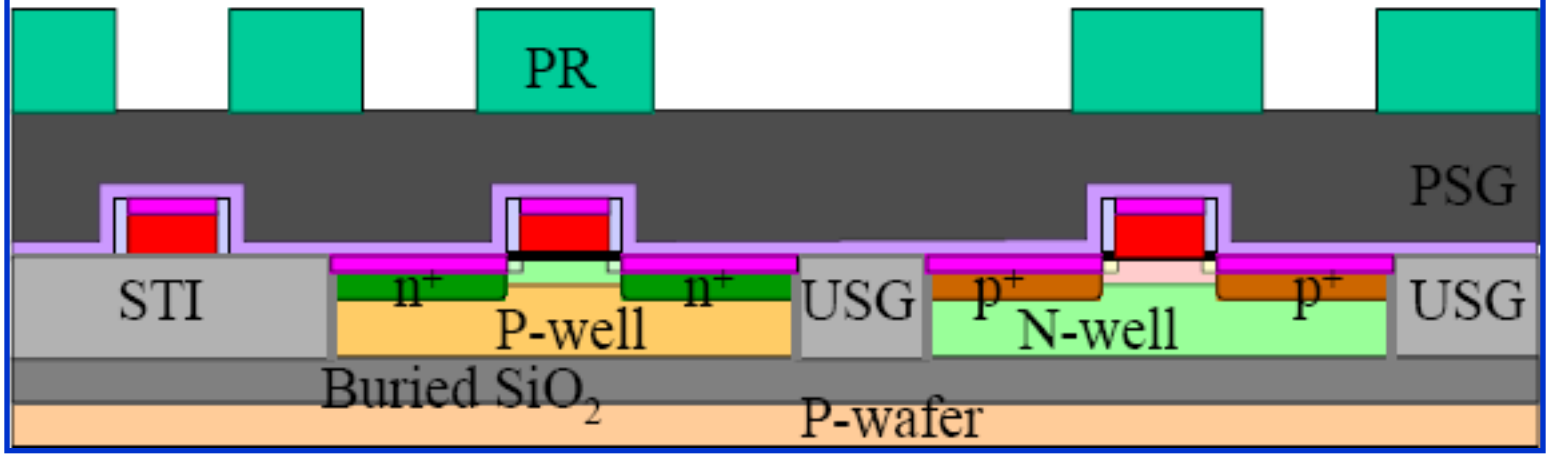

CMP PSG
PSG
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer

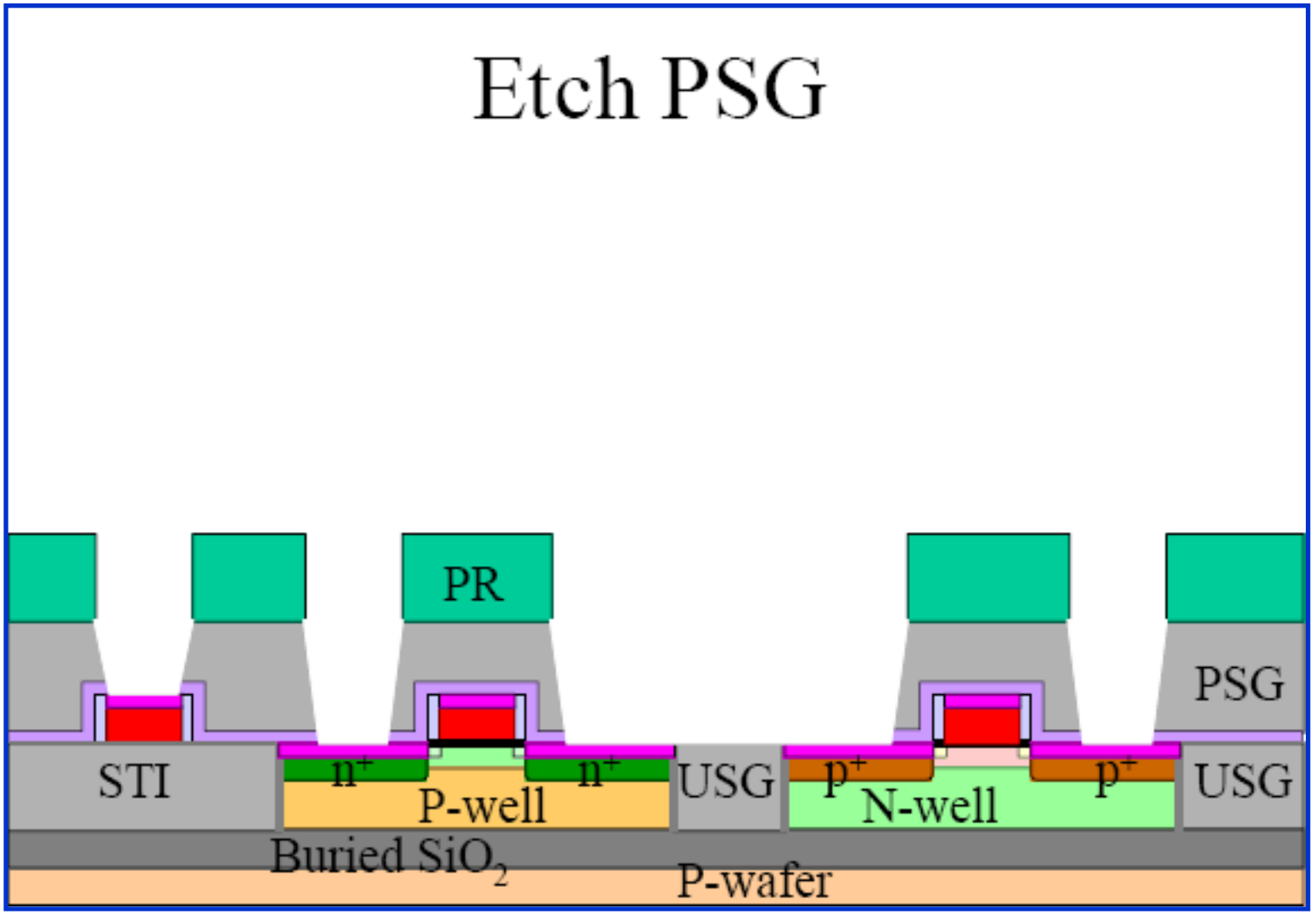
Mask 9, Contact and Local Interconnection

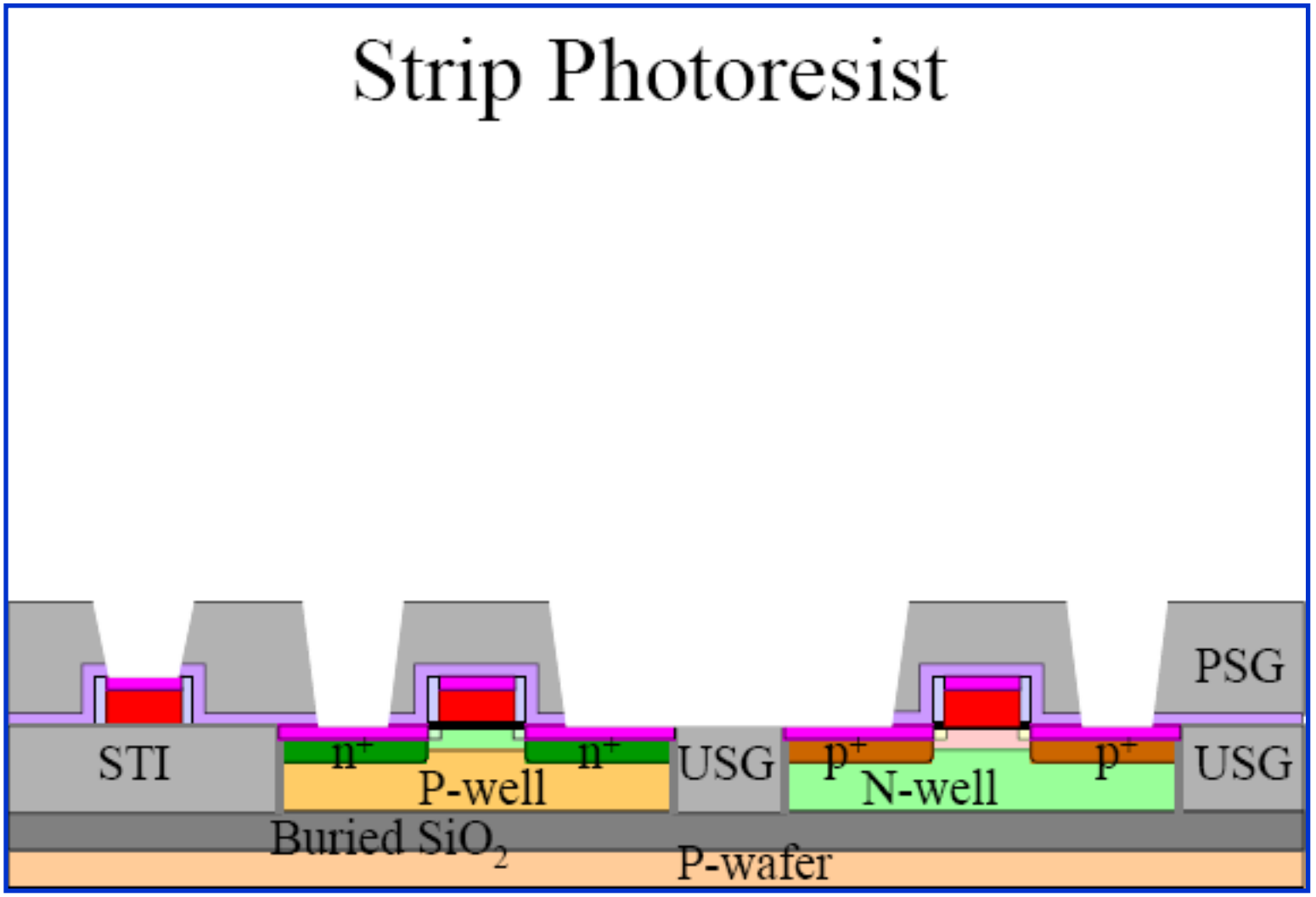


PR coating and pre-baking, mask alignment & exposure, PEB, development and inspection

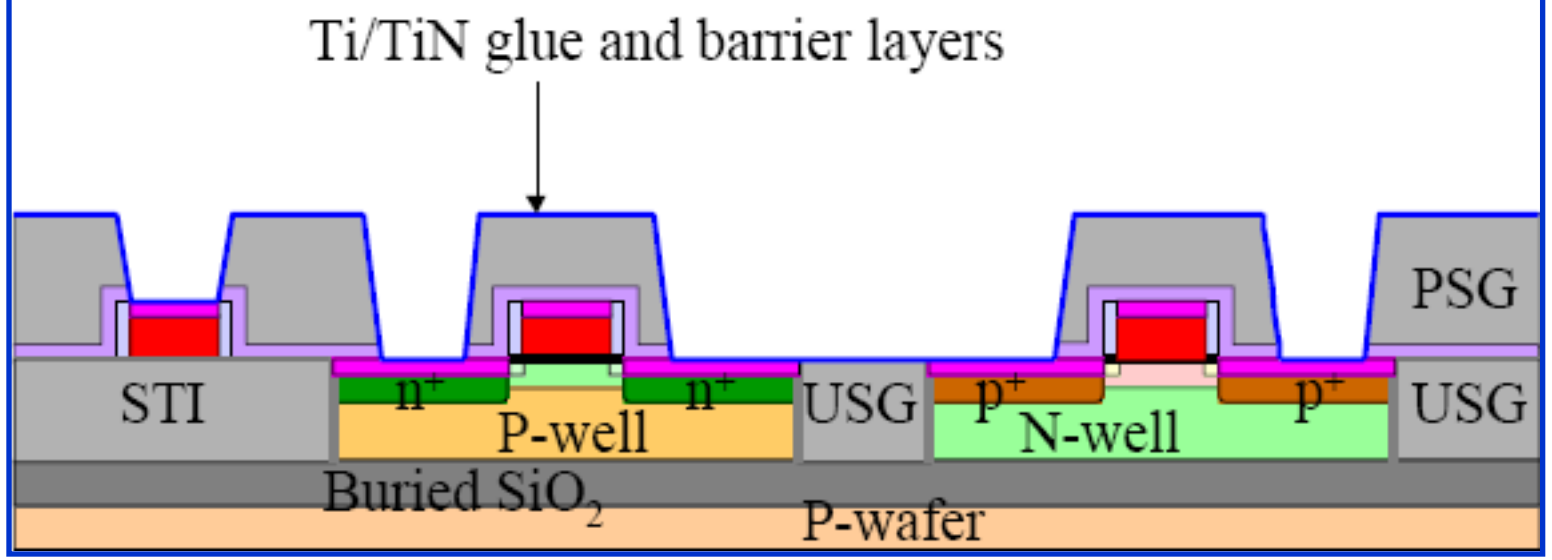
mask9

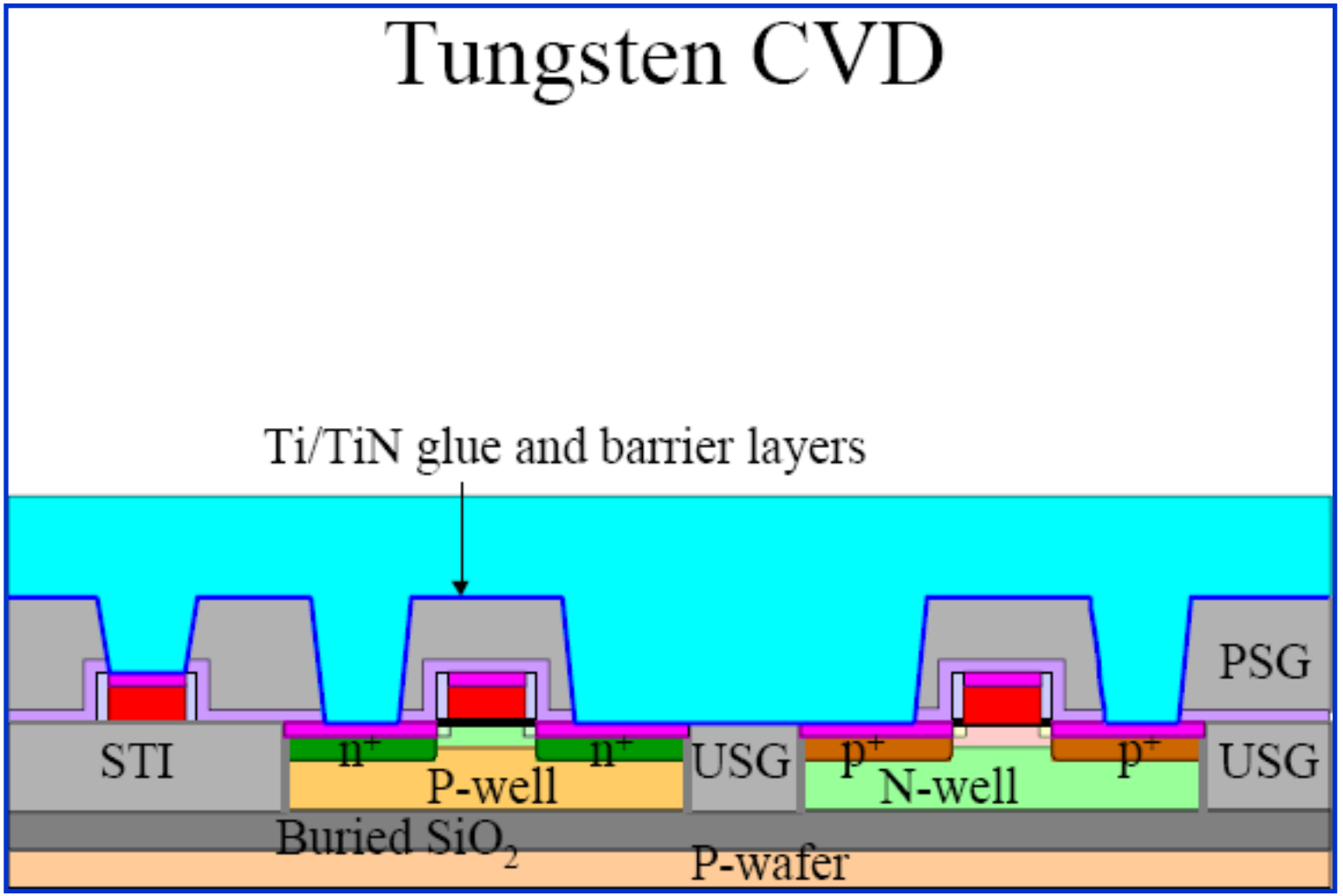



Etch PSG
PR
PSG
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer

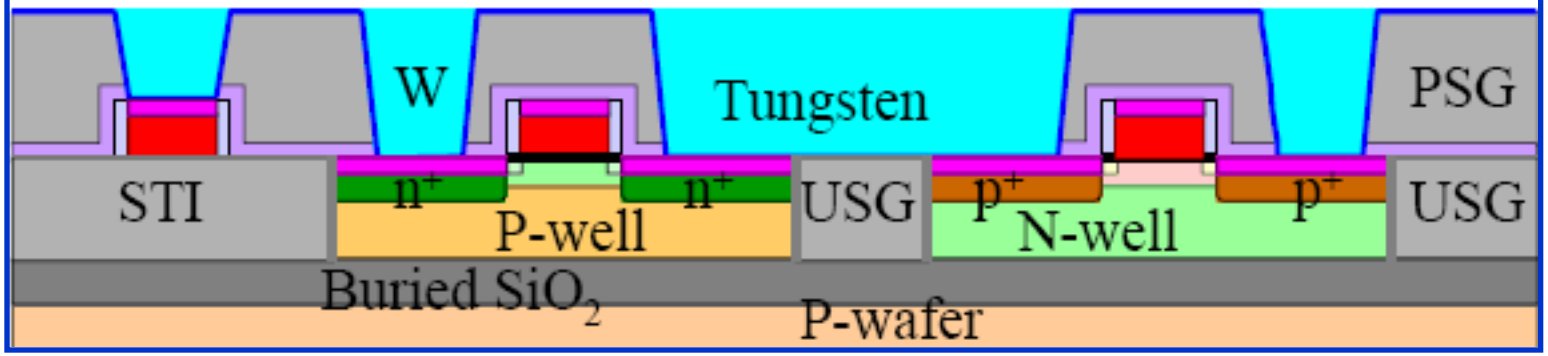

Strip Photoresist
PSG
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer

Ar sputtering etching
Ti and TiN Sputtering Deposition

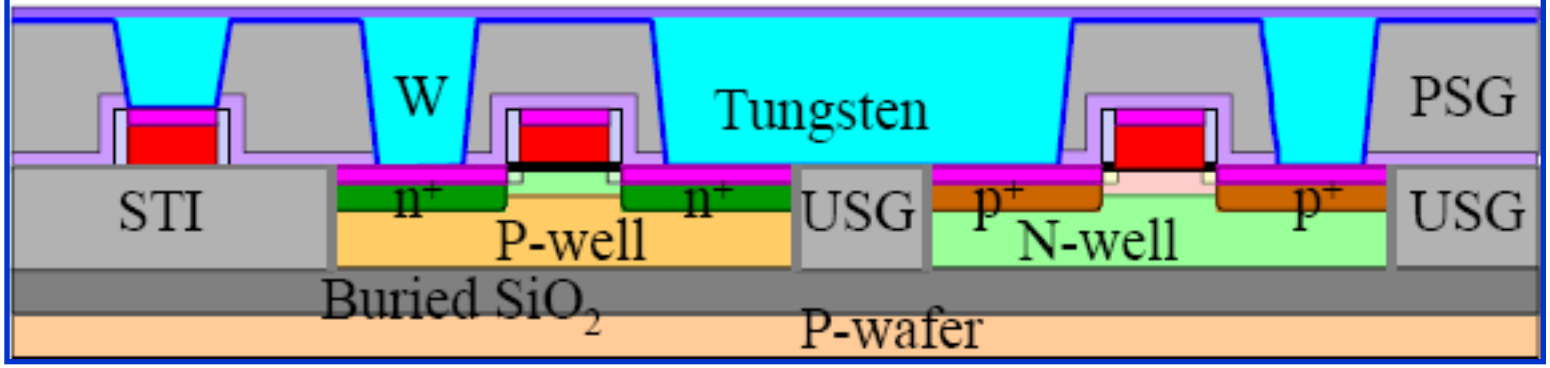



Tungsten CVD
Ti/TiN glue and barrier layers
PSG
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer

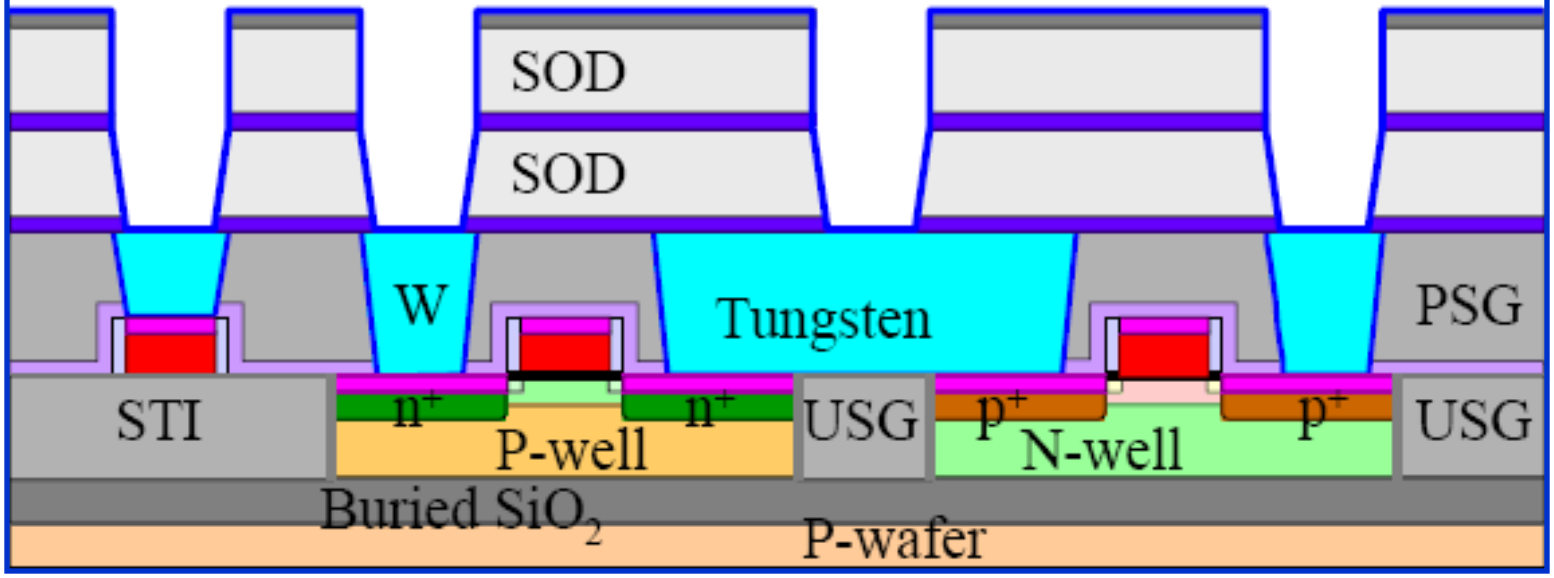
W, TiN, and Ti CMP



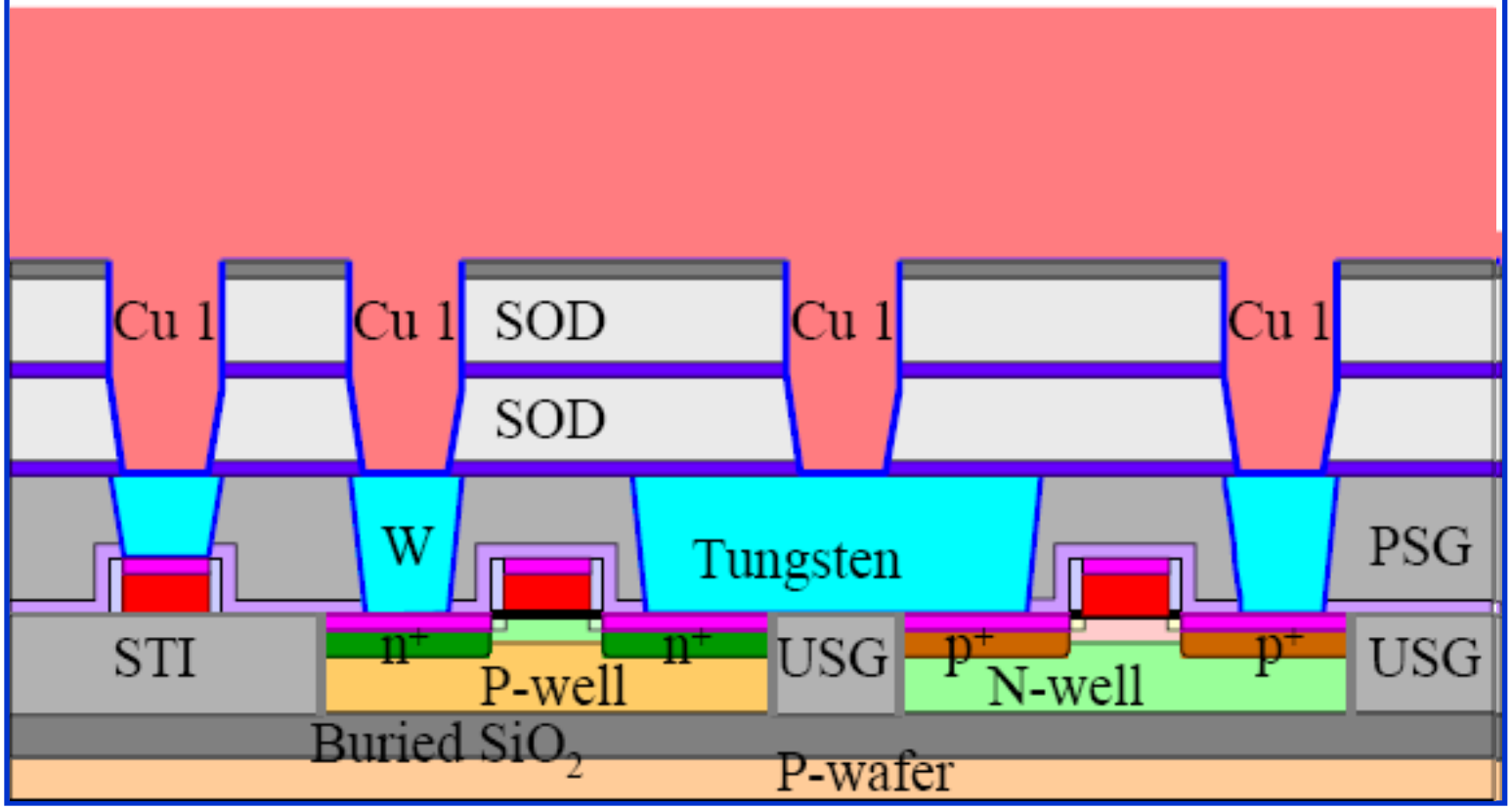
PECVD Silicon Carbide Seal Layer



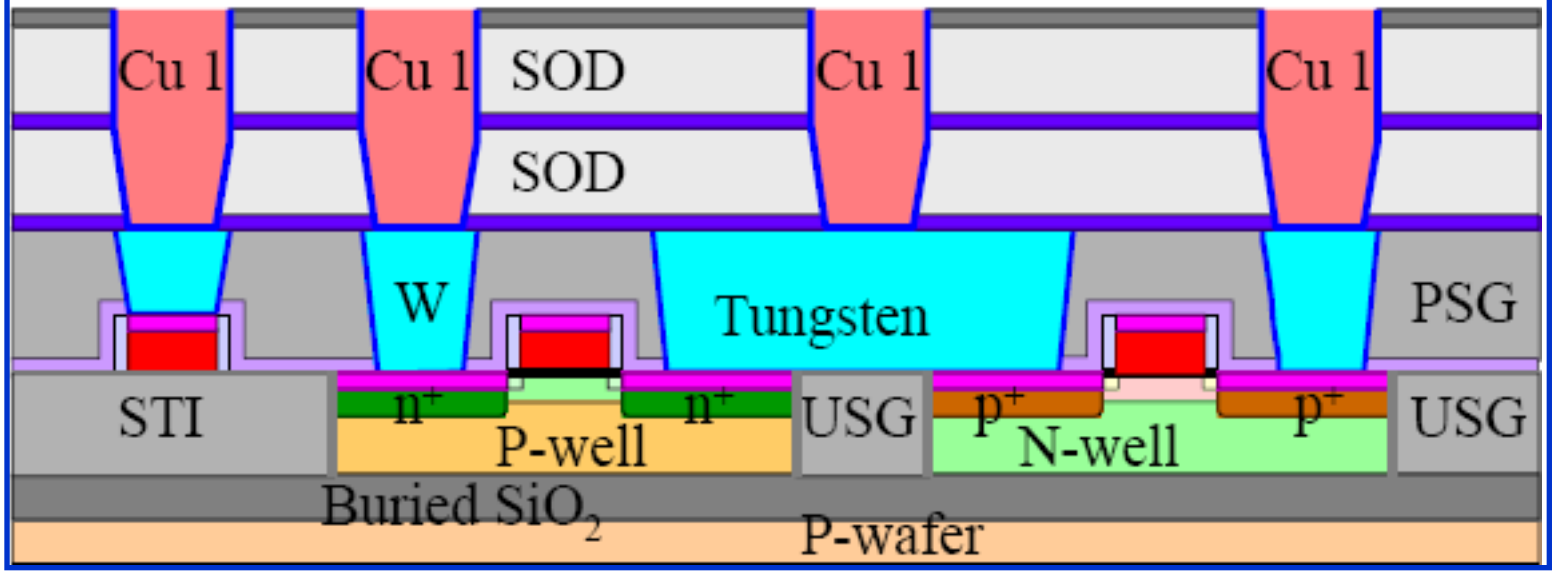
Ar Sputtering etching
Ta and TaN Barrier Layer PVD

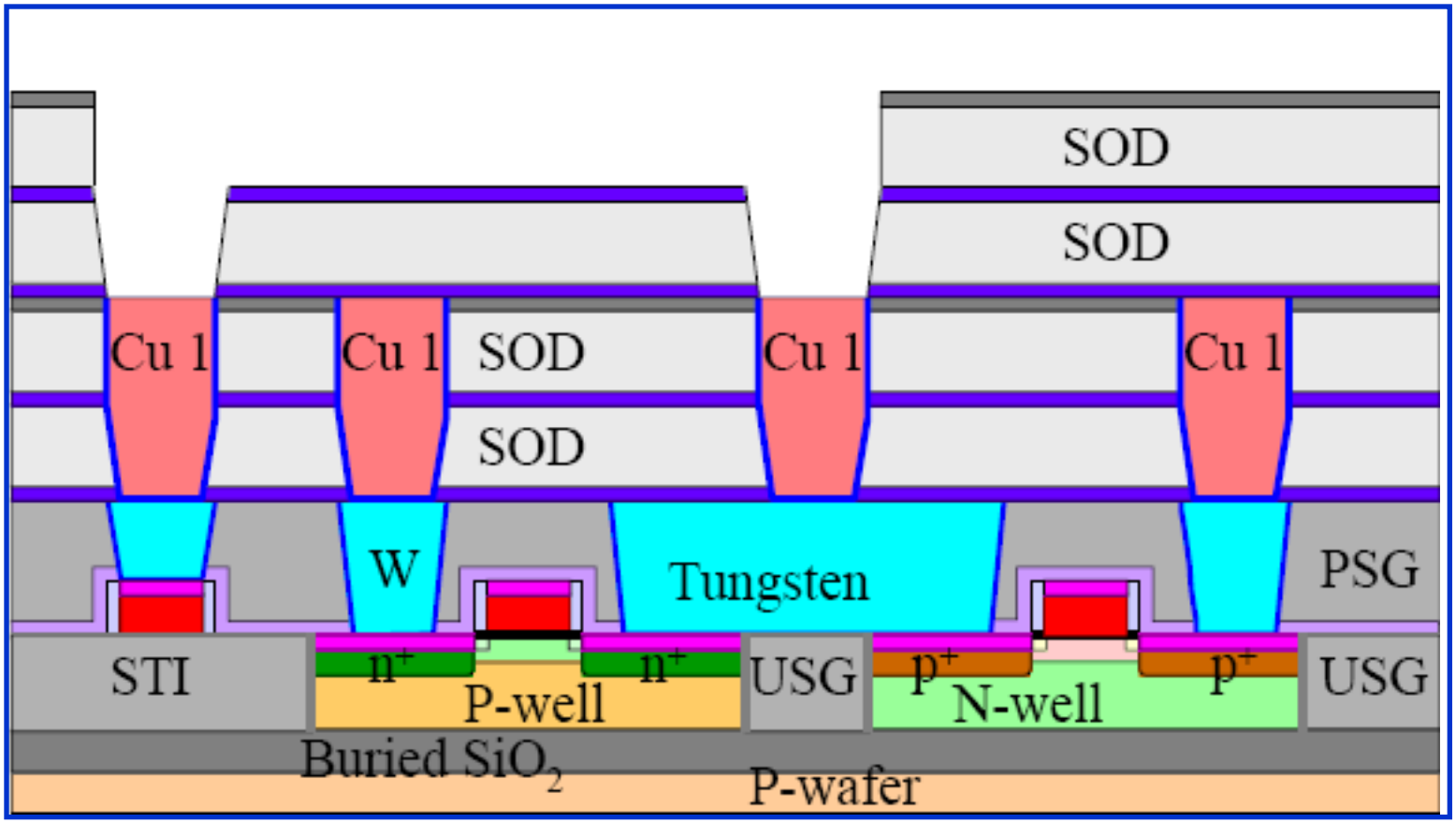


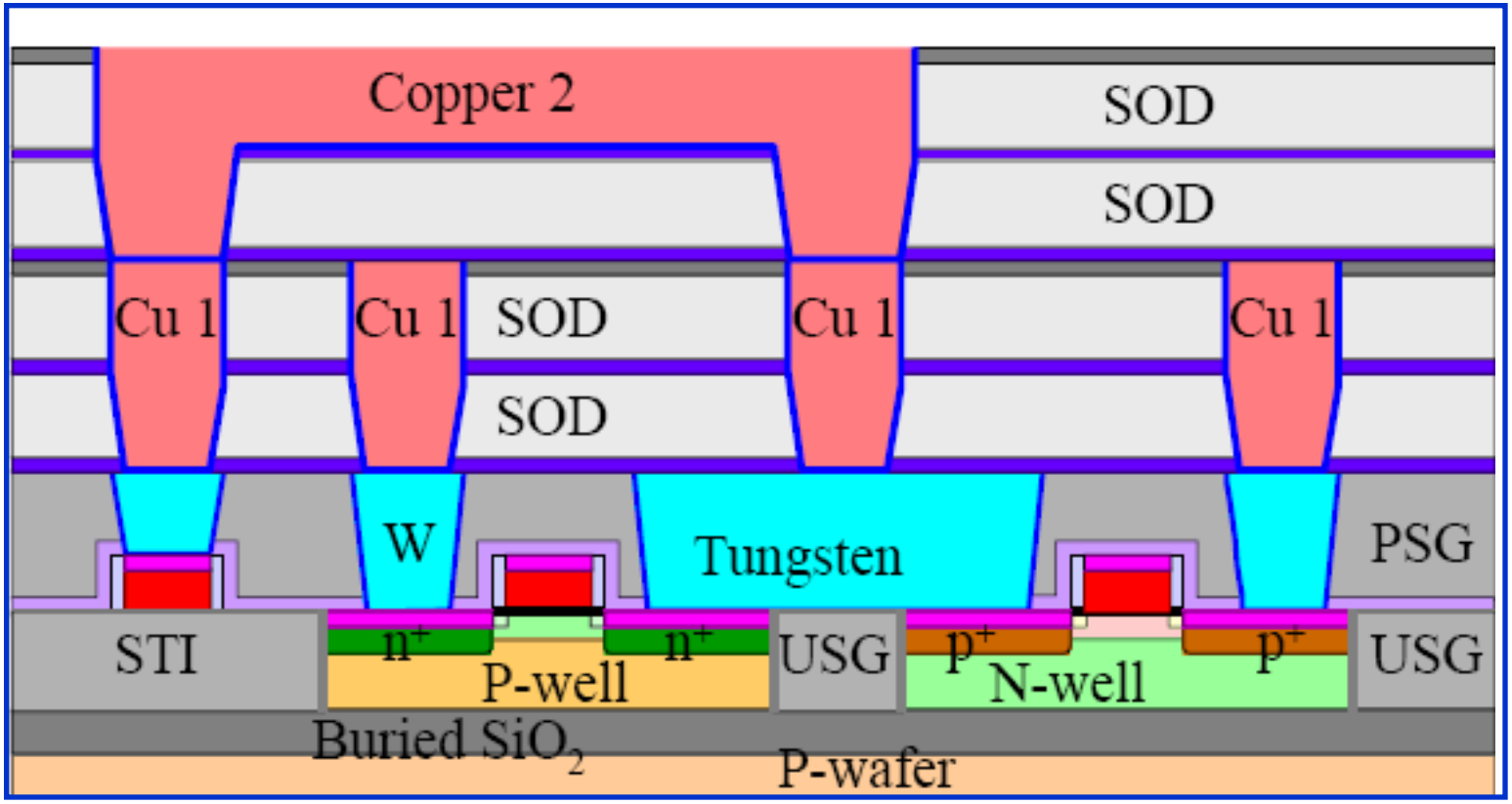
Bulk Cu ECP & annealing

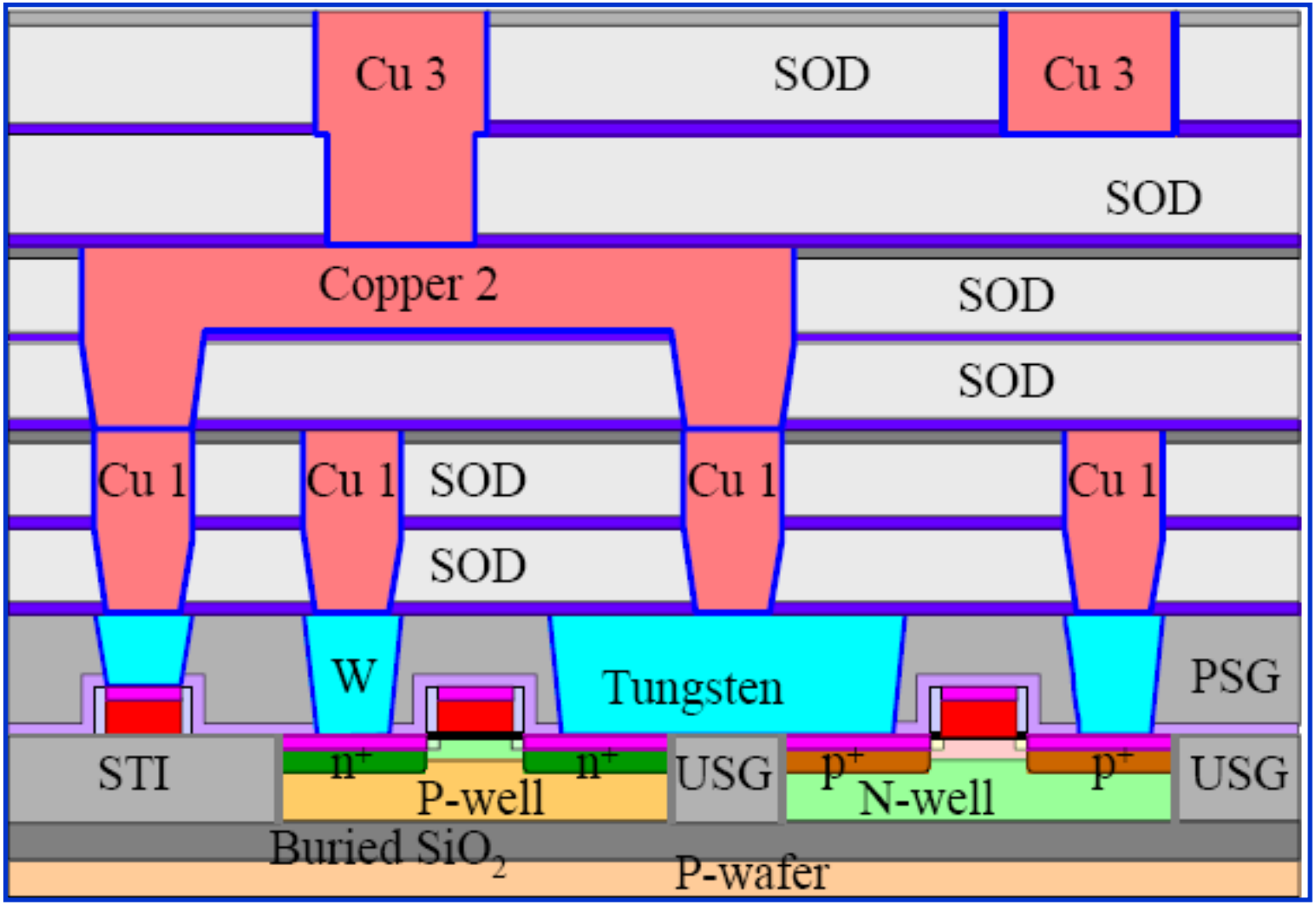


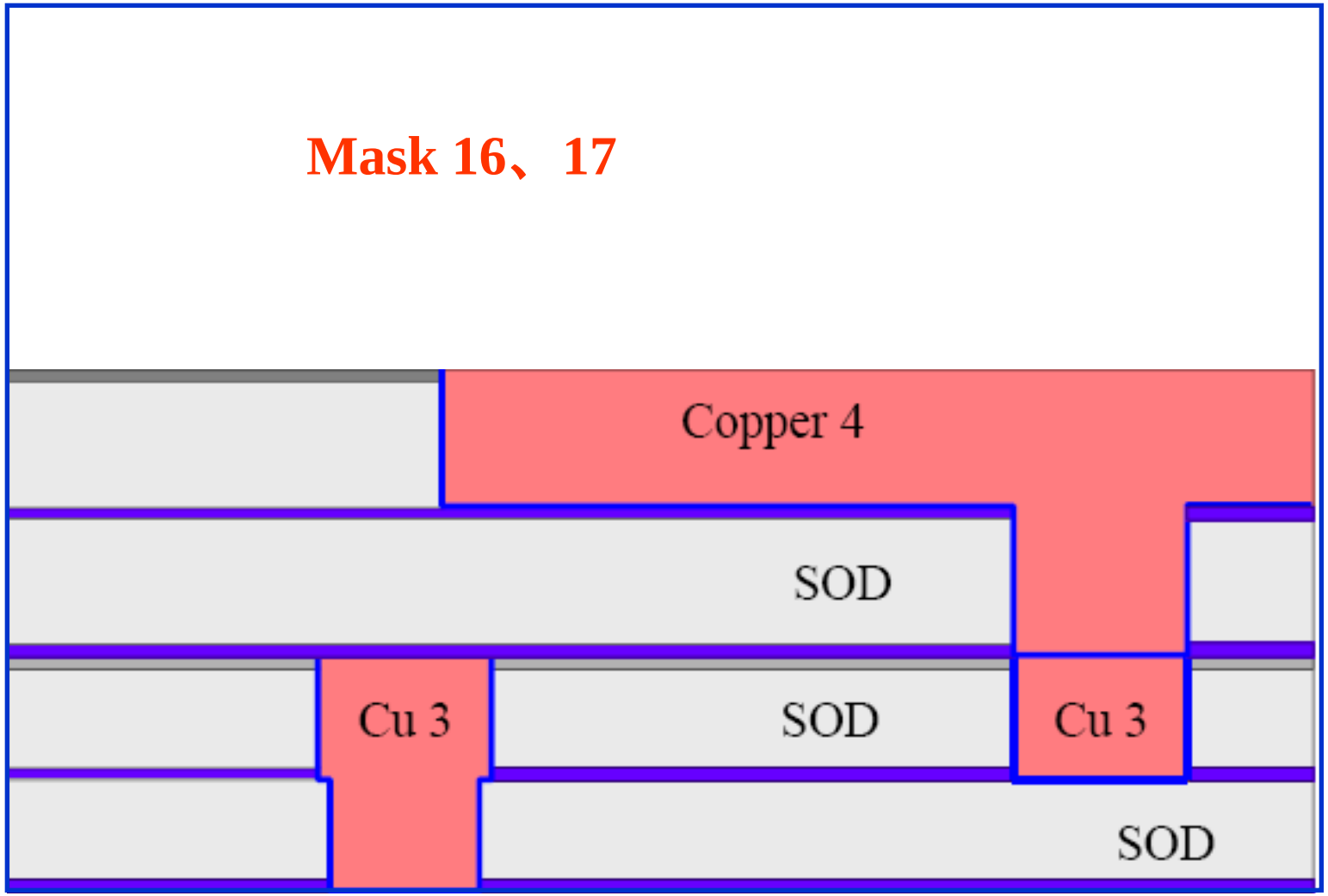
Cu, Ta, and TaN CMP

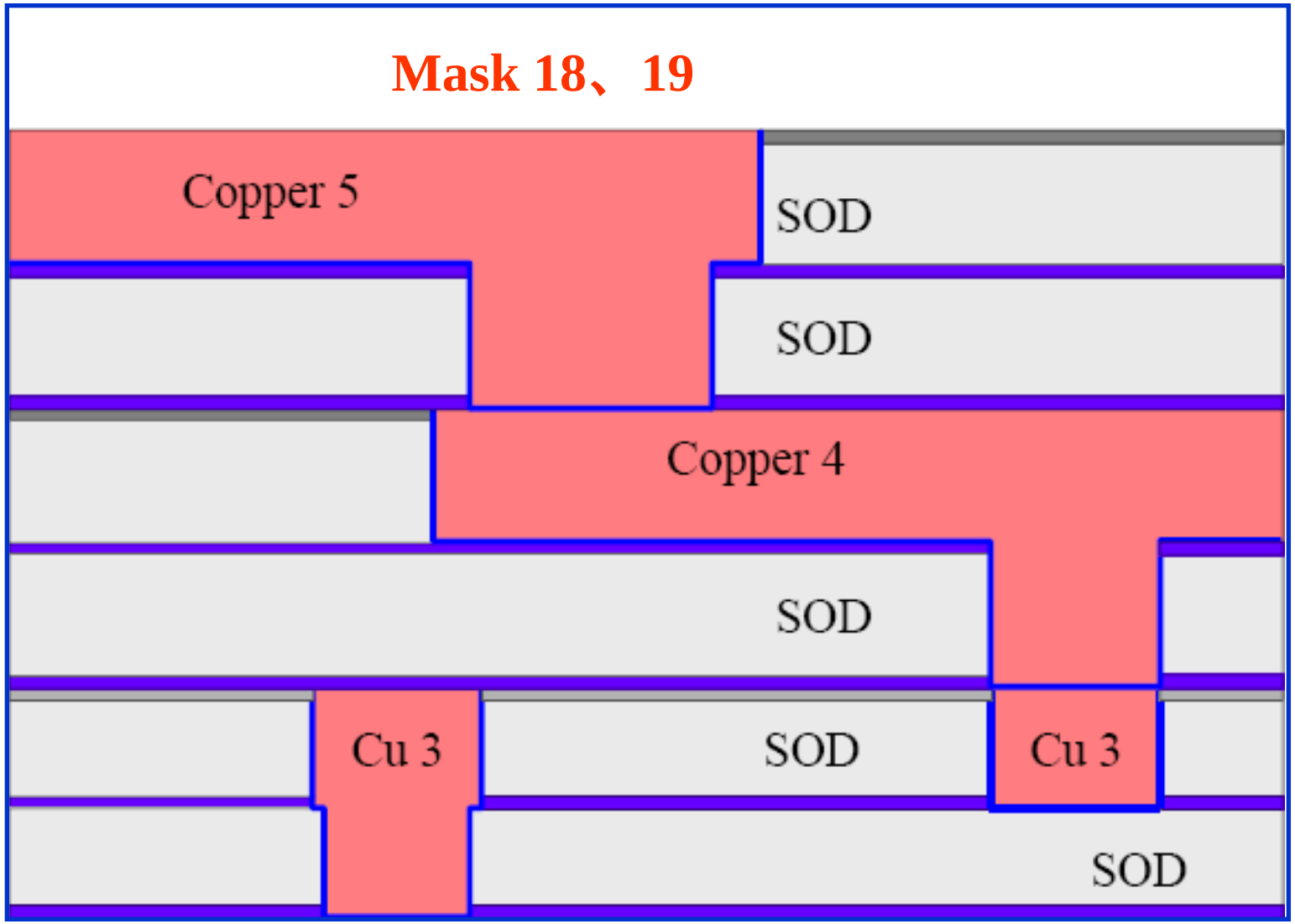



SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer

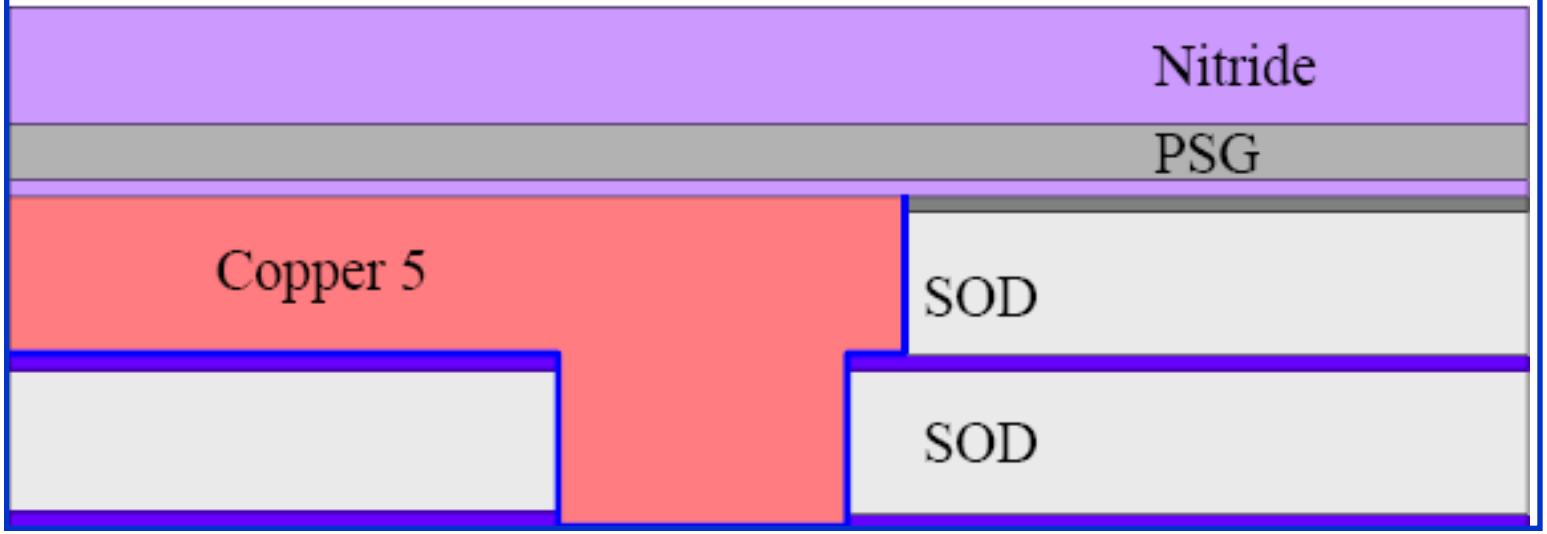

Copper 2
SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
P-well
USG
p+
p+
N-well
USG
Buried SiO2
P-wafer


Cu 3
SOD
Cu 3
SOD
Copper 2
SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer


Mask 16、17
Copper 4
SOD
Cu 3
SOD
Cu 3
SOD

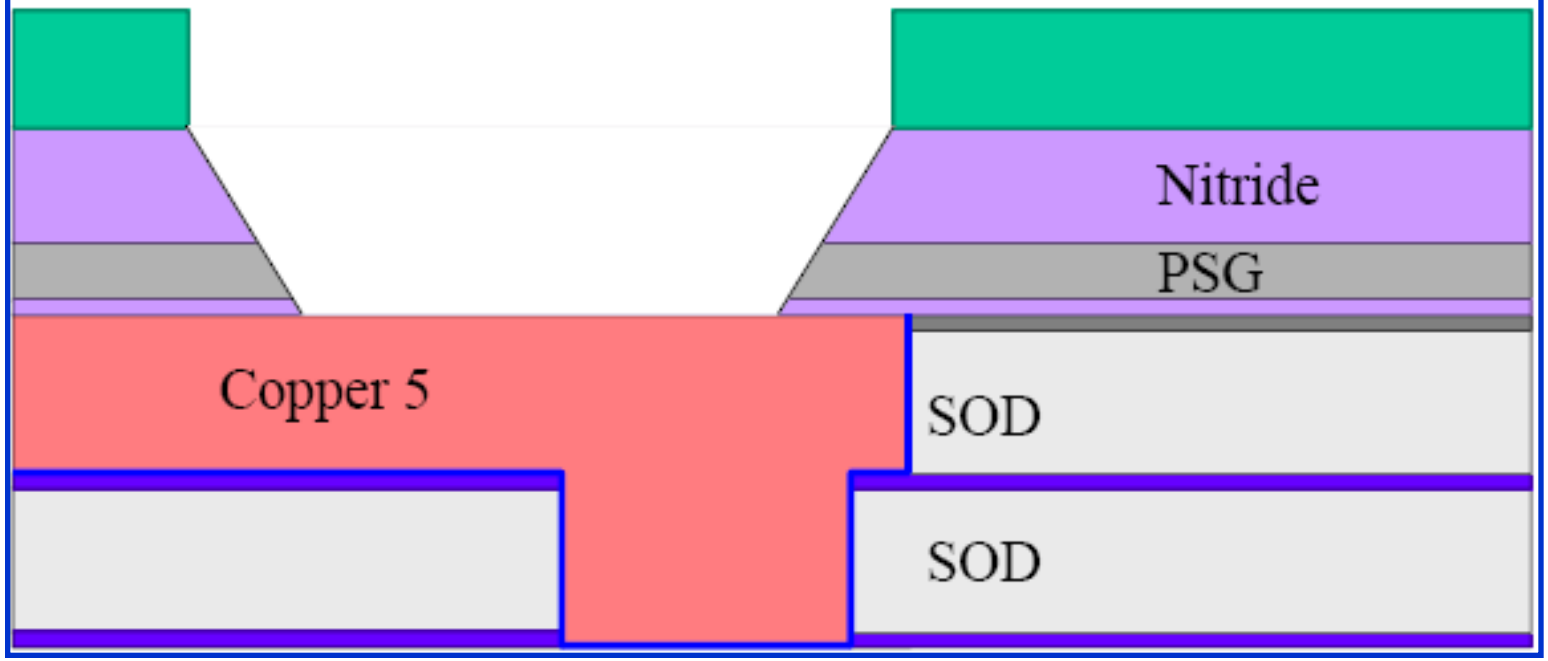

Mask 18、19
Copper 5
SOD
SOD
Copper 4
SOD
Cu 3
SOD
Cu 3
SOD

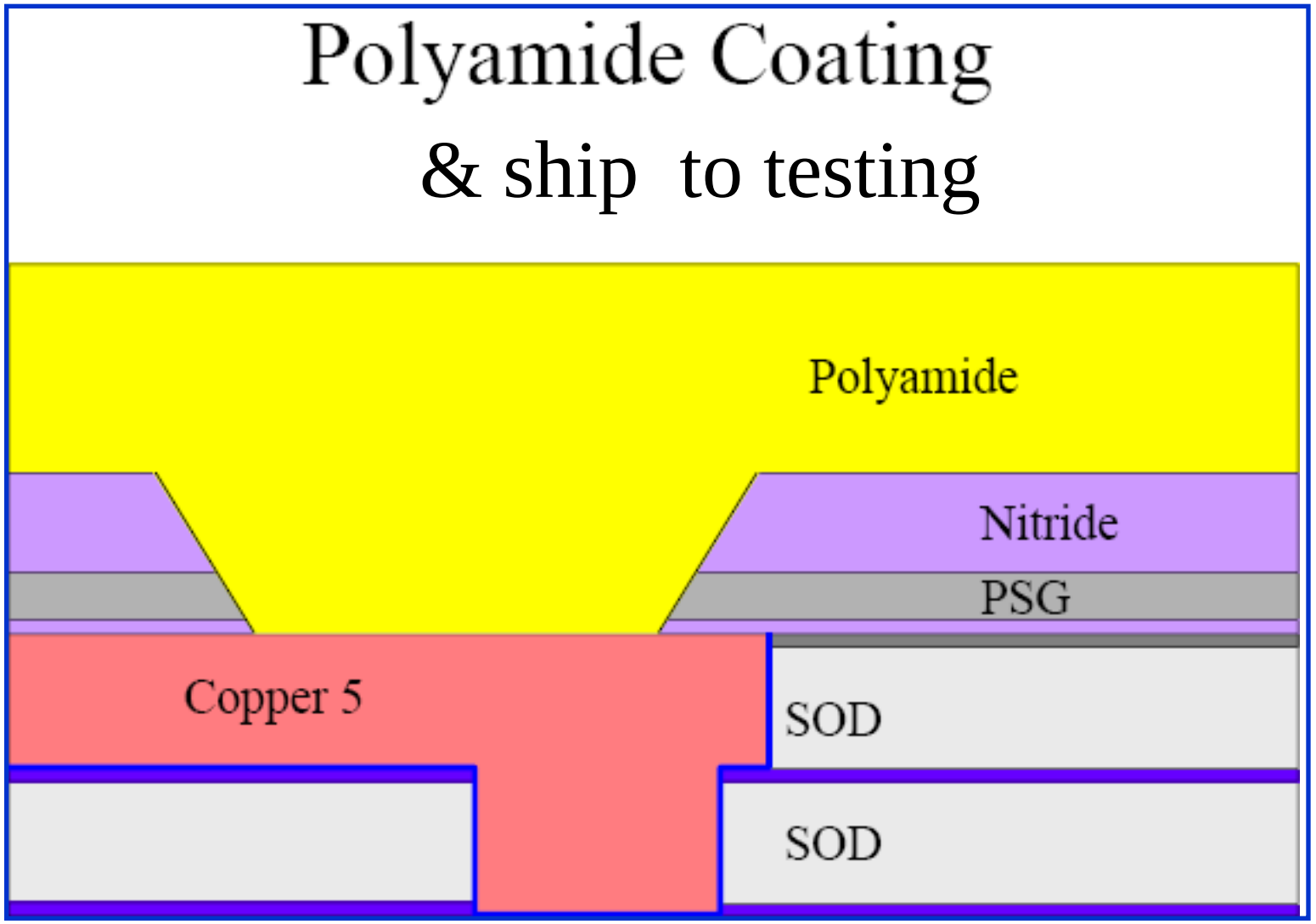
PECVD Passivation Layers: Nitride, PSG, and Nitride

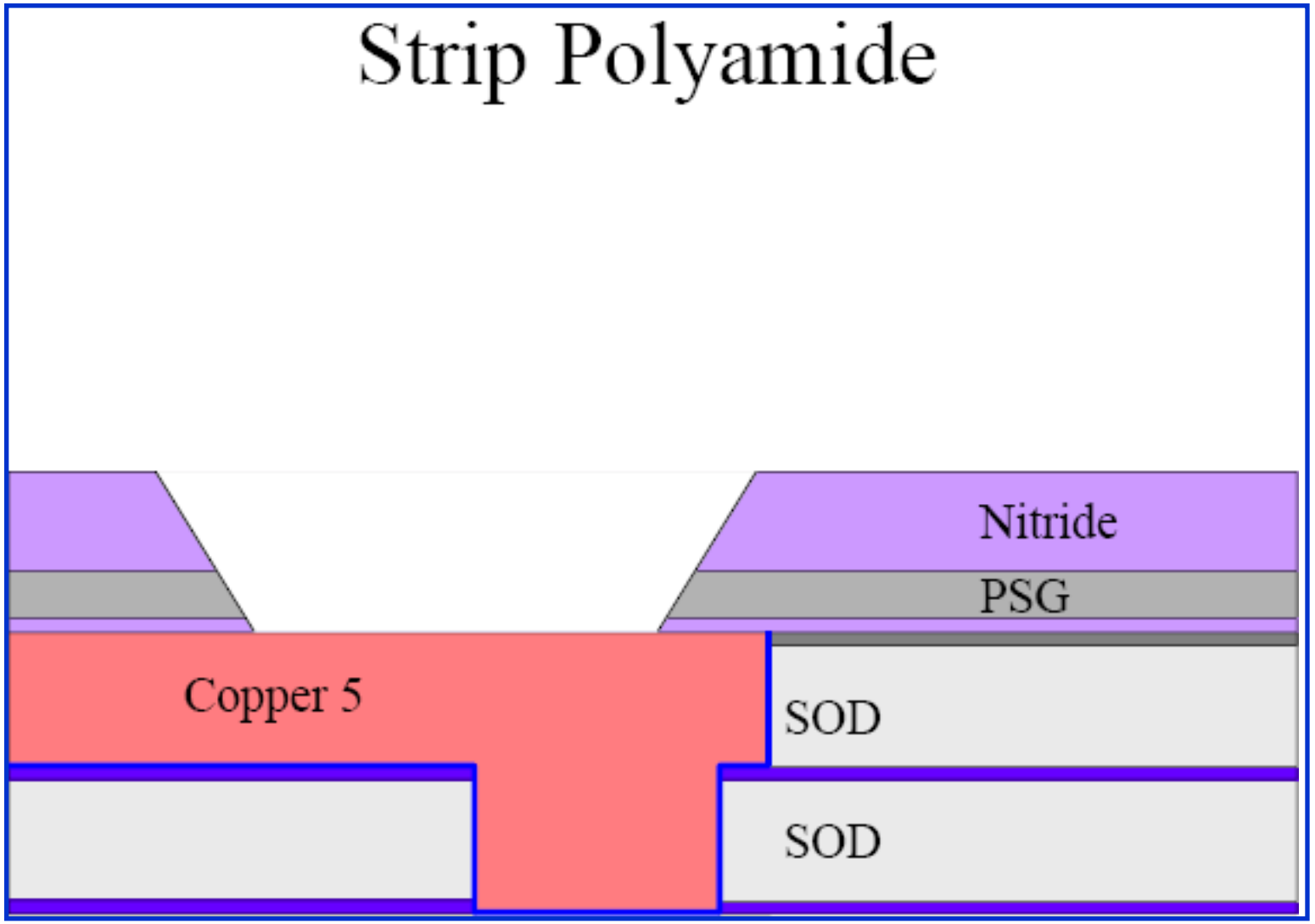


Etch Passivation Layers

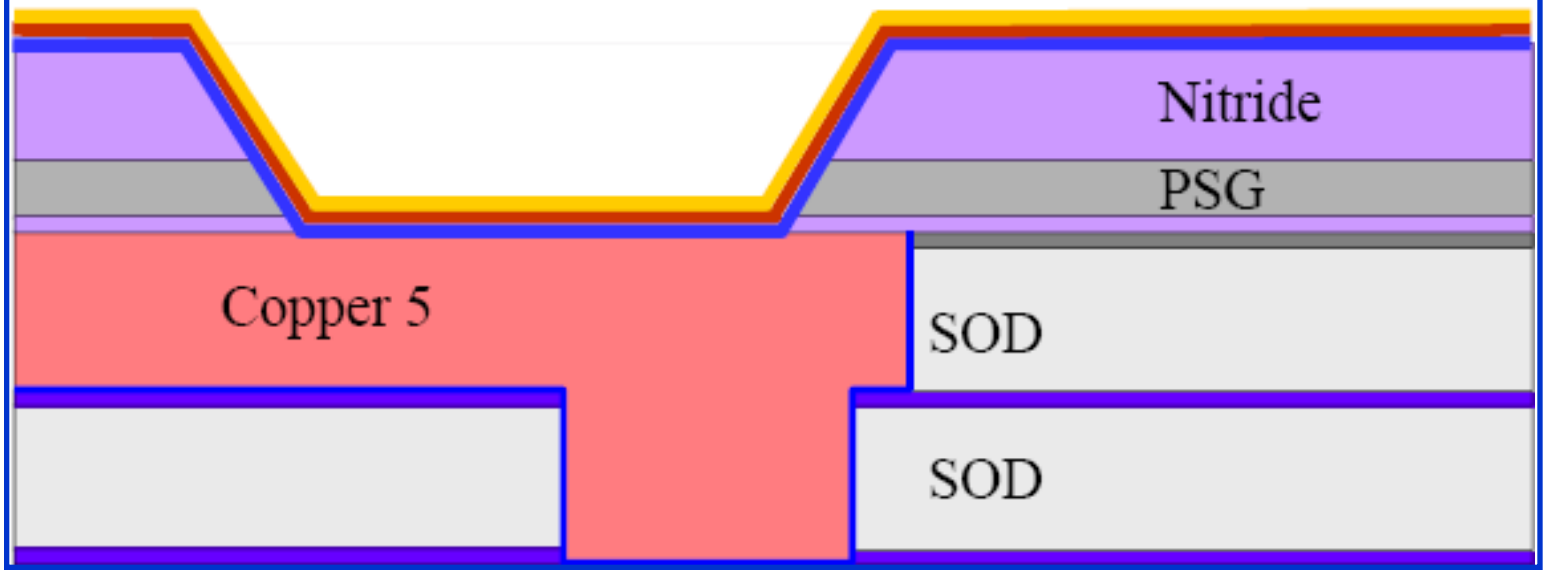
Mask 20

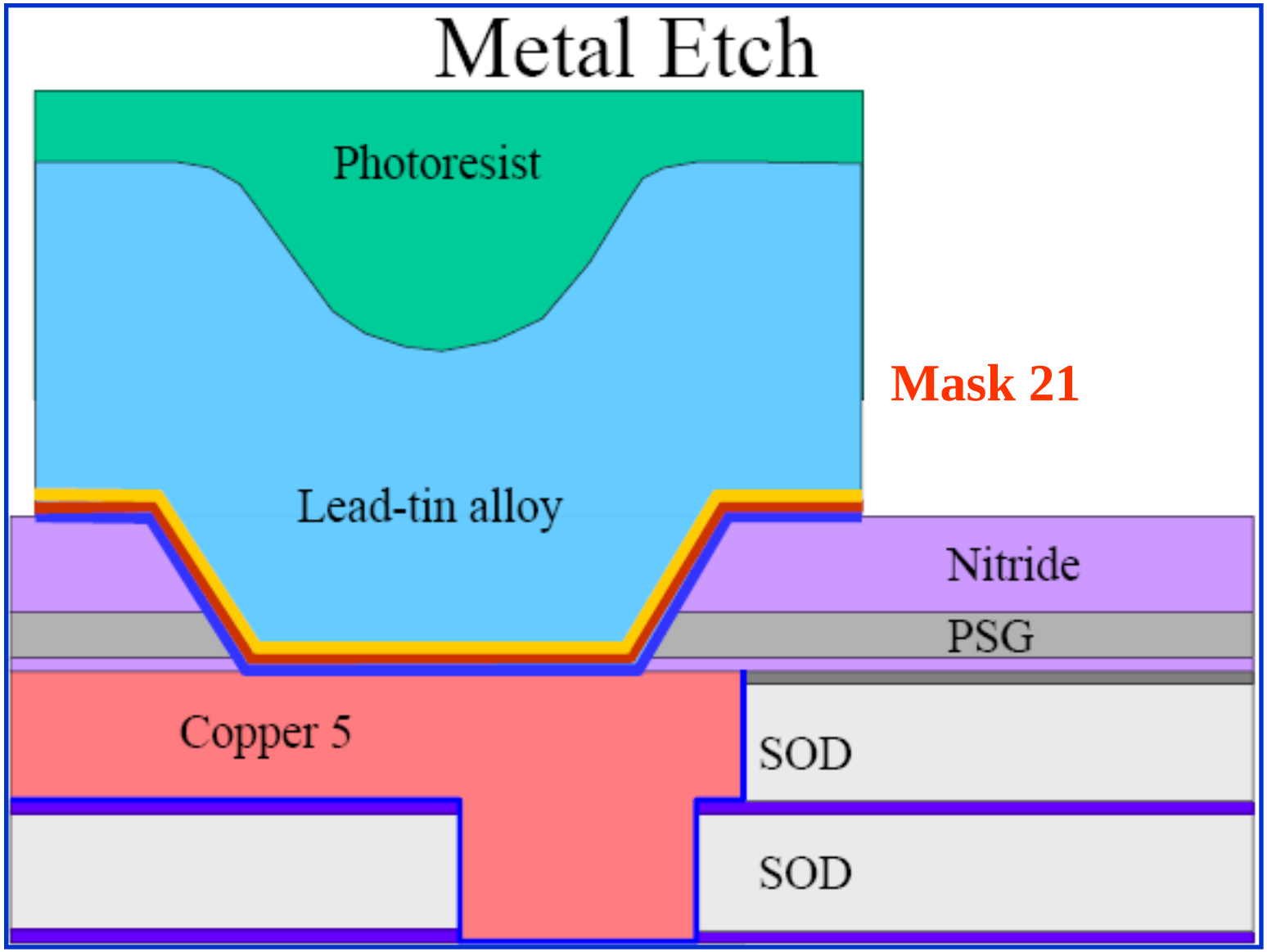


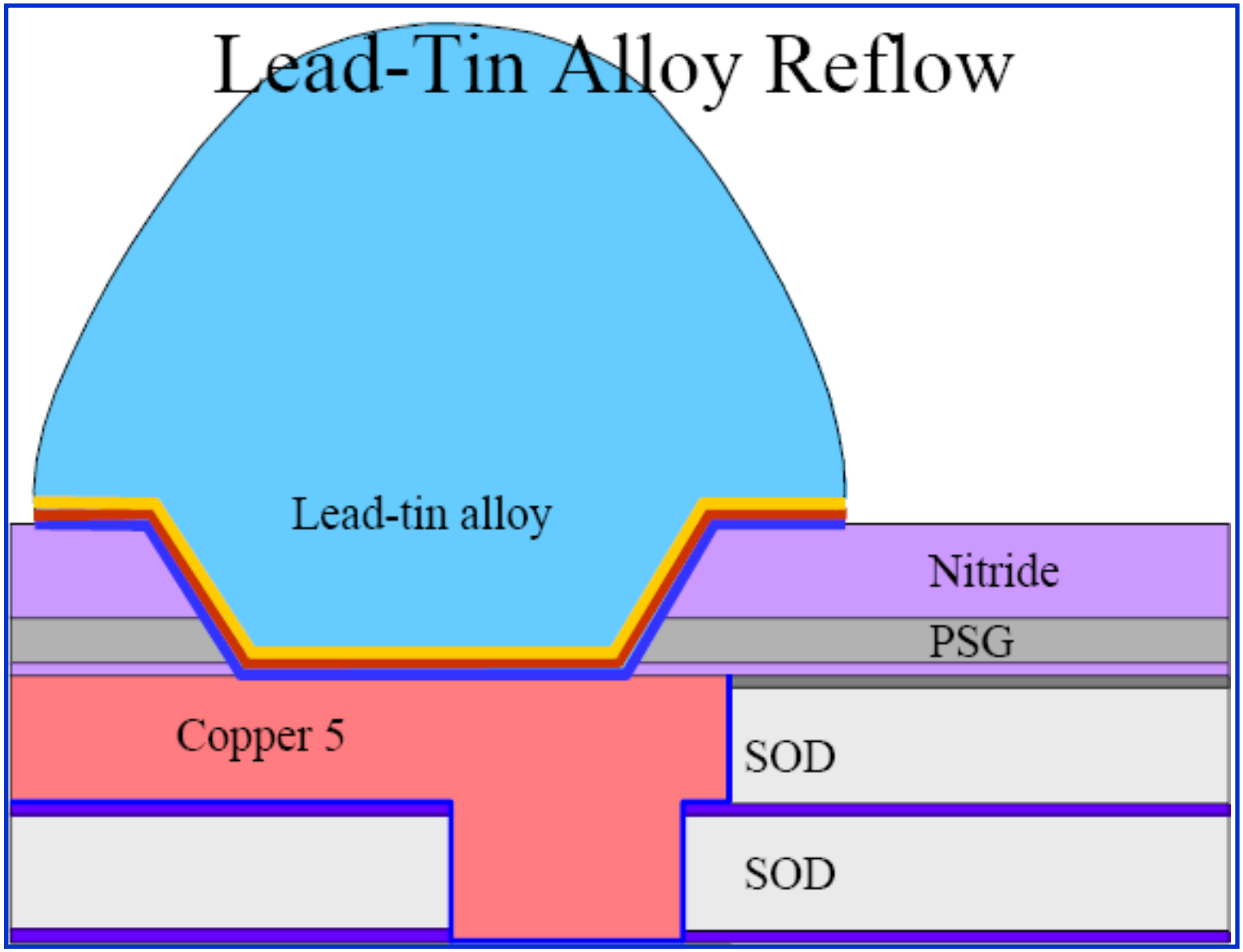

Polyamide Coating
& ship to testing
Polyamide
Nitride
PSG
Copper 5
SOD
SOD

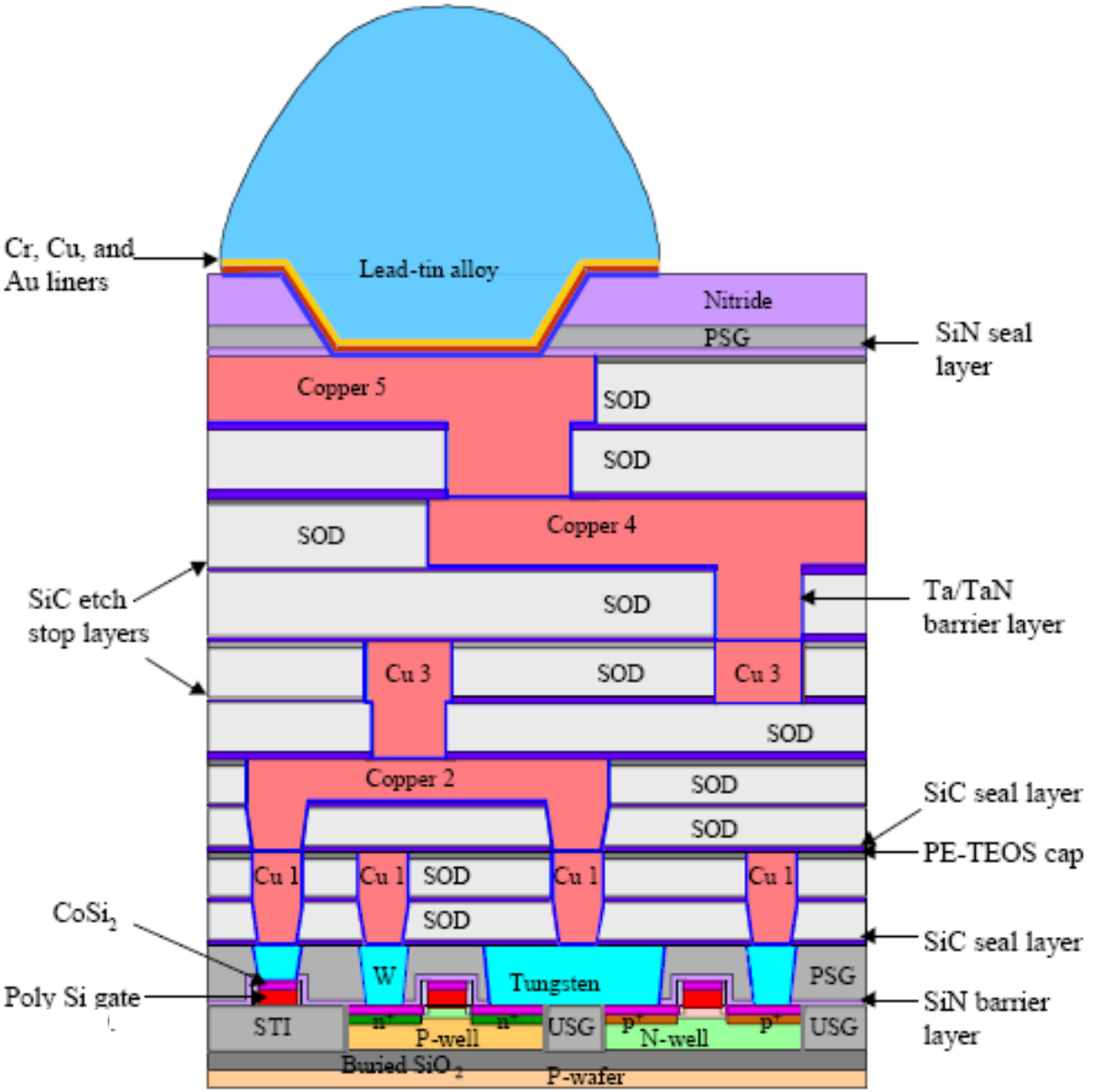

Strip Polyamide
Nitride
PSG
Copper 5
SOD
SOD

Ar sputtering etching
Cr, Cu, and Au Liner Coating




Metal Etch
Photoresist
Mask 21
Lead-tin alloy
Nitride
PSG
Copper 5
SOD
SOD


Lead-Tin Alloy Reflow
Lead-tin alloy
Nitride
PSG
Copper 5
SOD
SOD


Cr, Cu, and
Au liners
Lead-tin alloy
Nitride
PSG
SiN seal
layer
Copper 5
SOD
SOD
SOD
Copper 4
SiC etch
stop layers
SOD
Ta/TaN
barrier layer
Cu 3
SOD
Cu 3
SOD
Copper 2
SOD
SiC seal layer
SOD
PE-TEOS cap
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
CoSi2
SiC seal layer
W
Tungsten
PSG
Poly Si gate
SiN barrier
layer
STI
n+
P-well
n+
USG
p+
N-well
p+
USG
Buried SiO2
P-wafer

Process Integration - Overview

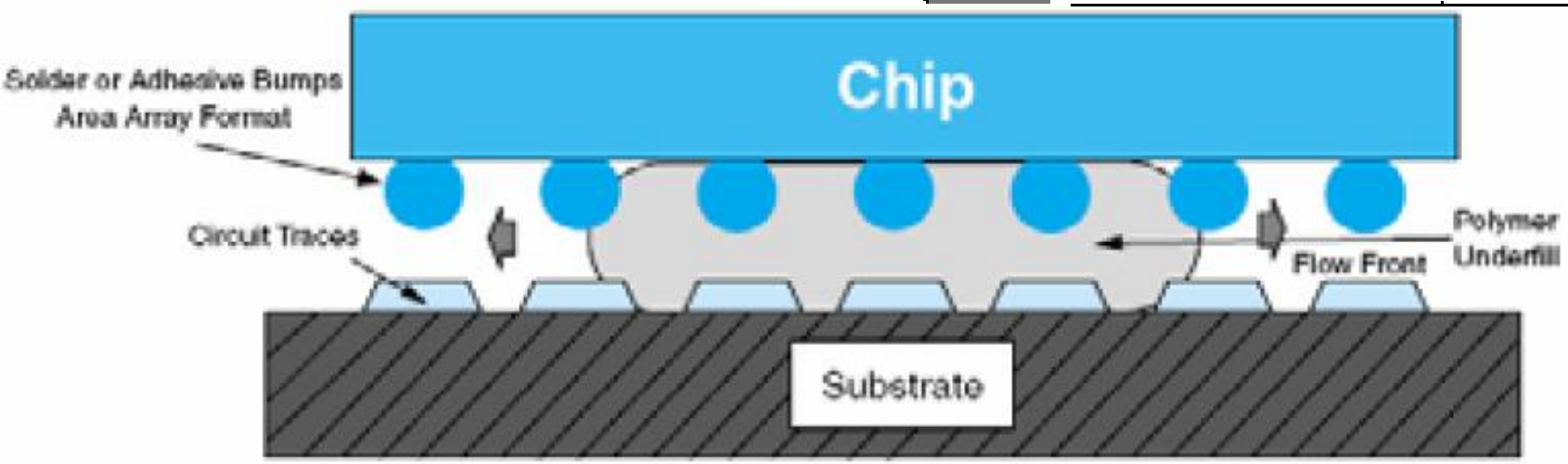
- Isolation Technology
- Gate Stack Options
- Advanced CMOS Integration
  - Full SOI CMOS Process
  - Flip Chip Packaging
  - Current Technology

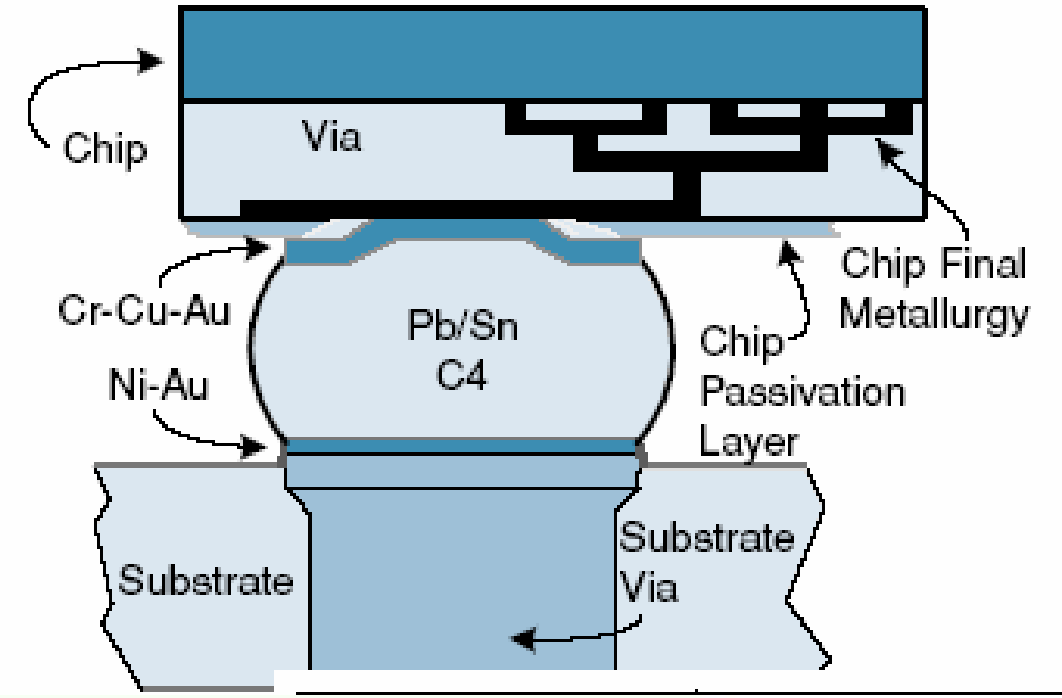
Flip Chip Packaging

Dicing, Packaging: e.g.,

Flip-chip packaging

Through Silicon Via (TSV)



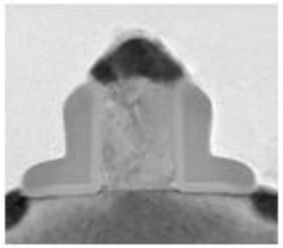
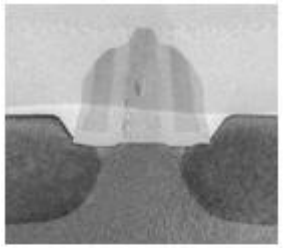
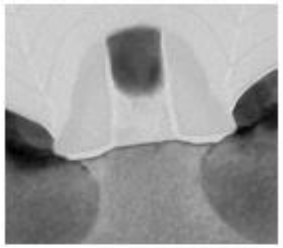
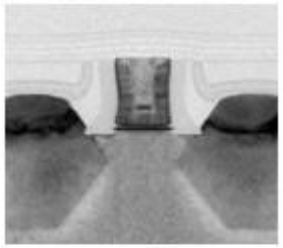
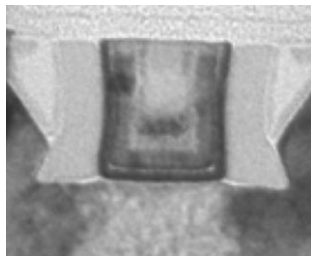


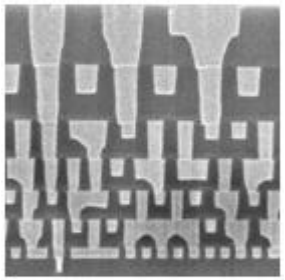
Process Integration - Overview

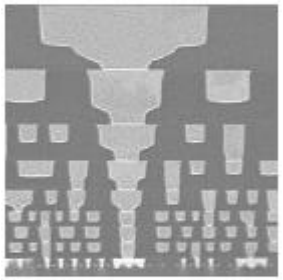
- Isolation Technology
- Gate Stack Options
- Advanced CMOS Integration
  - Full SOI CMOS Process
  - Flip Chip Packaging
  - Current Technology

On-Time 2 Year Cycles

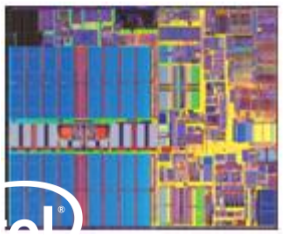
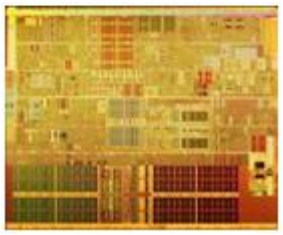
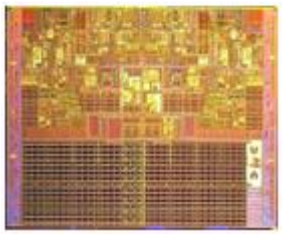
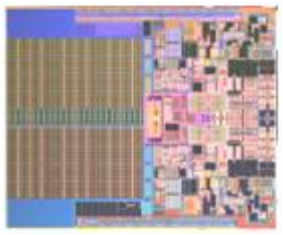
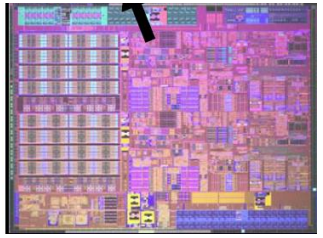
130 nm	90 nm	65 nm	45 nm	32 nm
2001	2003	2005	2007	2009

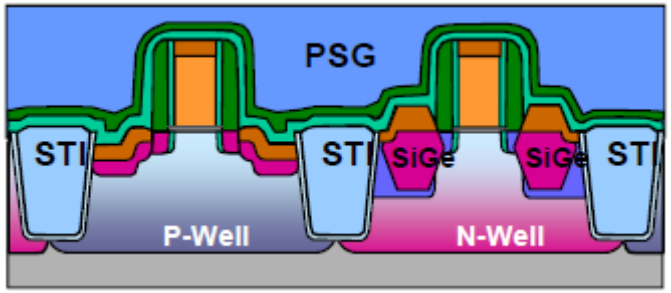


High-k
2nd Generation

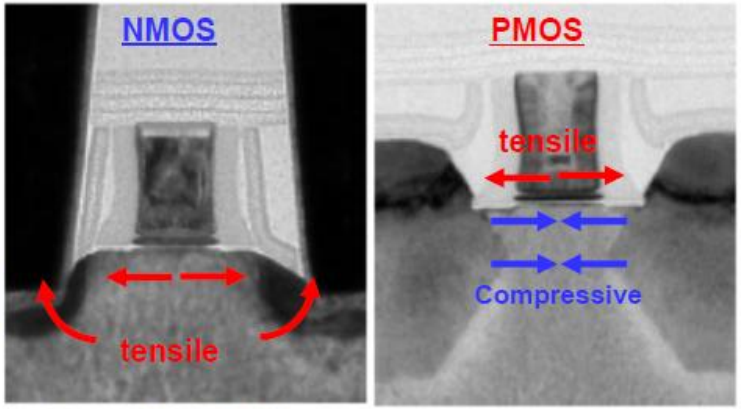






110622 SMT Symp.
M.Niwa

45nm High-k + Metal Gate Strain-Enhanced FETs (Intel)



Ge30% & Tensile
MG→Δμ: +50%

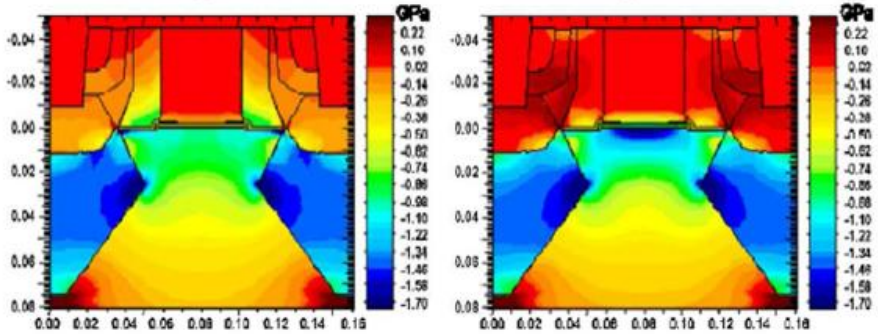


Tensile Trench Contact
MG →ΔId: +16%

Since PMOS 1st, NMOS process is free from P-metal stress

Before gate removal

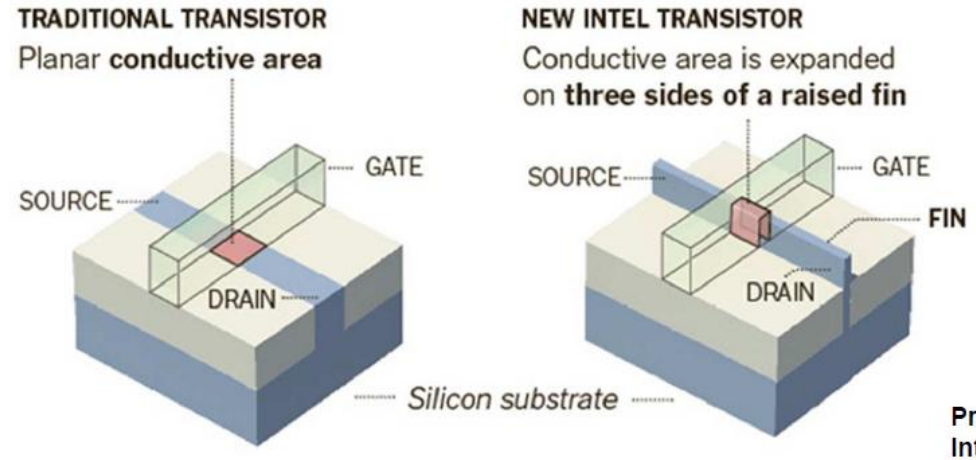
After gate removal



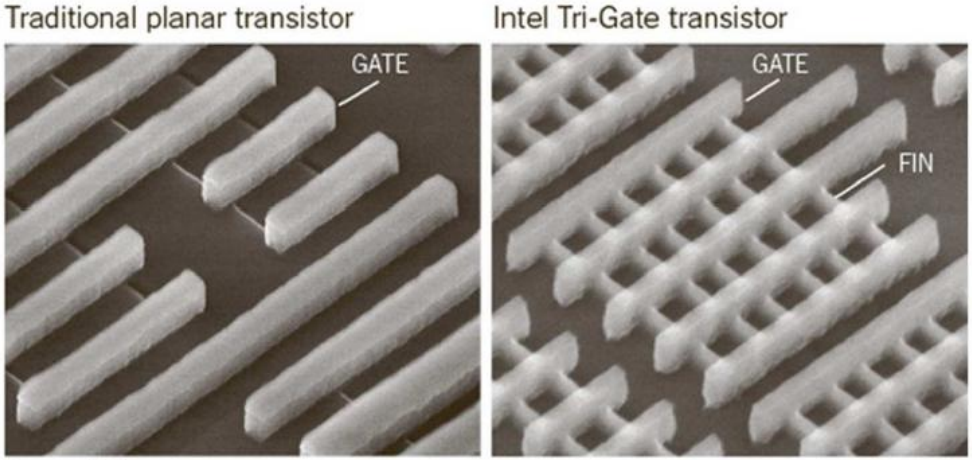
SiGe channel & Gate Last →Δμ(hole): +50%

C. Auth et al., VLSI Tech. Symp. 2008

Taken from: Masaaki Niwa, "Development of 32nm CMOS and Recent Trend for Beyond 32nm" SMT Symp. 2011



Press release by Intel; May, 2011



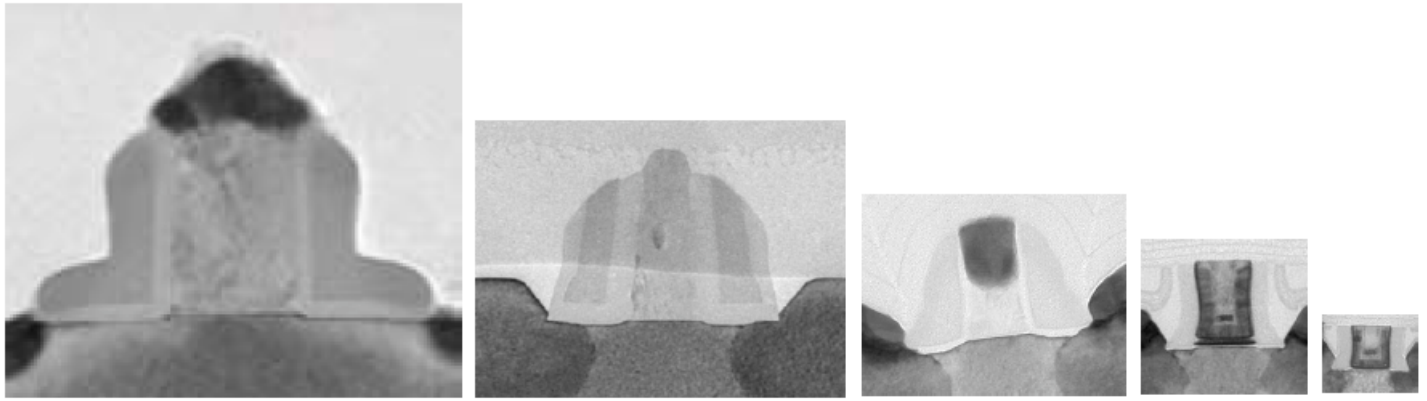
The New York Times May 5, 2011

New Transistor Grows in the Third Dimension

Taken from: Masaaki Niwa, "Development of 32nm CMOS and Recent Trend for Beyond 32nm" SMT Symp. 2011

Changes in Scaling

THEN	NOW
• Scaling drove down cost	• Scaling drives down cost
• Scaling drove performance	• Materials drive performance
• Performance constrained	• Power constrained
• Active power dominates	• Standby power dominates
• Independent design-process	• Collaborative design-process

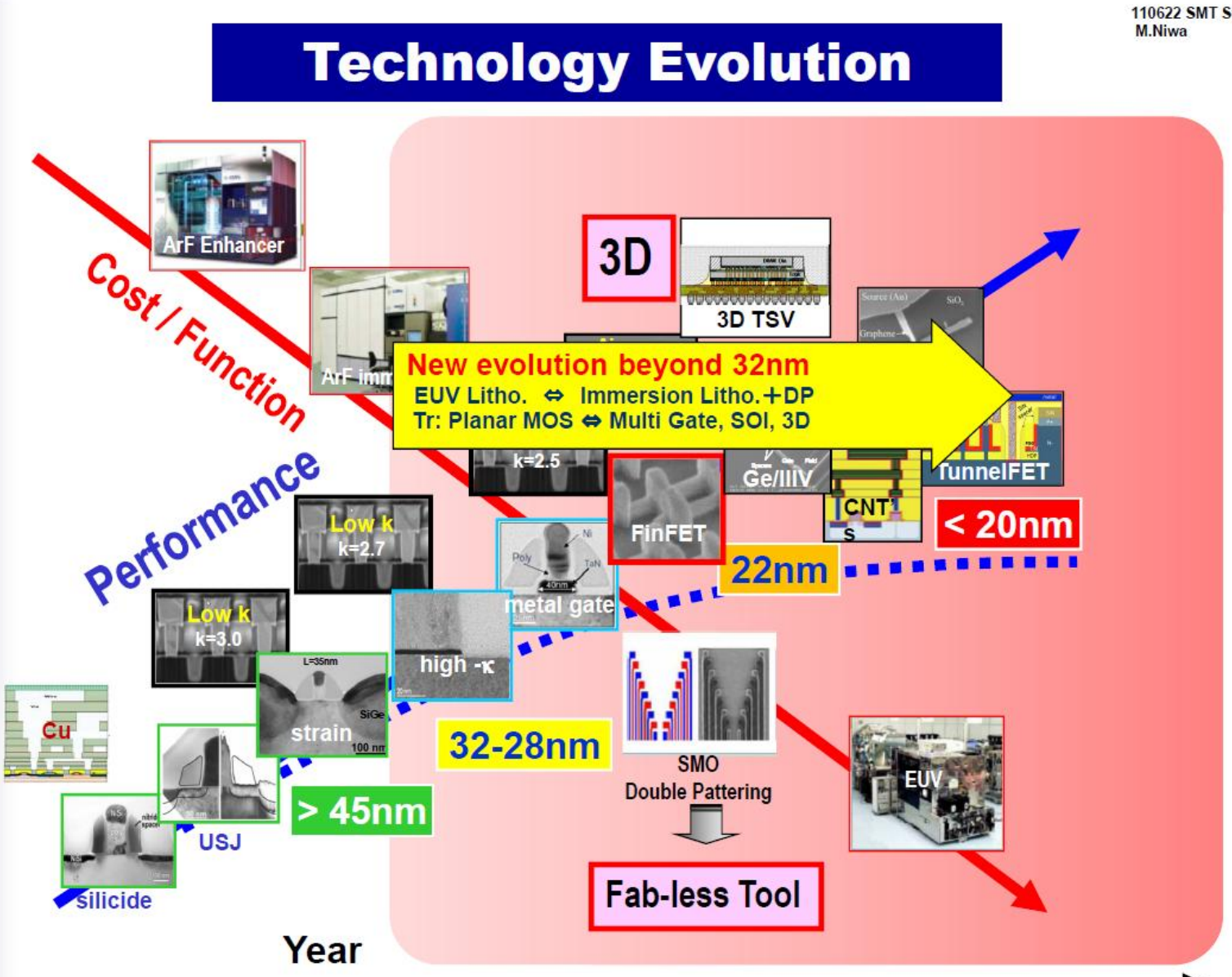


intel

Kelin Kuhn / SSDM / Japan / 2009

18

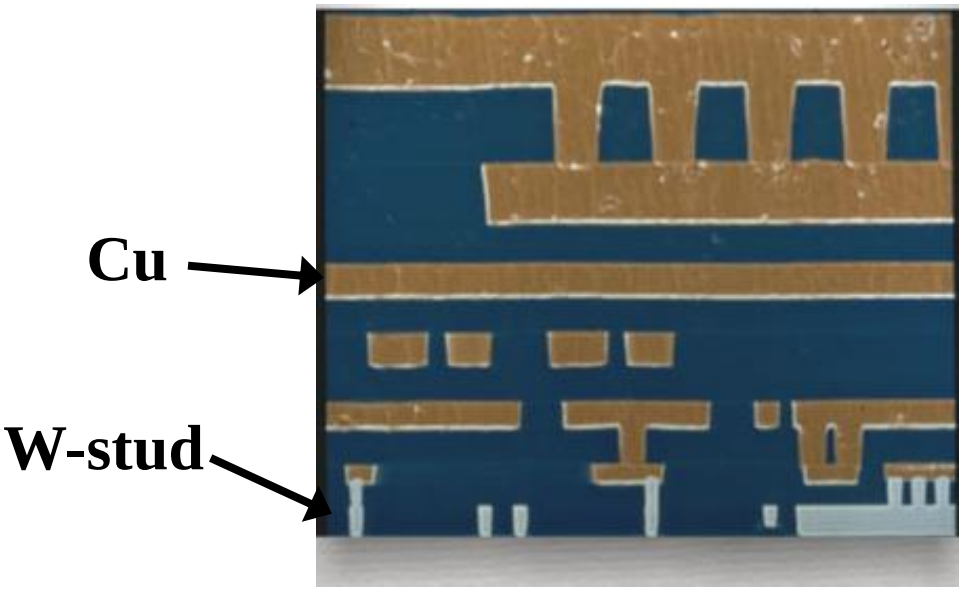
Taken from: Kelin Kuhn, “Moore's Law past 32nm: Future Challenges in Device Scaling” SSDM. 2009

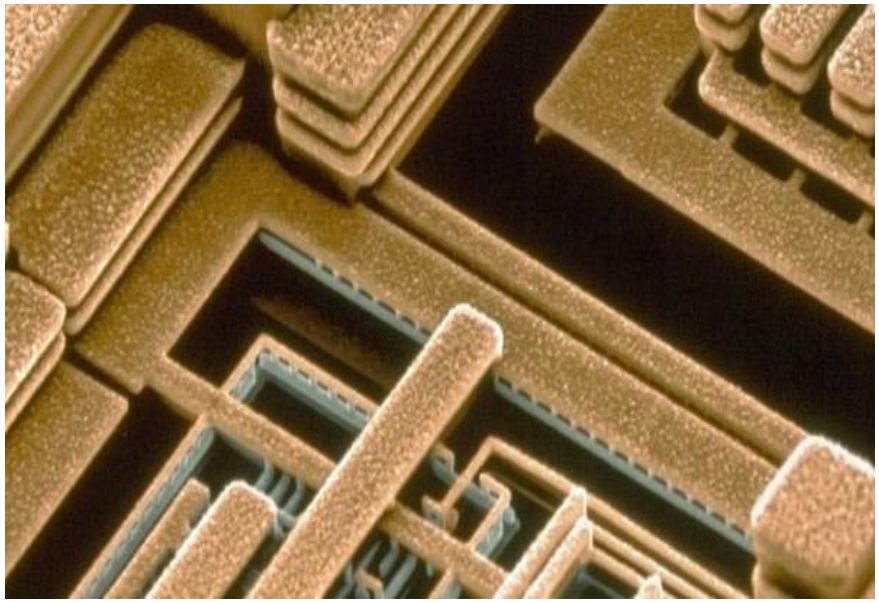


Taken from: Masaaki Niwa, "Development of 32nm CMOS and Recent Trend for Beyond 32nm" SMT Symp. 2011

IBM Cu Technology

To interconnect the extremely small transistors, a complex multi-level multi-layer metallization scheme is needed. Shown below is what IBM has done with their state-of-the-art Cu technology.





Six Cu metallization levels above the 1st metal level with tungsten studs to the transistors

http://www-3.ibm.com/chips/gallery/p-n2.html