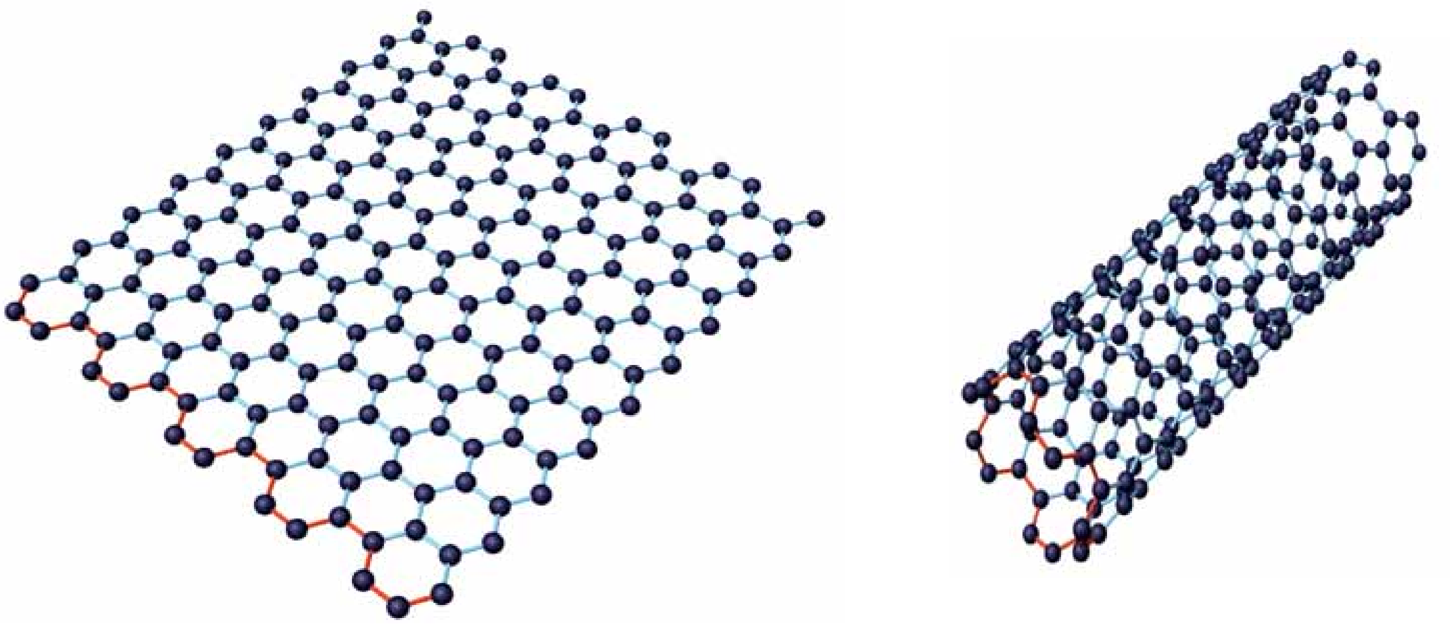
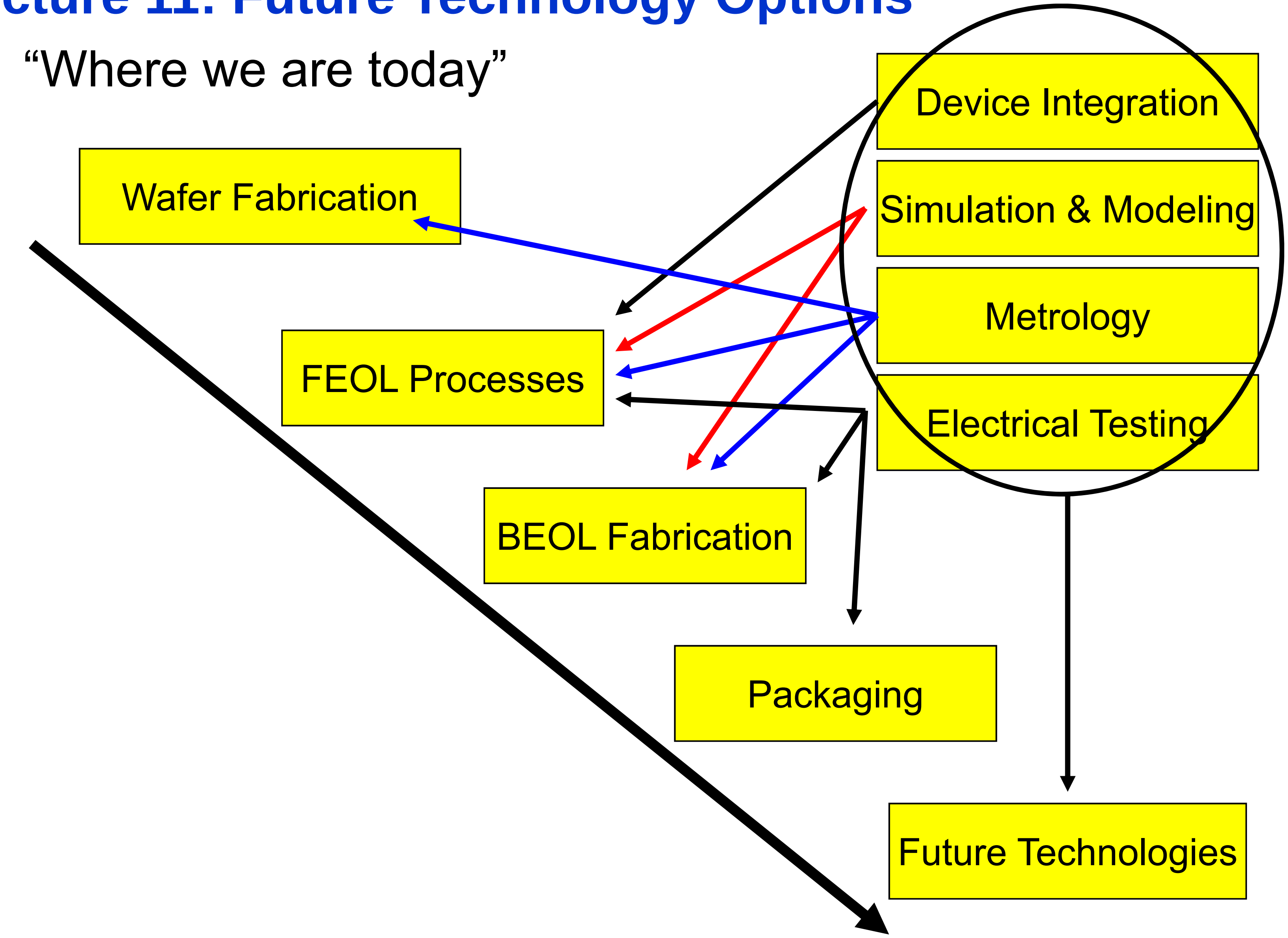
Lecture 12

Future Technology Options



Lecture 11: Future Technology Options

"Where we are today"



Device Integration

Simulation & Modeling

Metrology

Electrical Testing

Wafer Fabrication

FEOL Processes

BEOL Fabrication

Packaging

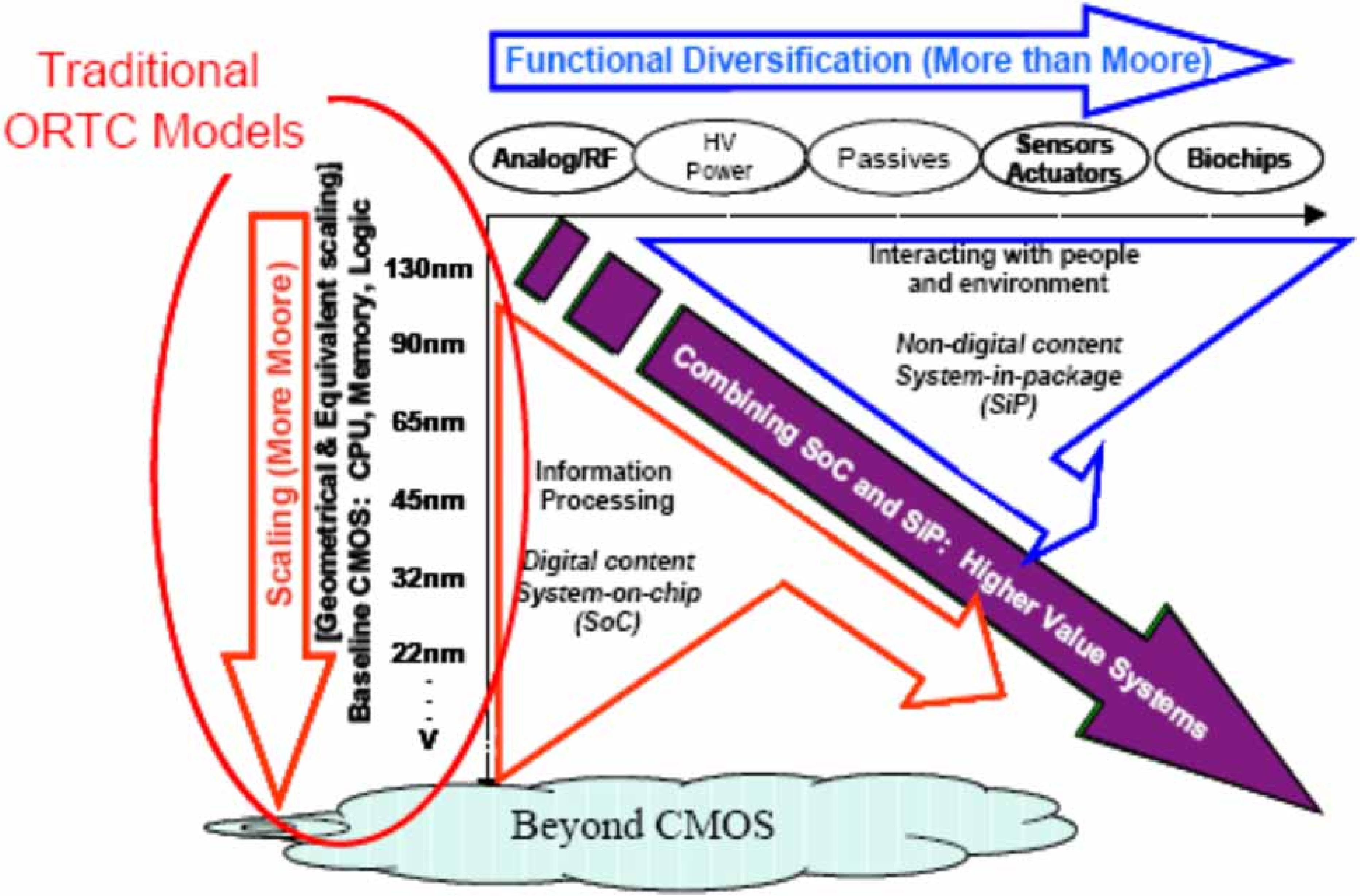
Future Technologies

Lecture 11: Outline

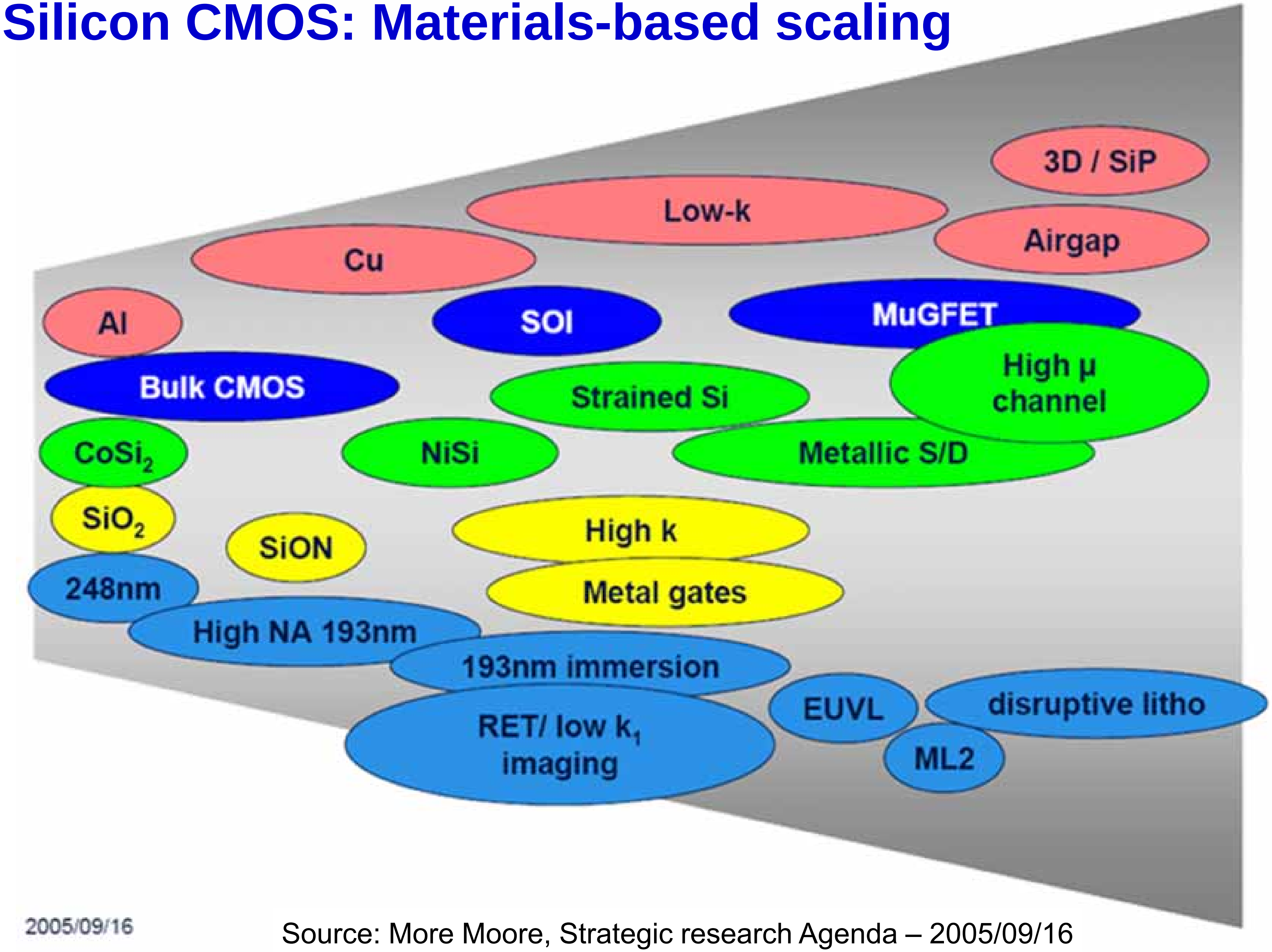
- Silicon CMOS
  - Scaling to the “End of the Roadmap”
- Carbon Technology
- Photonics
- Future Outlook

ITRS 2009

Moore's Law & More



Silicon CMOS: Materials-based scaling



Source: More Moore, Strategic research Agenda – 2005/09/16

FEOL Key Technologies

Atomic layer deposition (ALD)

Achieve atom-level control of gate oxide deposition

Pulsed laser annealing

Achieve ultra-fast, low-"thermal process" (small *Dt*) and high-temperature annealing

Plasma immersion implantation

Achieve ultra-shallow ion implantation

High mobility channel

Achieve local compact or tensile stress

and so on

Prof. Iwai, Tokyo Inst Tech.

BEOL Key Technologies

Atomic layer deposition (ALD)

Achieve atom-level control of depositions of Cu seed layer and diffusion barrier layer

Porous intermetal dielectric film materials and technology

Reduce interconnect parasitic capacitance

Damascene processing

Achieve advanced Cu interconnect to replace traditional Al interconnect

Multilevel-multilayer metallization,3D

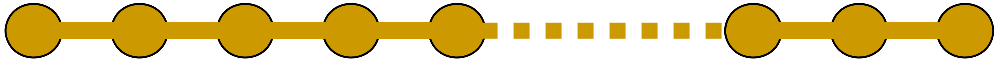
Make the best of the precious silicon surface and achieve ULSI technology

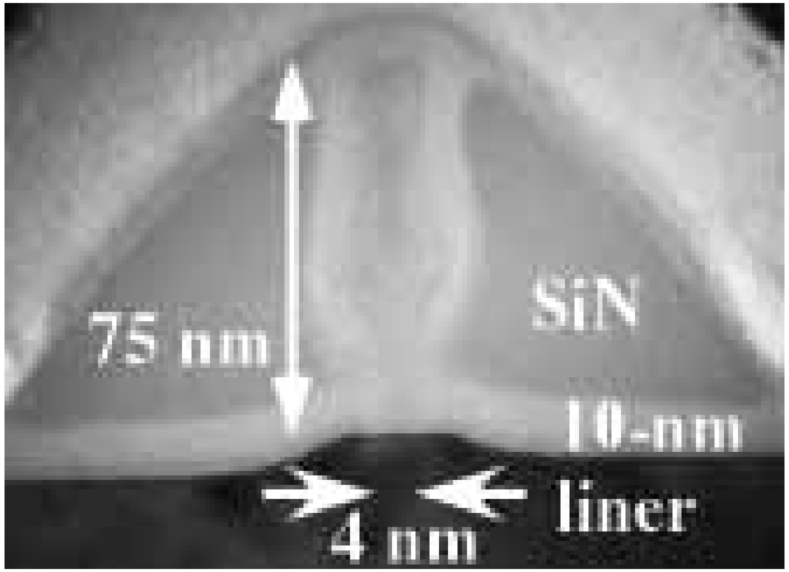
and so on

Prof. Iwai, Tokyo Inst Tech.

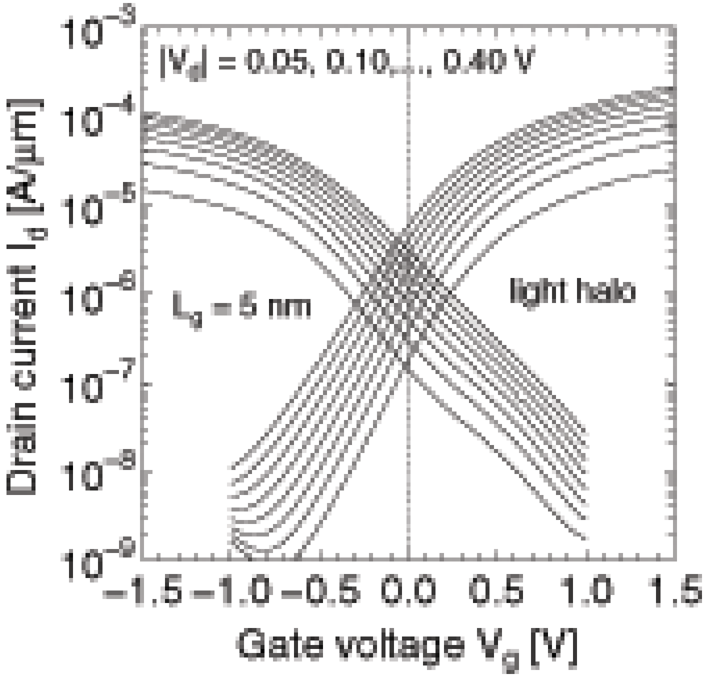
We have real (nano-device)!!

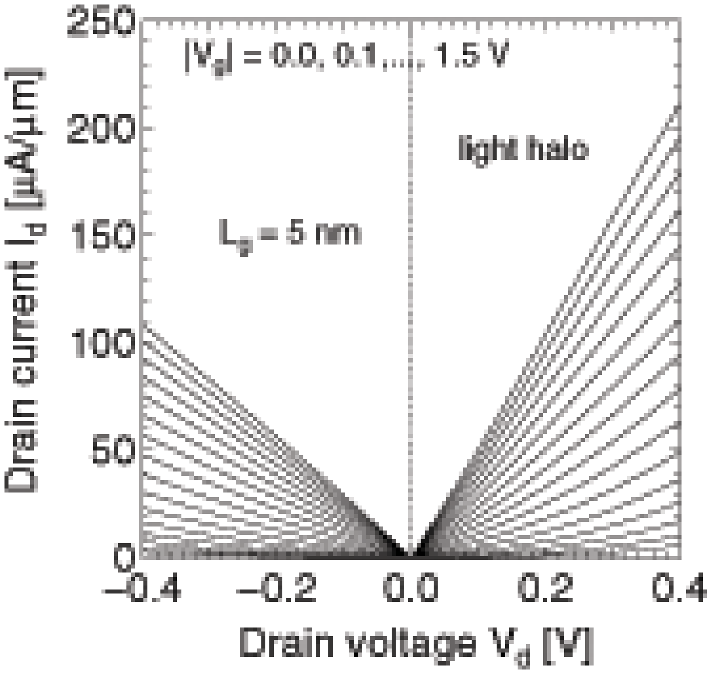
Length of 18 Si atoms





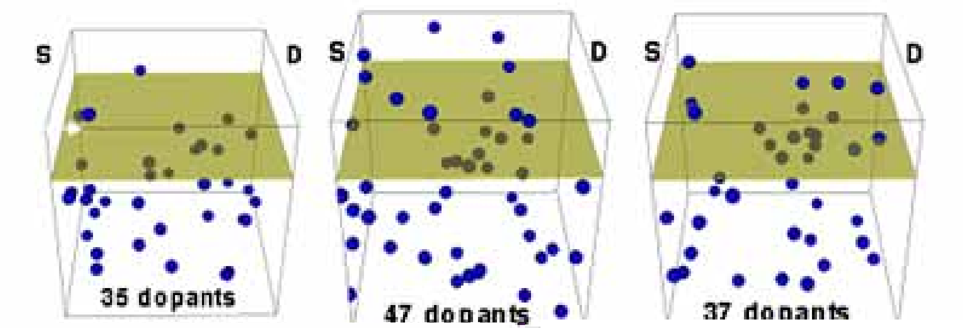
Wakabayashi
NEC

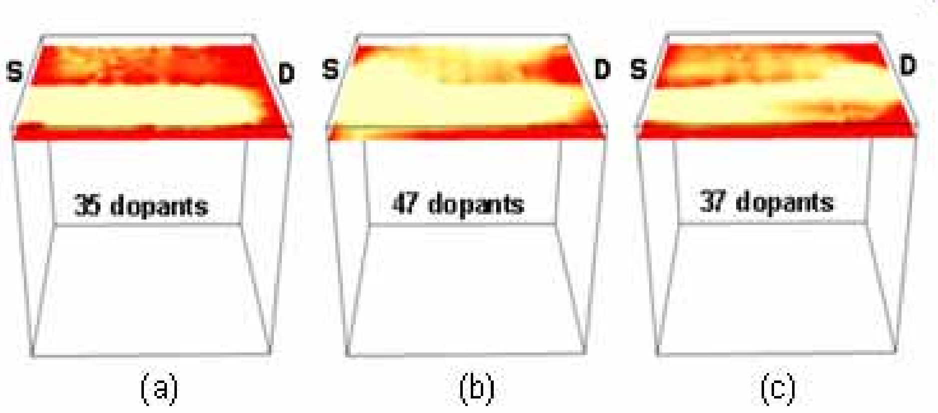




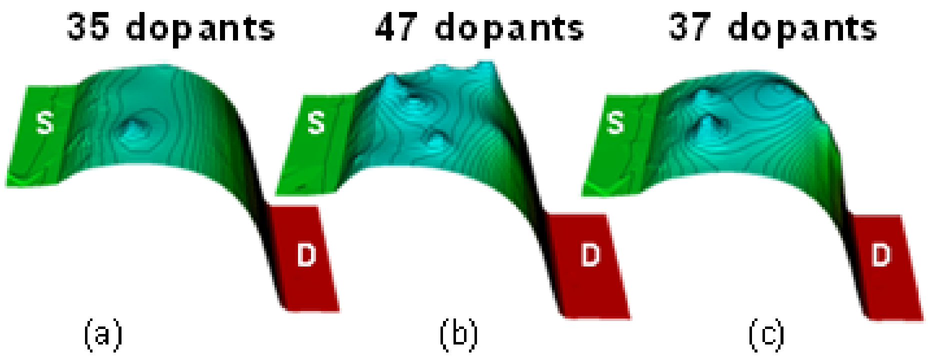
Random Dopant Fluctuation in Nano Devices

Random Dopant Fluctuations are a problem in nanoscale devices





On-state current distribution
(a) and (c) are similar
(b) is with smaller current due to the more discrete dopants positioned on channel surface



Off-state potential distribution
(b) and (c) are similar
(a) is with only one dopant positioned therefore has a larger off-state current

(C) 2011 National Nano Device Laboratories

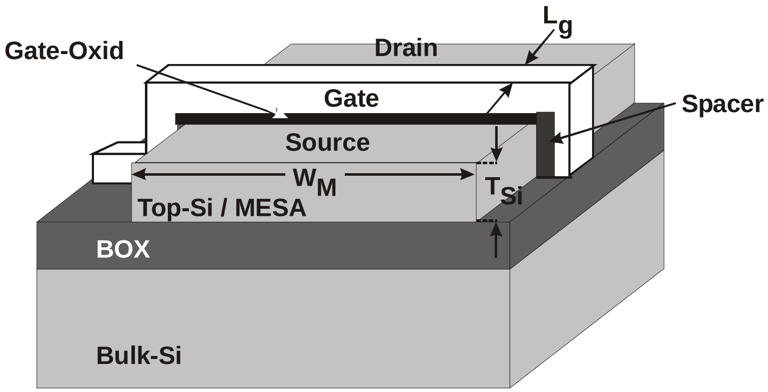
Novel 3-D Transistor Architectures

Goal: Reduce negative consequences of scaling!

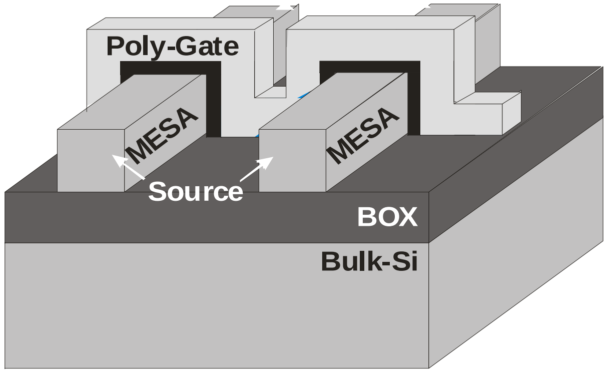
Solution to thermal & diode leakage:

Improved control of the transistor channel by multi gate architectures (Triple-Gate, Tri-Gate, FinFET, MuGFET)

Off-state current not blocked by doping, but by gate electrode



SOI MOSFET



Triple-Gate MOSFET

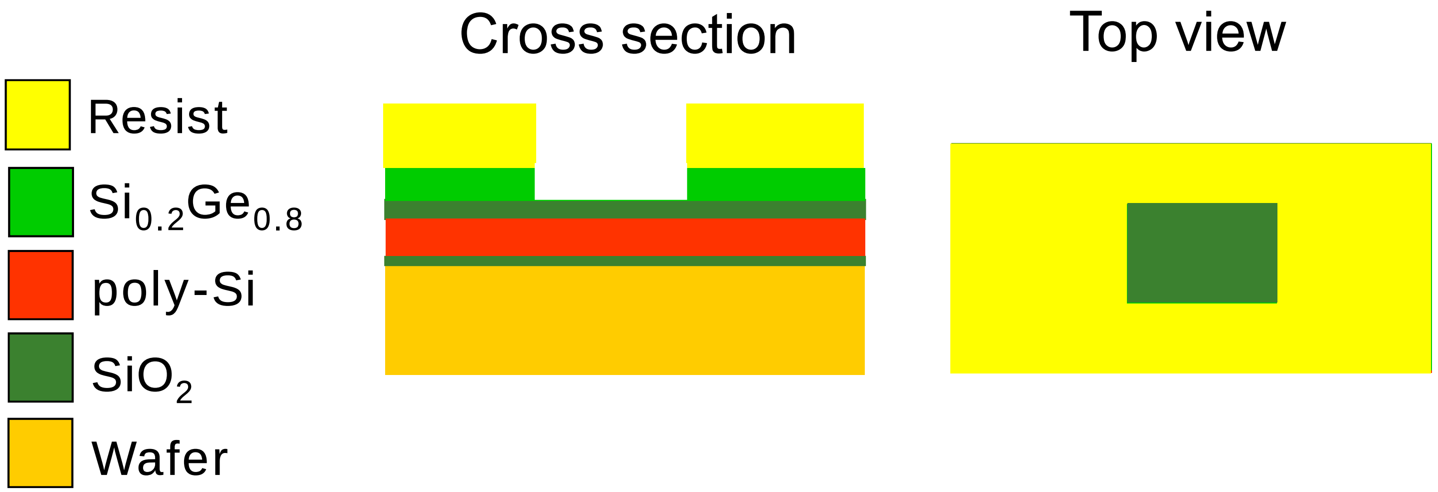
Sidewall Transfer Lithography:
An innovative process technology for nanoscale devices

Sidewall Transfer Lithography Characteristics and Advantages

- ✓ **Innovation and combination of normal lithography and standard silicon thin film technology**
- ✓ **For narrow lines, theoretically $k_1 \rightarrow 0$**
- ✓ **Pitch size depends on lithography resolution.**
- ✓ **The use of normal lithography guarantees high throughput.**

$$R = k_1 \frac{\lambda}{NA}$$

STL Technoloyg 1



Aim: Fabricate Nanoscale Poly-Si Gate (Red Strip)

STL Technoloyg 2

🟦 SiN

🟩 $Si_{0.2}Ge_{0.8}$

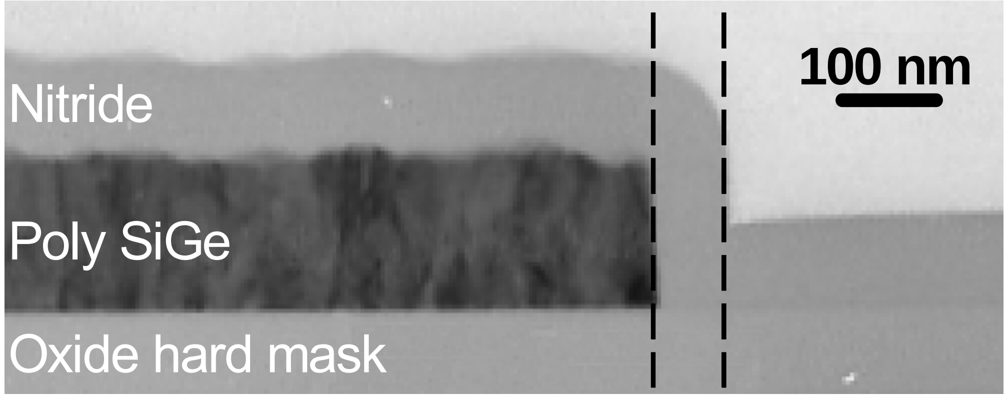
🟥 poly-Si

🟩 SiO_2

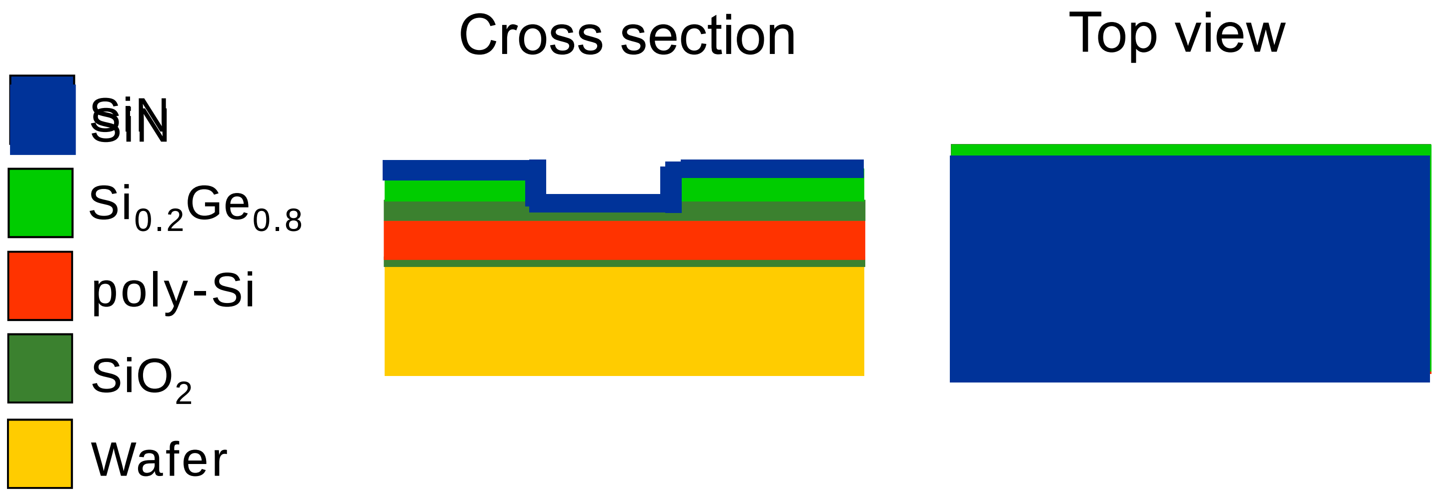
🟨 Wafer

Cross section

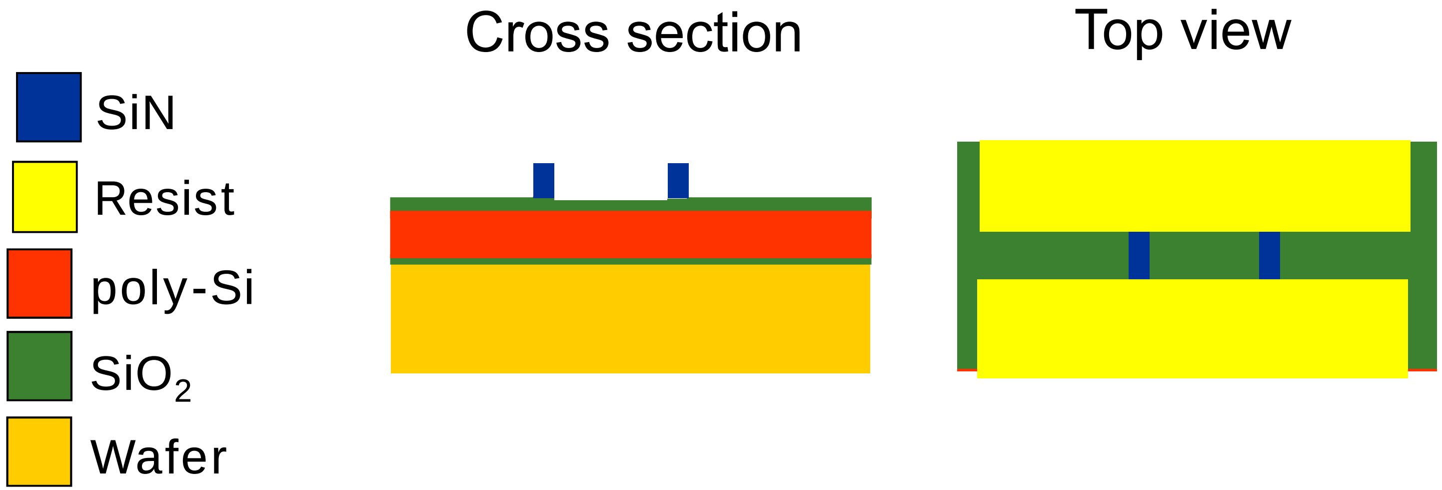
Top view



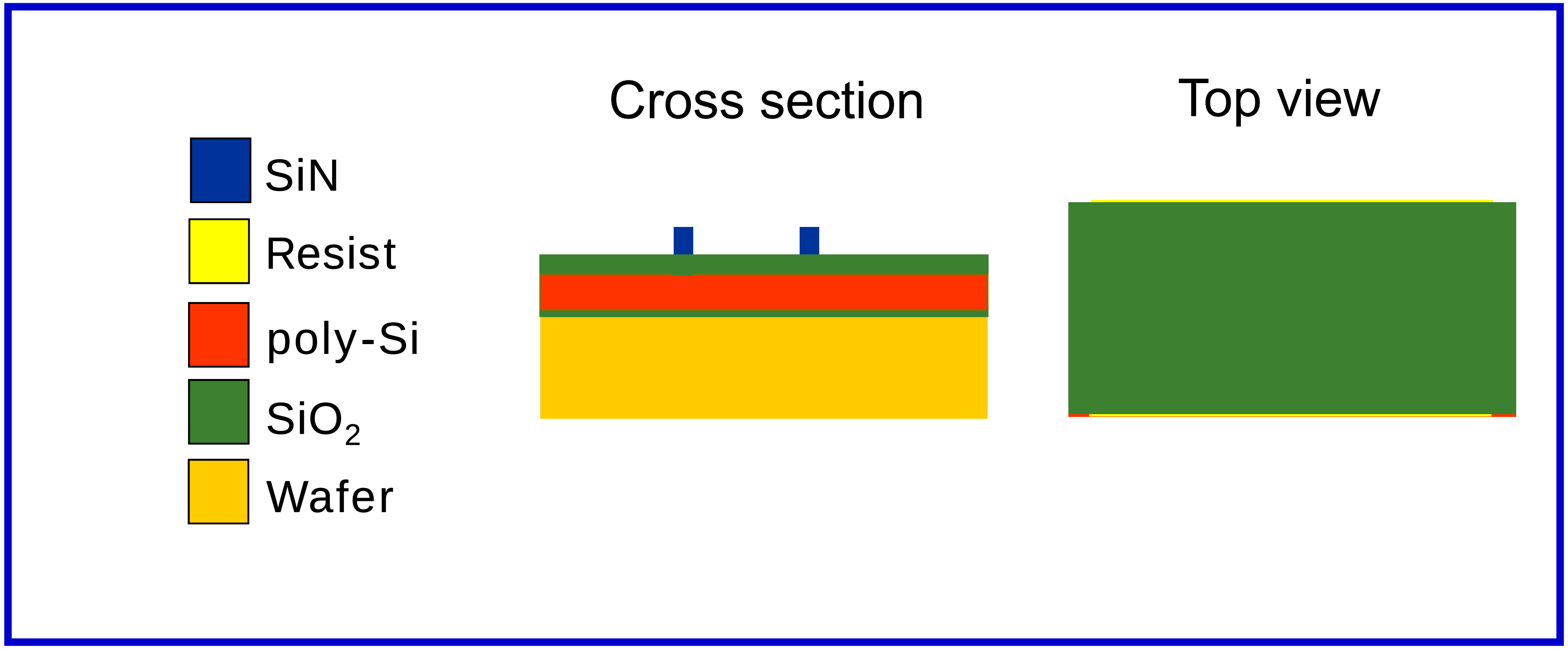
STL Technoloyg 3



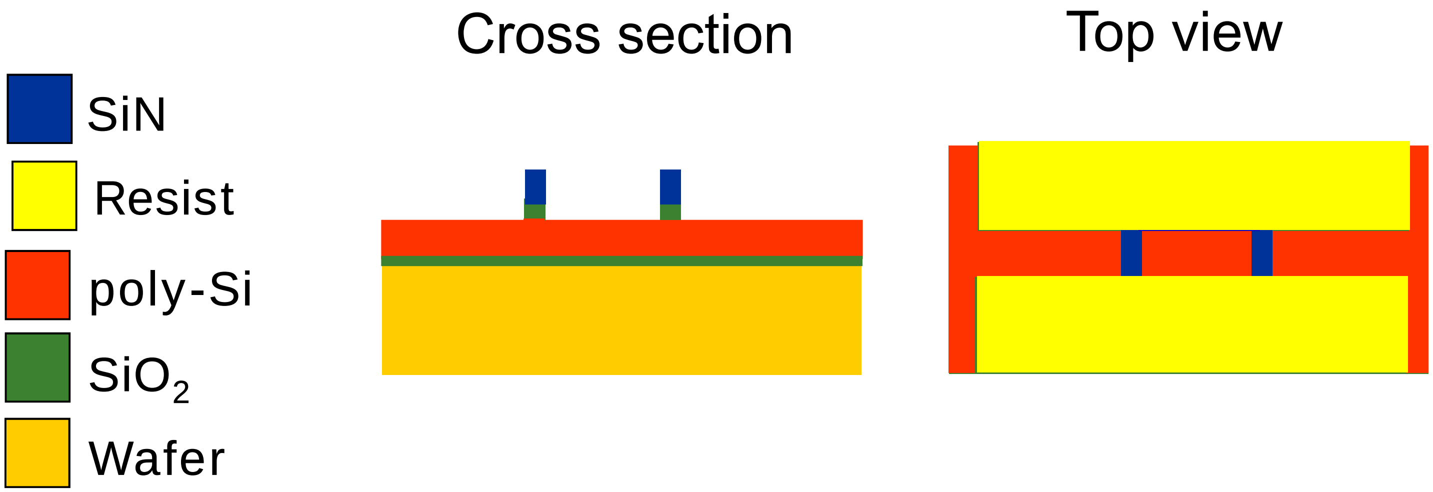
STL Technoloyg 4



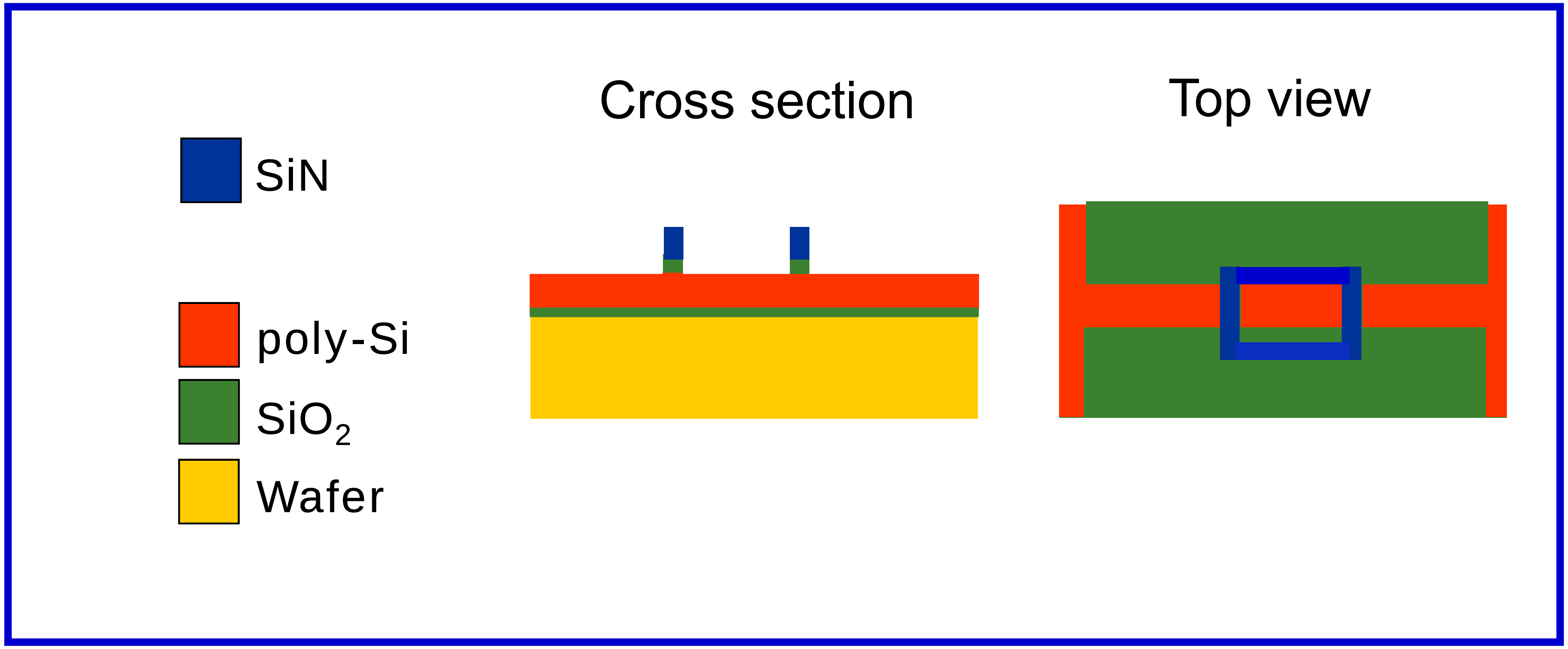
STL Technoloyg 5



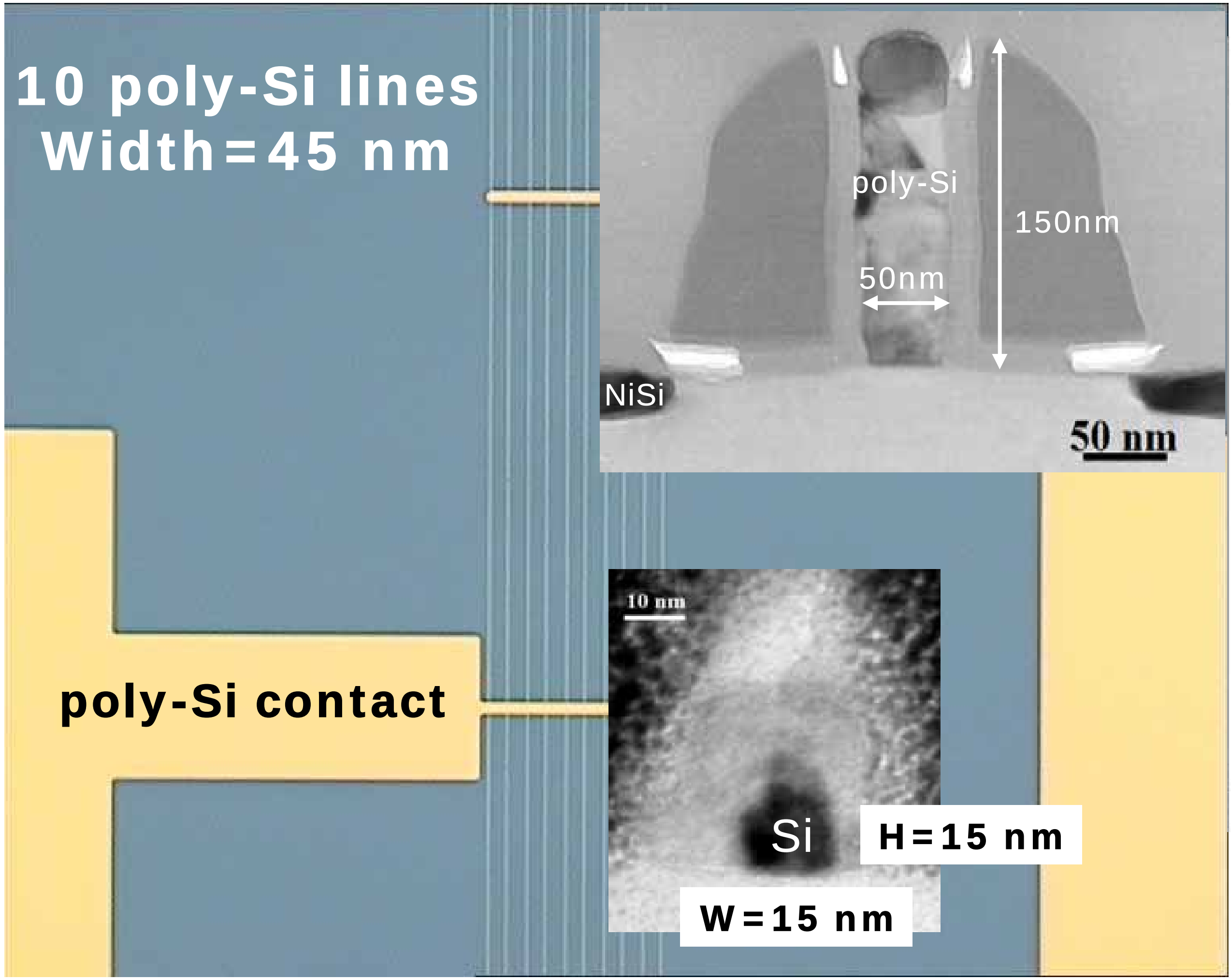
STL Technoloyg 6

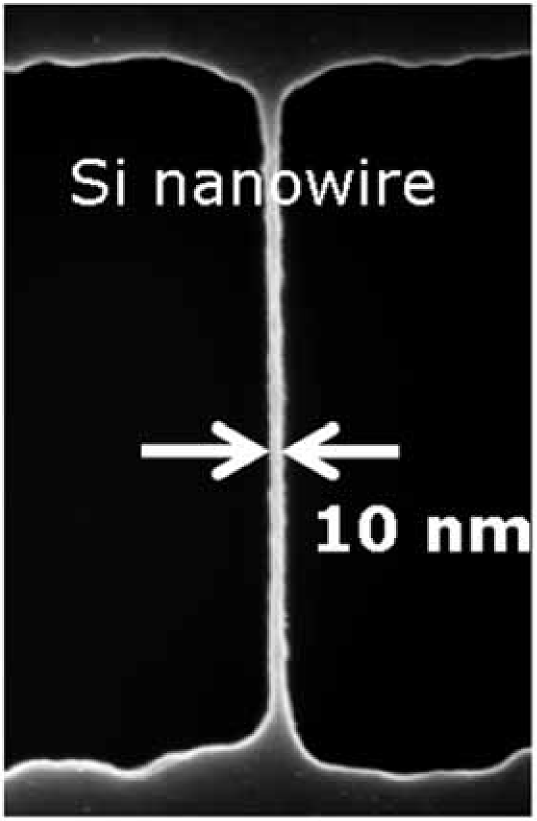


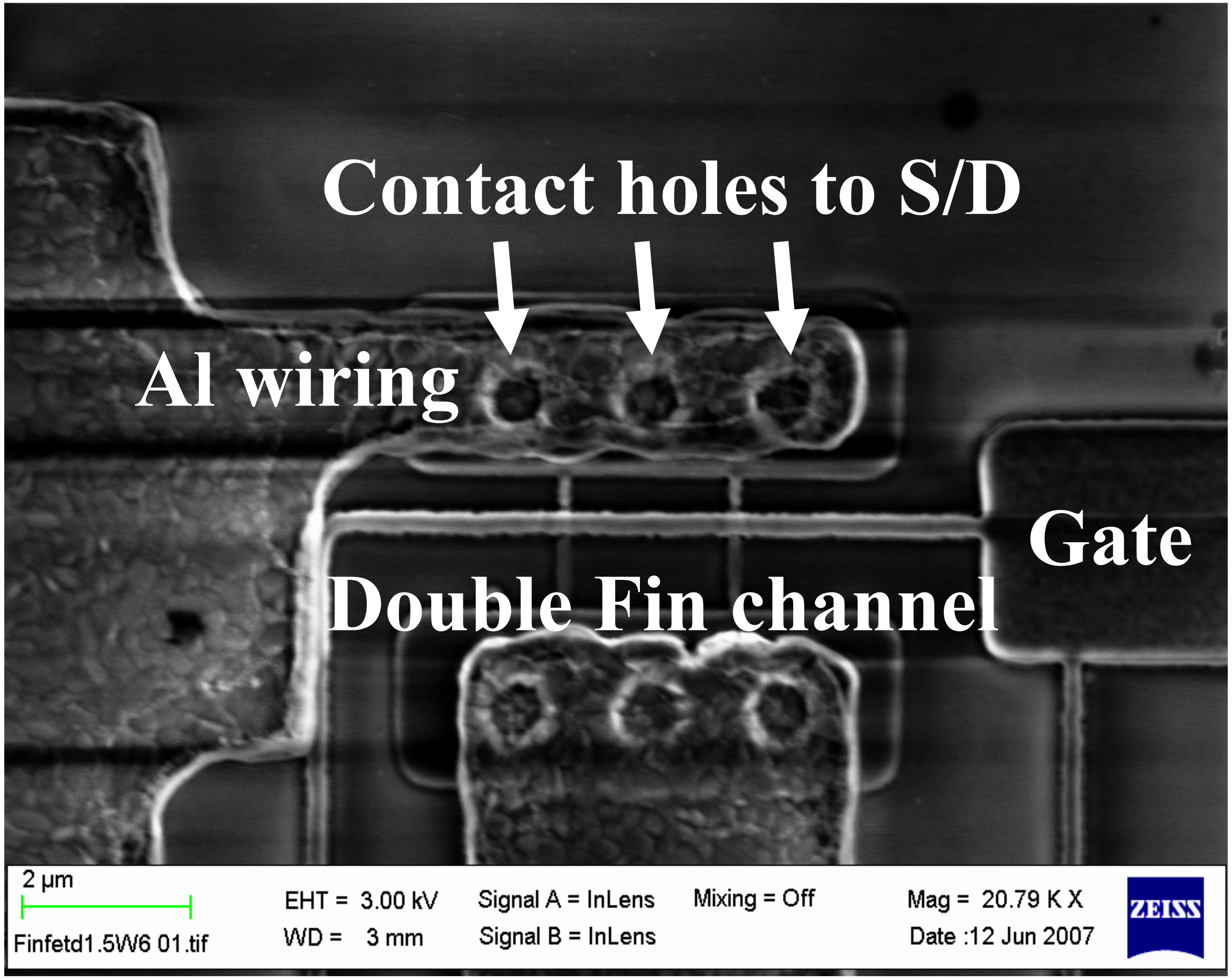
STL Technoloyg 7



STL Technoloyg 8







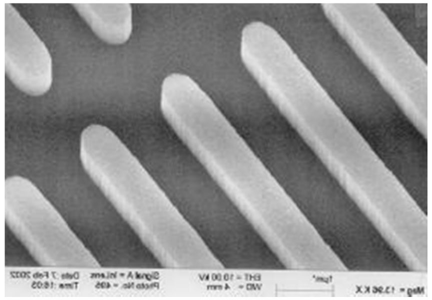
FinFET produced using STL twice

Fin W=35 nm
Fin H=27 nm
L=70 nm

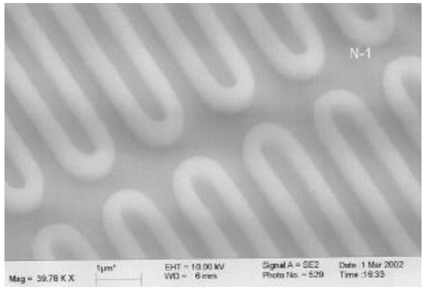
Zhang & Qiu *et al.* IEEE EDL May 2008

High-Density Patterns by STL Technology

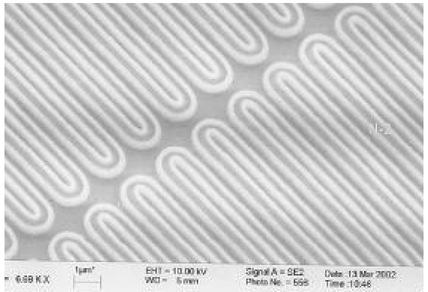
Photo-lithographically defined sacrificial structures



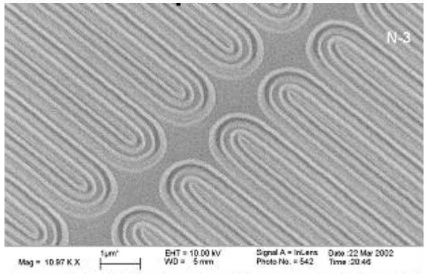
1st Spacers



2nd Spacers



3rd Spacers



2ⁿ lines after n iterations of spacer lithography!

Y.-K. Choi *et al*., *JVST-B* 21, 2951-2955 (2003)

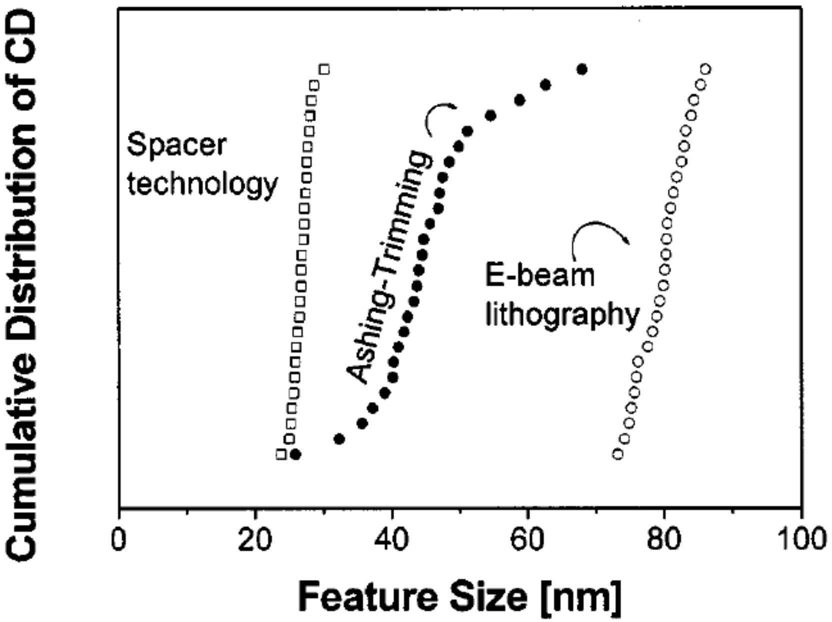
Wire Size Control in STL Technology

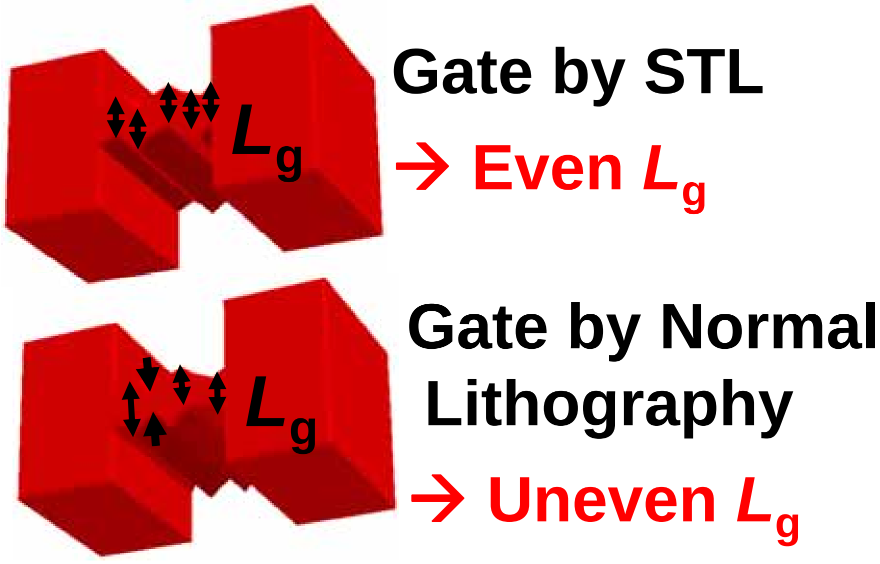
CVD deposited thin films have extraordinary uniformity and controllability

⇨STL nanowire width is determined by SiN thin films

⇨ STL nanowire thickness is determined by poly-Si thin films

Choi *et al.*, *IEEE T-ED* 49, 436（2002）





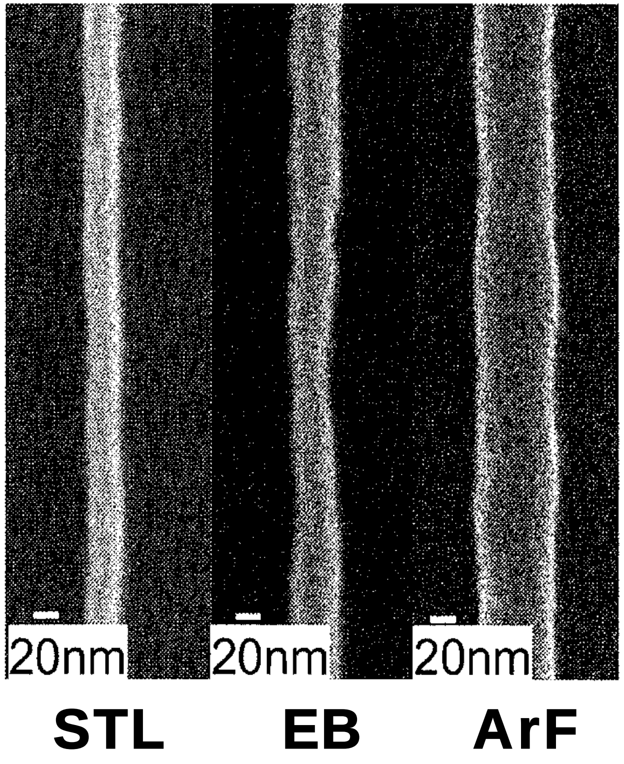
Gate by STL

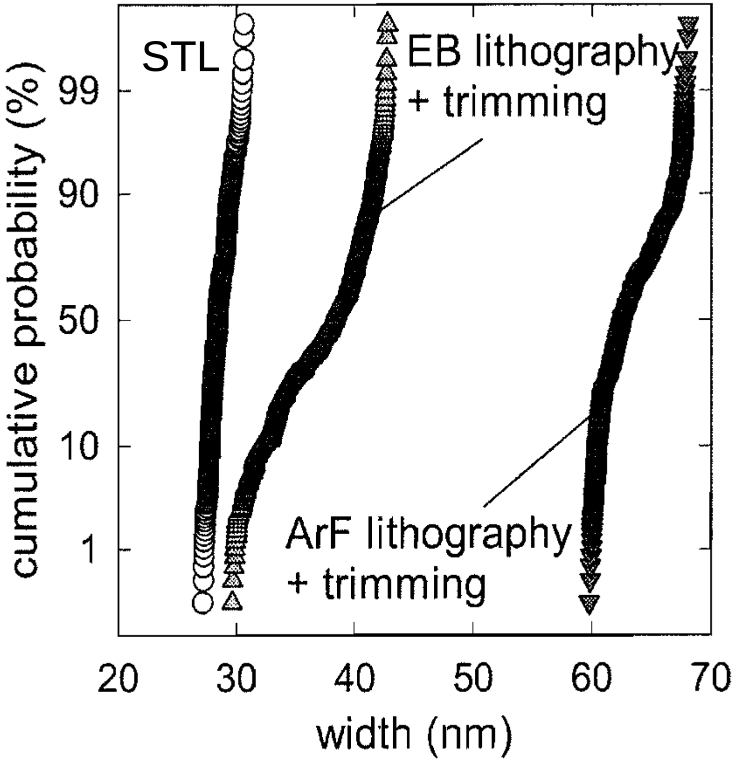
→ Even L_g

Gate by Normal Lithography

→ Uneven L_g

Very Small Width-Inhomogeneity in STL-Made Nanowires!

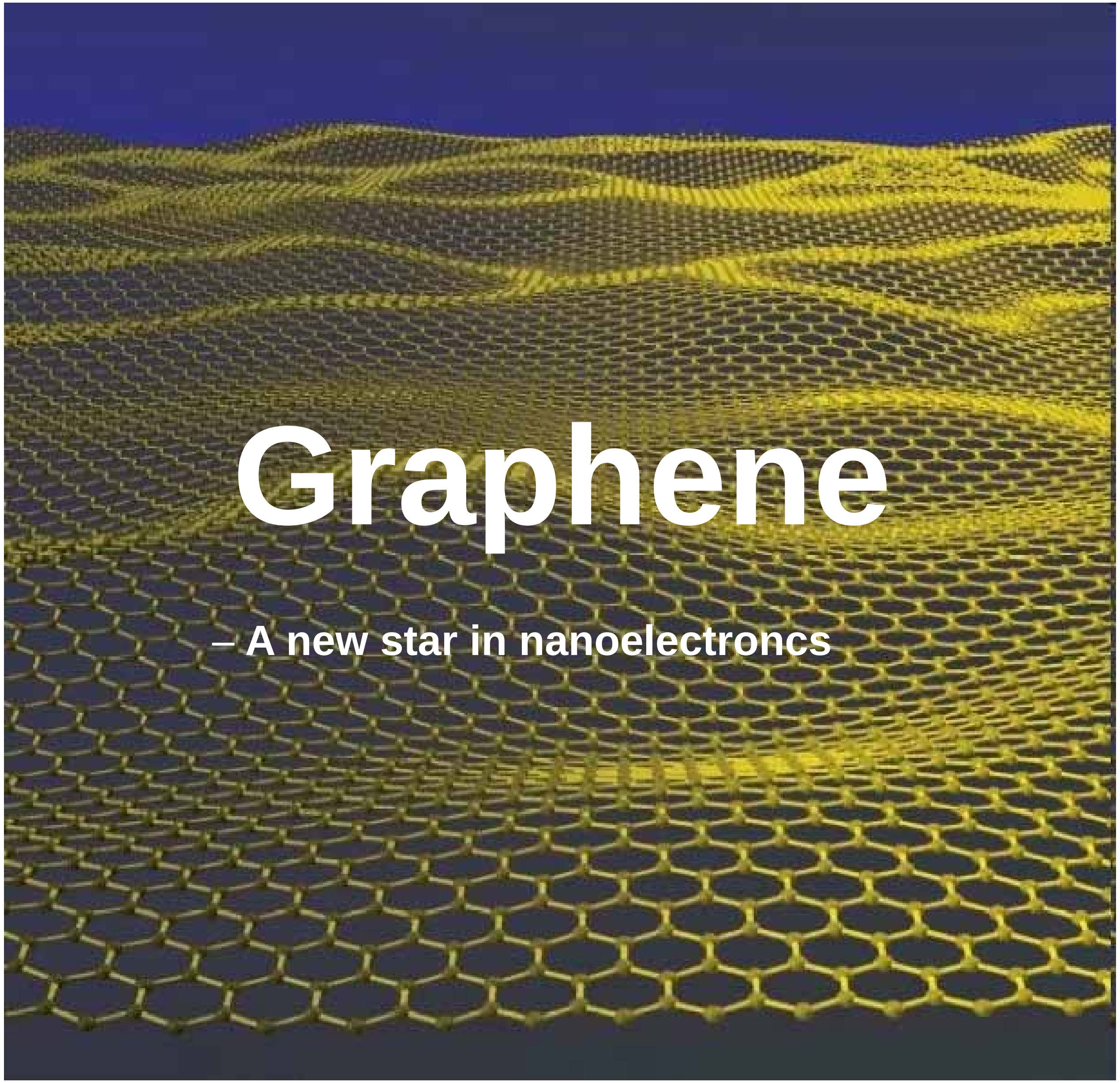




Kaneko et. al., IEDM2005

Lecture 11: Outline

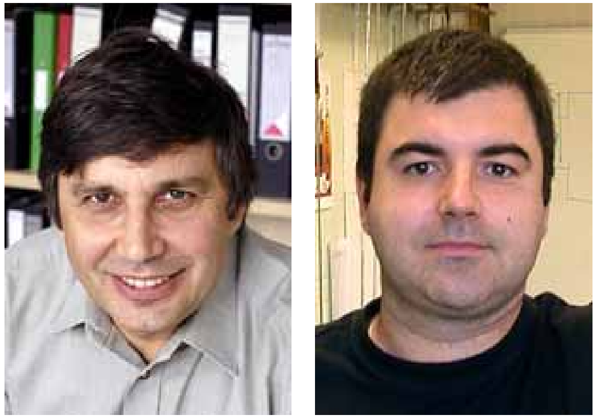
- Silicon CMOS
- Carbon Technology
  - Graphene
  - Carbon Nanotubes (CNTs)
- Photonics
- Future Outlook



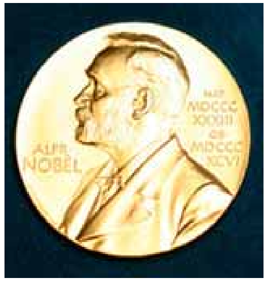
Graphene

– A new star in nanoelectroncs

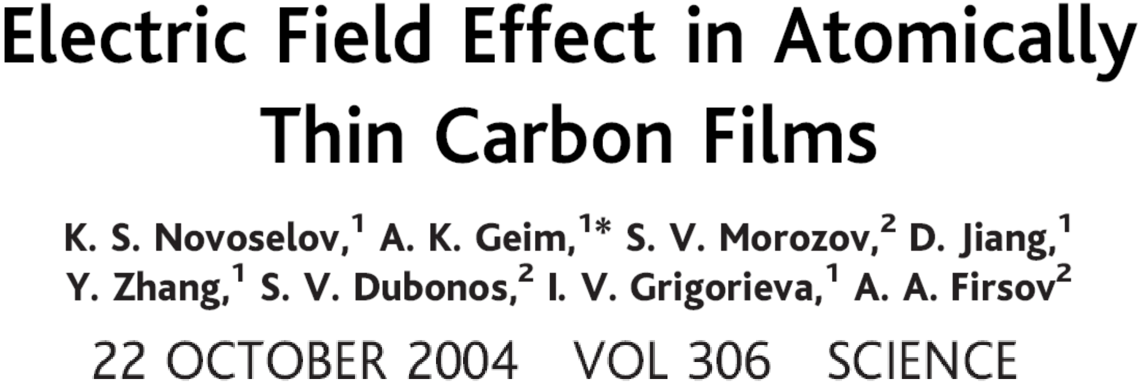
Graphene – A ”Nobel” Material



The Nobel Prize in Physics 2010
Andre Geim, Konstantin Novoselov



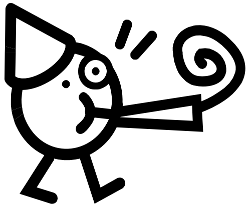
"for groundbreaking experiments regarding the two-dimensional material graphene"

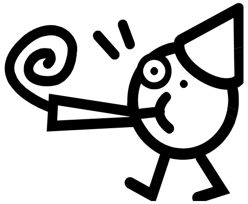


Electric Field Effect in Atomically Thin Carbon Films

K. S. Novoselov,[1] A. K. Geim,[1*] S. V. Morozov,[2] D. Jiang,[1]
Y. Zhang,[1] S. V. Dubonos,[2] I. V. Grigorieva,[1] A. A. Firsov[2]

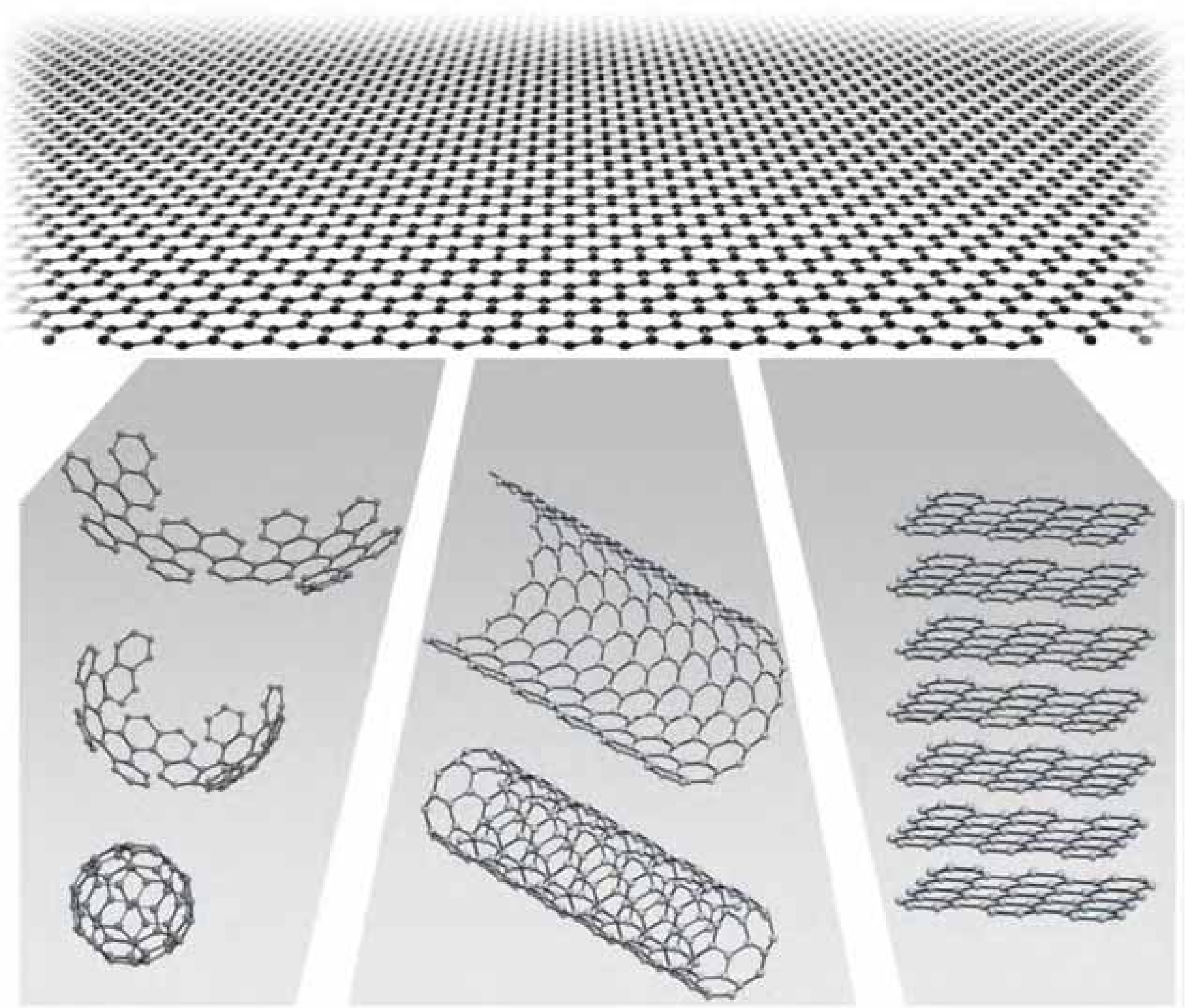
22 OCTOBER 2004 VOL 306 SCIENCE





Graphene

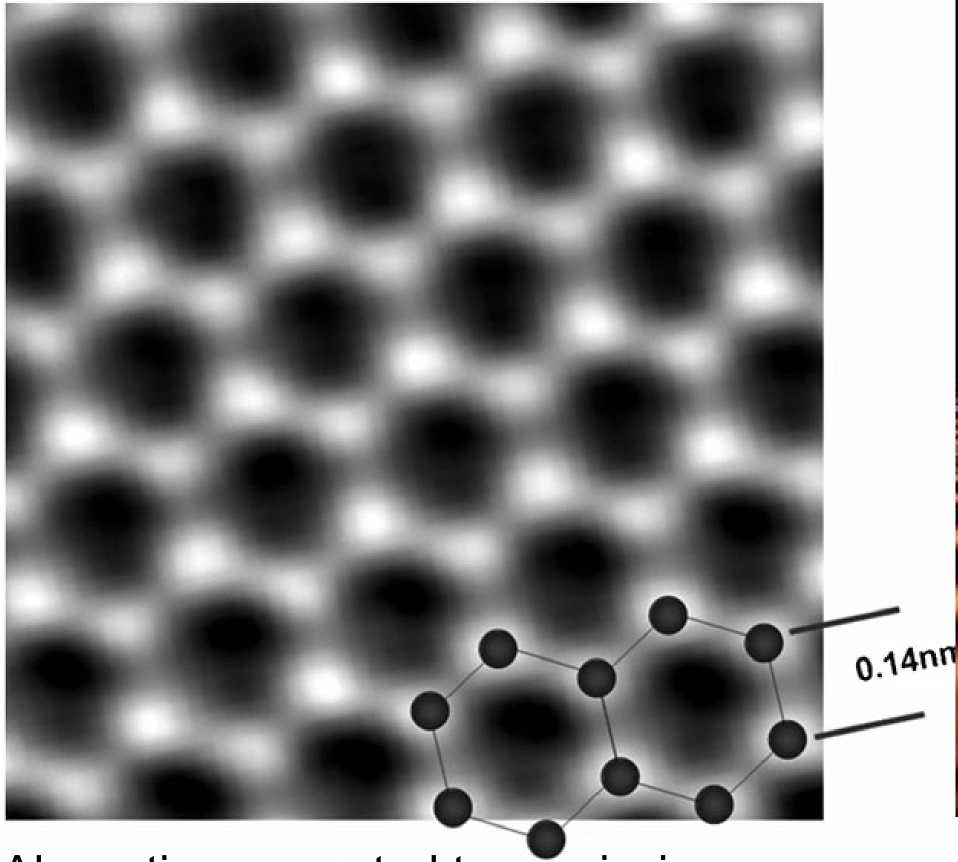
Mother of all graphitic forms



0 D buckyballs 1 D nanotubes 3 D graphite *Nature Mater*. **6**., 183, 2007

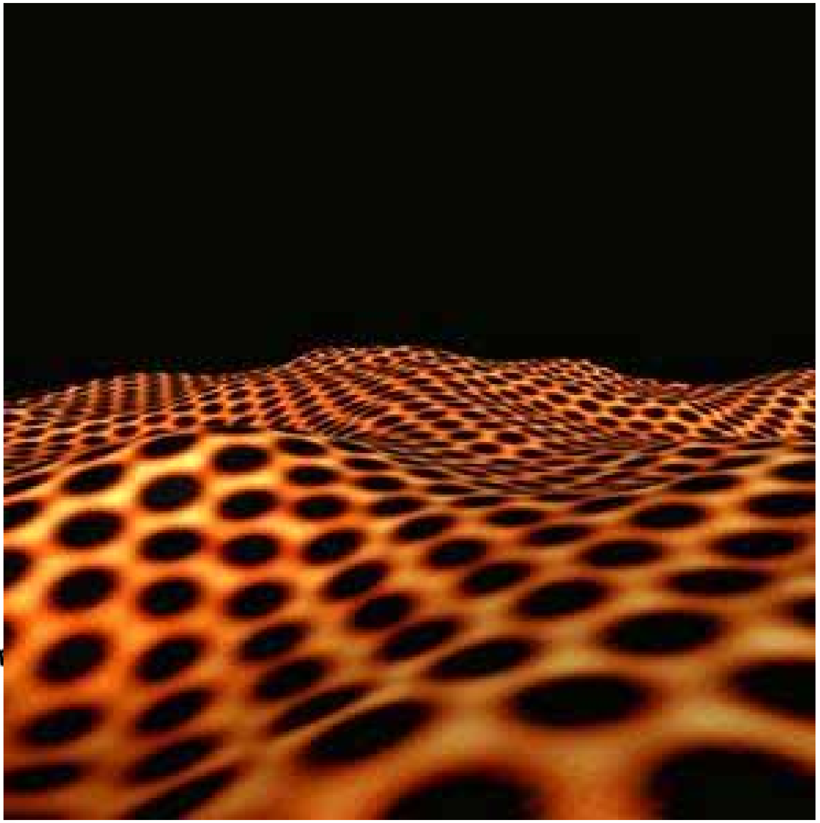
Graphene: Images

Visualization of graphene by HRTEM… and by STM



Aberration-corrected transmission electron microscope (TEAM 0.5)

Chem. Commun., 2009, 6095 - 6097

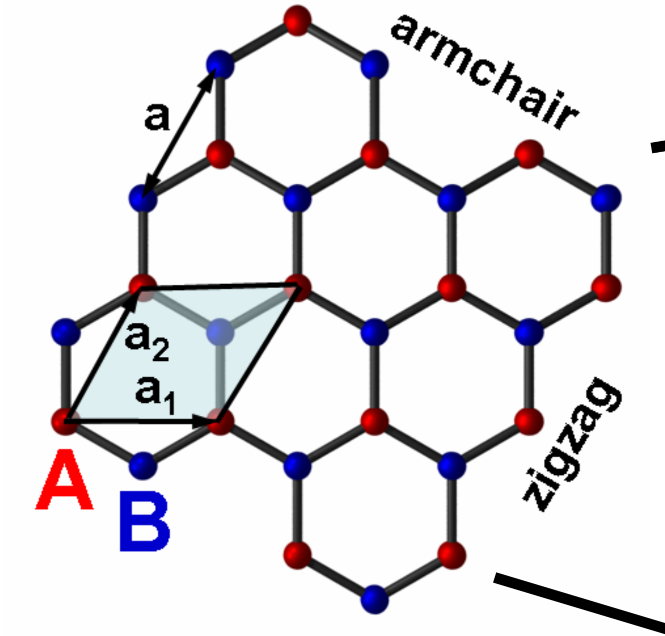


Scanning tunneling microscope image of graphene on SiO_2

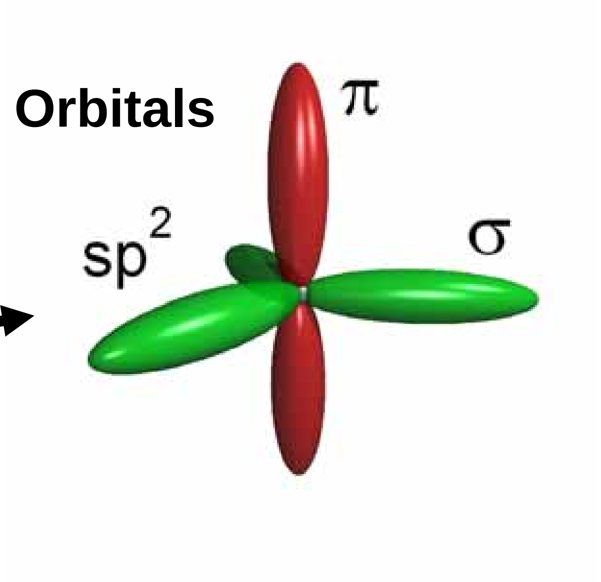
Mashoff et al, Nanoletters 2010

Graphene: Properties

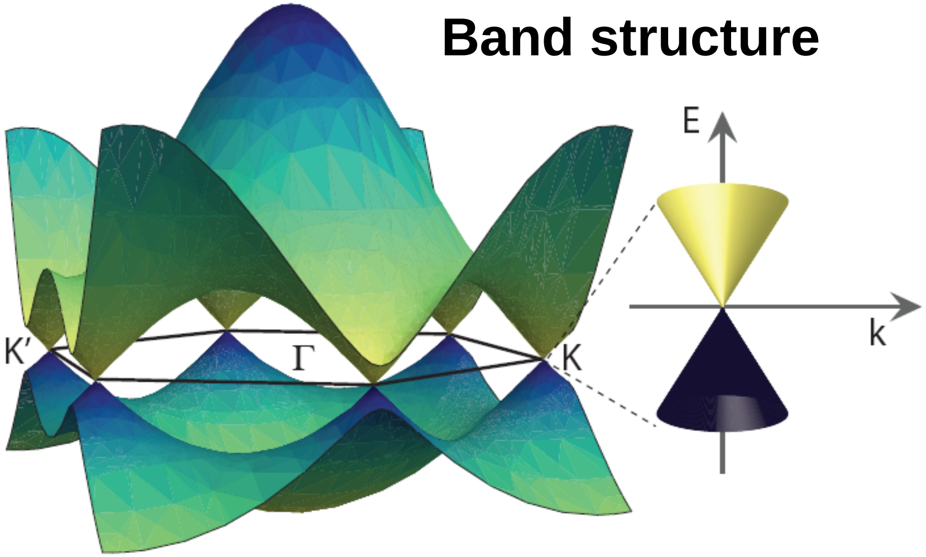
2D-crystal lattice



Orbitals



Band structure



Sublattice constant:

a = 0.246 nm

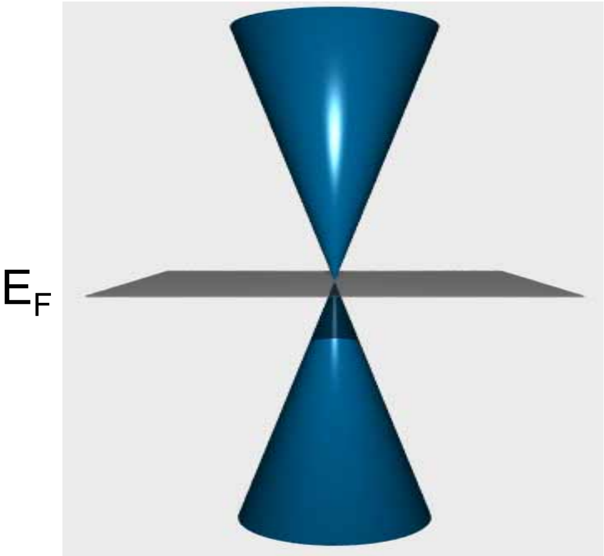
“Thickness”:

d = 0.34 nm

After: Wallace, Phys. Rev. 71, 622 (1947)

Graphene: Properties

E-k diagram of graphene



„Zero-gap semiconductor“ or „semimetal“

Linear dispersion relation (Fermi-Dirac instead of Schrödinger equation)

Massless dirac fermions, v ~ c/300

Mobility µ: > 25.000 cm^2/Vs @ RT
up to ~ 200.000 cm^2/Vs suspended

Mean free path: L_{MFP} ~ 400nm @ RT

Current density: $J > 10^8$ A/cm^2

Thermal conductivity ~5×10^3 to W/mK @ RT

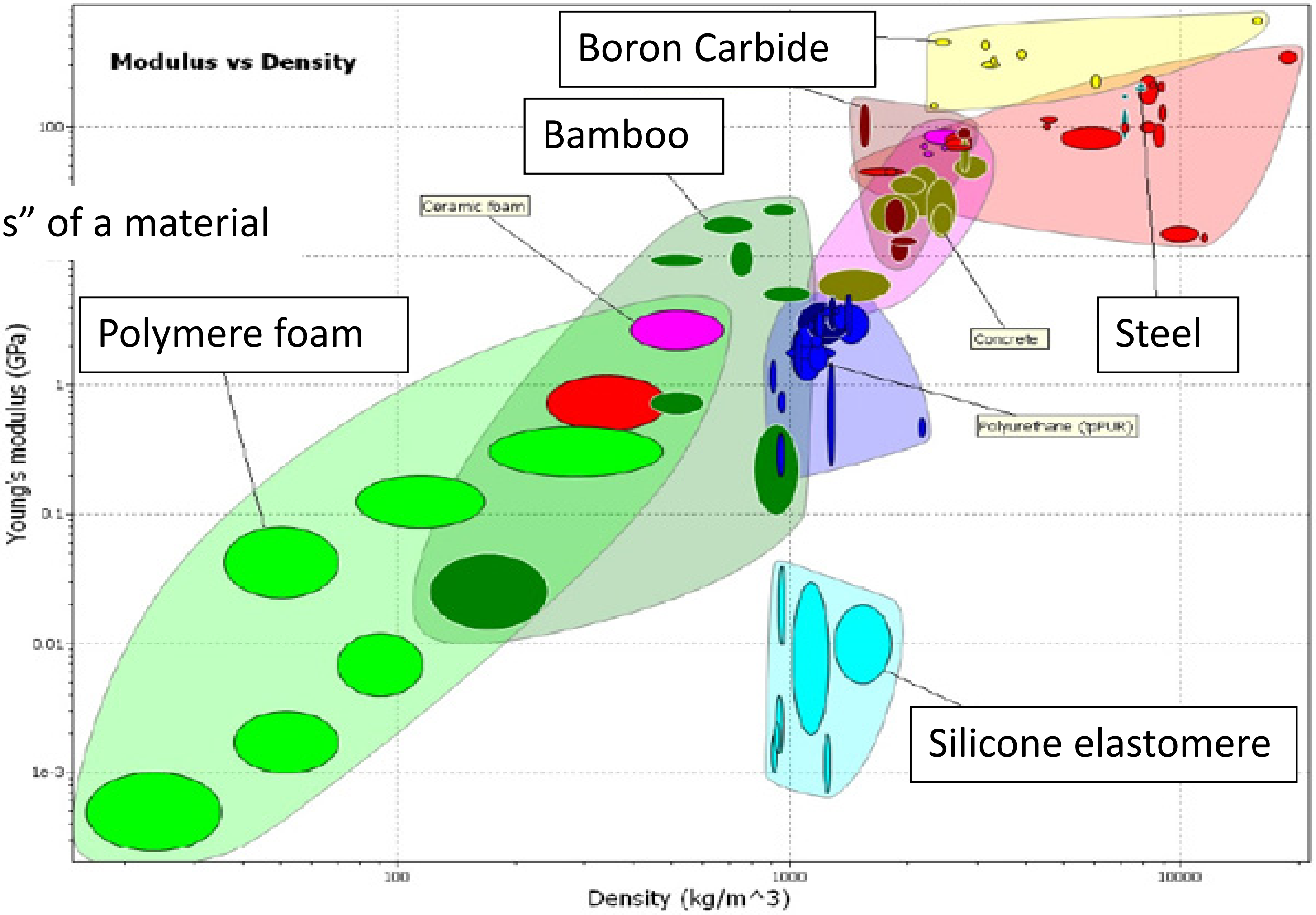
Potential for:

- High switching speeds
- Interconnects
- Optoelectronics
- Ballistic devices

Graphene: Properties

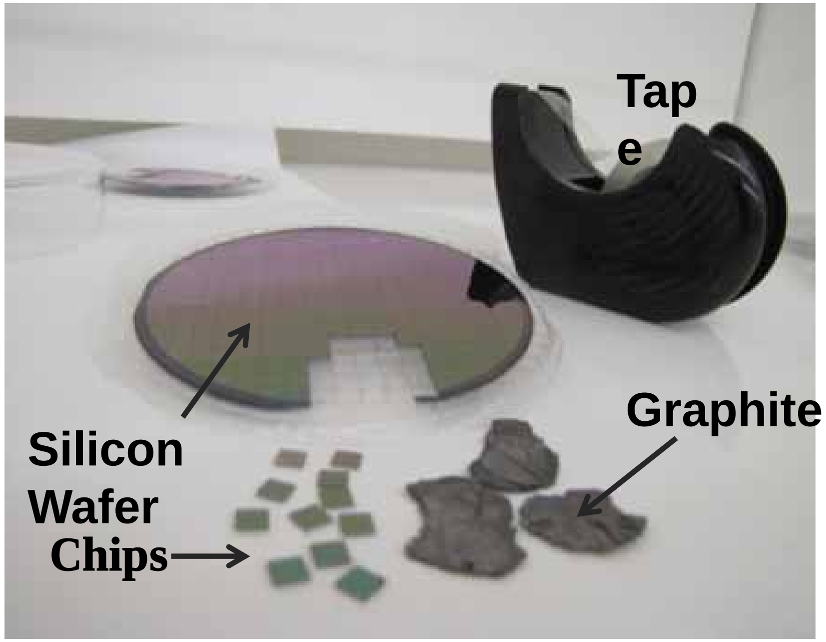
● Graphene

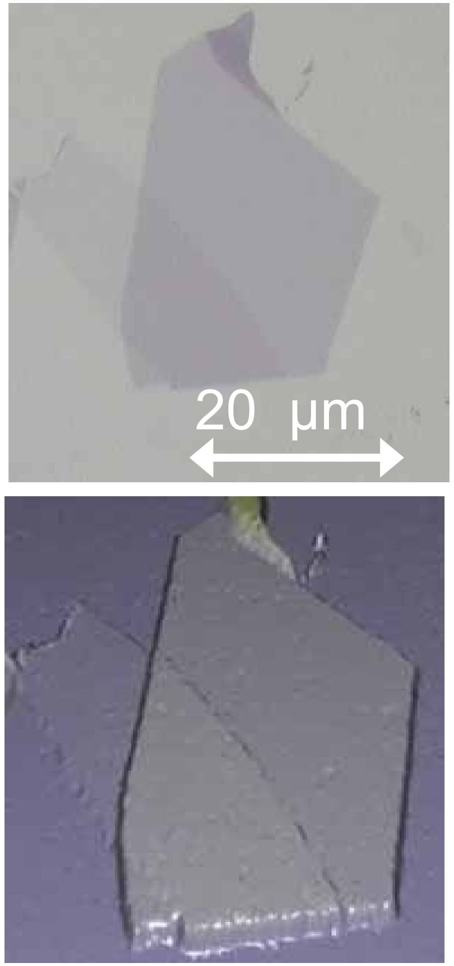
”Stiffness” of a material



Graphene Fabrication Methods: Exfoliation (1/4)

Exfoliation with adhesive tape



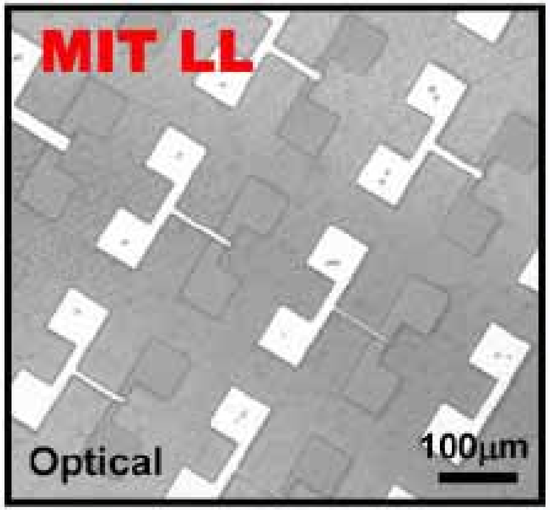


- Novoselov et al., Science 306, 666 (2004)
- flake size: 5 – 100 mm
- random location
- simple process for proof-of-concept
- ***no industrial relevance***

Graphene Fabrication Methods: Epitaxy (2/4)

Thermal decomposition of SiC (epitaxial graphene)

- Berger et al., J. Phys. Chem. B 108, 2004
- limited scalability
- experimentally complex (8N H2…)
- high temperatures (~1500°C)
- high cost of material



Kedzierski et al., IEEE TED, 2008

KTH approach: SiC growth on Silicon

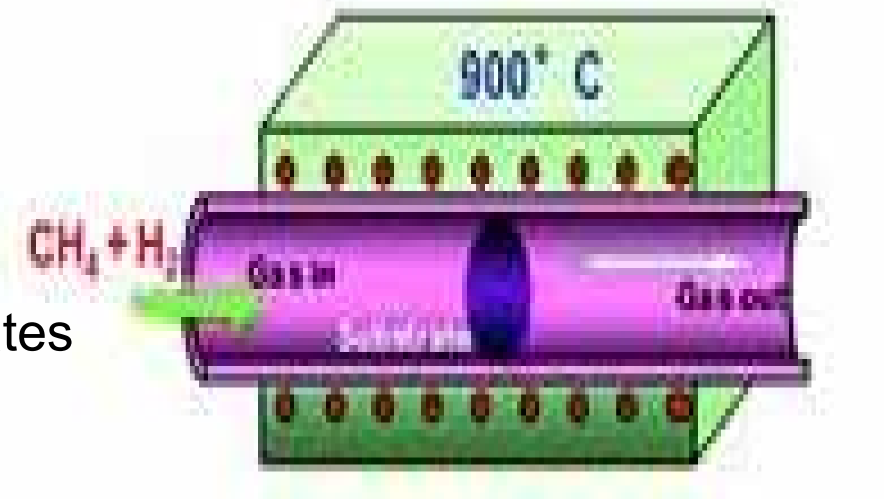
- scalable
- modest temperatures (~1000°C)
- Silicon Technology compatible (CMOS compatible)

Source: Infineon

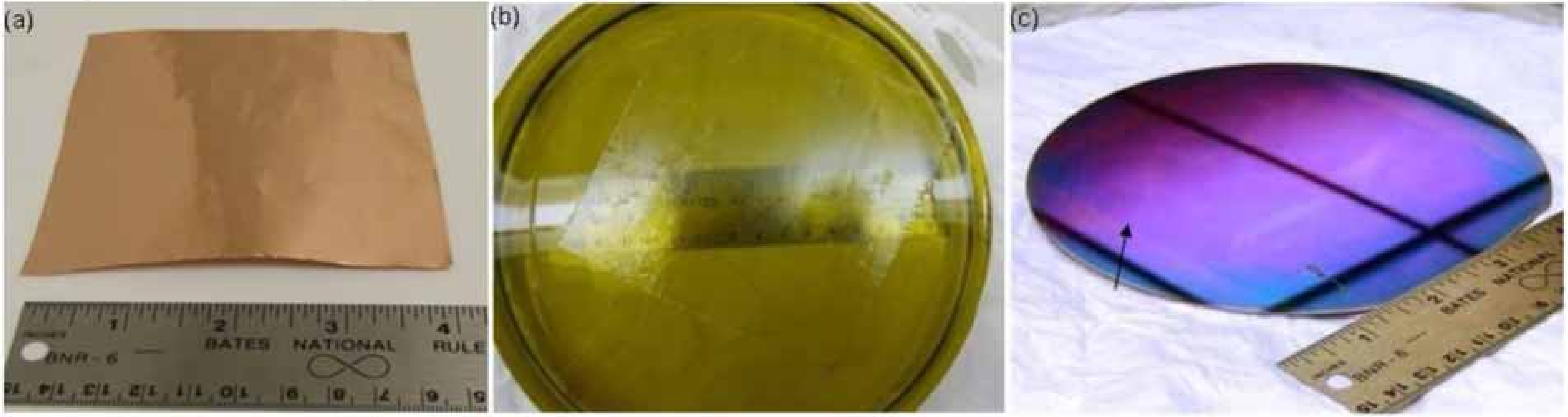
Graphene Fabrication Methods: CVD (3/4)

Chemical Vapor Deposition (CVD)

- CVD on Nickel, Copper, etc.
- High potential for large areas
- Graphene transfer to random substrates
- Monolayers vs. Multilayers?

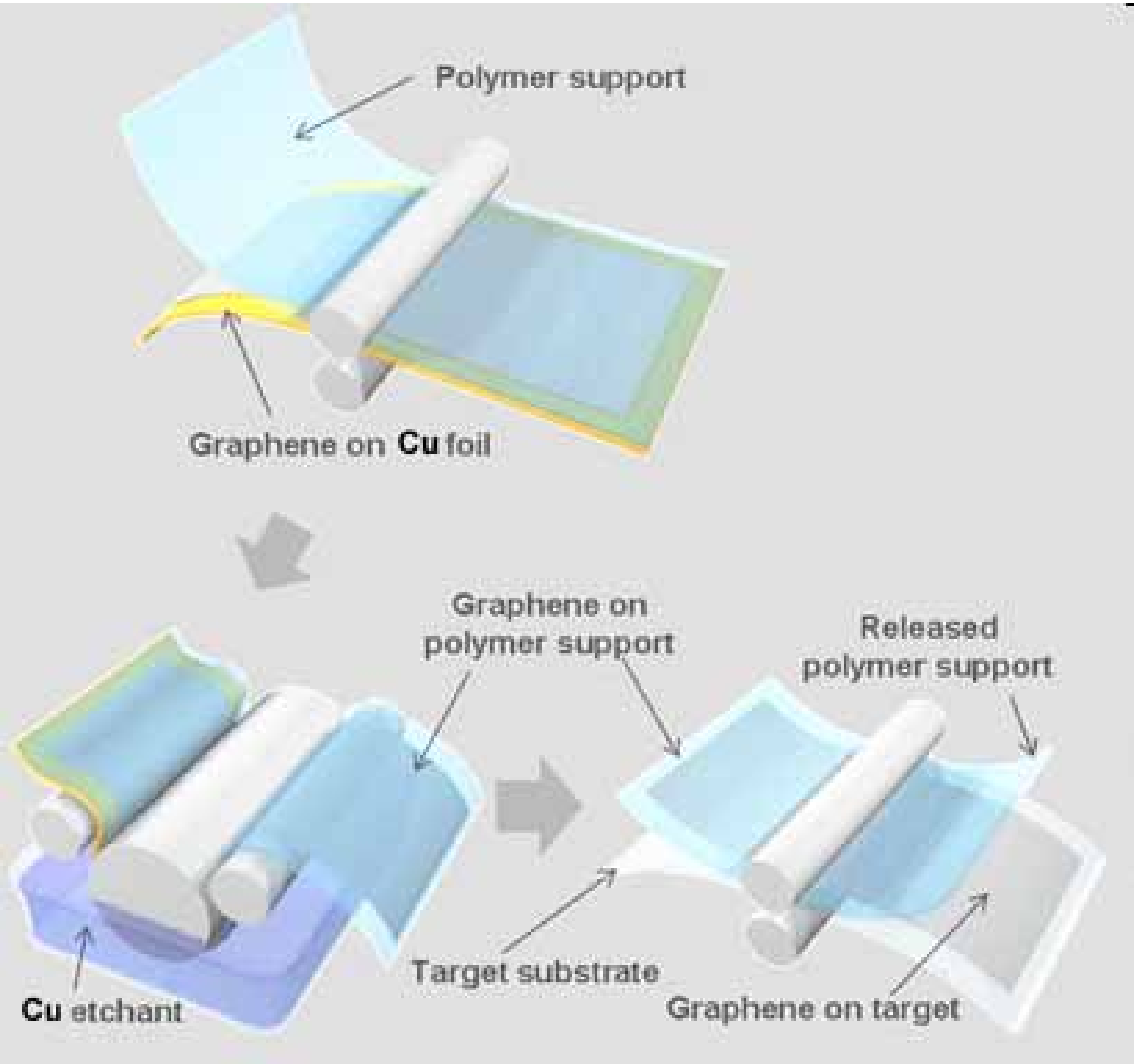


Graphene on Copper -> PMMA -> Silicon



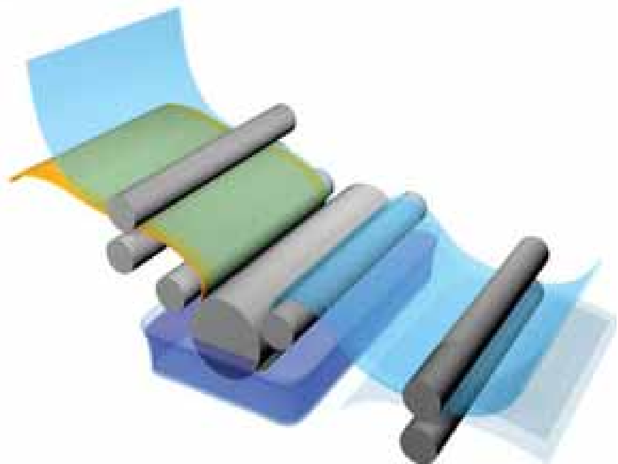
Cao et al, Applied Physics Letters 96, 122106 (2010)

Graphene Fabrication Methods: CVD (3/4)

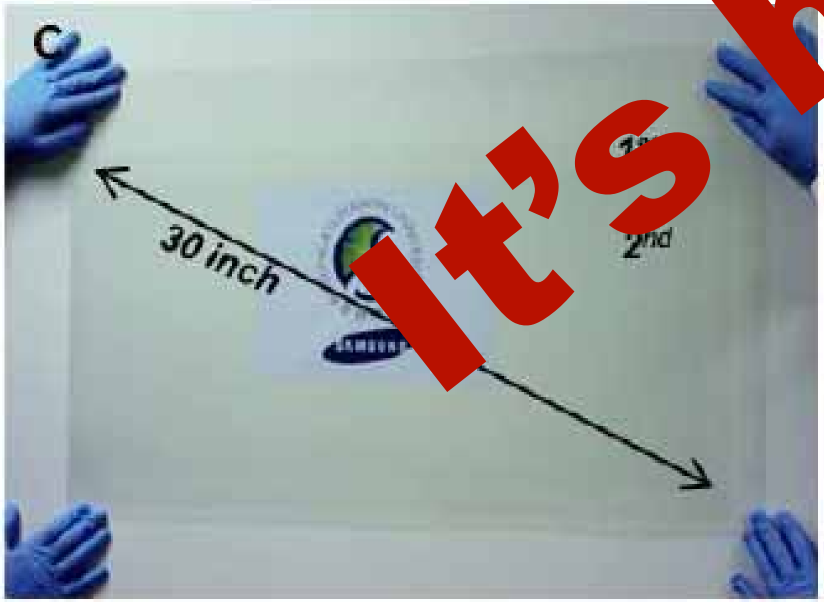


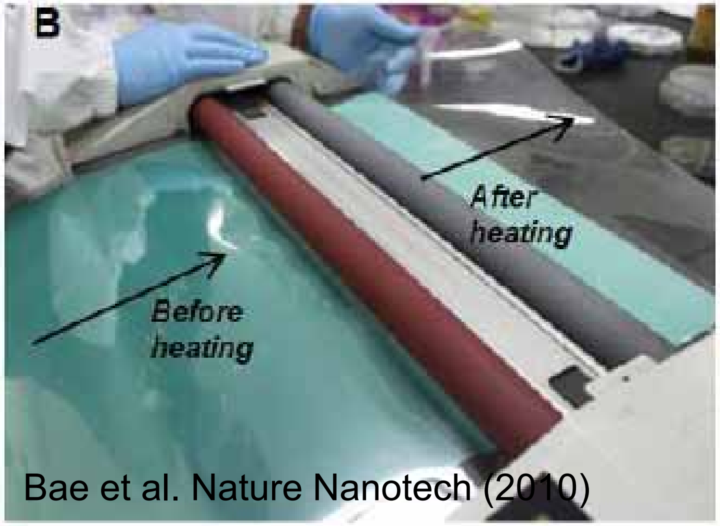
Chen, Nature Nanotech. 5, (2010)

Graphene Fabrication Methods: CVD (3/4)



Chen, Nature Nanotech. 5, 559 - 560 (2010)





Bae et al. Nature Nanotech (2010)

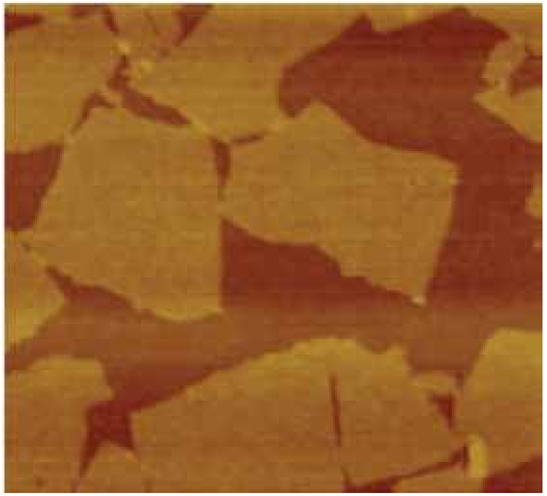
It's here!

Graphene Fabrication Methods: Chemical Exfoliation (4/4)

Exfoliation process
(treatment in acids)

natural graphite

Graphene solution

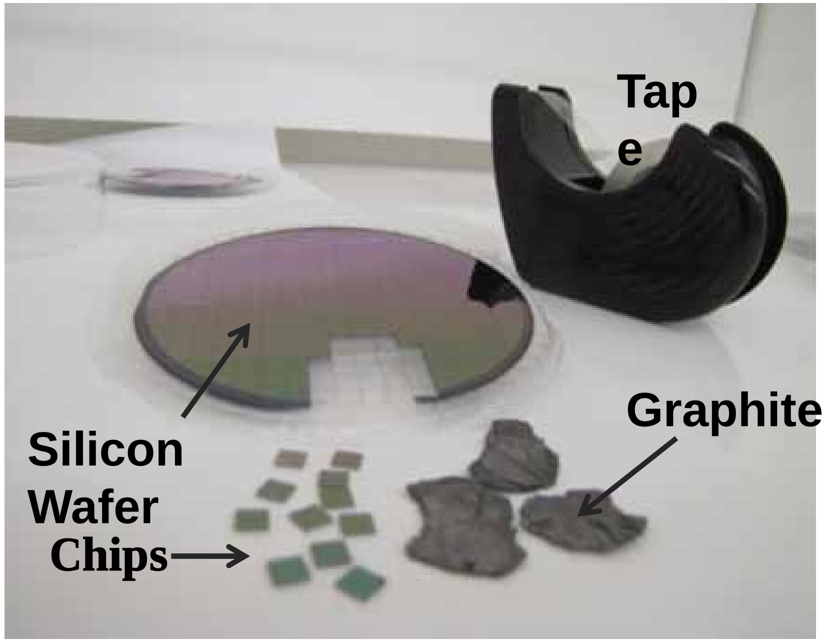


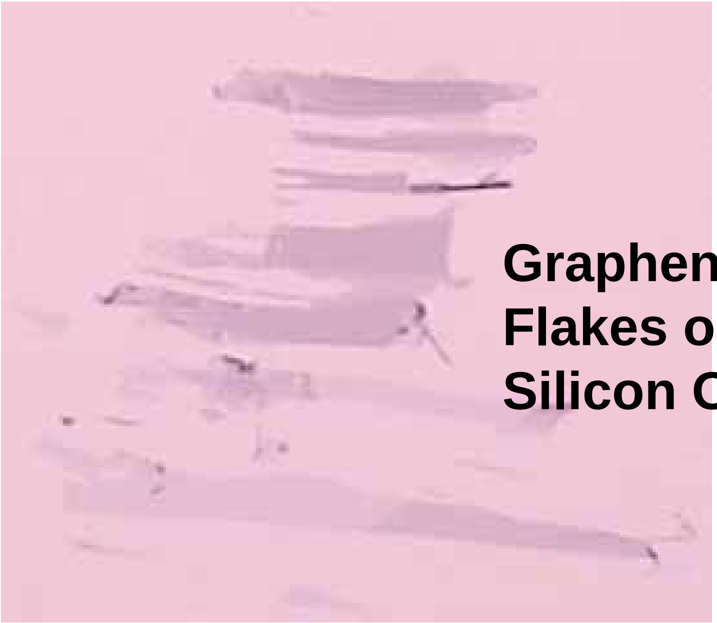
Deposition of graphene

- Process at room temperature
- Industrial scale manufacturing possible

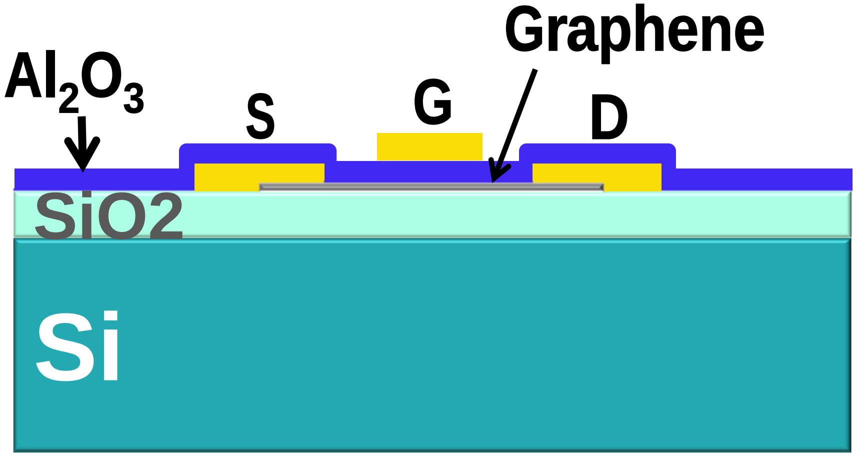
Nature Nanotech. **3,** 101, 2008

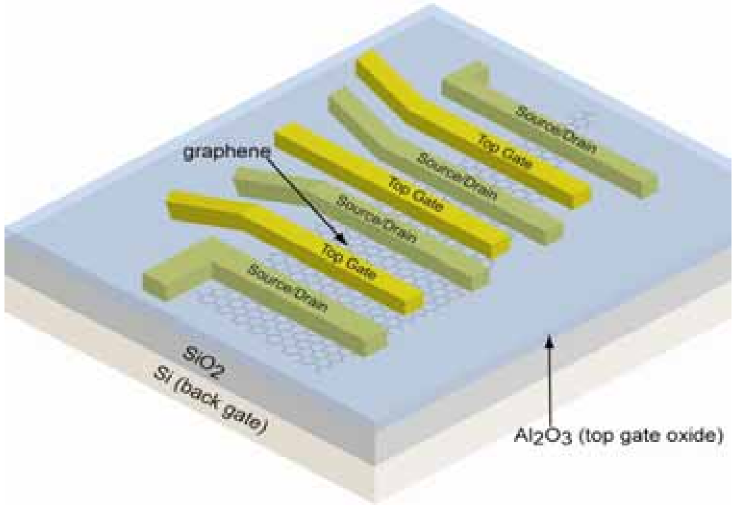
Graphene Device Technology at KTH





Graphene Flakes on Silicon Oxide





Graphene Device Technology at KTH

Si Thermal Oxidation

Lithography

E-Beam Marker

Lift Off

Wafer Dicing

Graphene Transfer

E-Beam Lithography

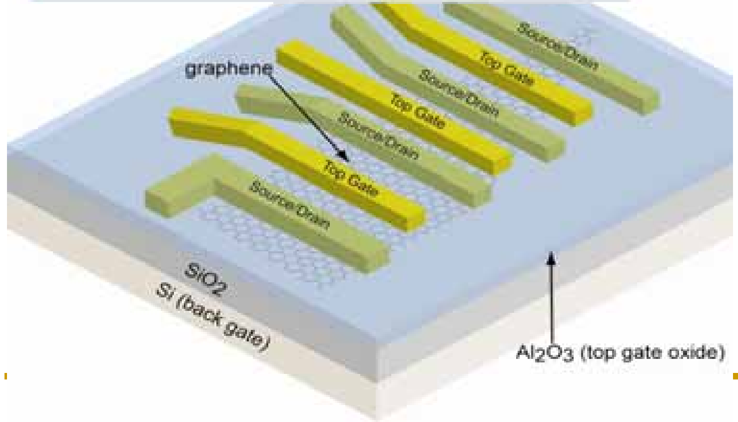
Lift Off

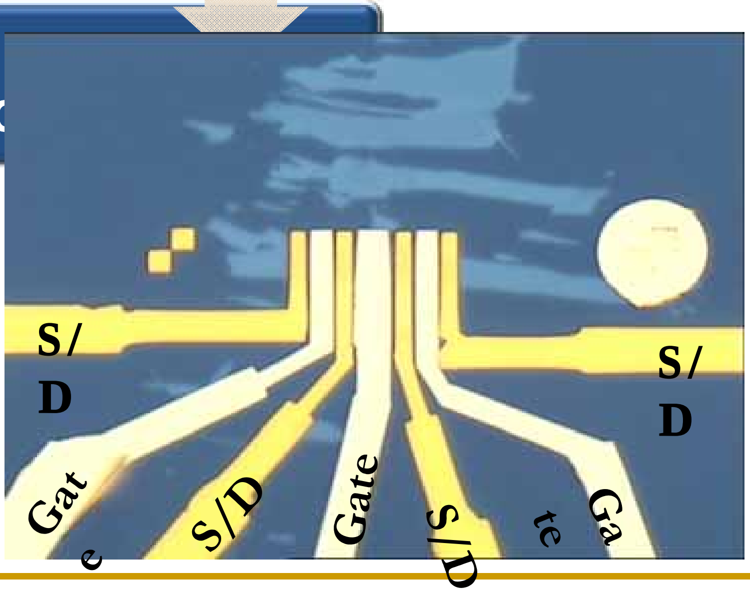
High K Depositi

-Beam ithography

ate lectrode eposition

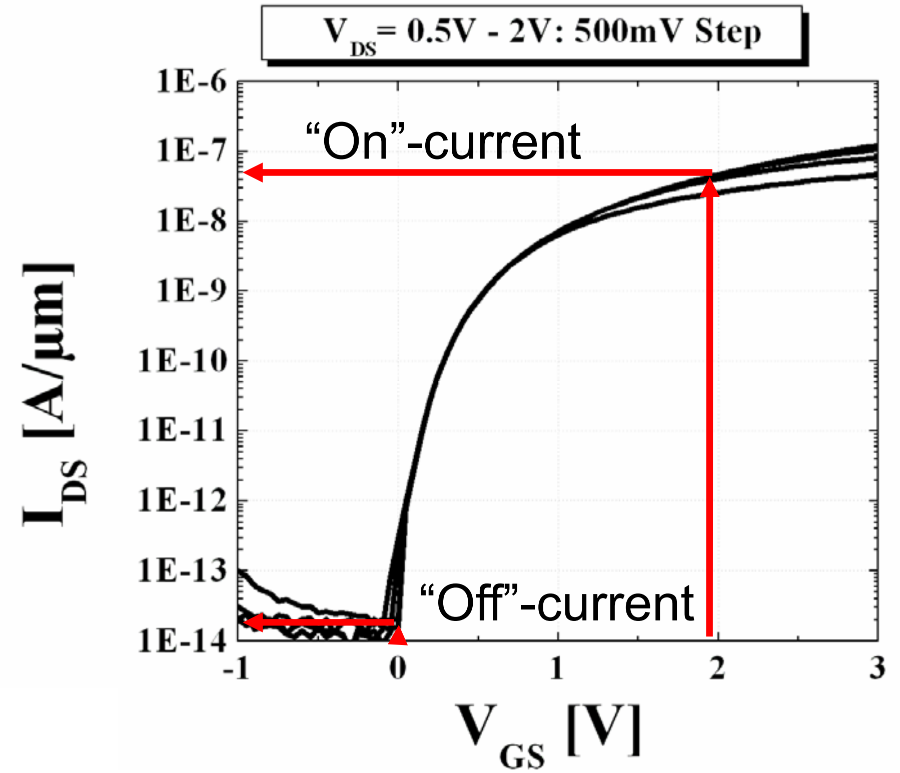
ift Off





Graphene: Transistors

Silicon MOSFET



Schmidt et al., Sol. St. Electr., 2009

Silicon Technology

- Highly mature technology
- Billions of devices in parallel
- Near ideal switch
- I_{on}/I_{off} ratio: several decades
- Speed ~ I_{on} ~ μ_{eff} (carrier mobility)

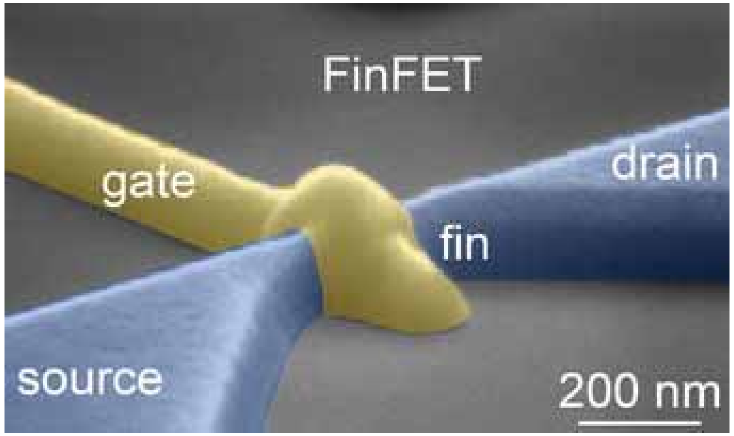
µ - Silicon: 100-450 cm^2/Vs

µ - Graphene: 1.0000 – 200.000 cm^2/Vs

Graphen MOSFET!?

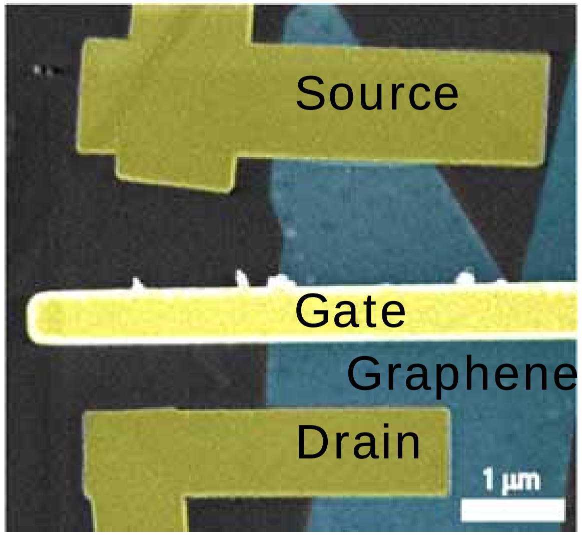
Graphene: Transistors

Silicon MOSFET



Source: TU Delft

Graphene MOSFET

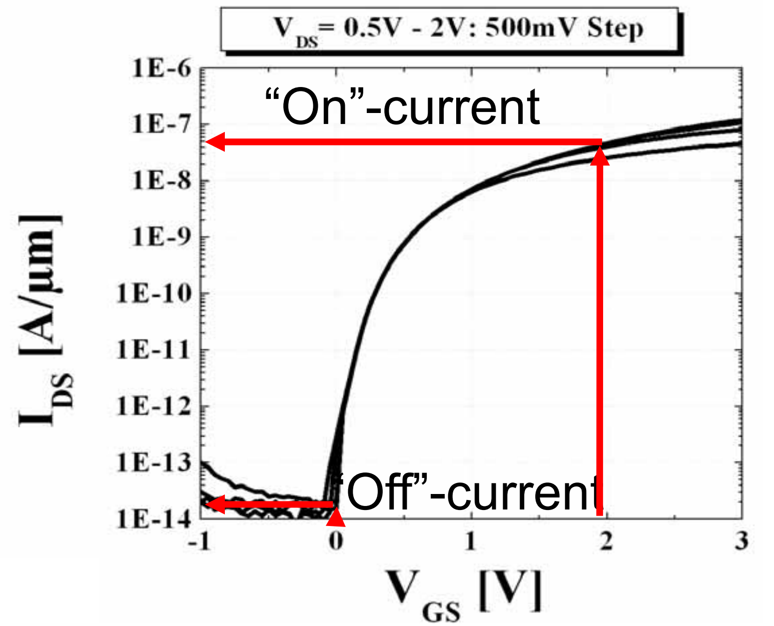


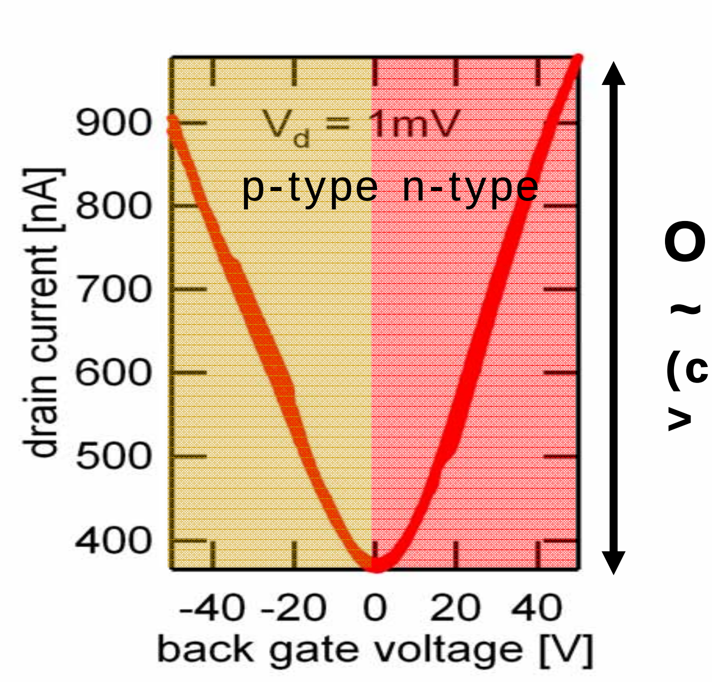
Graphene Transistors:

- Silicon process technology can be applied („Top-Down“)
- Graphene is compatible with (most) standard processes
- …Graphene MOSFET!?

Graphene: Transistors

Transfer characteristics





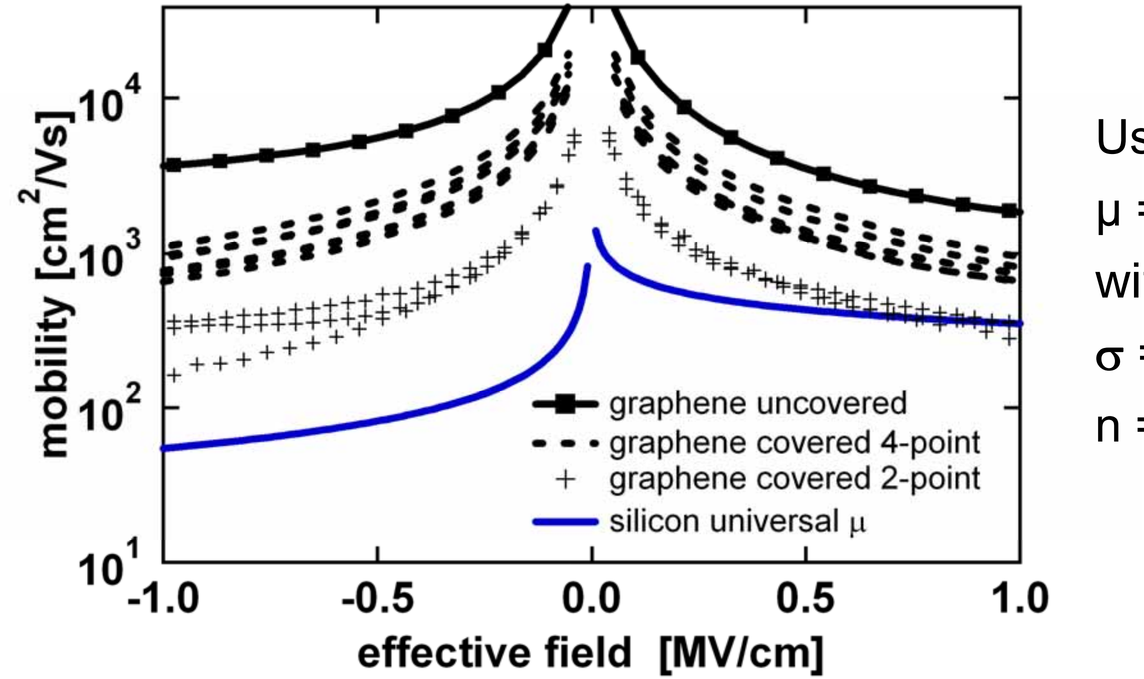
On-Off ratio: ~2 x

(compare Silicon: > 1.000.000 x)

Graphene Transistors:

- Ambipolar behaviour (n- und p-type conduction)
- I_{on}/I_{off} ratio inherently limited by band structure (semimetall)
- NOT a direct replacement for Silicon logic...
- ... but for high speed analog transistors!

Graphen FETs: Mobility



Using Drude model:

$\mu = \sigma / (n * q)$

with

$\sigma = J/E_{ds} = I/\text{width} * \text{length}/V_{ds}$

$n = \varepsilon * E_{eff}/q$

Mobility reduced considerably (> 1/10) in a SiO_2-”Sandwich”

→ Coulomb-scattering through dielectrics

Still much better mobility compared to silicon

→ especially Ultra Thin Body SOI MOSFETs

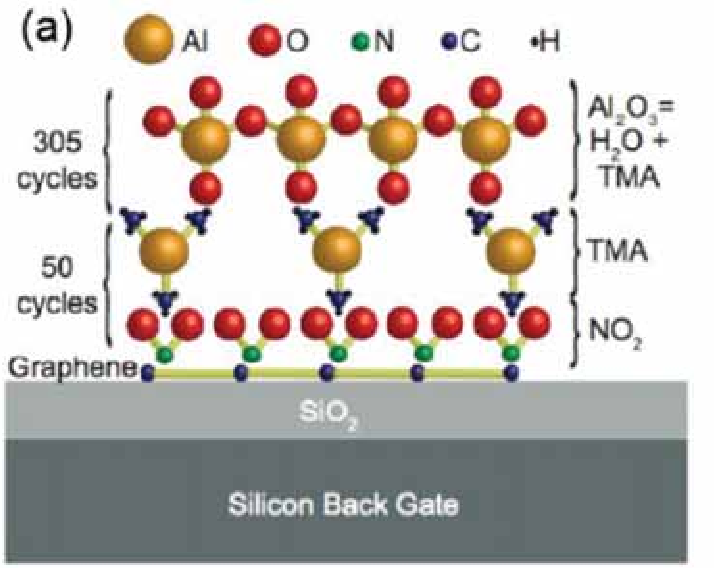
Graphen FETs: Interface Engineering

Problem:

Mobility degradation due to dielectric

Solution:

- ***Atomic Layer Deposition*** of high-k dielectrics
- Seed layer: alternating Deposition of NO_2 und trimethyl aluminum (TMA)
- Subsequent deposition of Al_2O_3 by ALD



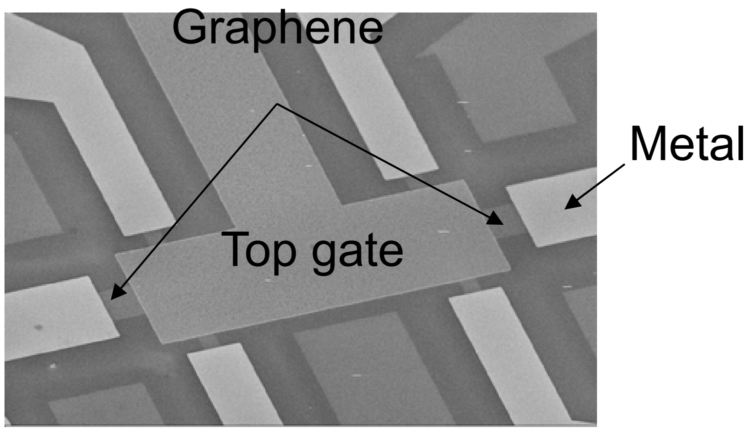
J.R. Williams et al., *Science*, vol. 317, 638 (2007).

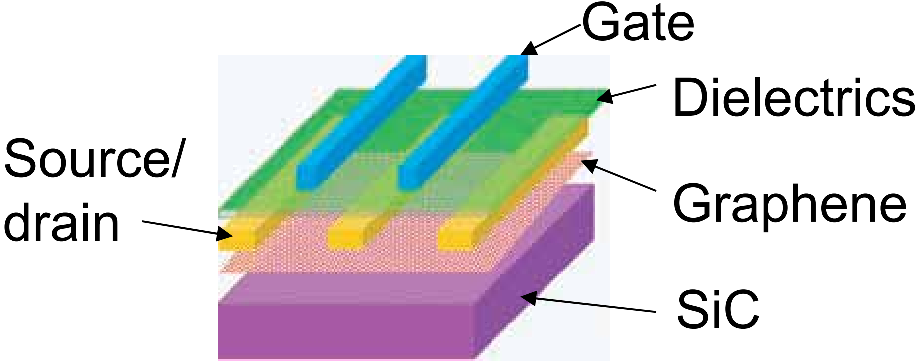
- V_{CNP} = 0 V
- $\mu = 7000\ cm^2/Vs$
- Quantum Hall Effect in graphene 2DEG demonstrated

➡ ONE approach (the beginnning rather than the end of optimization…)

Graphene: Transistors

Graphene High frequency analog electronics





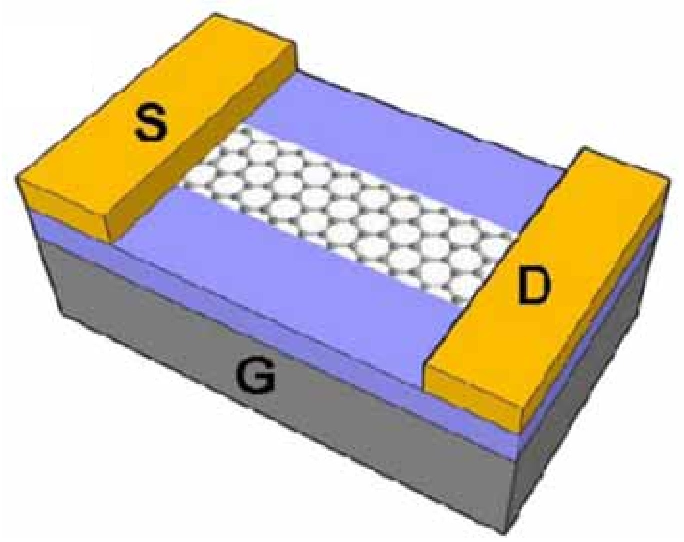
Gate length: 240 nm
Cut-off frequency: **100 GHz**!

Science, **327**, 662, 2010

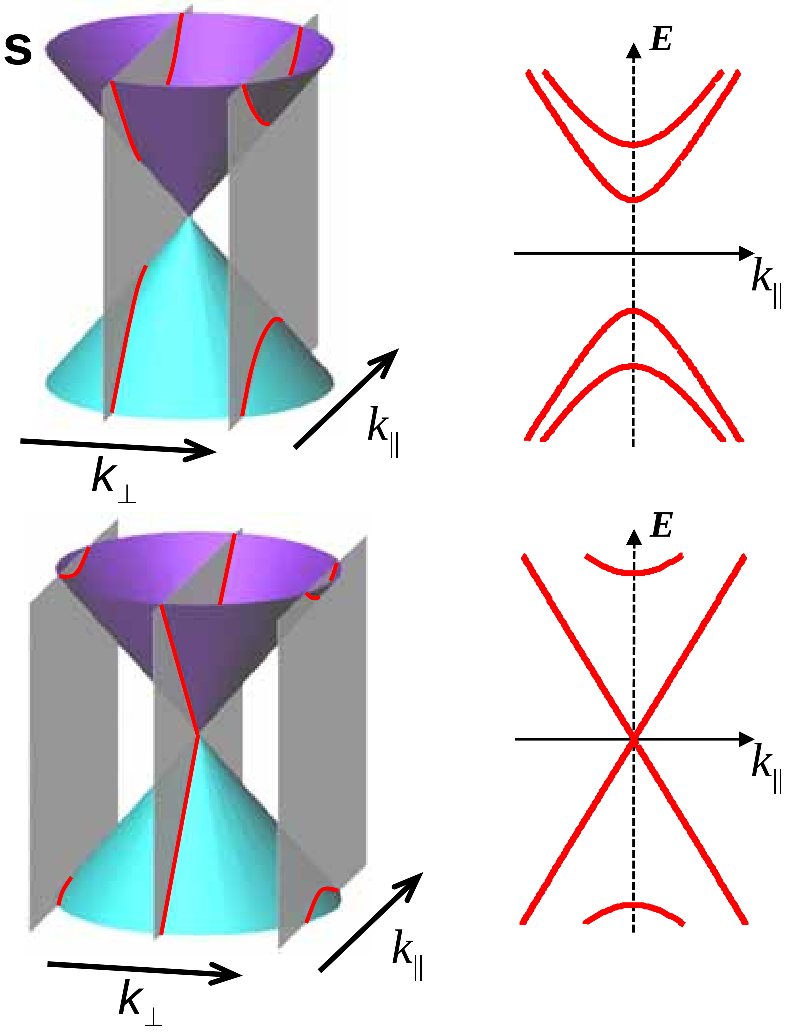
Graphene: Nanoribbon Transistors

Nanoribbons: lateral constrictions

- Transition from 2D to 1D material
- Geometry induced band gap
- $E_g \sim 1/W$

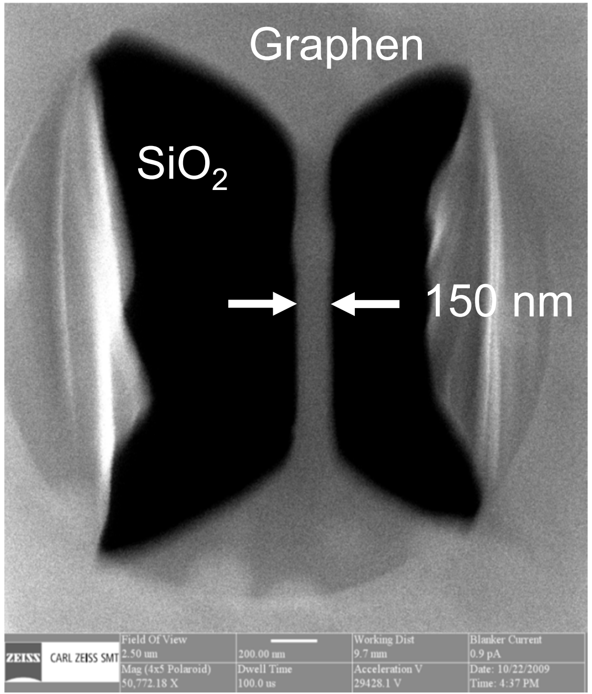


Source: S. Ilani, Cornell



Graphene: Nanoribbon Transistors

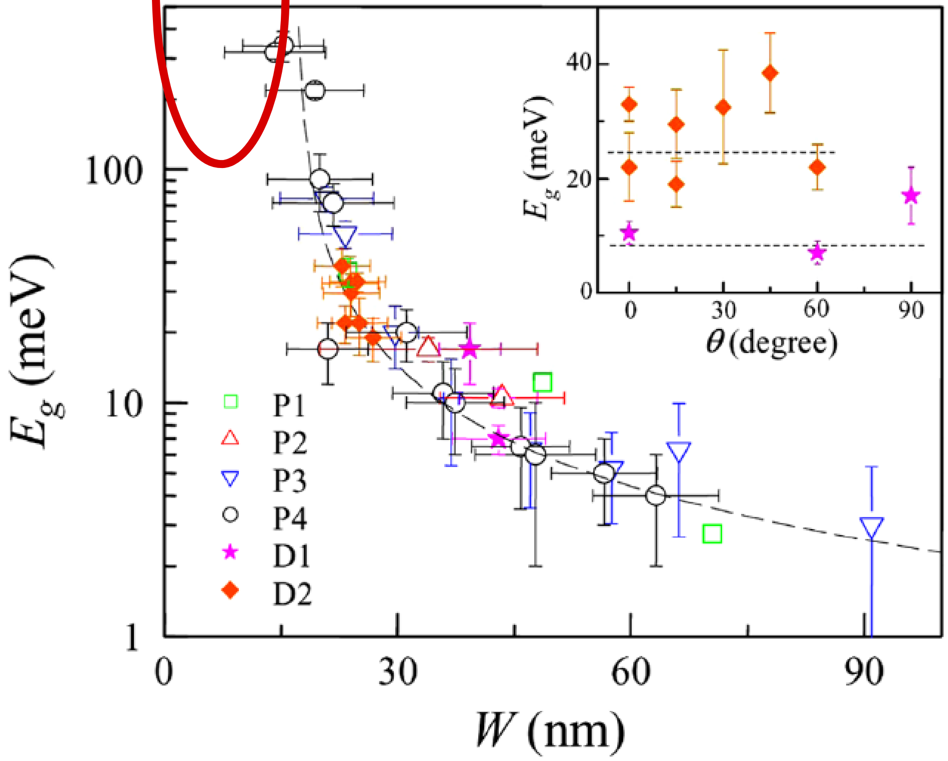
Nanoribbons: lateral constrictions



suspended GNR (unpublished)

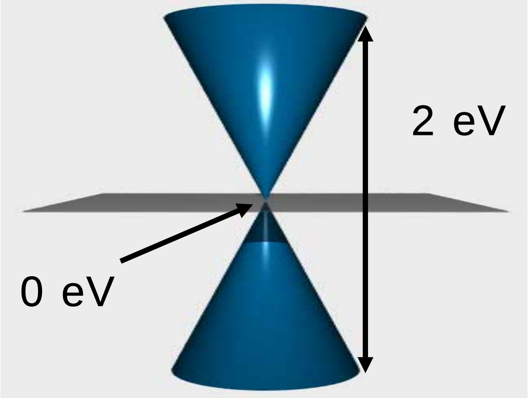
sub 15nm GNR !

Han et. al., PRL 98, 2007



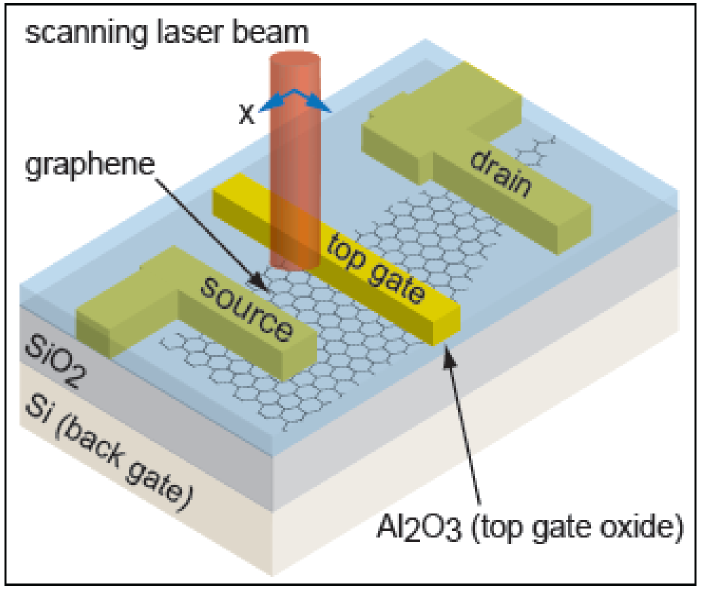
GNRS under 15 nm relevant for FETs!

Graphene: Photodetection

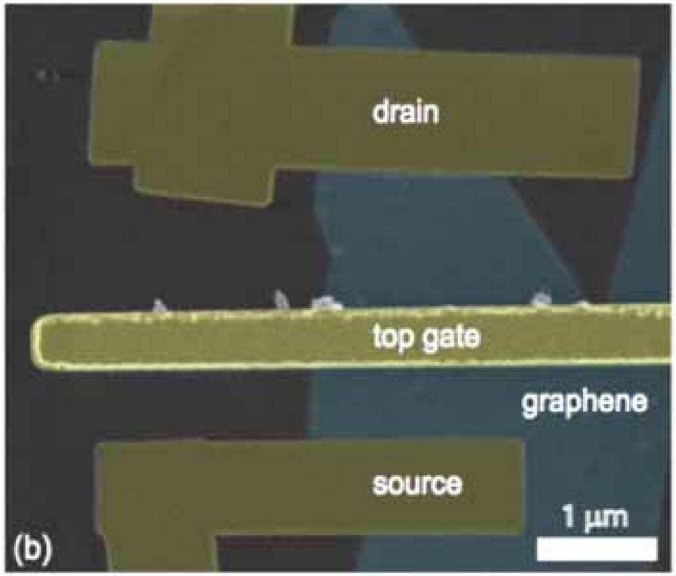


Graphene photodetectors

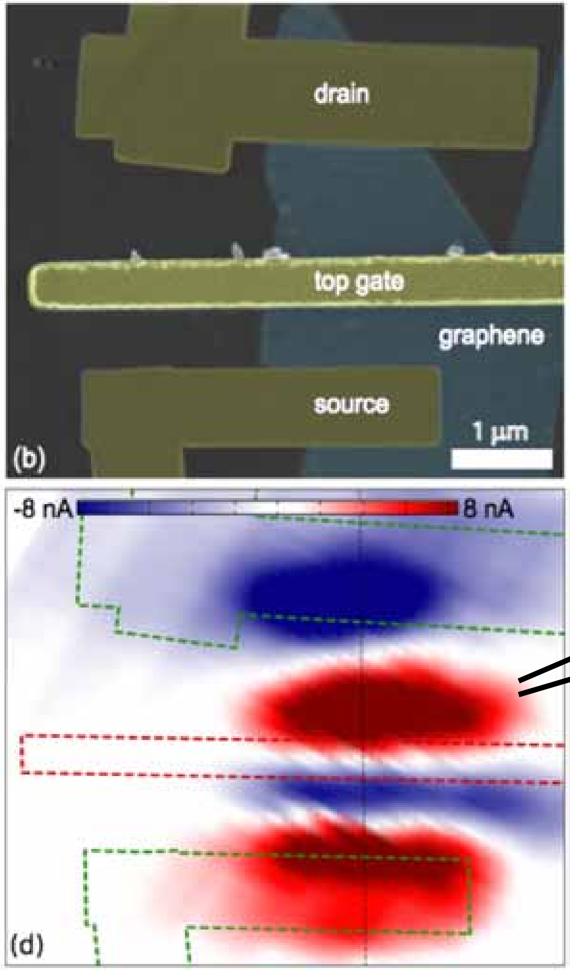
- E-k linear up to +- 1eV
- Potential from visible spectrum to THz
- High data rates



Lemme et al., cond-mat/1012.4745, 2010



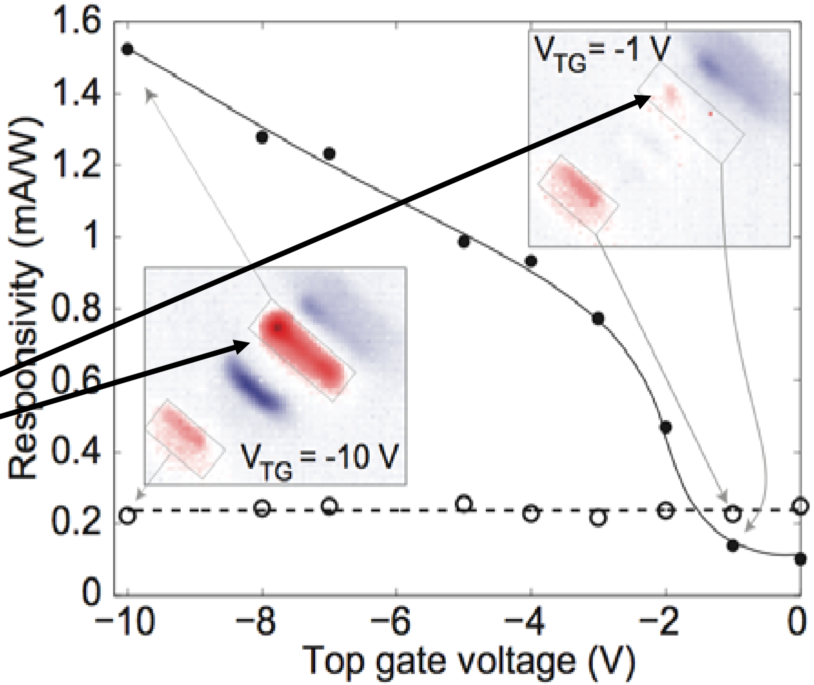
Graphene: Photodetection



Lemme et al., cond-mat/1012.4745, 2010

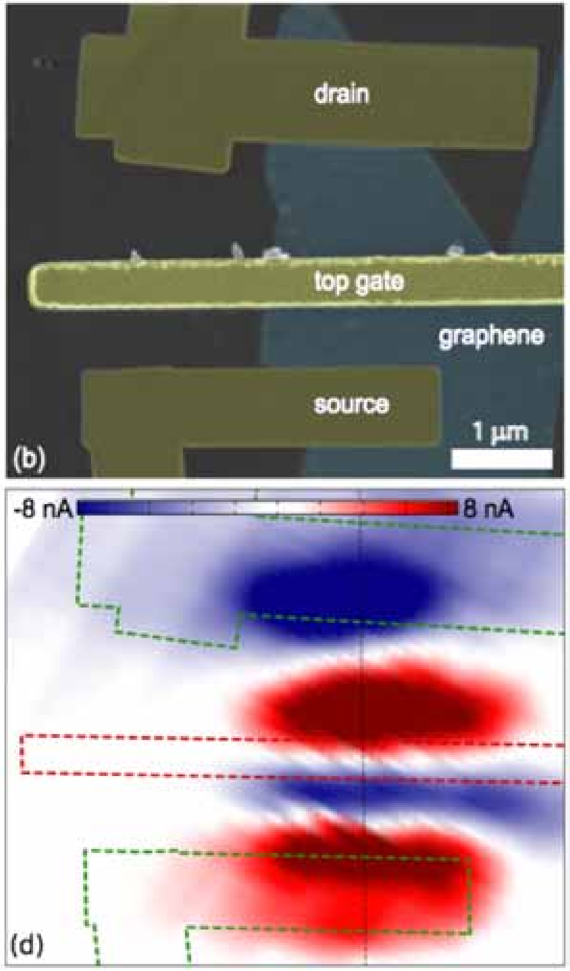
Local On-Off Control of a Graphene p-n Photodetector

Lemme et al., cond-mat/1012.4745, 2010



Local control of p-n junction allows on-off control of photodetection.

Graphene: Photodetection



Lemme et al., cond-mat/1012.4745, 2010

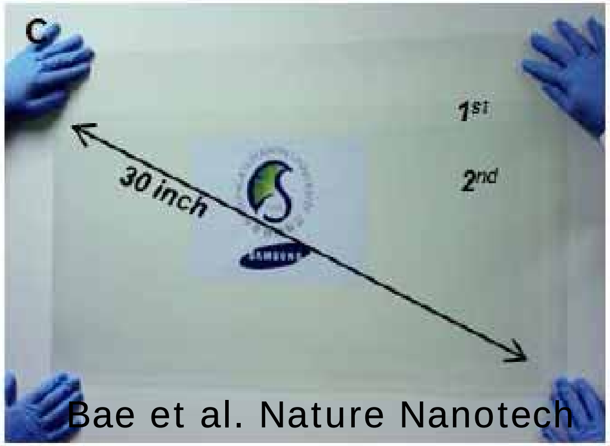
Local On-Off Control of a Graphene p-n Photodetector

Lemme et al., cond-mat/1012.4745, 2010

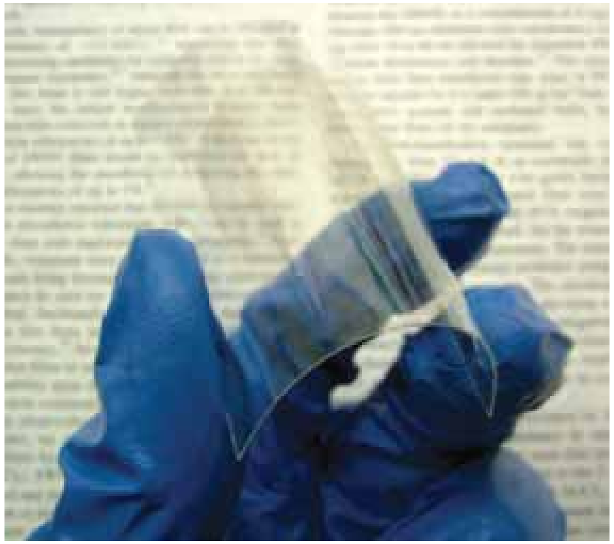
- **In part depending on Seebeck effect (pn-junction required)**
- **Local contol of p-n junction allows on-off control of photodetection.**
- **No biasing required (no dark current)**
- **Scalability to submicron gates**
- **Potential to integrate graphene optoelectronics into existing platforms**

Graphene: Applications beyond Moore's Law

We have this:



Bae et al. Nature Nanotech



Nature Nanotech. **3**, 270, 2008

Status Quo of CVD Graphene:

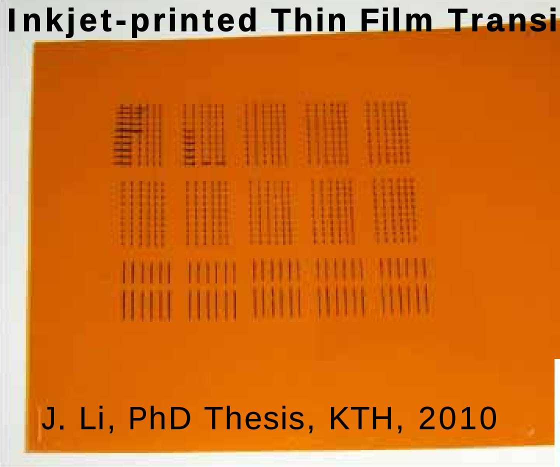
- Fabrication from solution at room temperature
- Arbitrary large area CVD
- Highly conductive
- Transparent
- Flexible and stretchable
- Printable (in solution)

Potential for

- Replacement for Indium Tin Oxide (ITO)
  - Transparent electrodes for Solar Cells
  - Transparent electrodes for Touch Screens
- Electronics on arbitrary (flexible) substrates
- Supercapacitors and superbatteries

Graphene: Applications beyond Moore’s Law

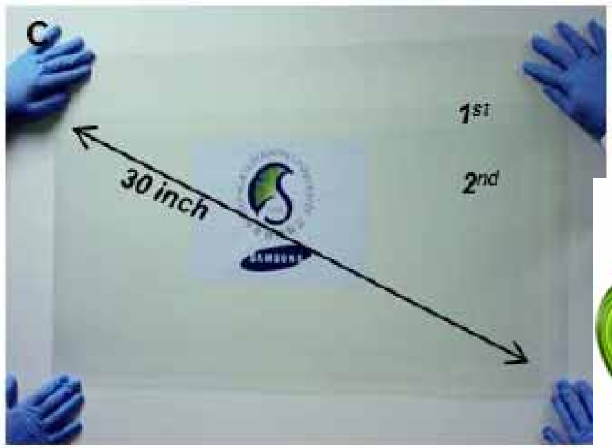
Electronic paper

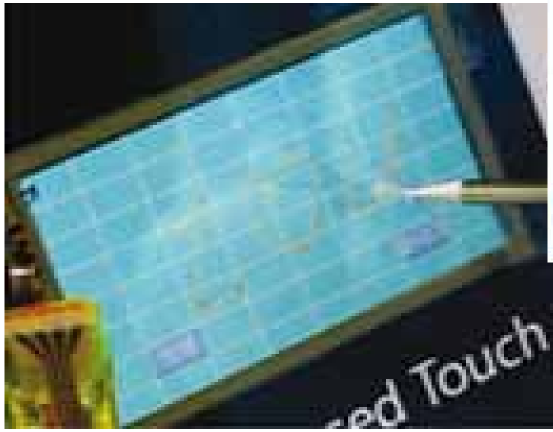

Inkjet-printed Thin Film Transistors

J. Li, PhD Thesis, KTH, 2010

E-clothes
(solar, functional)

We have this:





Displays and Touch Screens

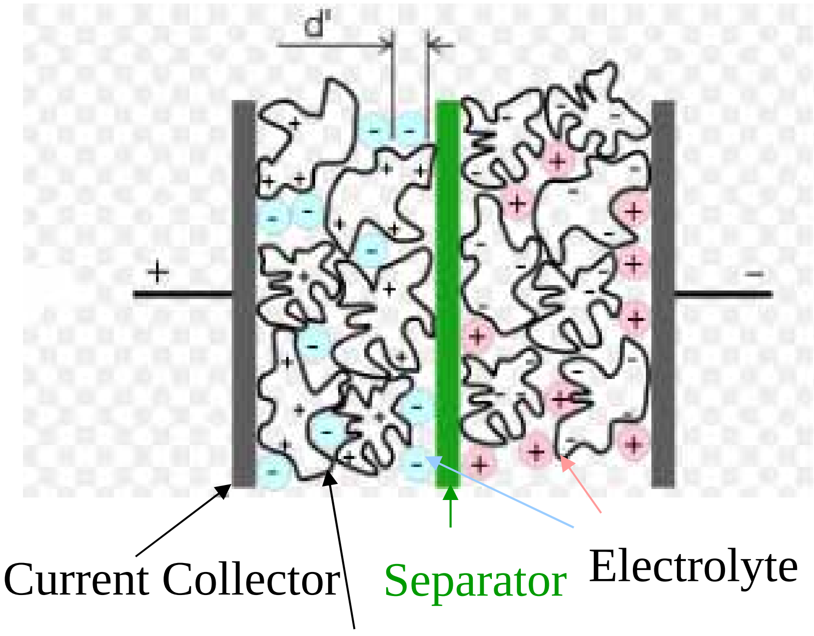

Source: Nokia

Flexible gadgets

Graphene: Applications beyond Moore's Law

Supercapacitor, Ultracapacitor

Electrochemical Double Layer Capacitor



Current Collector

Separator

Electrolyte

Electrode (Porous)

Graphene-based Supercapacitor

Science 329, 1637 (2010)

Vertially Oriented Graphene

Surface area ~ 1100 m^2/g

Theoretical value ~ 2600 m^2/g

Lecture 11: Outline

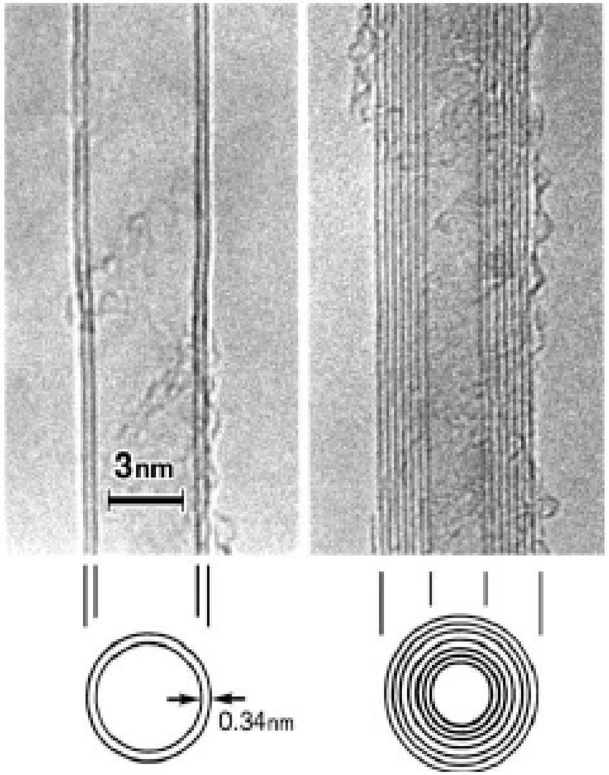
- Silicon CMOS
- Carbon Technology
  - Graphene
  - Carbon Nanotubes (CNTs)
- Photonics
- Future Outlook

Carbon Nanotube Electronics

- Discovery and growth of carbon nanotbes
- Structure and electronic properties of CNT
- CNT-based devices
- Fabrication of CNT-based devices
- Semiconducting CNT
- Metallic CNT
- CNT network
- Graphene

Discovery of CNTs

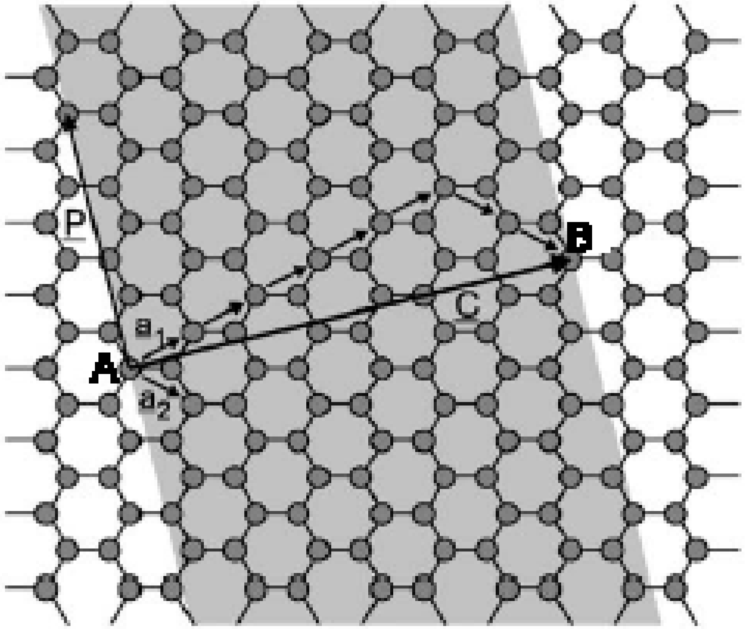
Sumio Iijima

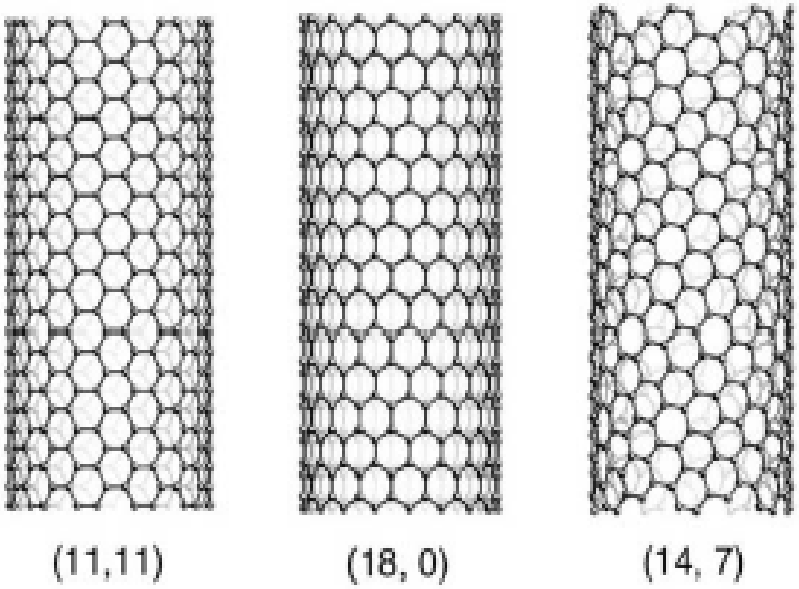


Multi-walled CNTs (MWNT), 1991 *Nature*, vol.354, p56 (1991)
single-walled CNTs, 1993. *Nature*, vol.363, p603 (1993)

CNT presentation provided by Dr Zhibin Zhang

Structure





Armchair
n=m

Zigzag
m=0 or
n=0

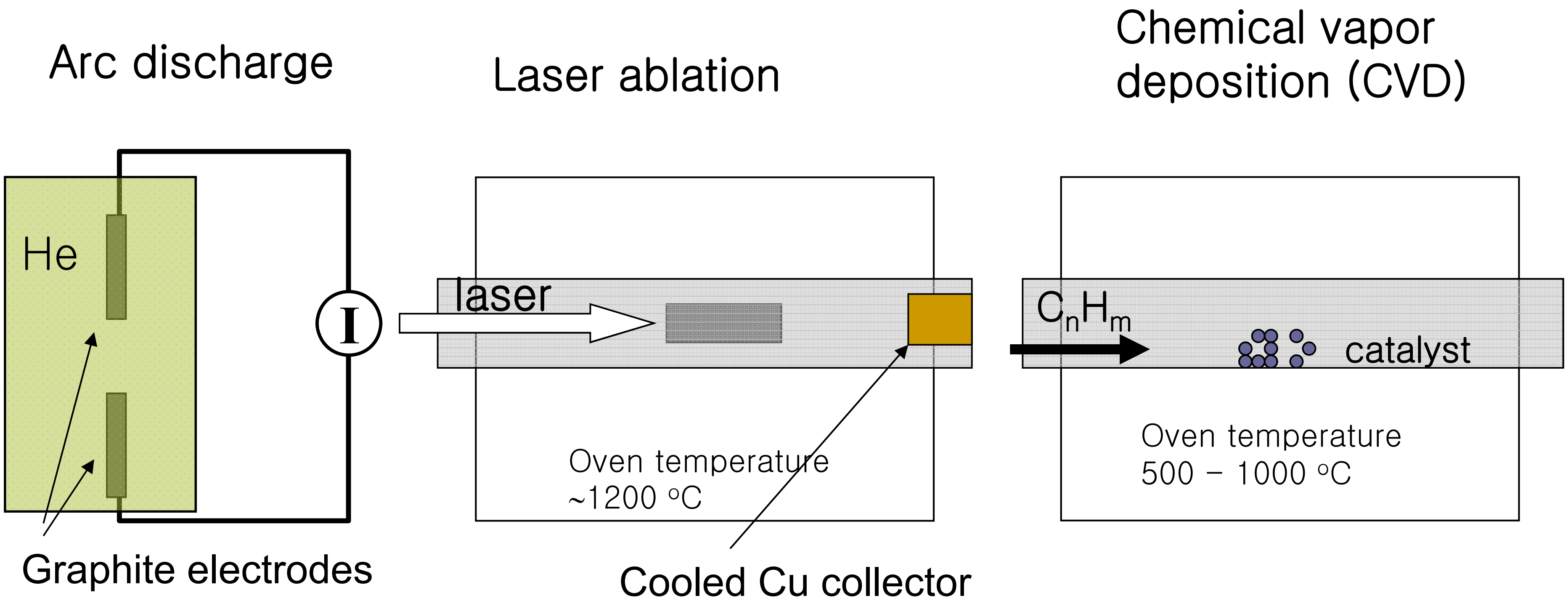
Chiral
Other cases

Generation of a CNT by

rolling a graphitic atomic sheet along

chirality vector C = BA = na_1+ma_2

Approaches of growth of CNTs



Arc discharge

He

I

Graphite electrodes

Laser ablation

laser

Oven temperature ~1200 °C

Cooled Cu collector

Chemical vapor deposition (CVD)

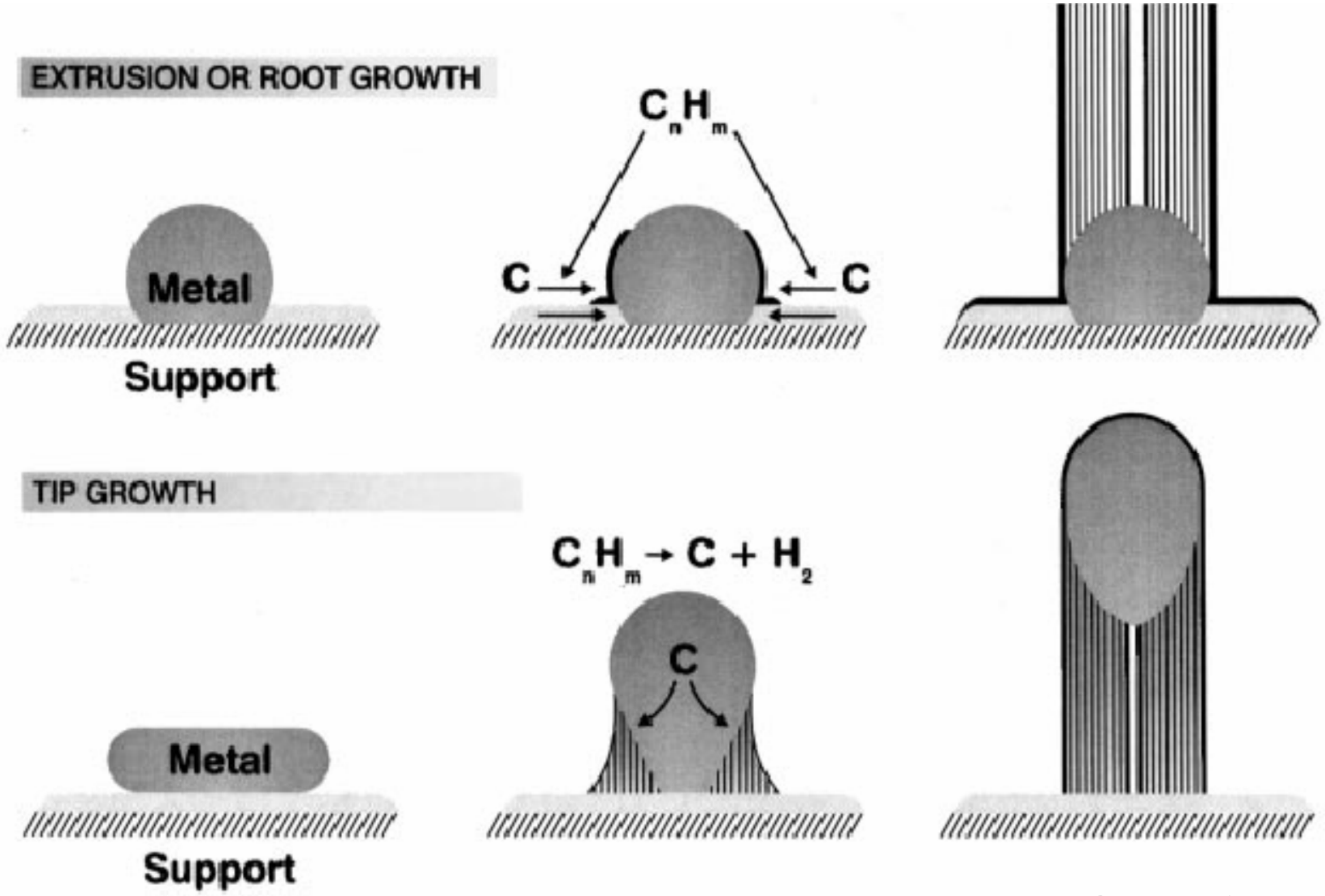
C_nH_m

catalyst

Oven temperature 500 – 1000 °C

SWNTs growth with use of catalyst containing Fe, Co, Ni

A possible growth mechanism (CVD)



High temperature

Dissociation, dissolution, saturation and precipitation

Growth

Band structure and electronic properties

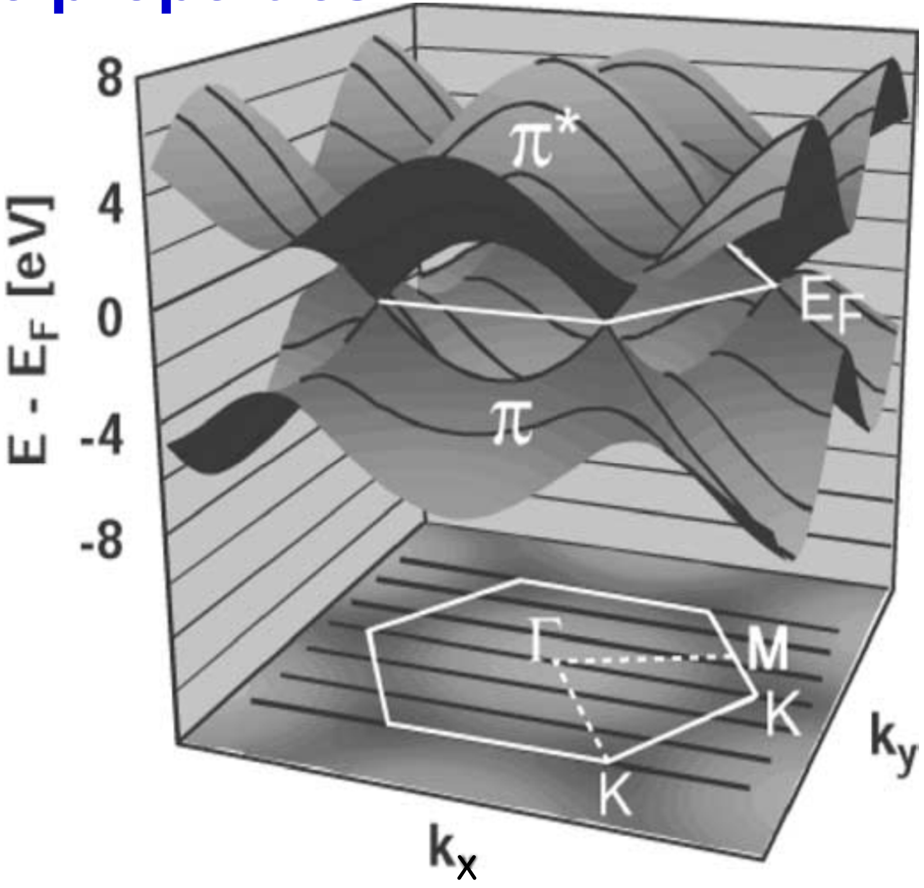
The band structure of a CNT is obtained by slicing the Fermi plane of the graphene according to the required quantization condition on the CNT

→ Metallic and Semiconducting CNTs

For instance

Consider armchair CNTs (n, n)
The quantization condition is

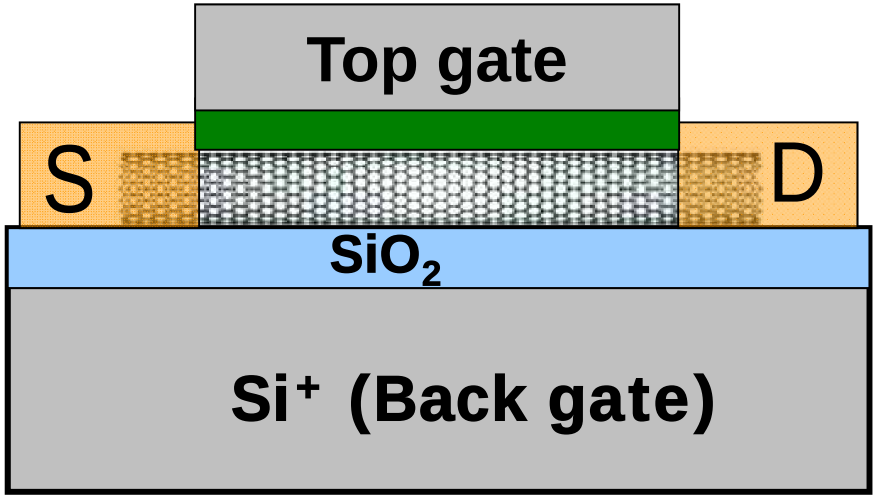
$$k_\perp = \sqrt{3}nak_x = 2\pi j\,(j = 0,1,2,\cdots 2n)$$

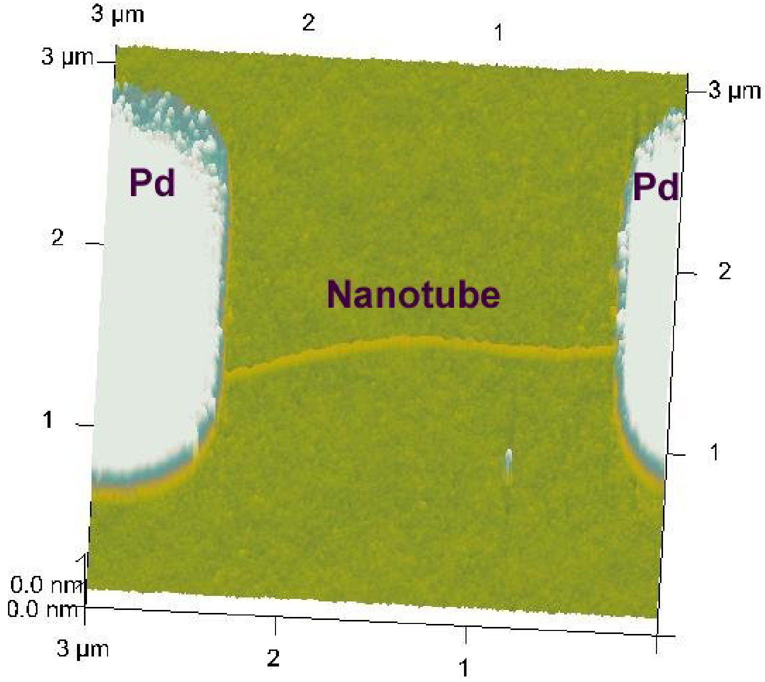


Band structure of graphene

Basic structure of CNT-based electronic devices

🟧 Contact metal 🟩 Top gate oxide





KTH device

- Contact metals to semiconducting CNT

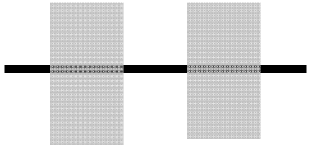
Schottky contact: Ti, Al, etc with low work function

Ohmic contatc: Pd, Pt, etc with large work function

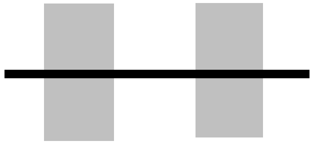
- Top gate oxide: high k material

Fabrication of individual CNT devices

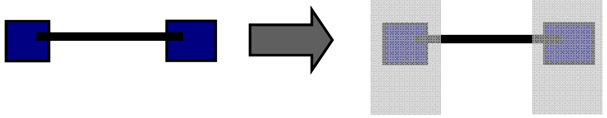
- ➢locating randomly placed tubes by SEM, AFM, making contacts using electron beam lithography (EBL)



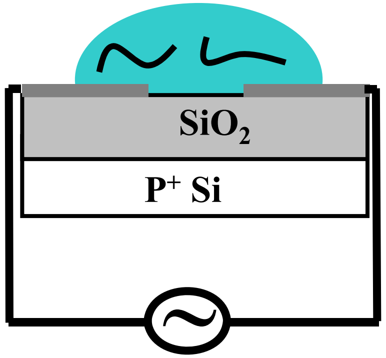
- ➢Random tube deposition on pre-patterned wafers

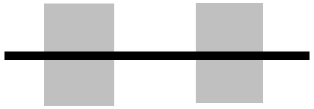


- ➢Direct tube growth between pre-defined catalyst islands



- ➢**AC-dielectrophoresis of CNTs between pre-defined electrodes**

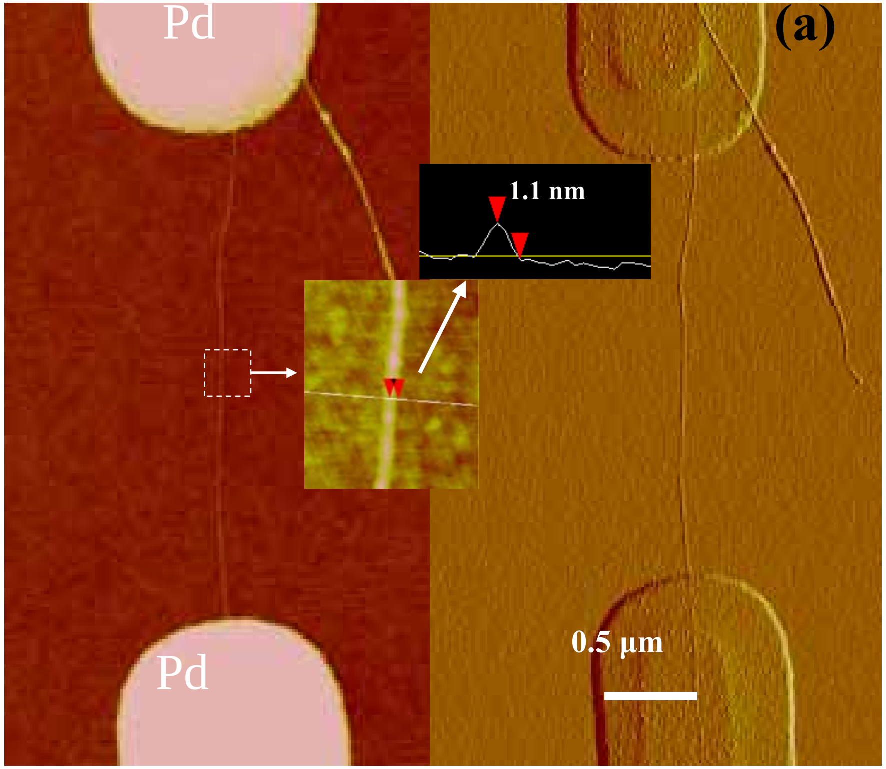


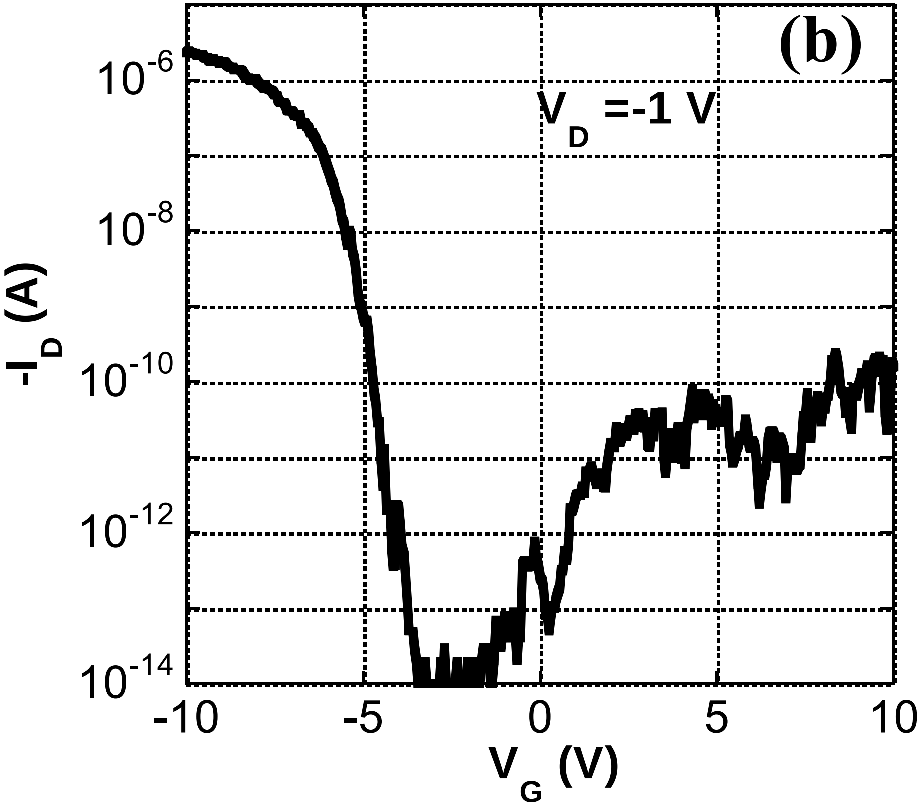


KTH

Fabrication of individual CNT devices

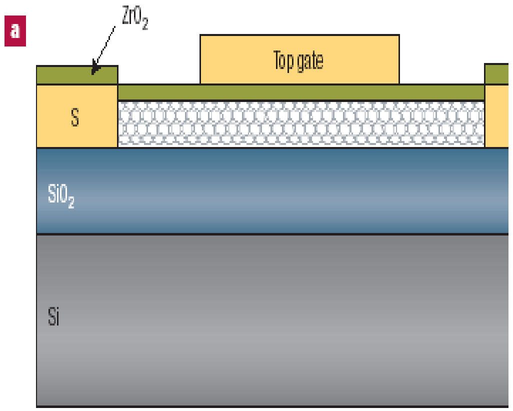
Direct assembly of individual semiconducting nanotube by means of AC-Dielectrophoresis

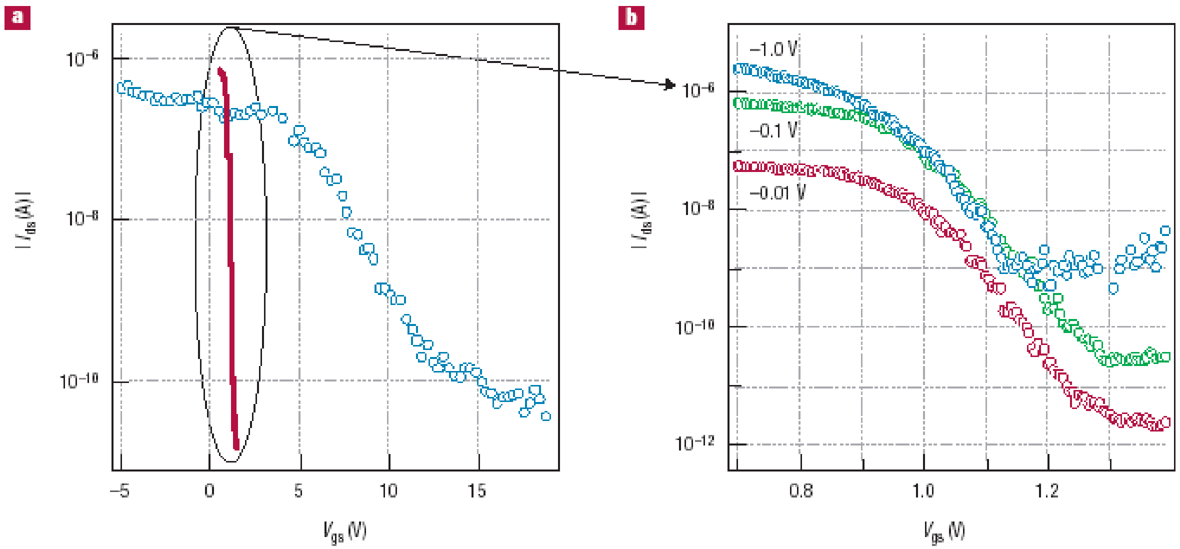




Fabrication of individual CNT devices

High–performance p–type CNFET





Gate length: 2 μm

SiO_2: 500 nm

ZrO_2 ~8 nm

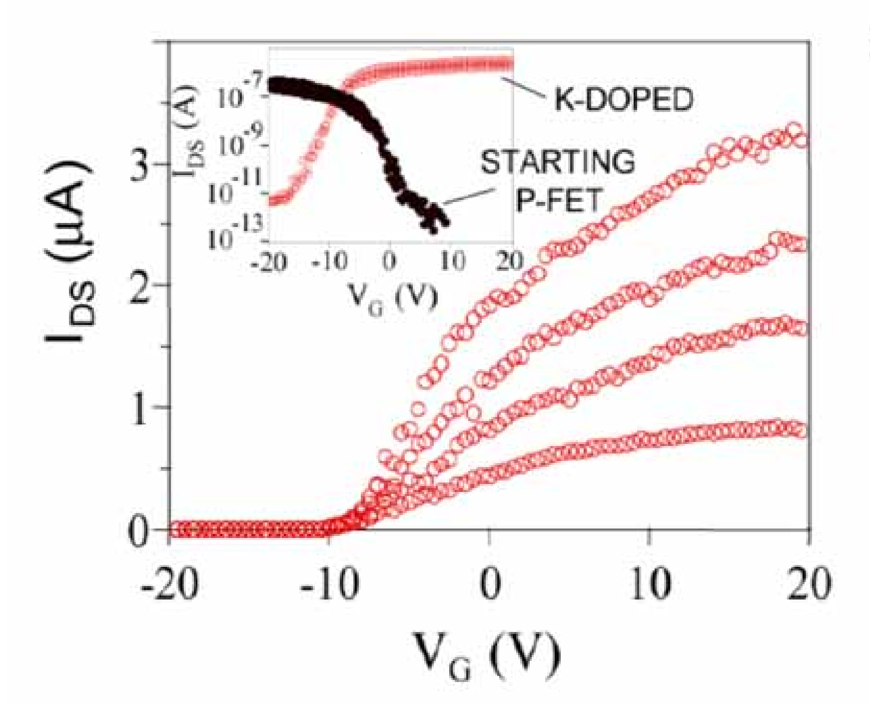
Blue: back gate, Red: top gate

- Subthreshold swing: 70 mV/dec
- Transconductance: 6000 S m^{-1}
- Hole mobility: 3000 cm^2 V^{-1} S^{-1}

Ali Javey,et., Nature **424**, 654 (2003)

Fabrication of n-CNFET

- By using metals of low work function, e.g., Al, Sc
- By removal of O_2 at the contacts with metals of high work function, Au, Pd, Ti etc (changing Schottky barrier at contacts)



electrons)

p–type to n–type by potassium doping

Metallic CNT (m-CNT)

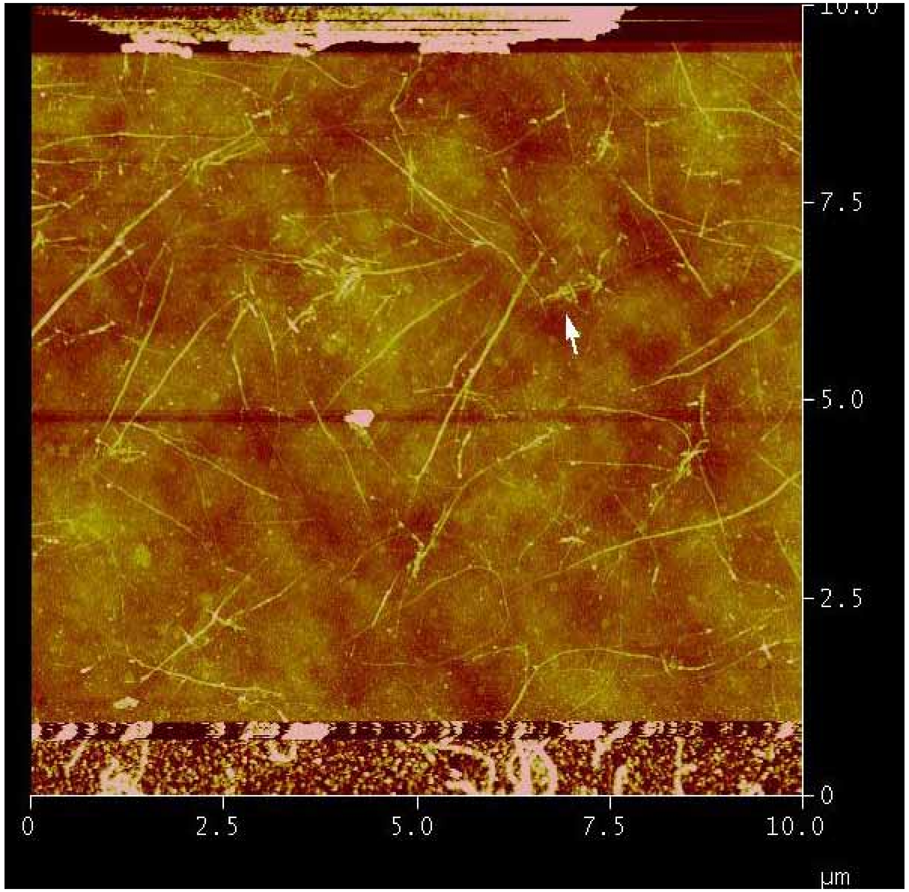
Properties

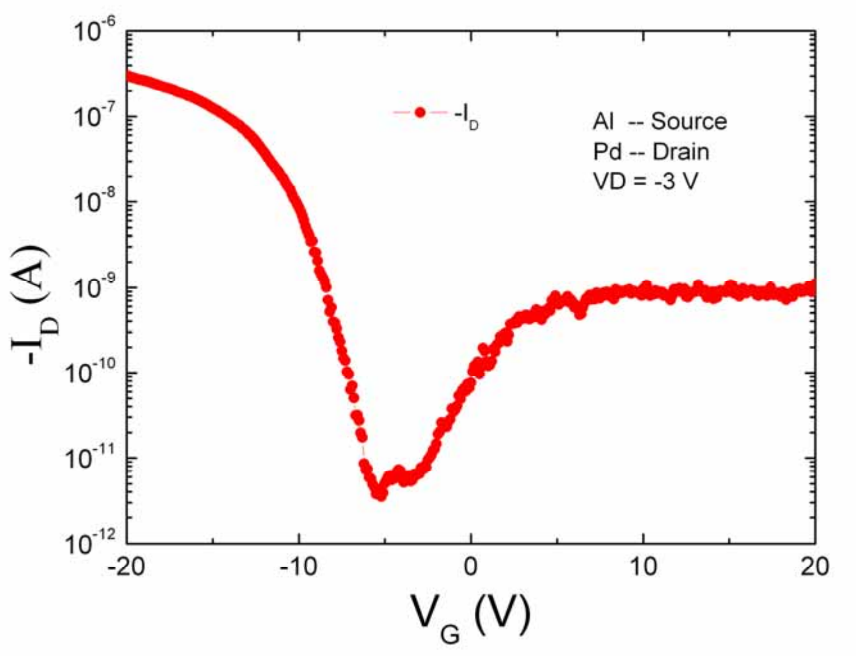
- Electron mean free path at room temperature: 1.6 μm
- Capability of current density: 10^9 A/cm^2

Applications

- Interconnection without electromigration effect due to strong C–C bonds
- Coherent electron waveguide when low contact resistance
- Quantum dot when high contact resistance(Low Temperatue)

CNT-FET based on nanotube network



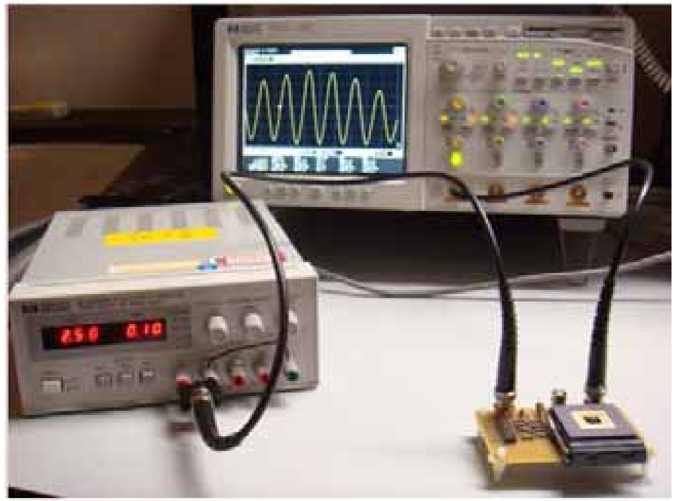


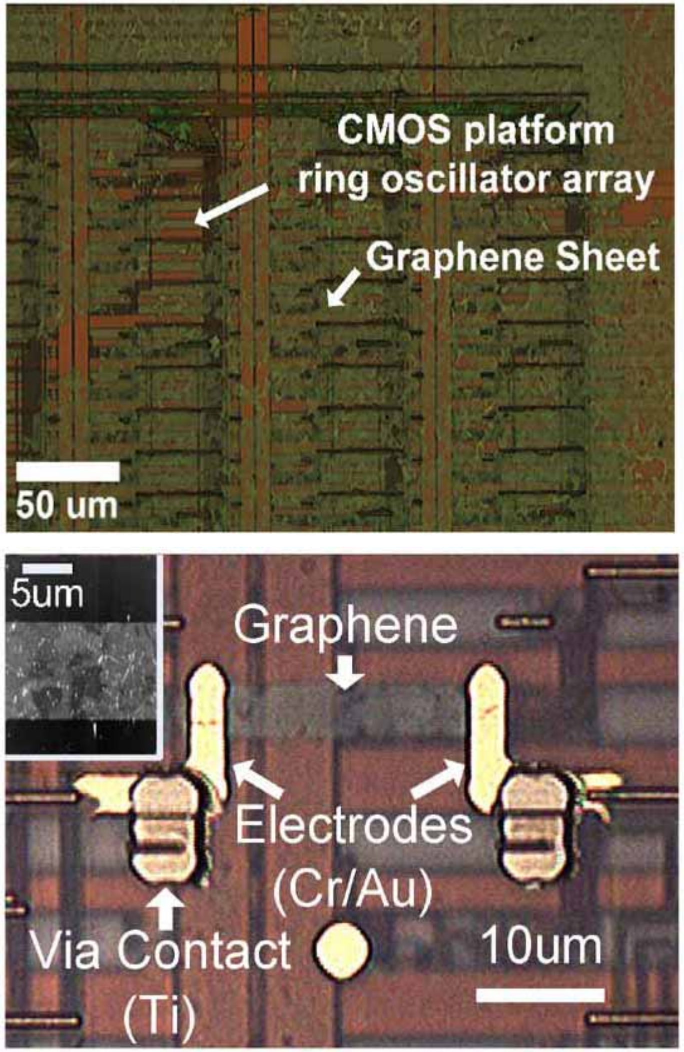
- CNT-FET was realized by percolation of nanotubes
- Metallic nanotubes were not percolated

Graphene & CNT Interconnects

Graphene & CNT Interconnects

- Prediction: below 10nm carbon outperforms copper in terms of
  - Resistivity
  - Maximum current density
- Chen et al.: Maximum frequency in graphene interconnects: 1.3 GHz





All images: Chen et al., IEEE TED, 2010

Lecture 11: Outline

- Silicon CMOS
- Carbon Technology
  - Graphene
  - Carbon Nanotubes (CNTs)
- Photonics
- Future Outlook

Photonic Crystals

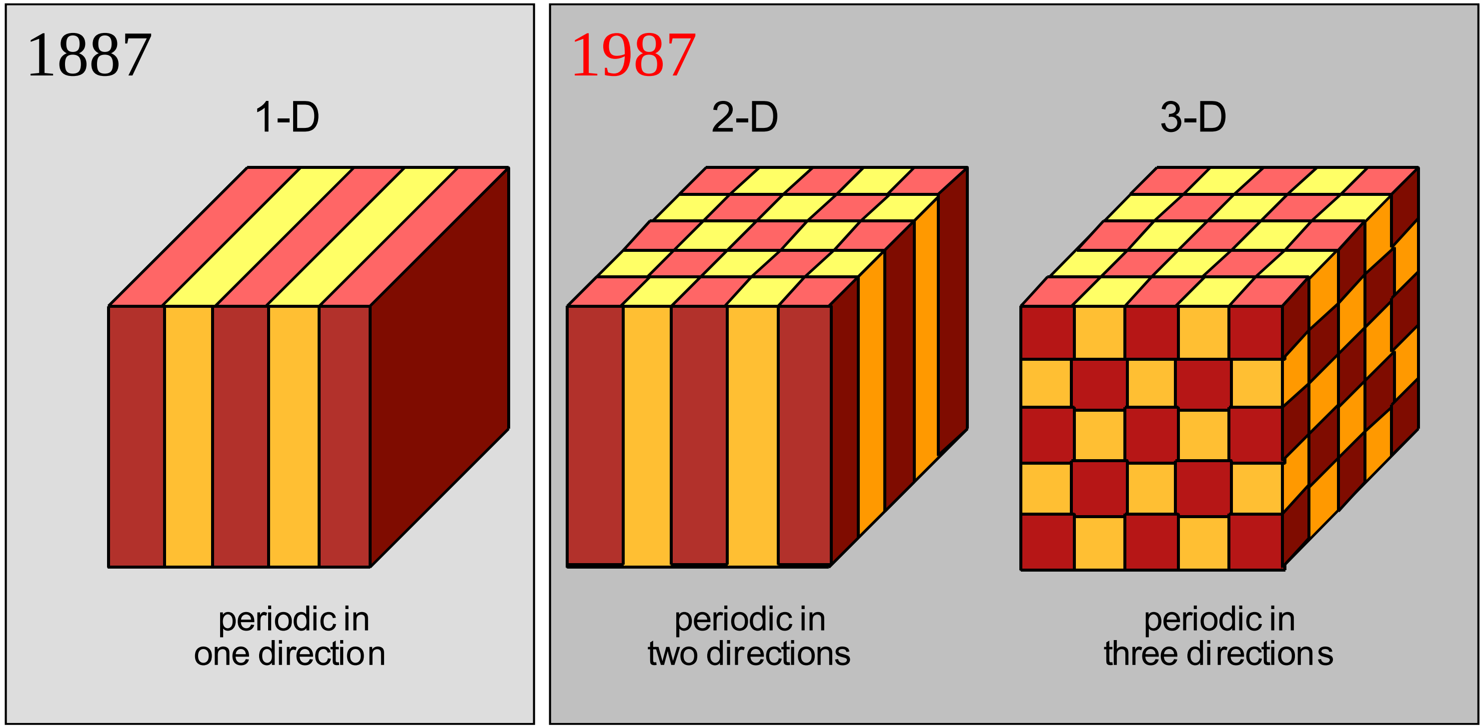
Eli Yablonovitch,UCLA,
inventor of Photonic Crystals
and Strained Layer QW lasers

“The opportunity is now emerging for the creation of a broad technology of photonic integrated circuits, in analogy with the creation of the monolithic Si integrated circuits in the 1950's. This new design paradigm would take advantage of the miniaturization provided by photonic bandgaps structures“

Plenary talk, CLEO Pacific Rim, 2001, Chiba, Japan

What are Photonic Crystals ?

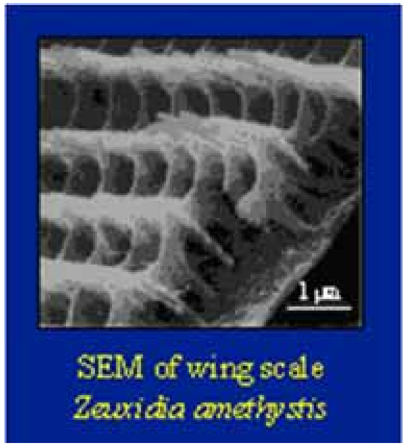
Photonic crystals are artificial structures with a refractive index periodically modulated on a length scale comparable to a light wavelength.



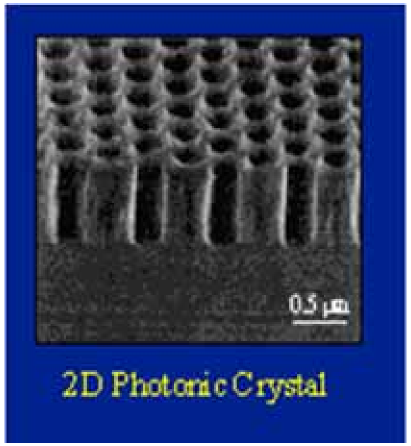
Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

Photonic Crystals in Nature

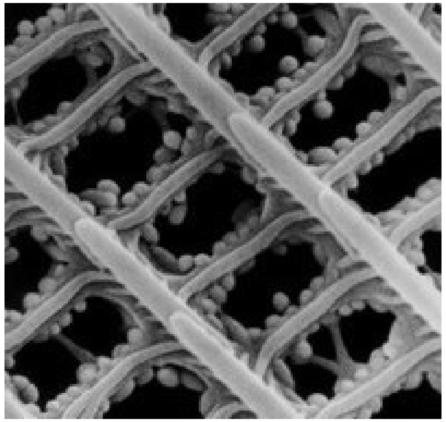

Adonis Blue Butterfly
Lysandra bellargus



SEM of wing scale
Zauxidia amethystis



2D Photonic Crystal



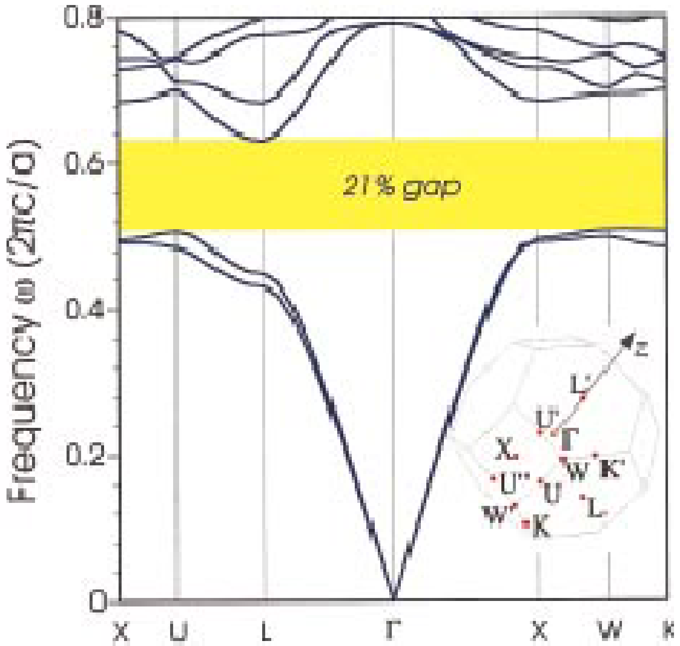
Nature is fantastic!

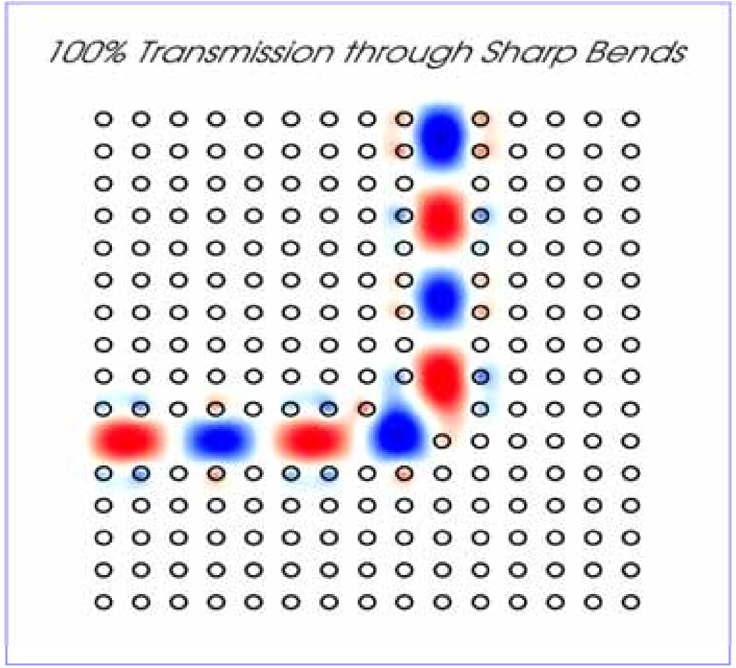
Band Structure and Photonic Band Gap

When electromagnetic waves propagate in a photonic crystal, there is a relation between the propagation wave vectors and the frequencies, i.e., *dispersion relation*. This relation is called the *band structure* of the photonic crystal.

If, for some frequency range, the electromagnetic waves cannot propagate, we say that the crystal has a *photonic band gap*

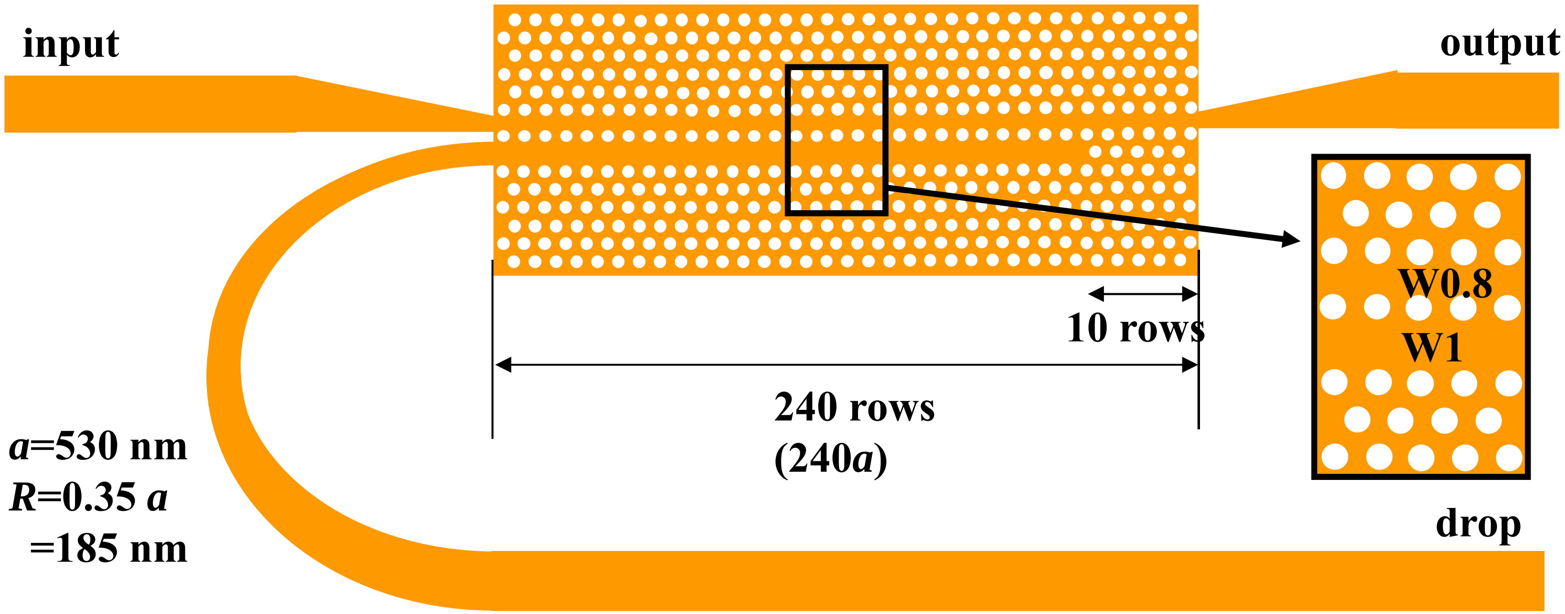
This is the optical analog of electronic bandstructure



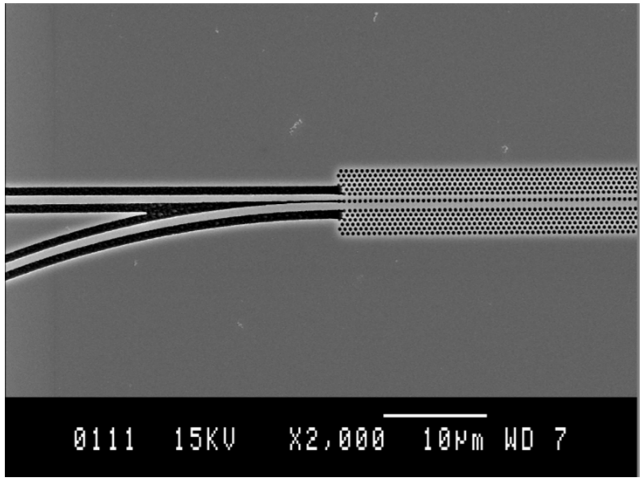


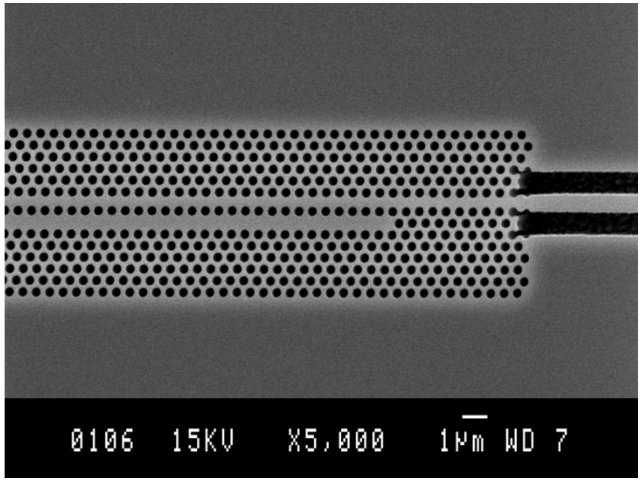
S.G. Johnson *et al*., *Appl. Phys. Lett.* **77**, 3490 (2000)

2D Fabrication



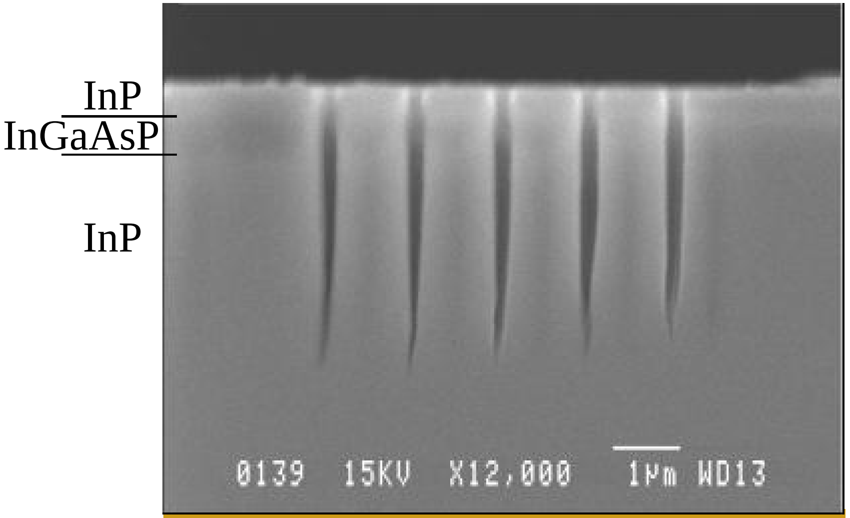
a=530 nm
R=0.35 *a*
=185 nm





Etched PC structures @ KTH

- MOVPE (metal organic vapor phase epitaxy) growth
- E-beam lithography
- Ar/Cl_2 Chemical Assisted Ion beam Etching

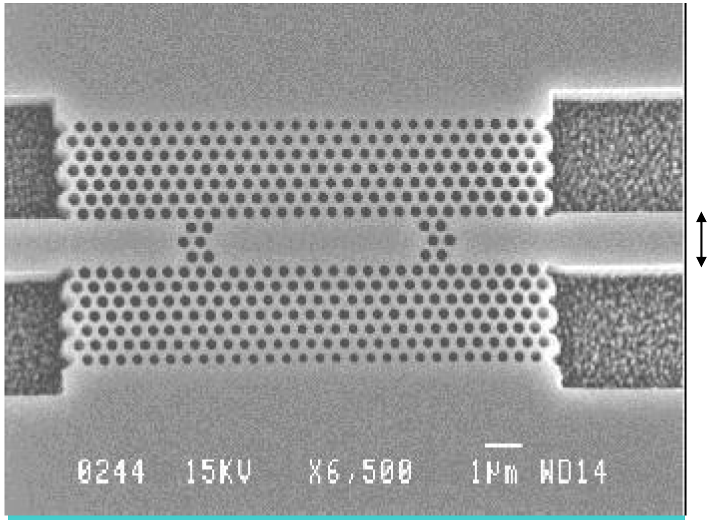


Cut View

Etch depth: > 4 μm

Higher etch depth ⇨

Less scattering loss into the substrate



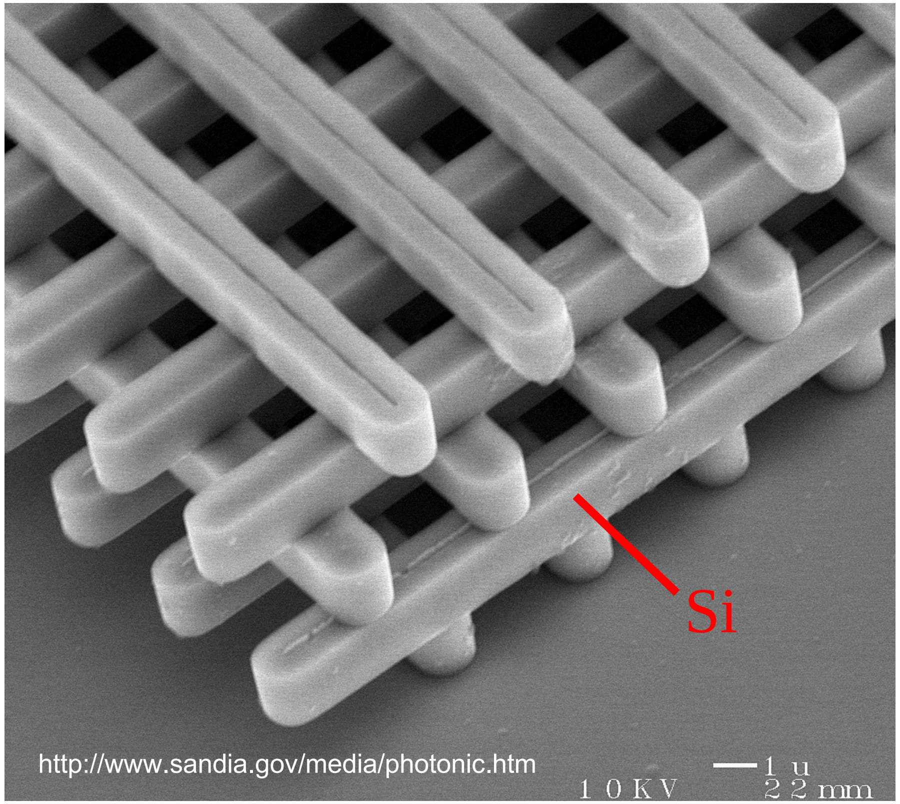
Top view

PC waveguide

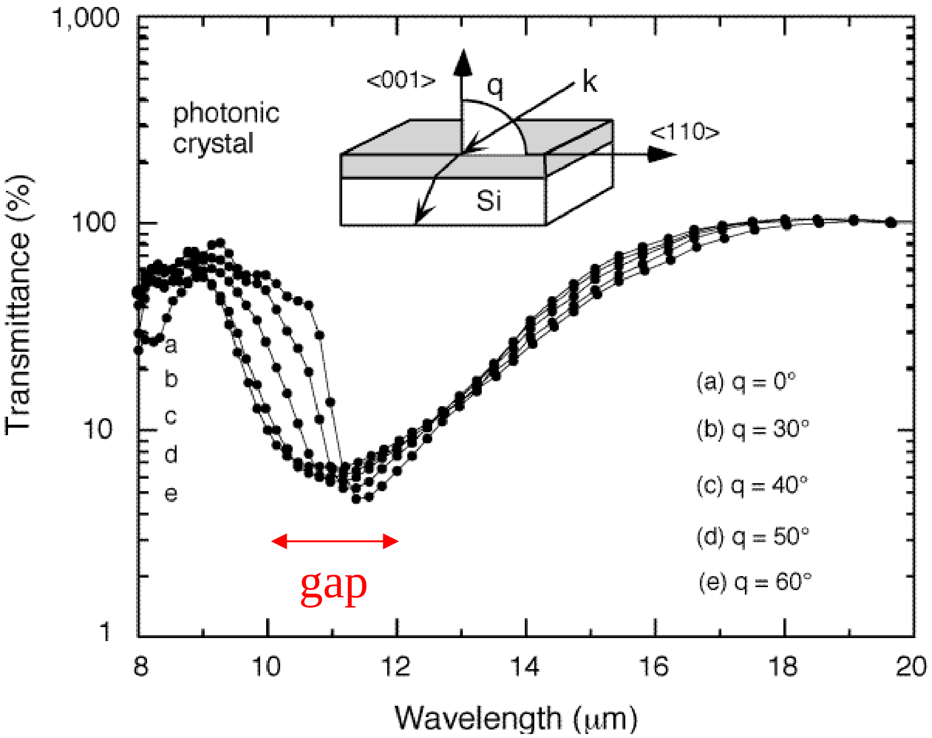
3D Fabrication: The "Woodpile" Crystal

[K. Ho *et al.*, *Solid State Comm.* **89**, 413 (1994)] [H. S. Sözüer *et al.*, *J. Mod. Opt.* **41**, 231 (1994)]

(4 "log" layers = 1 period)

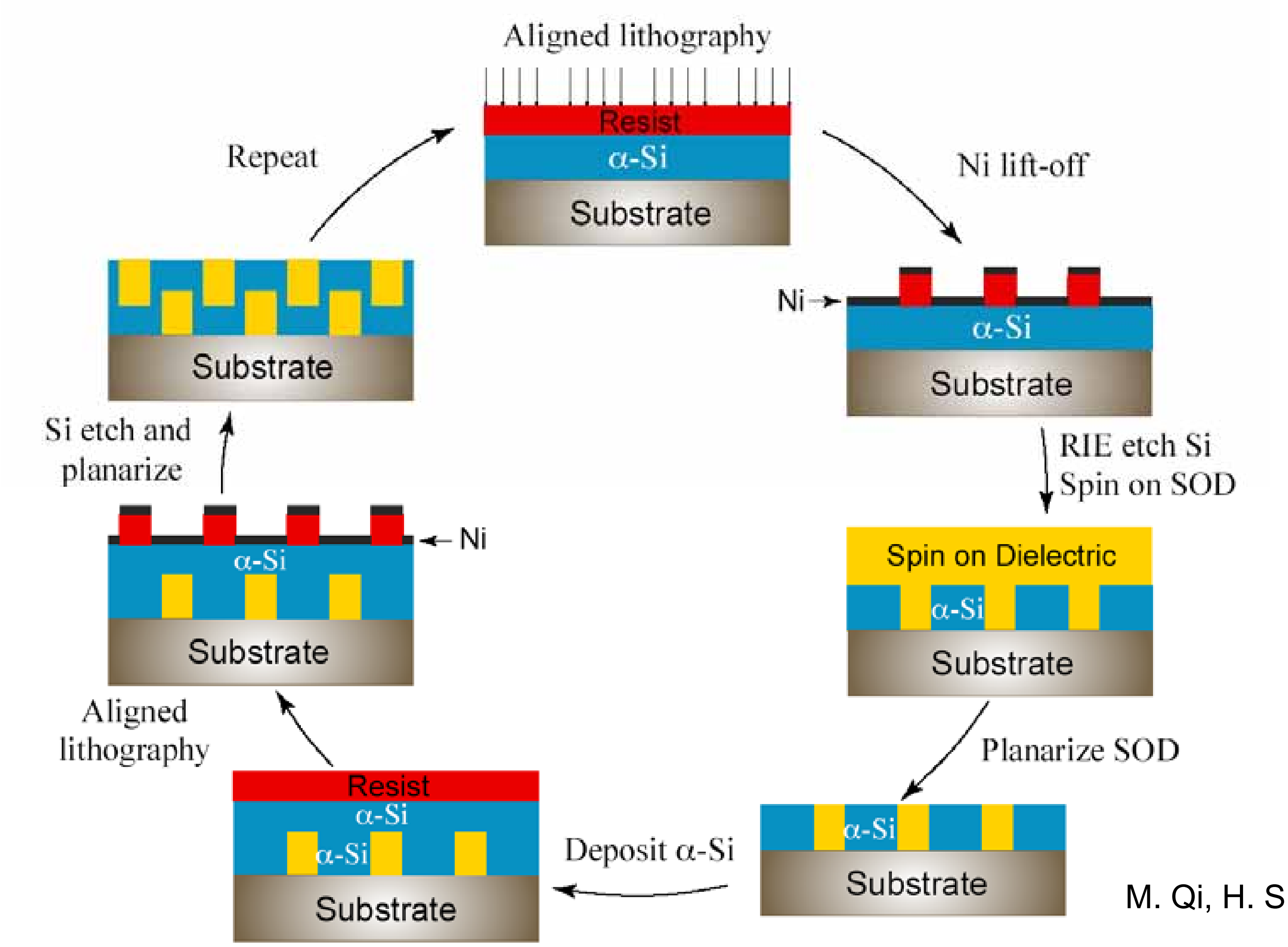


[S. Y. Lin *et al.*, *Nature* **394**, 251 (1998)]



Source: S.G. Johnson, "Photonic Crystals: A Crash Course in Designer Electromagnetism"

3D Fabrication: “Standard” Technology



M. Qi, H. Smith, MIT

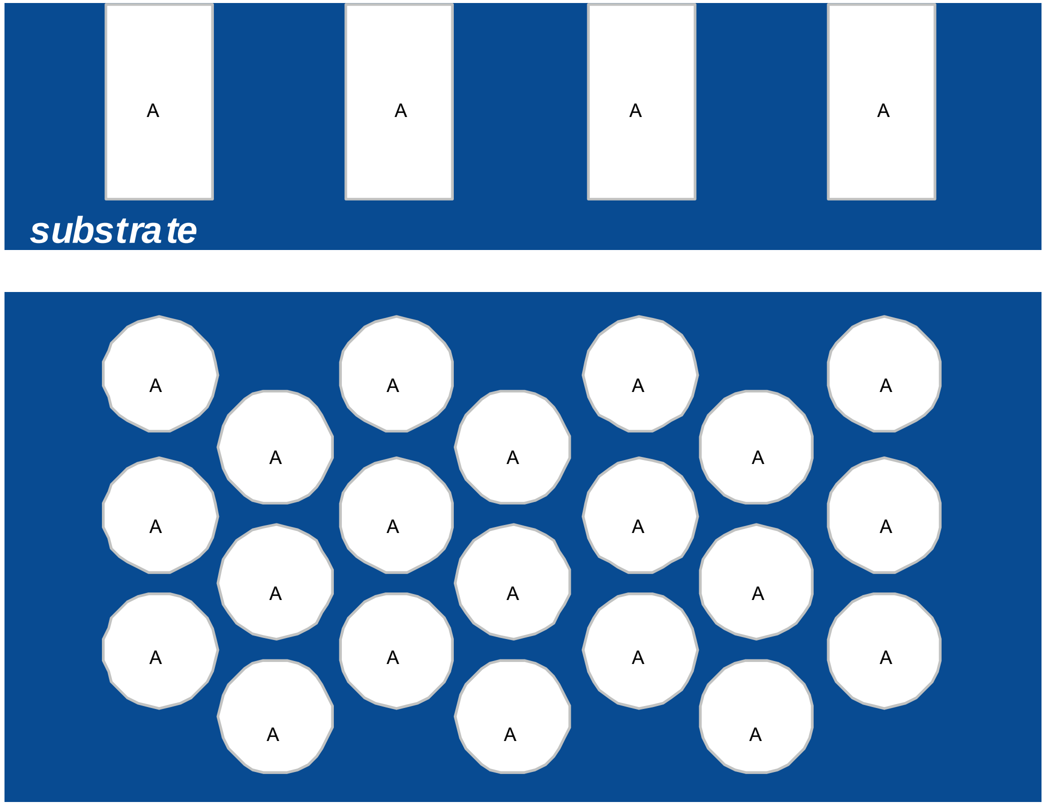
Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication: A Schematic

Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication: A Schematic

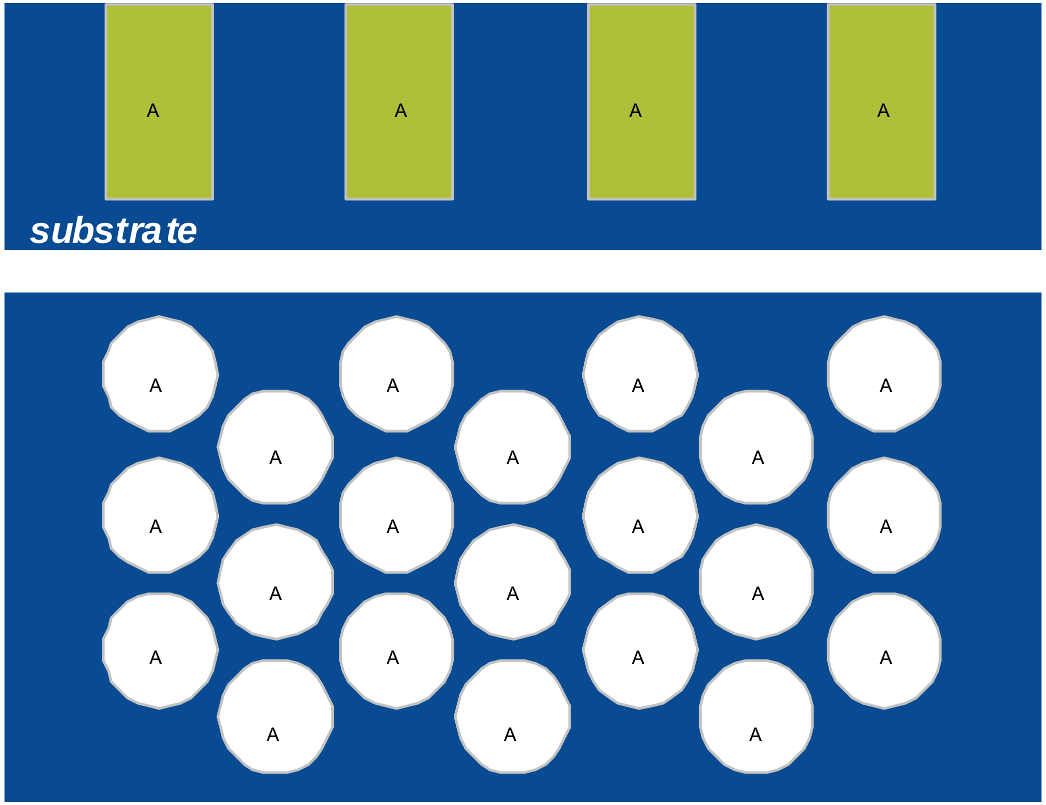
expose/etch
holes



Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication: A Schematic

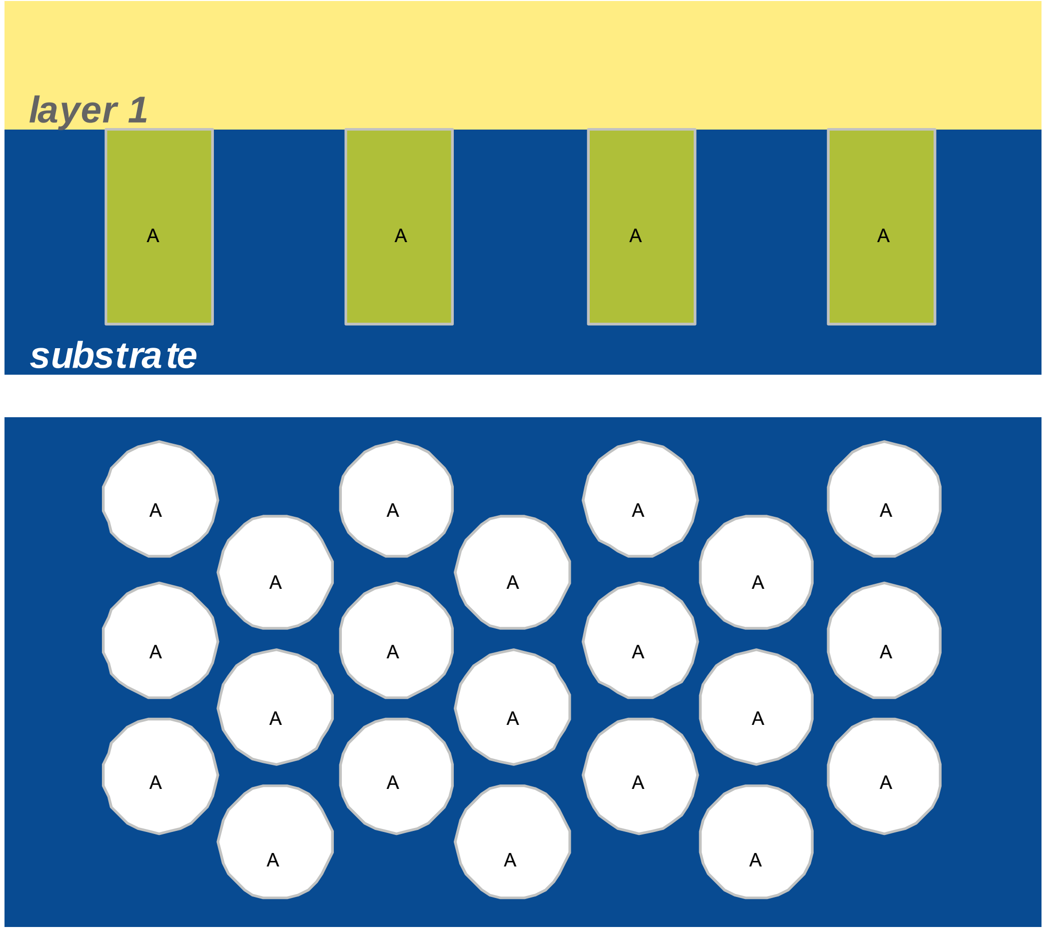
backfill with
silica (SiO_2)
& polish



Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication: A Schematic

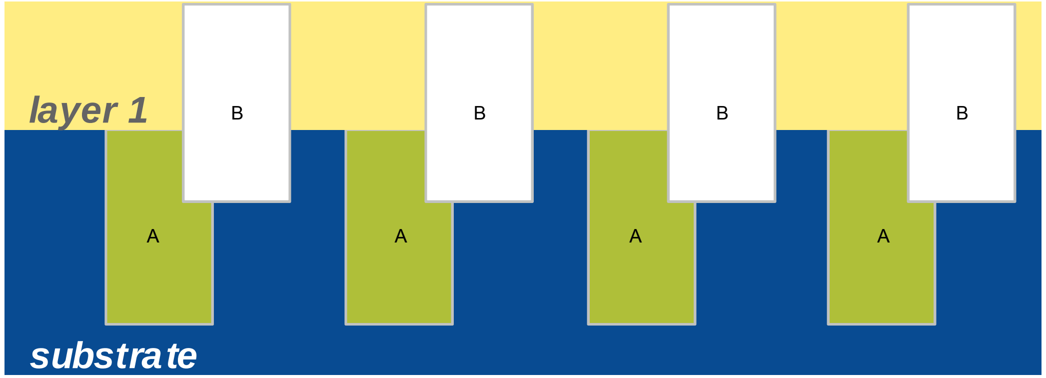
deposit another
Si layer

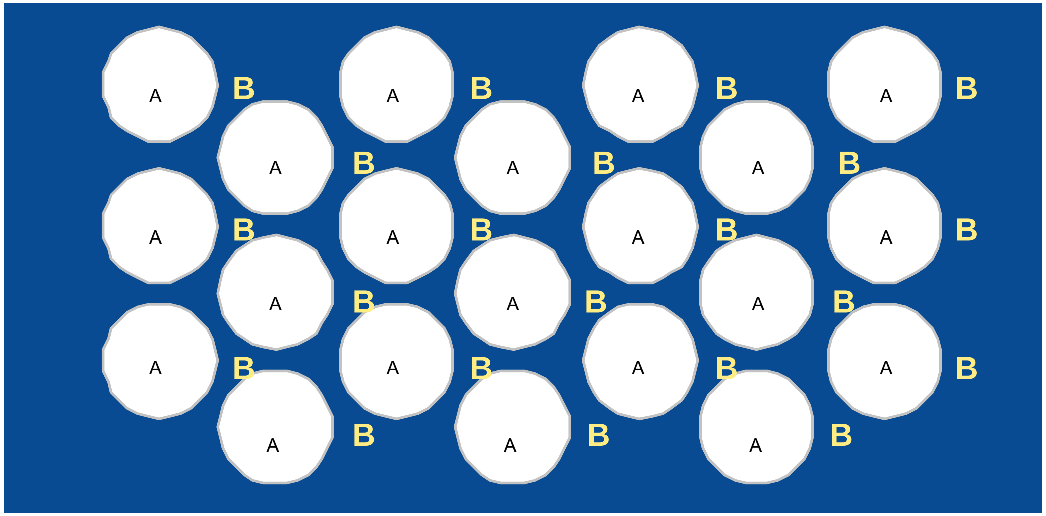


Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication: A Schematic

dig more holes
offset
& overlapping

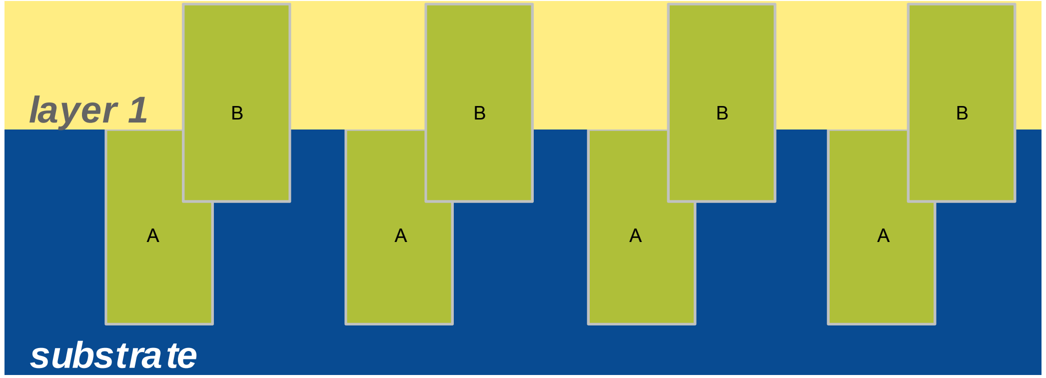


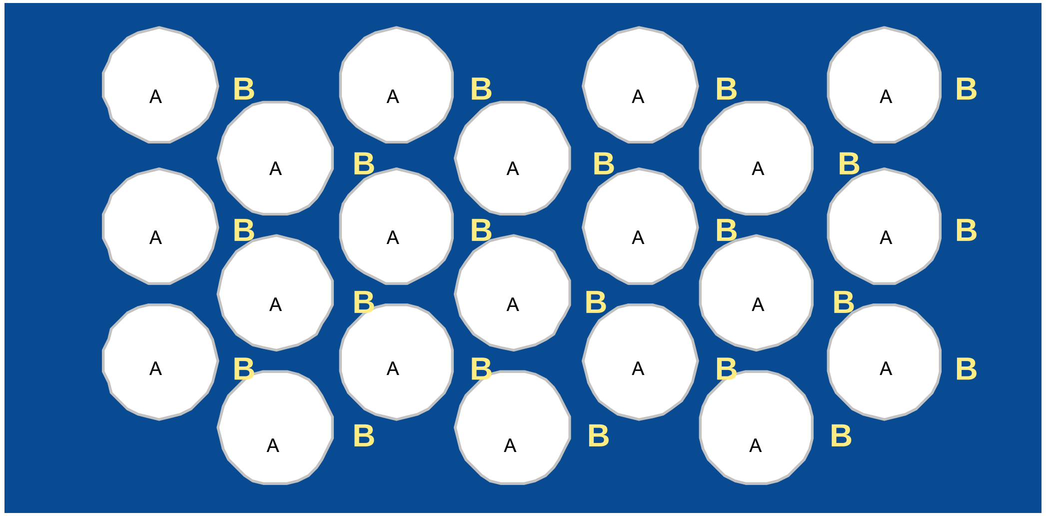


Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication: A Schematic

backfill



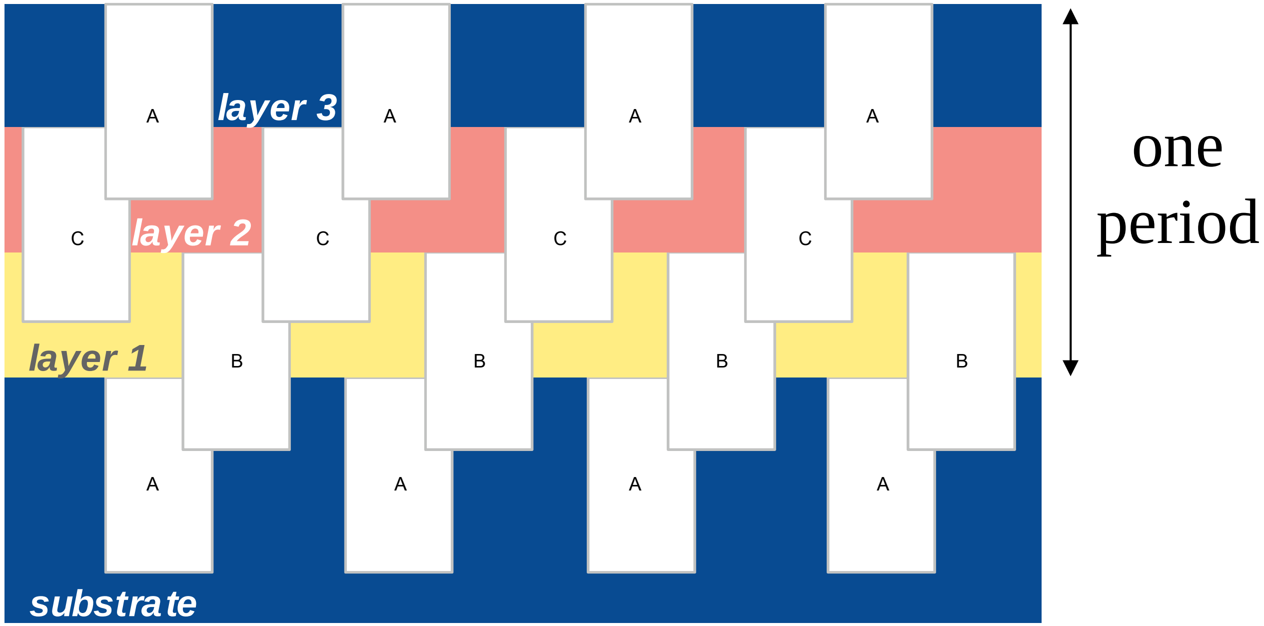


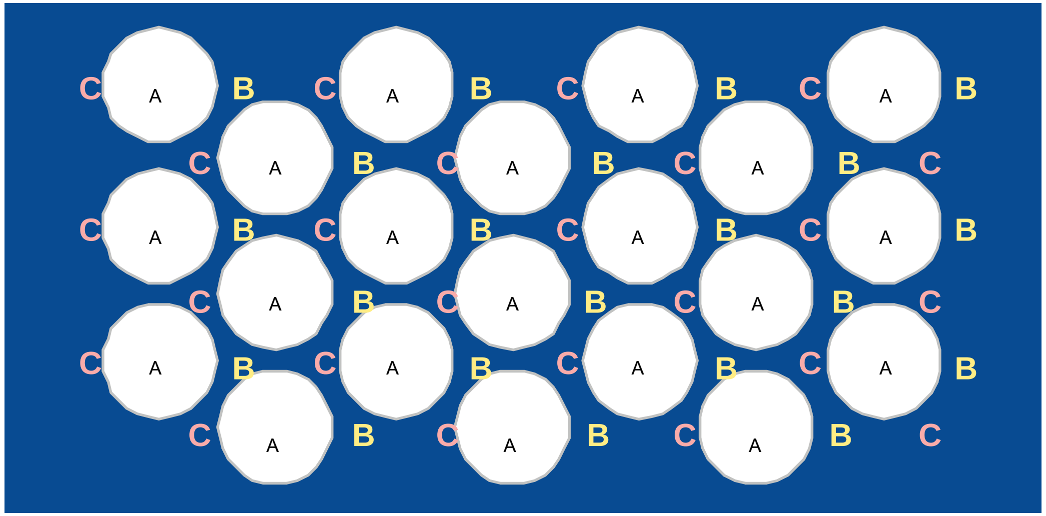
Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication

etcetera

(dissolve silica when done)

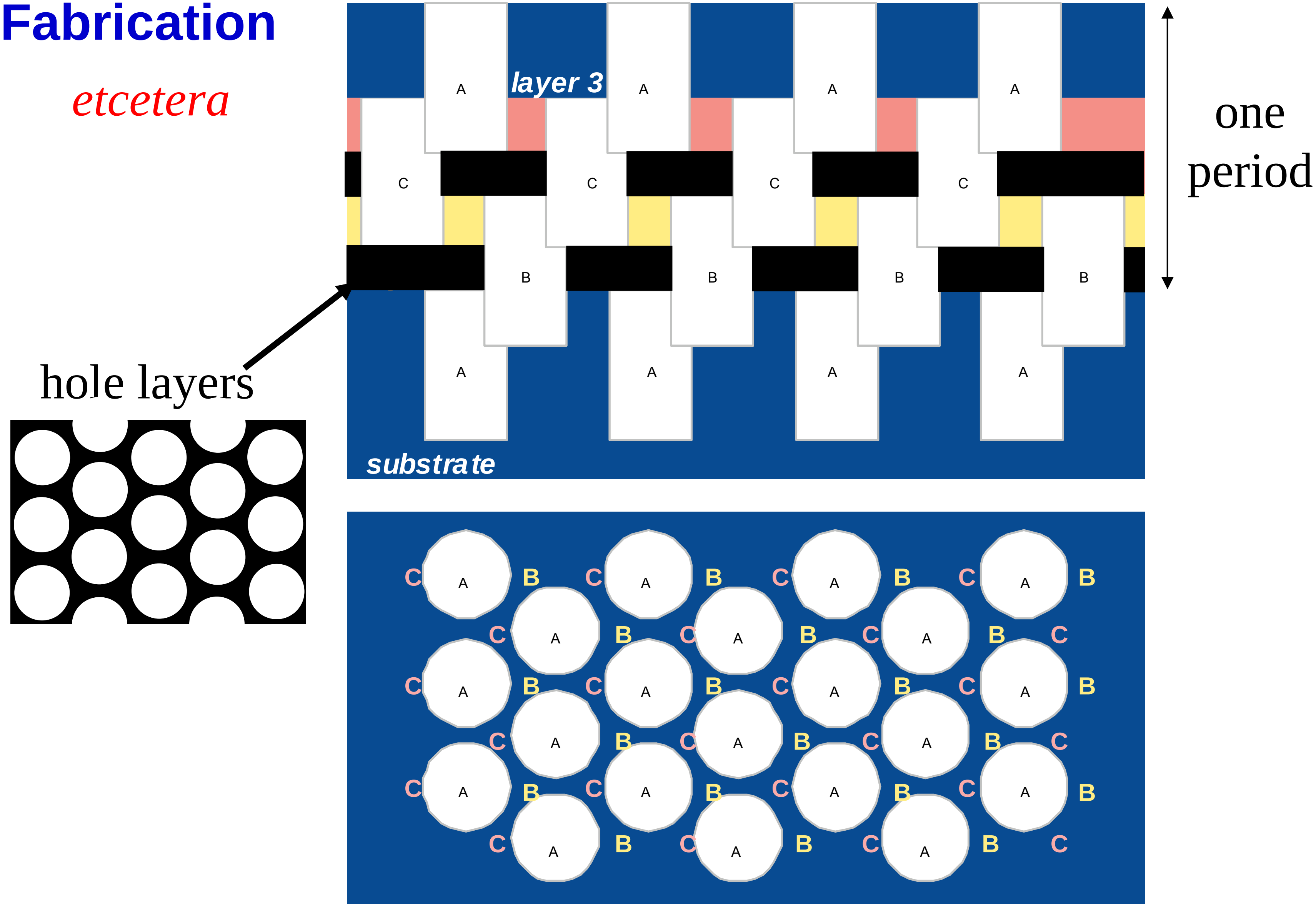




Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication

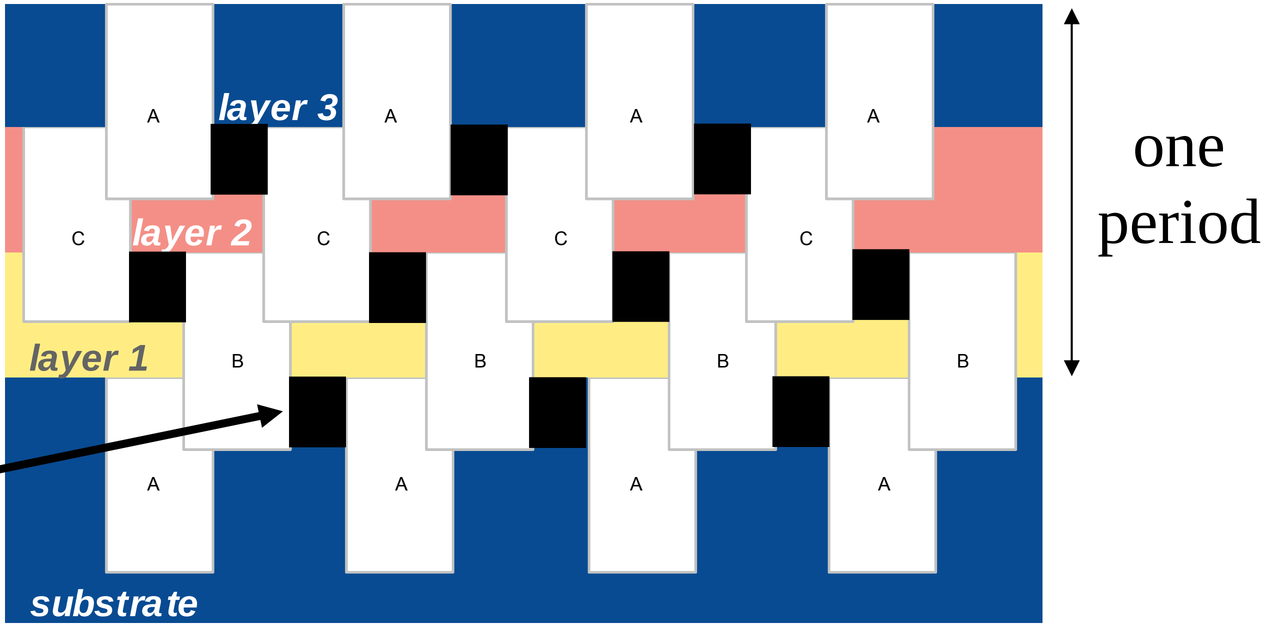
etcetera

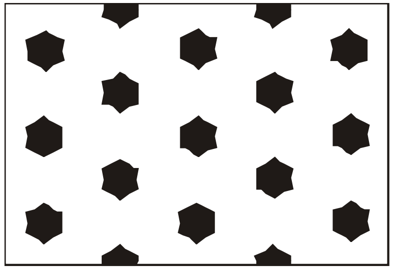


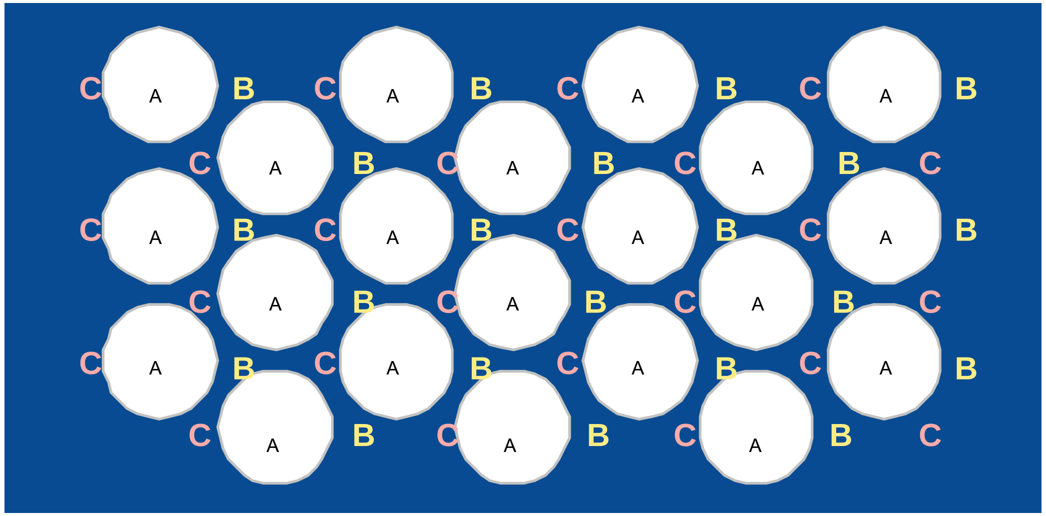
Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

3D Fabrication

etcetera

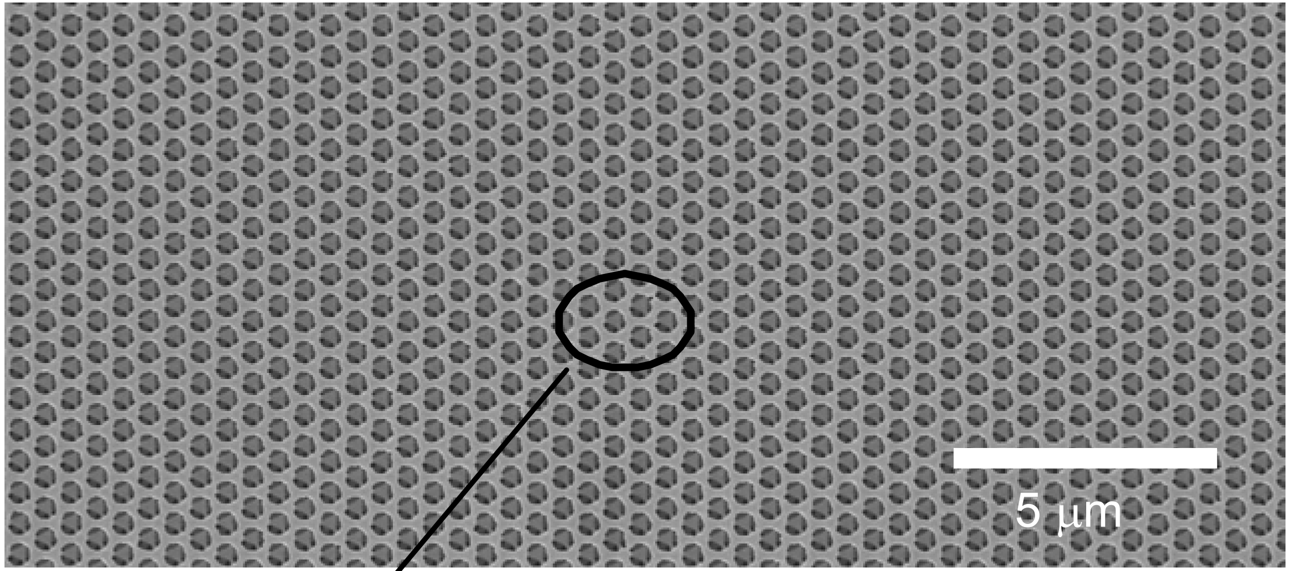


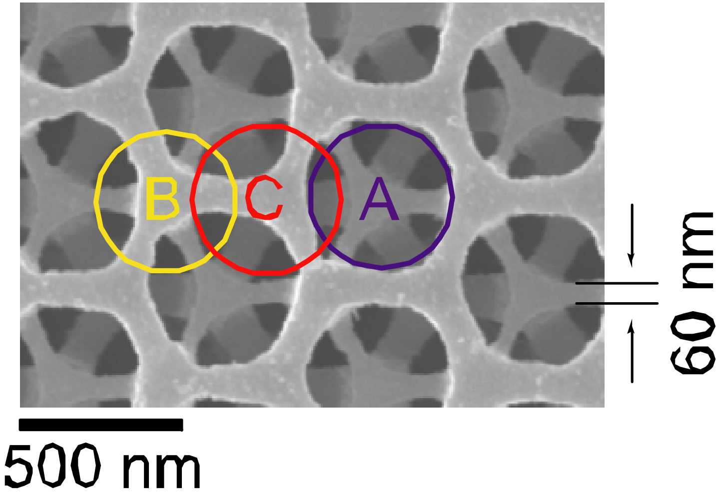


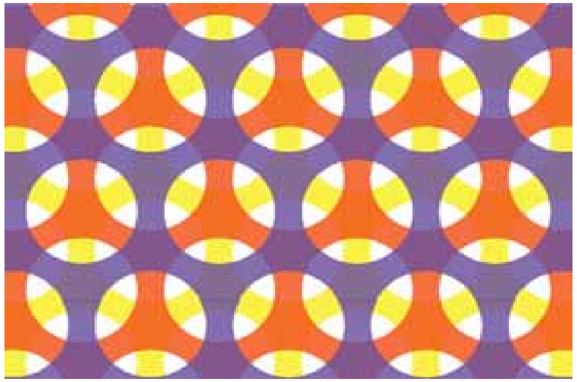


Source: S.G. Johnson, "Photonic Crystals: A Crash Course in Designer Electromagnetism"

Example: 7-layer E-Beam Fabrication



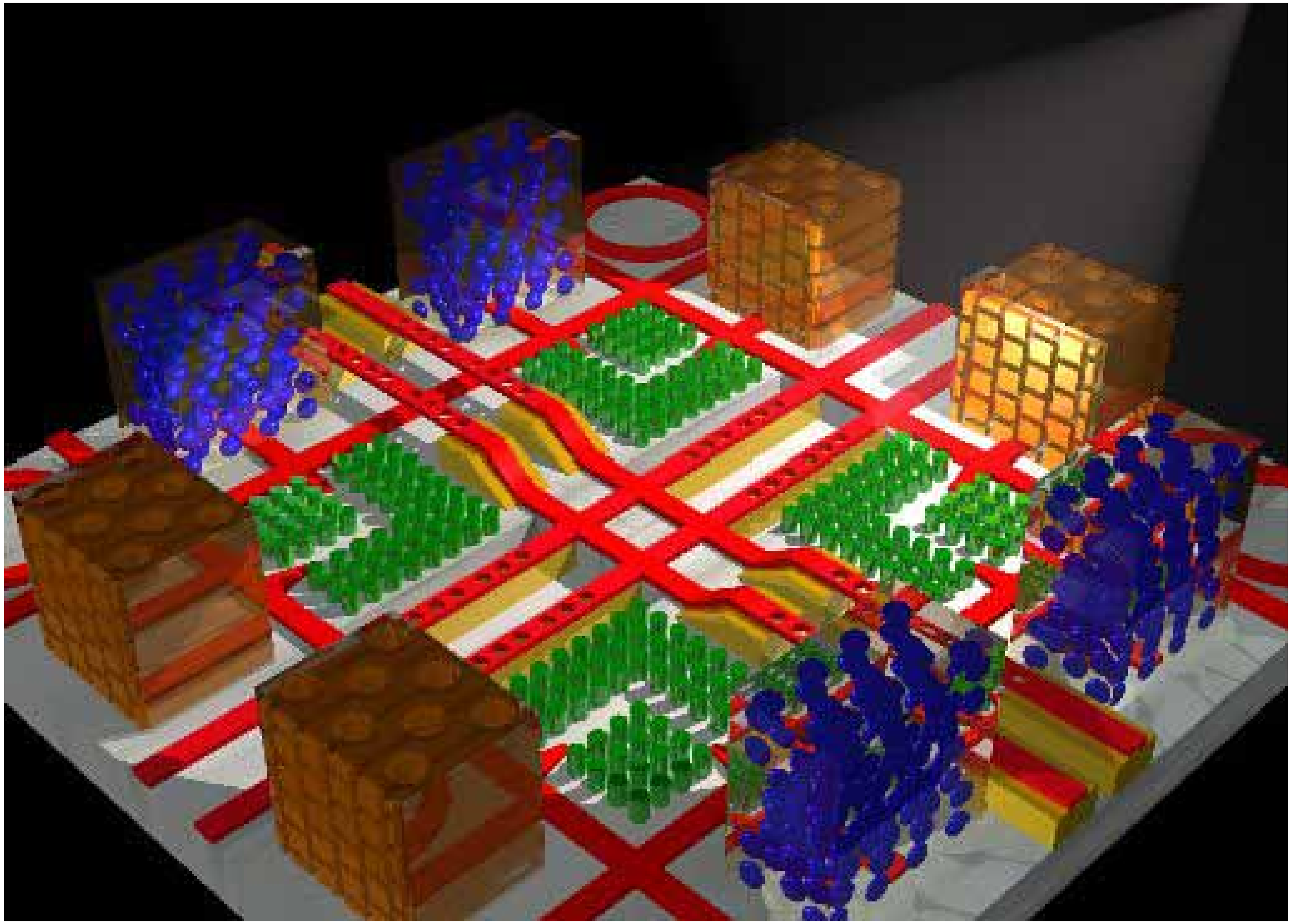




M. Qi, *et al.*, *Nature* **429**, 538 (2004)

Source: S.G. Johnson, “Photonic Crystals: A Crash Course in Designer Electromagnetism”

Photonic Micropolis



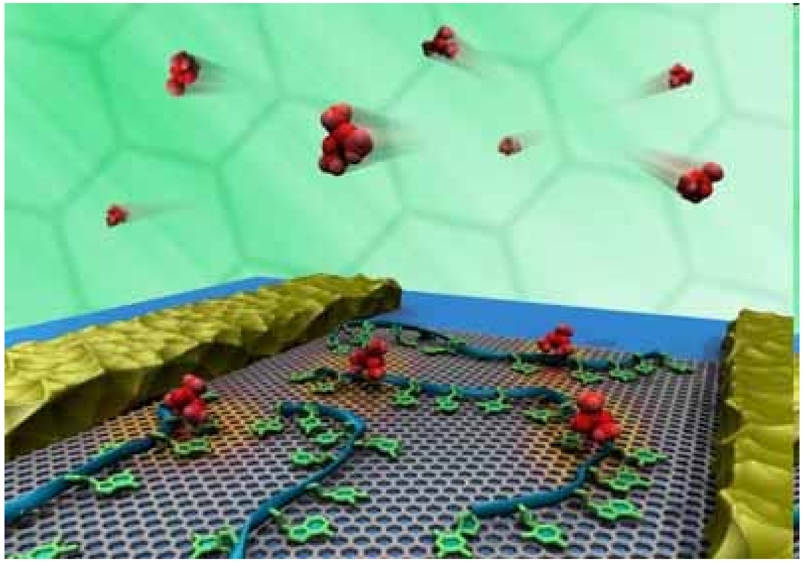
http://ab-initio.mit.edu/photons/

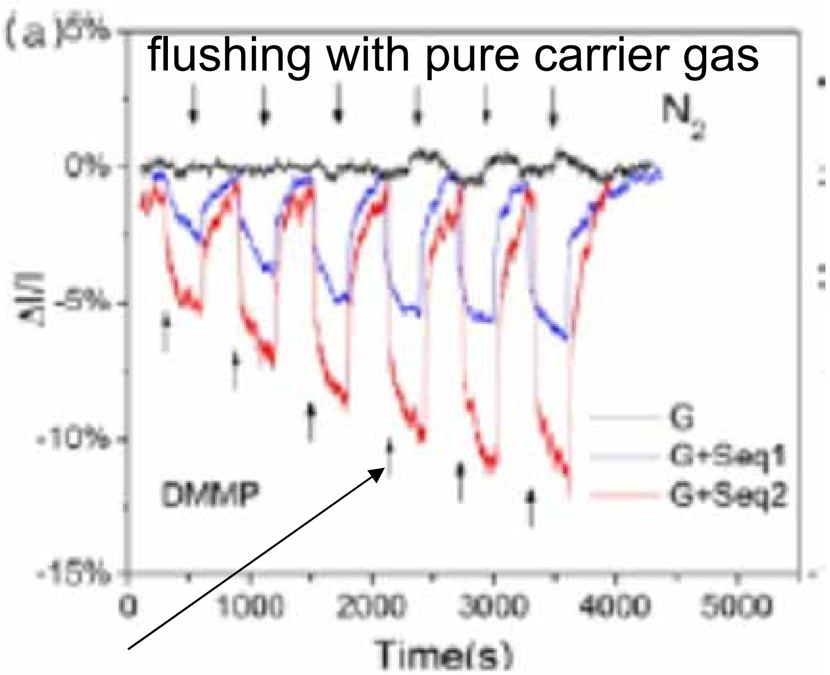
Lecture 11: Outline

- Silicon CMOS
- Carbon Technology
- Photonics
- Future Outlook
    - Biotechnology

Outlook: Biotechnology

DNA decorated graphene chemical sensors





flushing with pure carrier gas

Introduction of analyte at progressively larger concentrations

Changes in current versus time for ssDNA-graphene vapor responses

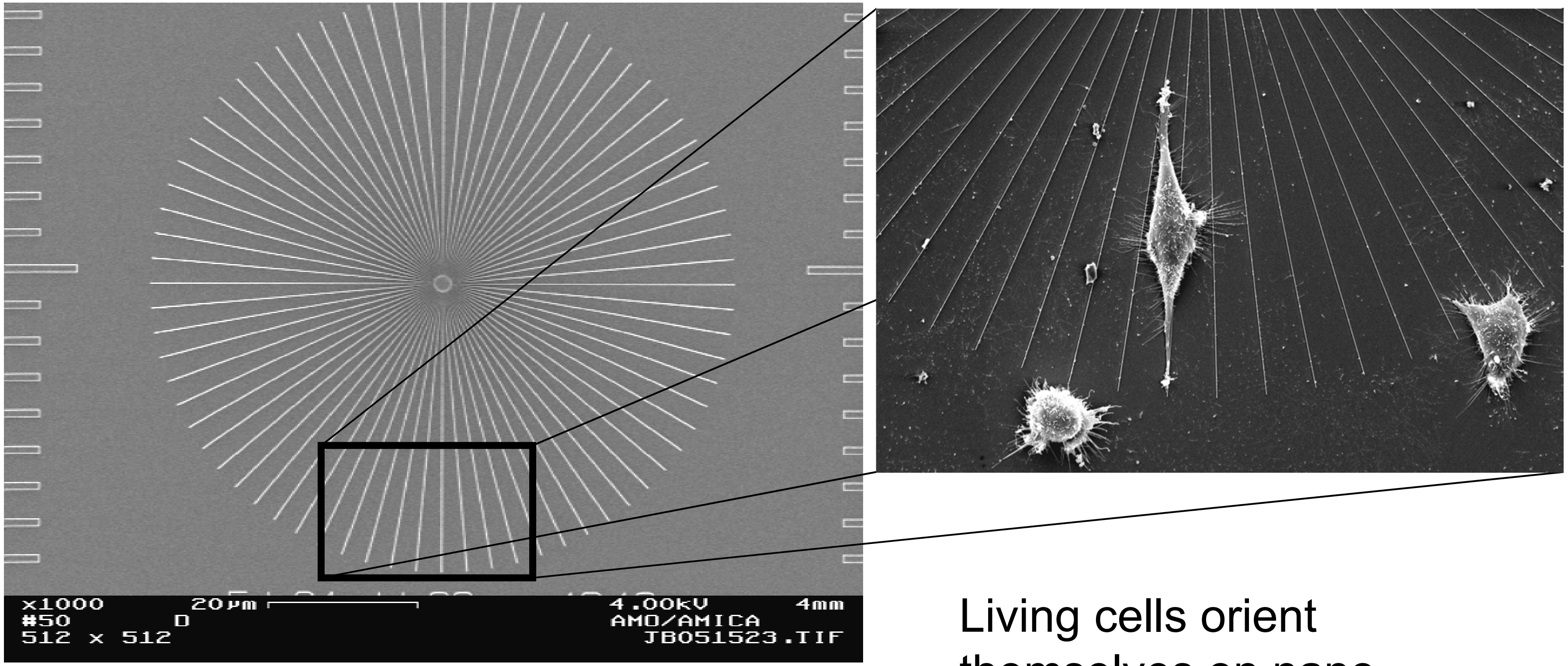
- Clean graphene devices (black data) show very weak vapor responses barely above the noise floor
- Devices functionalized (red & blue data) show significant sequence-dependent responses

Lu et al., "DNA decorated graphene chemical sensors", Appl. Phys. Lett. 97, 083107 (2010)

Outlook: Biotechnology

CellPROM
Cell Programming by
Nanoscaled Devices

Nanostructured surface determines the development of individual cells

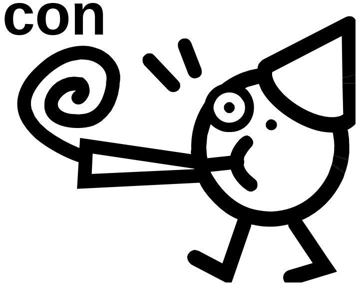


Nanostructured surfaces to study cell adhesion, growth and differentiation

Living cells orient themselves on nano-landscapes

Future Technology Options

- Silicon Nanowire FETs (FinFET, MUGFET)
- Carbon FETs: Graphen-Nanoribbon (GNR)-FETs, Tunnel-GFETs, RF-GFETs, CNT FETs
- Sensors (Functionalization, Biocompatibility)
- Transparent Electrodes (Solar, Flat Panel Displays)
- Photonics (silicon, carbon)
- THz Detection / Generation
- Spintronics (Spin-Valves, SpinMOSFET, SpinFET)
- Energy Storage (Supercapacitors)
- Thermoelectricity (el. vs. therm. Conductivity, silicon nanowires)
- MEMS / NEMS (silicon, graphene)



A Day in the Clean Room