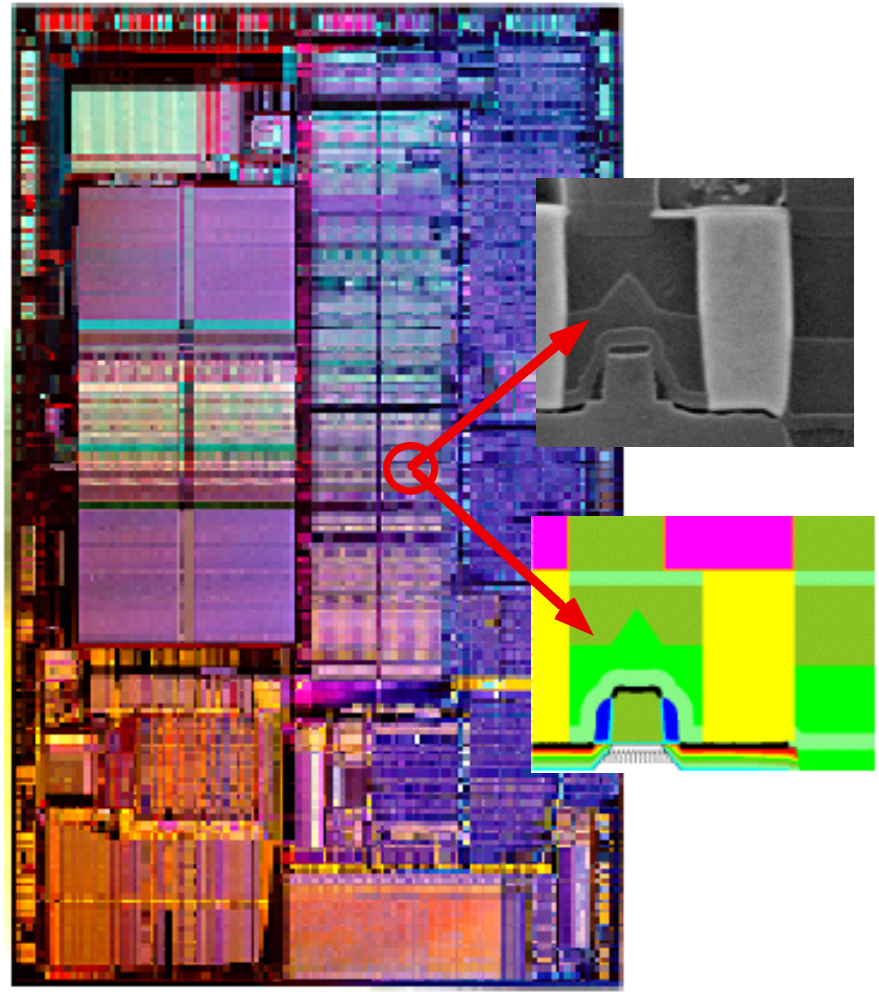
Lecture 1
Introduction and technology roadmap



- Introduction to IH2655
- Brief historic overview
- Moore's Law and the ITRS Roadmap
- MOS Transistor (re-cap)
- From Geometrical to Material-based scaling
- CMOS Process Flow

Course PM

Subject: Advanced course of the physical and technological concepts used in modern CMOS and bipolar/BiCMOS fabrication.

Prerequisites: Semiconductor Devices (IH1611) or Semiconductor Theory and Device Physics (IH2651) or equivalent knowledge in semiconductor device physics.

Course content: 26 h lectures week 3-10 (see Daisy schedule).
Approximately 8 h laboratory exercises (2 labs), to be scheduled in groups of 4-5.

Language: English

Course PM cont'd

Lecturer and Course Director: Prof. Mikael Östling, Department of Integrated Devices & Circuits (EKT), School of ICT, KTH.
E-mail: ostling@kth.se, phone: 08-790 4301

Lectures will also be given by: Dr Christoph Henkel 08-790 4177, chenkel@kth.se and Assoc. prof Gunnar Malm, gunta@kth.se, 08-790 4332, same department

Laboratory asisstants are Mr Eugenio Dentoni Litta, eudl@kth.se, and Mr Sam Vaziri, vaziri@kth.se, same department.

Literature: Plummer, Deal and Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling*. Prentice-Hall 2000, ISBN 0-13-085037-3. (725 kr THS Bookstore in Kista)

Examples from other VLSI books and journal articles

Strong Suggestion: Read chapters before class – Concept Tests will help you much more

Examination: Two written lab reports on time and 1 h Oral examination.

Signup sheets for labs and exam through Daisy.

https://www.kth.se/social/course/IH2655/

Course PM cont'd

NOTE: LAB REPORTS ARE DUE ONE WEEK AFTER THE LAB!

IF YOUR LAB REPORT IS LATE YOUR MAXIMUM GRADE IS E

Individual laboratory reports are required and please observe that any signs of plagiarism will directly be reported to the Disciplinary board

Schedule

#	Date	Time	Room	Subject
1	14-Jan	13-15	Ka439	Introduction. MOSFETs,Technology roadmap. Overview of fabrication flow (M Östling)
2	15-Jan	10-12	Ka439	Wafer fabrication and silicon epitaxy (M Östling)
3	21-Jan	13-15	Ka439	Wafer clean and wet processing, (C Henkel)
4	22-Jan	10-12	Ka439	Electrical characterization. (G Malm)
5	28-Jan	13-15	Ka439	Thermal oxidation of silicon (C Henkel)
6	29-Jan	10-12	Ka439	Annealing (FA & RTA) Diffusion and ion implantation, (C Henkel)
7	4-Feb	13-15	Ka439	Dry etching (M Östling)
8	5-Feb	10-12	Ka439	Deposition of dielectrics and polysilicon (C Henkel)
9	11-Feb	13-15	Ka439	Microlithography (M Östling)
10	12-Feb	10-12	Ka439	Metallization and contacts (M Östling)
11	18-Feb	13-15	Ka439	Back-end processing (M. Östling)
12	19-Feb	10-12	Ka439	Process integration: MOS and Bipolar
13	25-Feb	13-15	Ka439	Sustainable fabrication (G Malm)
14	26-Mar	10-12	Ka439	Nanostructures / nanophysics (M Östling)
15	4-Mar	10-12	Ka439	Reserve time

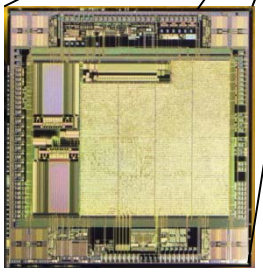
Microelectronic processing

Clean room environment

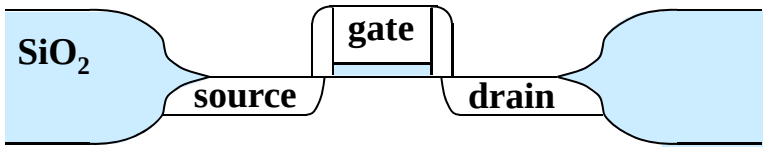
Source: Infineon

Wafer level

Source: Infineon



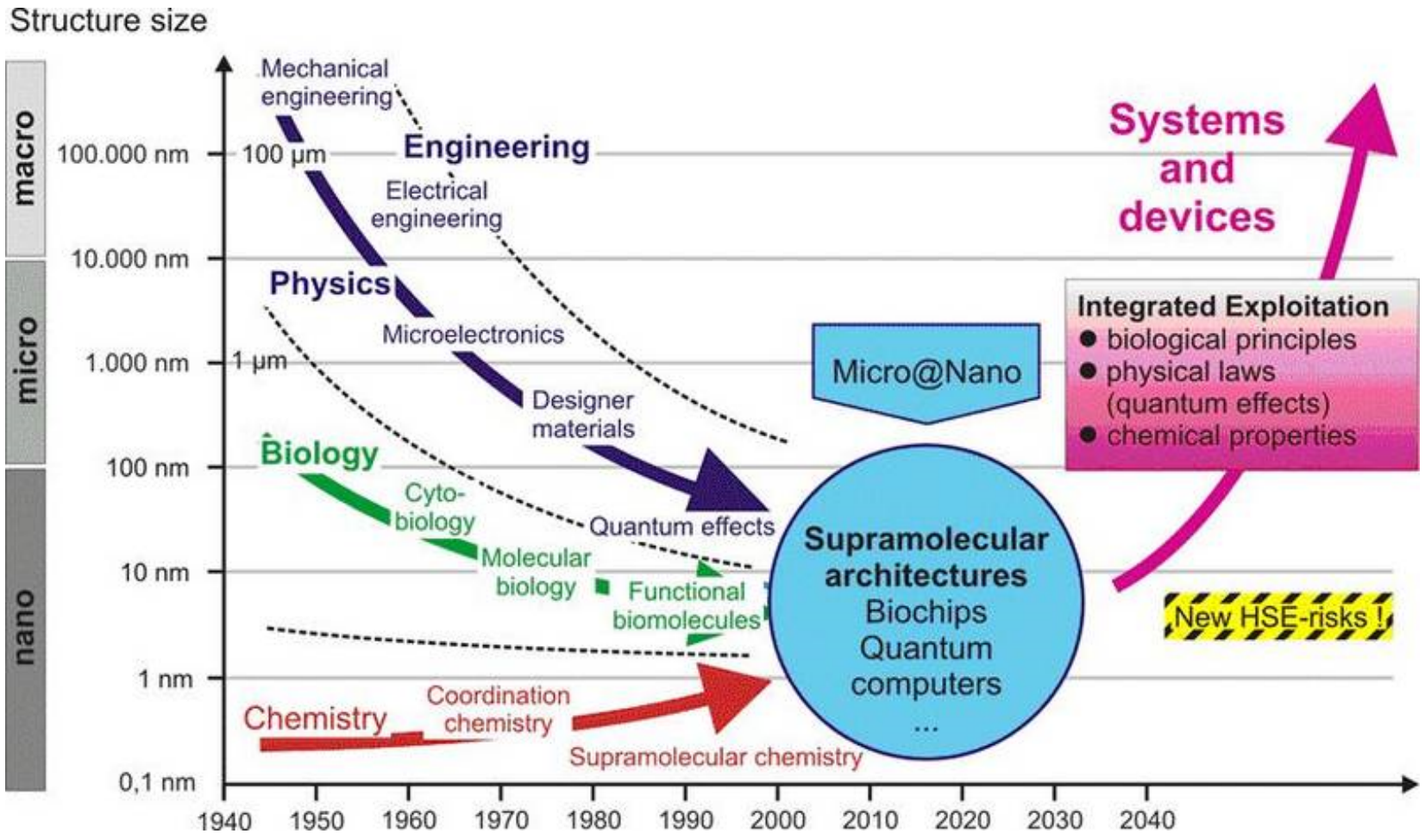
Chip level



Transistor level

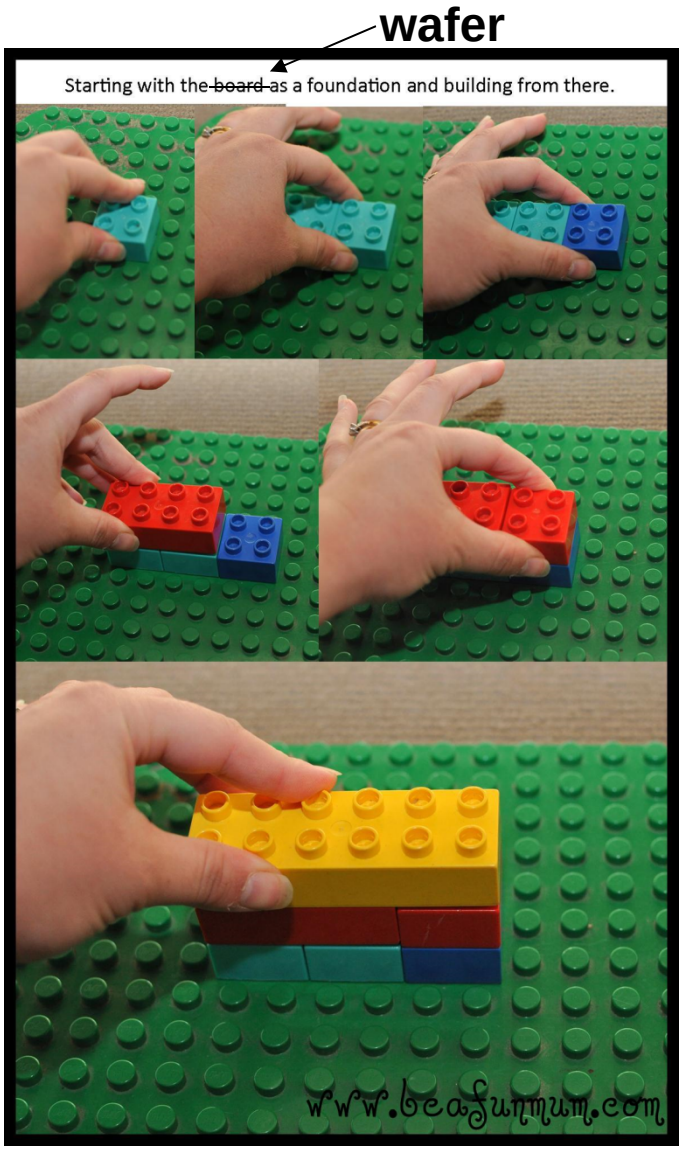
…so why should you care if you plan to work in Nanoscience, MEMS, PV or Photonics?

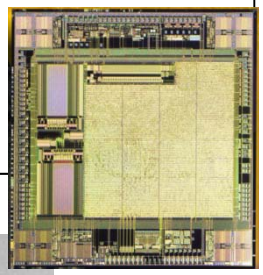
Top down AND Bottom Up



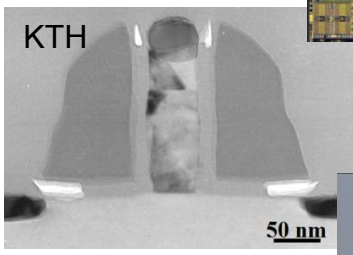
Source: website Univ. Wien

IH2655: Lego for grown-ups

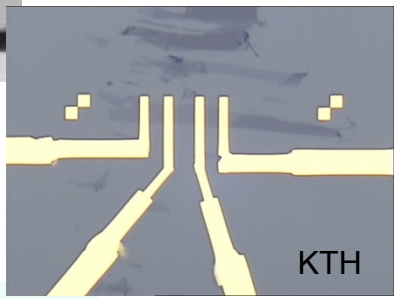




Silicon MOSFET

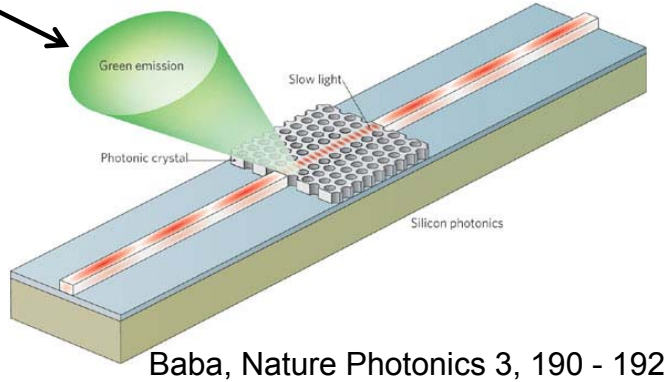


Graphene and CNTs



Photovoltaics

Photonics



Baba, Nature Photonics 3, 190 - 192 (2009)

IH2655 Aim

This course is about the process technology used to ***manufacture semiconductor devices***. It aims to familiarize with the related ***technical vocabulary*** and to provide the students with a ***tool kit of fabrication methods*** for a range of devices.

After the course the student should be able to

describe the technological processes involved in the fabrication of nano- and microelectronic devices and circuits

compare alternative fabrication methods

apply the knowledge to specific device requirements through careful ***selection*** among a number of choices

assess pros and cons of different fabrication methods

combine fabrication methods to ***develop*** complex process flows for functional devices and circuits in a range of applications (e.g. transistors, solar cells, optoelectronics...)

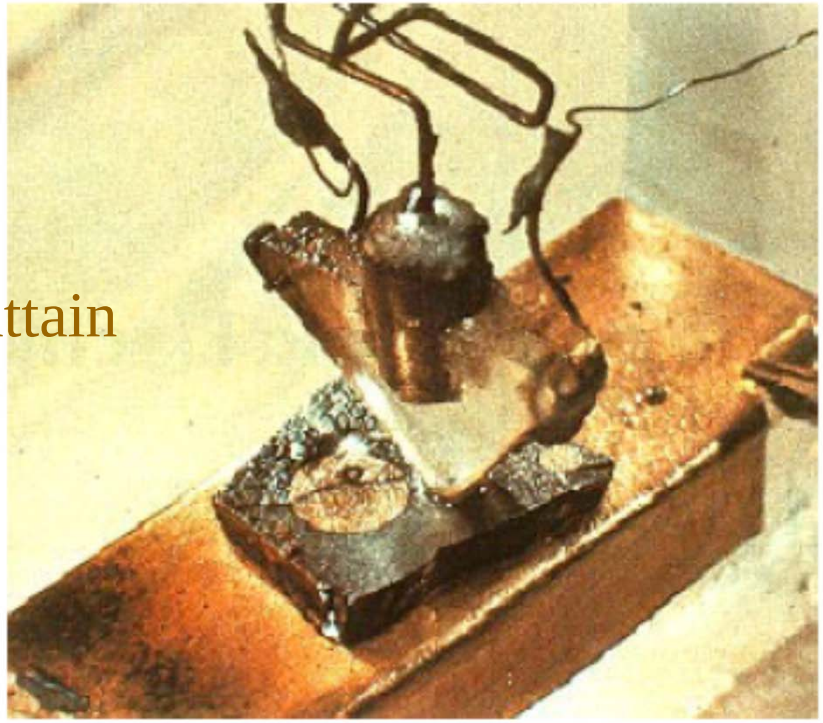
- Introduction to IH2655
- Brief historic overview
- Moore's Law and the ITRS Roadmap
- MOS Transistor (re-cap)
- From Geometrical to Material-based scaling
- CMOS Process Flow

Brief retrospect： A great invention based on Sciences

- **Bardeen, Brattain, Shockley**, First Ge-based bipolar transistor invented 1947, Bell Labs. **Nobel prize 1956**
- **Atalla**, First Si-based MOSFET invented 1958, Bell Labs.
- **Kilby** (TI) & **Noyce** (Fairchild), Invention of integrated circuits 1959, **Nobel prize**
- Planar technology, **Jean Hoerni**, Fairchild, 1960
- First CMOS invented early 1960's
- "**Moore**'s law" coined 1965, Fairchild
- **Dennard**, scaling rule presented 1974, IBM
- First Si technology roadmap published 1994, USA

Bardeen, Brattain, Shockley, First Ge-based bipolar transistor invented 1947, Bell Labs. **Nobel prize 1956**

1st point contact transistor -- by Bell Lab



(Reprinted with permission of Lucent Technologies).

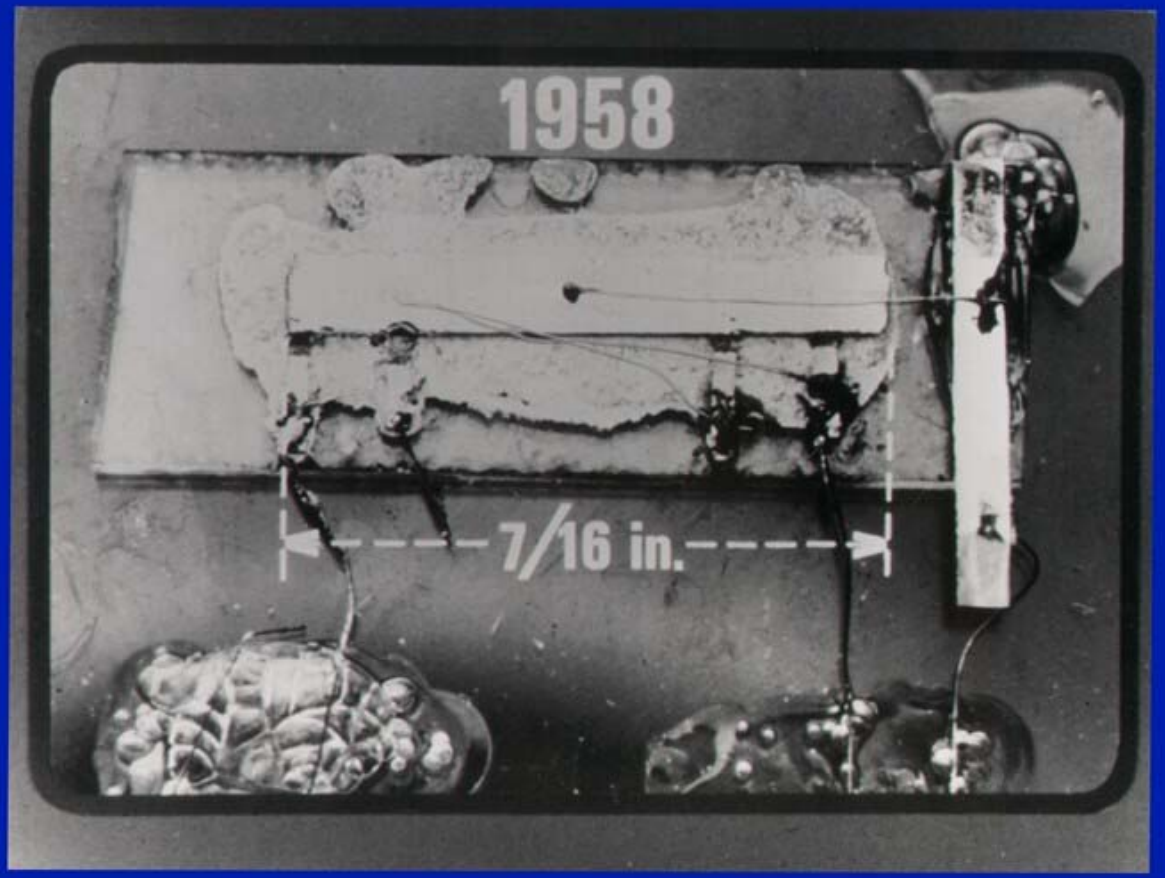
Polycrystalline Ge
1956 Nobel Physics Prize

Transistor=transfer + resistor
--Transferring electrical signal across a resistor

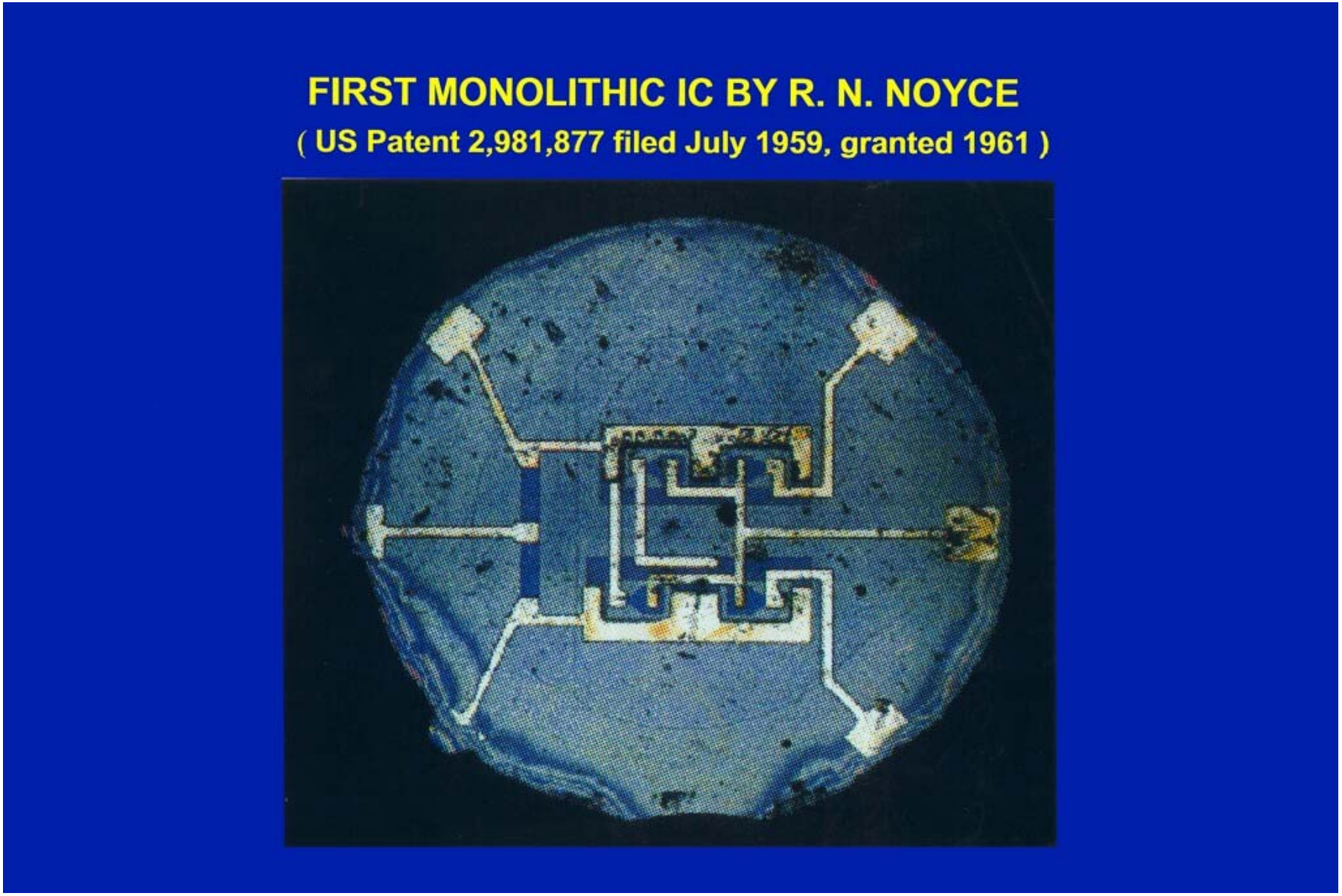
Kilby (TI) & **Noyce** (Fairchild), Invention of integrated circuits 1959, **Nobel prize**

FIRST INTEGRATED CIRCUIT BY J. S. KILBY

(US Patent 3,138,763 filed Feb. 1959, granted 1964)



Kilby (TI) & **Noyce** (Fairchild), Invention of integrated circuits 1959, **Nobel prize**



This marked the start of an amazing development -> Increasing integration of components

Planar technology, **Jean Hoerni**, Fairchild, 1960

Planar process

Invented by Jean Hoerni at Fairchild Semiconductor (late 50's)

April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 2

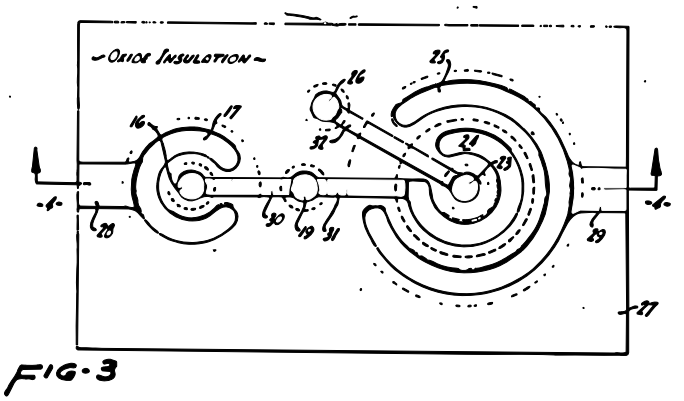


FIG. 3

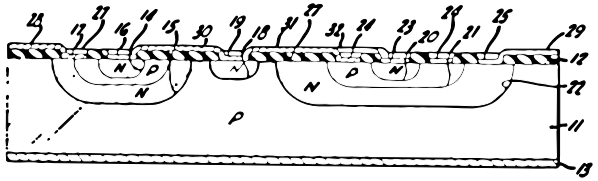


FIG. 4

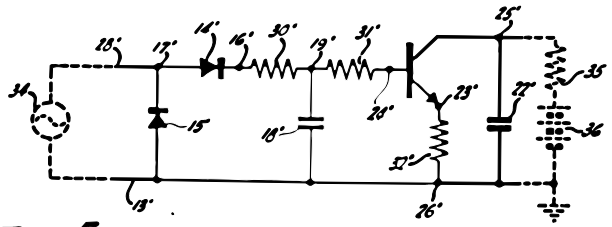


FIG. 5

INVENTOR.
ROBERT N. NOYCE
BY Lippincott & Ralls

Dennard, scaling rule presented 1974, IBM

NMOS technology

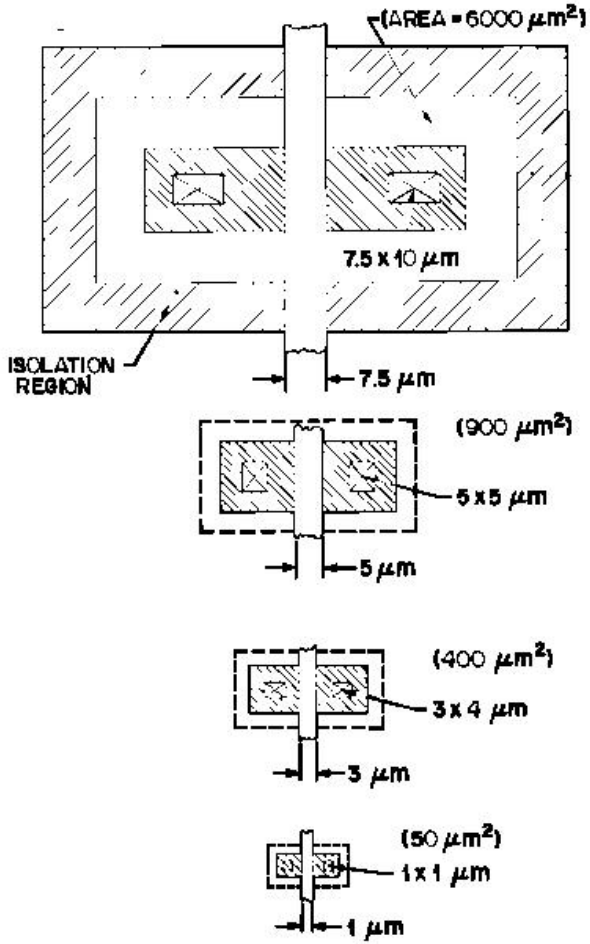


Fig. 13 Reduction in the area of MOSFET as the gate length (minimum feature length) is reduced.[9]

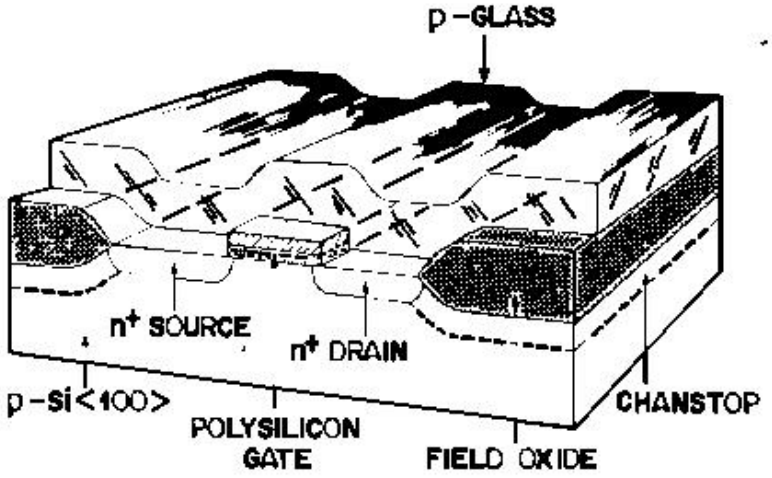


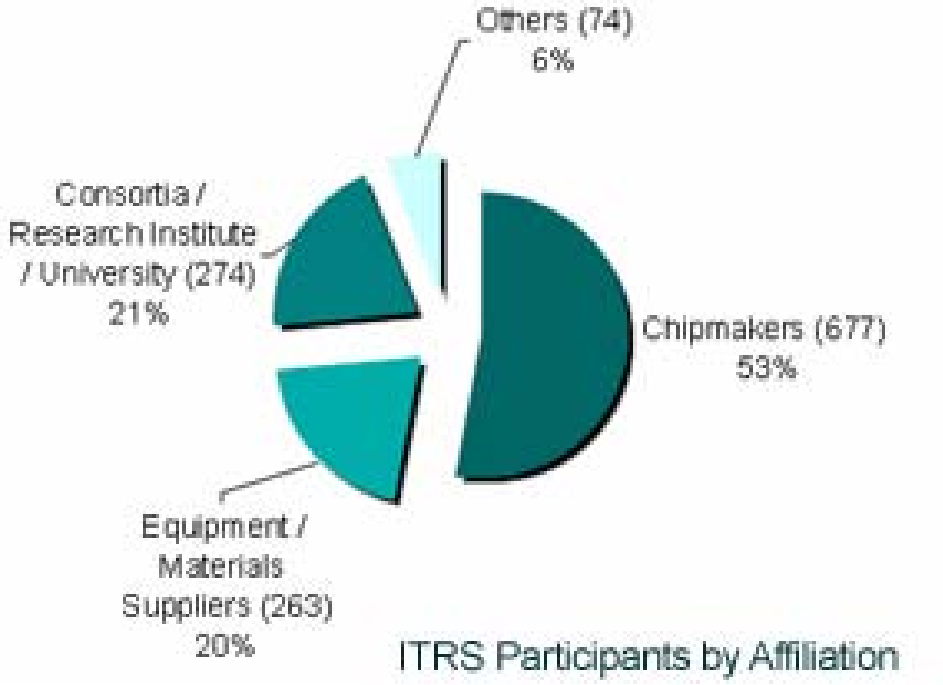
Fig. 14 Perspective view of an *n*-channel MOSFET.[9]

First Si technology roadmap published 1994, USA

Started by Semiconductor Industry Association (SIA) in USA
1994: creation of an American style roadmap
The National Technology Roadmap for Semiconductors (NTRS)

1998, the SIA became closer to its European, Japanese, Korean and Taiwanese counterparts by creating the first global roadmap
The International Technology Roadmap for Semiconductors (ITRS).

Today: Over 1000 companies and research institutions



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- System Drivers
- Design
- Test & Test Equipment
- Process Integration, Devices, & Structures
- RF and A/MS Technologies for Wireless Communications
- Emerging Research Devices
- Emerging Research Materials
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly & Packaging
- Environment, Safety, & Health
- Yield Enhancement
- Metrology
- Modeling & Simulation

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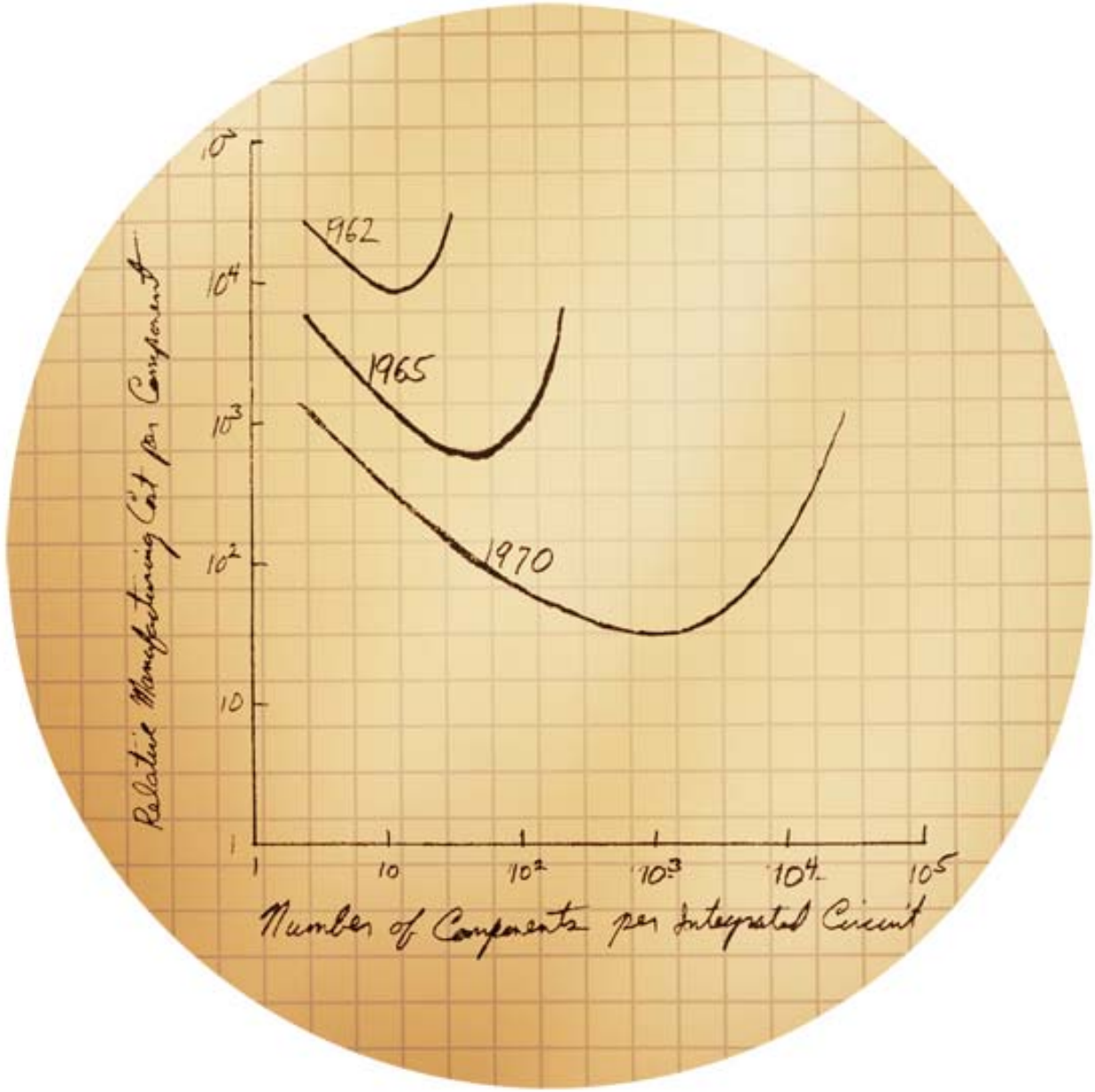
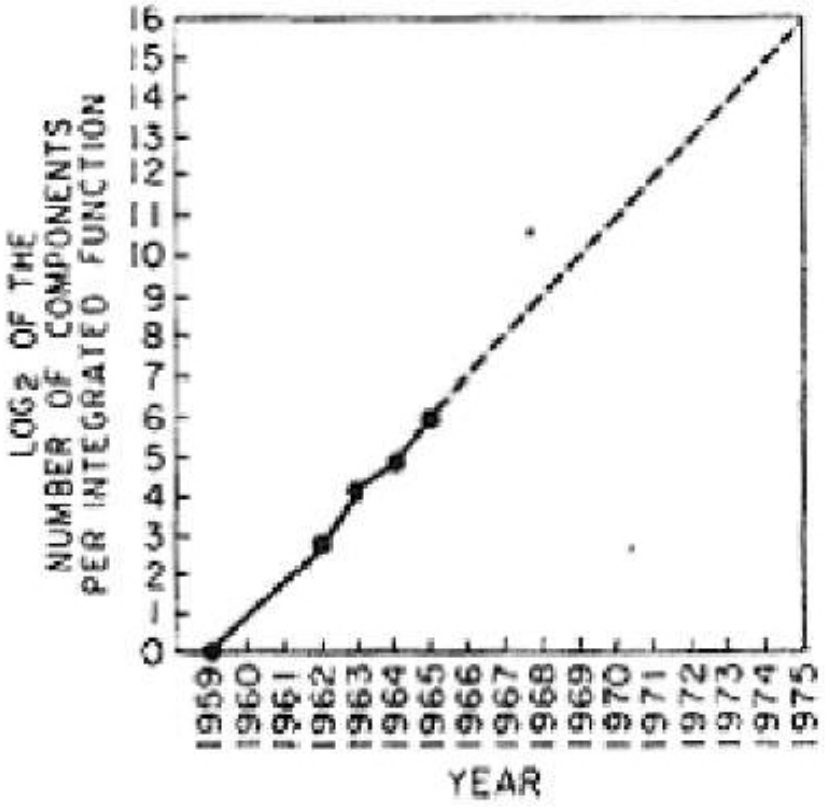
“**Moore**’s law”: coined 1965, Fairchild

Gordon Moore’s original Ideas in 1965

Source; Intel



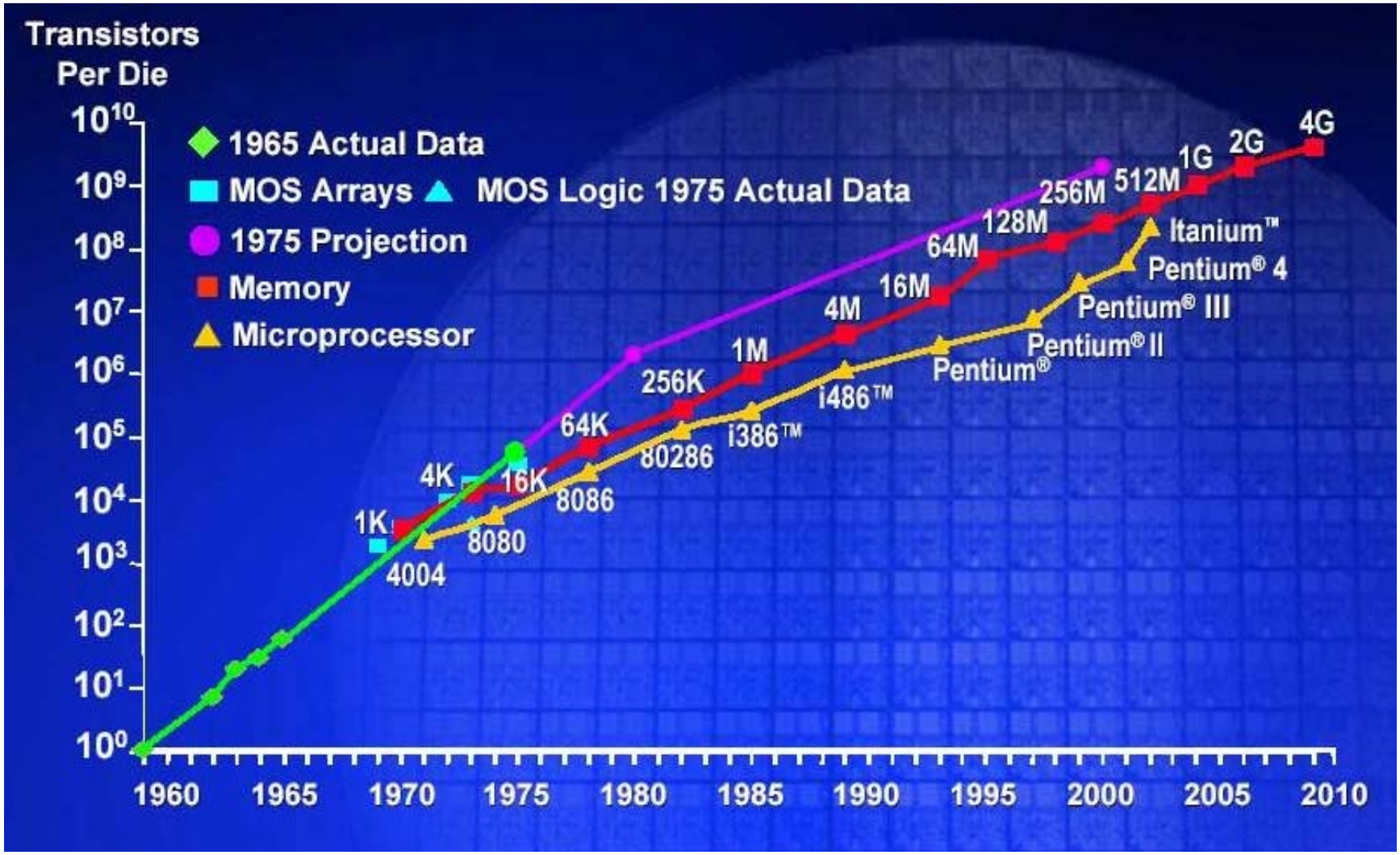
“**Moore**’s law”: coined 1965, Fairchild



1965: Components per „integrated function“

Source: G.E. Moore, Cramming more components onto integrated circuits, Electronics, Volume 38, Number 8, April 19, 1965

“**Moore**’s law”: rewritten in 1975, INtel



1975: Transistors per chip. Basis: Exponential behavior…

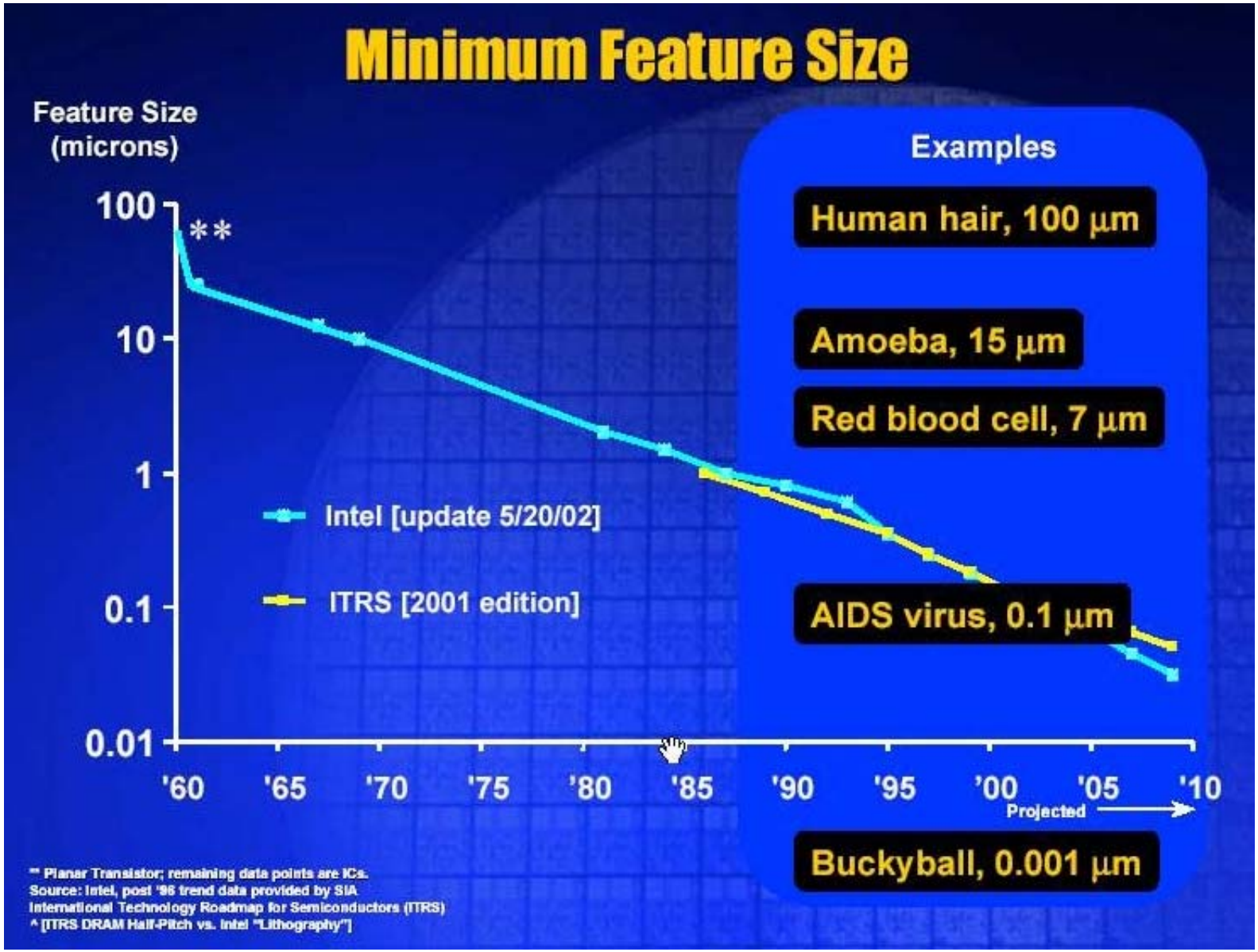
Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

“**Moore**’s law”: the real motivation

... Driven by $$$...

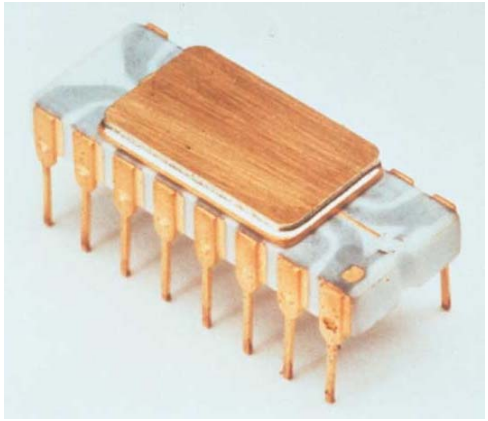
Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

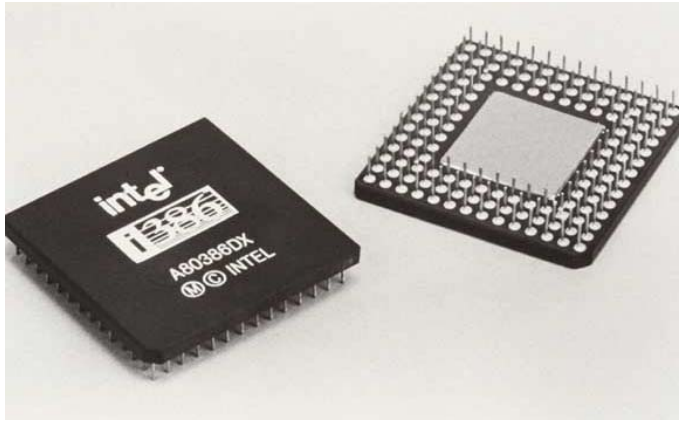
“**Moore**’s law”: enabled by scaling



Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

“**Moore**’s law”: enabled by scaling

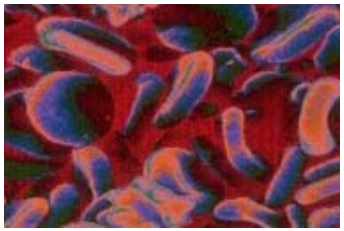


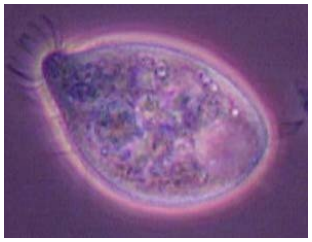


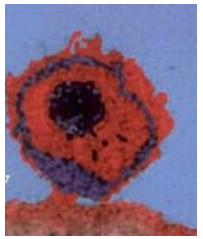
4004 386 Pentium 4

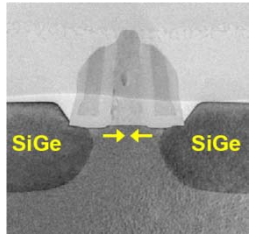
10 µm **1 µm** **0.1 µm**

Human hair **Red blood cell** **Bacteria** **Virus** **MOSFET**









“**Moore**’s law”: enabled by scaling

MOSFET metrics provide additional advantage

A simple model for I_{Don} is given by the MOSFET ***“Square-Law” Equation:***

$$\mathbf{I_{Don} = (W/L)\ (\mu\varepsilon_{ox}/t_{ox})\ (V_{GS} - V_T)^2}$$

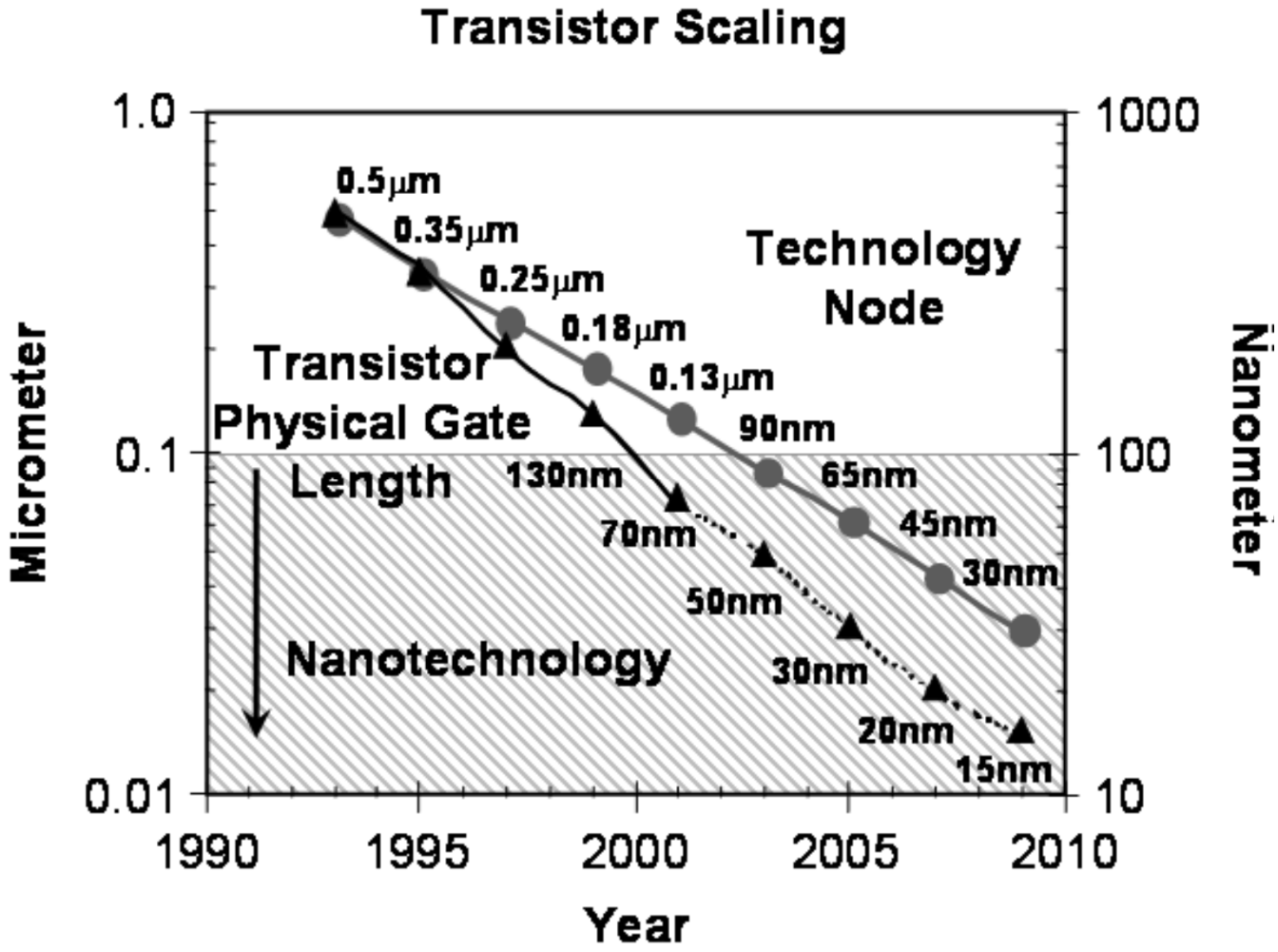
Chips are faster if the gate length L is reduced

“**Moore**’s law”: enabled by scaling

IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 4, NO. 2, MARCH 2005 , p153

Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications

Robert Chau *et al*

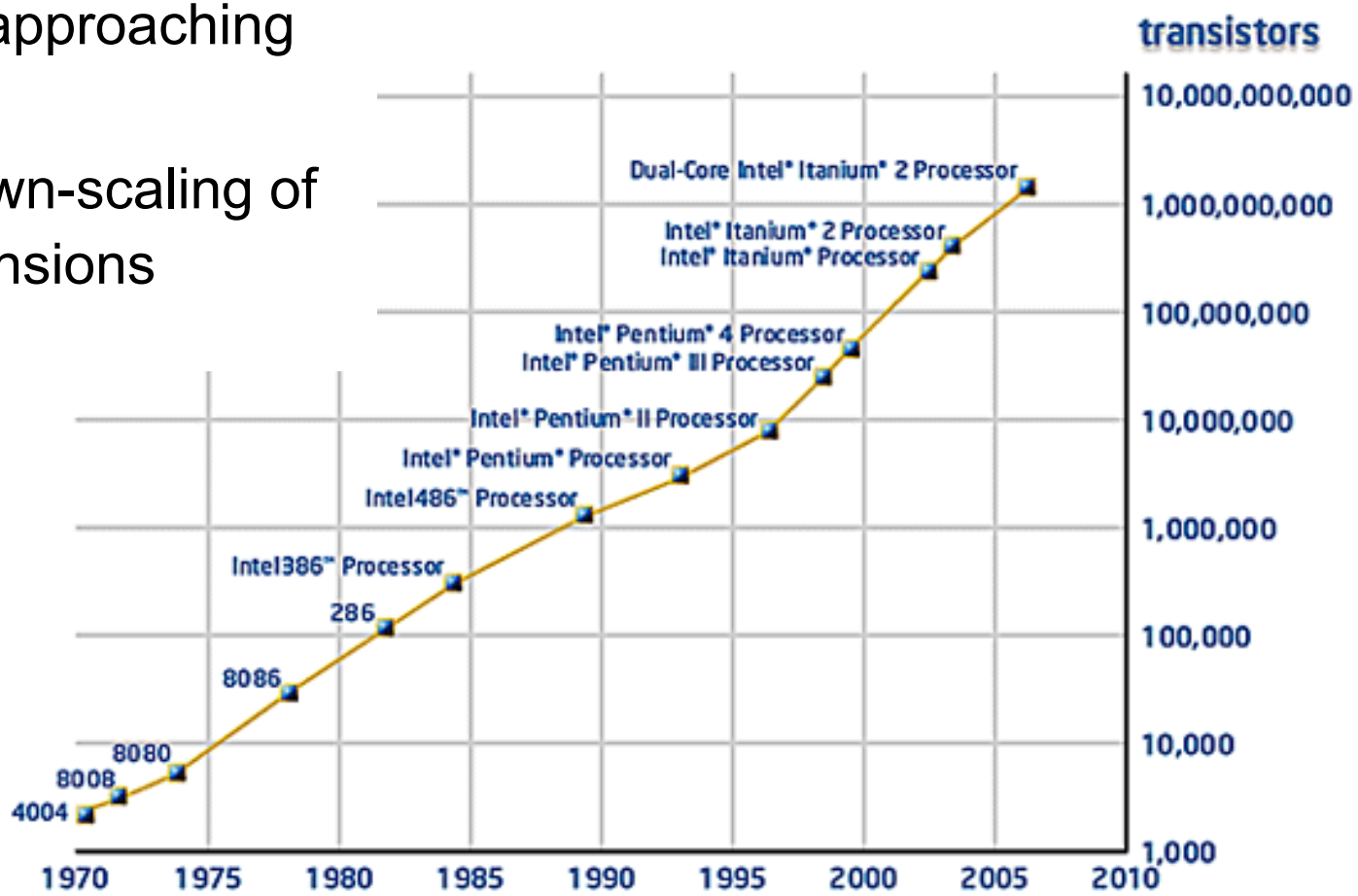


“**Moore**’s law”: still going strong in 2010

Transistors are found in processors, memories etc.

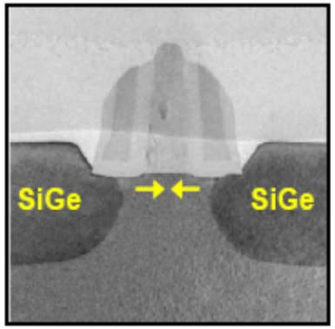
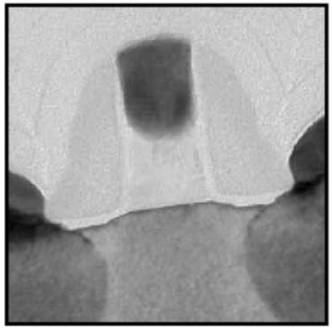
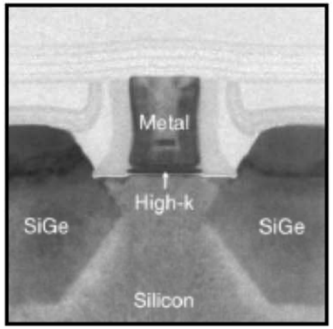
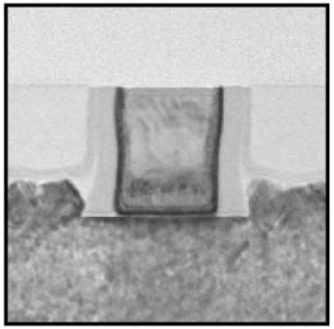
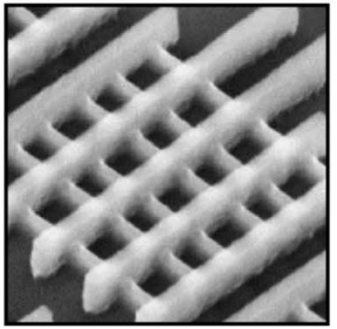
Number of transistors grows exponentially, approaching 1,000,000,000!

Continuous down-scaling of transistor dimensions



Source: Intel

Intel Transistor Leadership

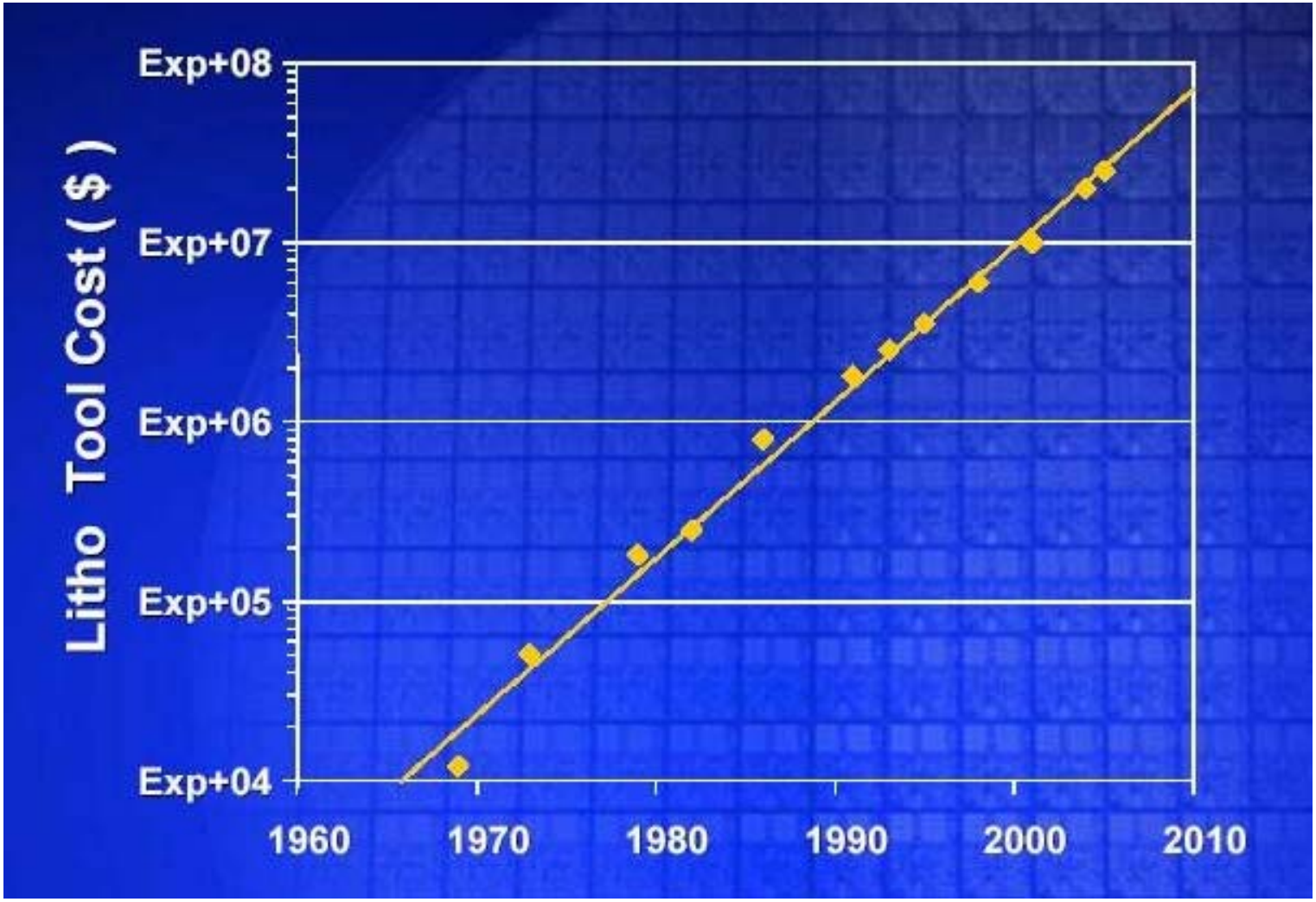
2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm
				
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon

High-k Metal Gate

Tri-Gate

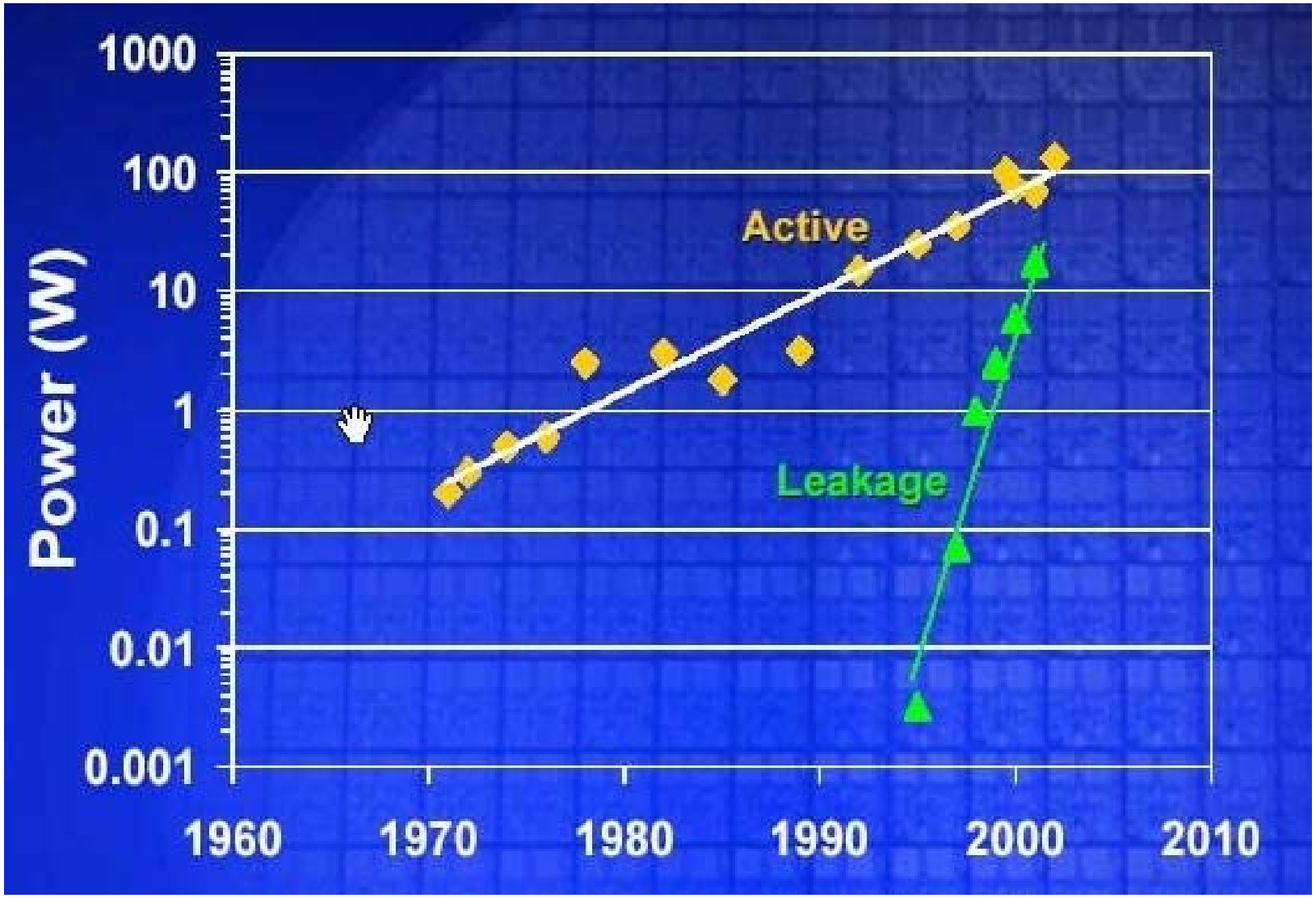
“**Moore**’s law”: However! (or: The notorious „e“)



Costs are rising exponentially, too!!!

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

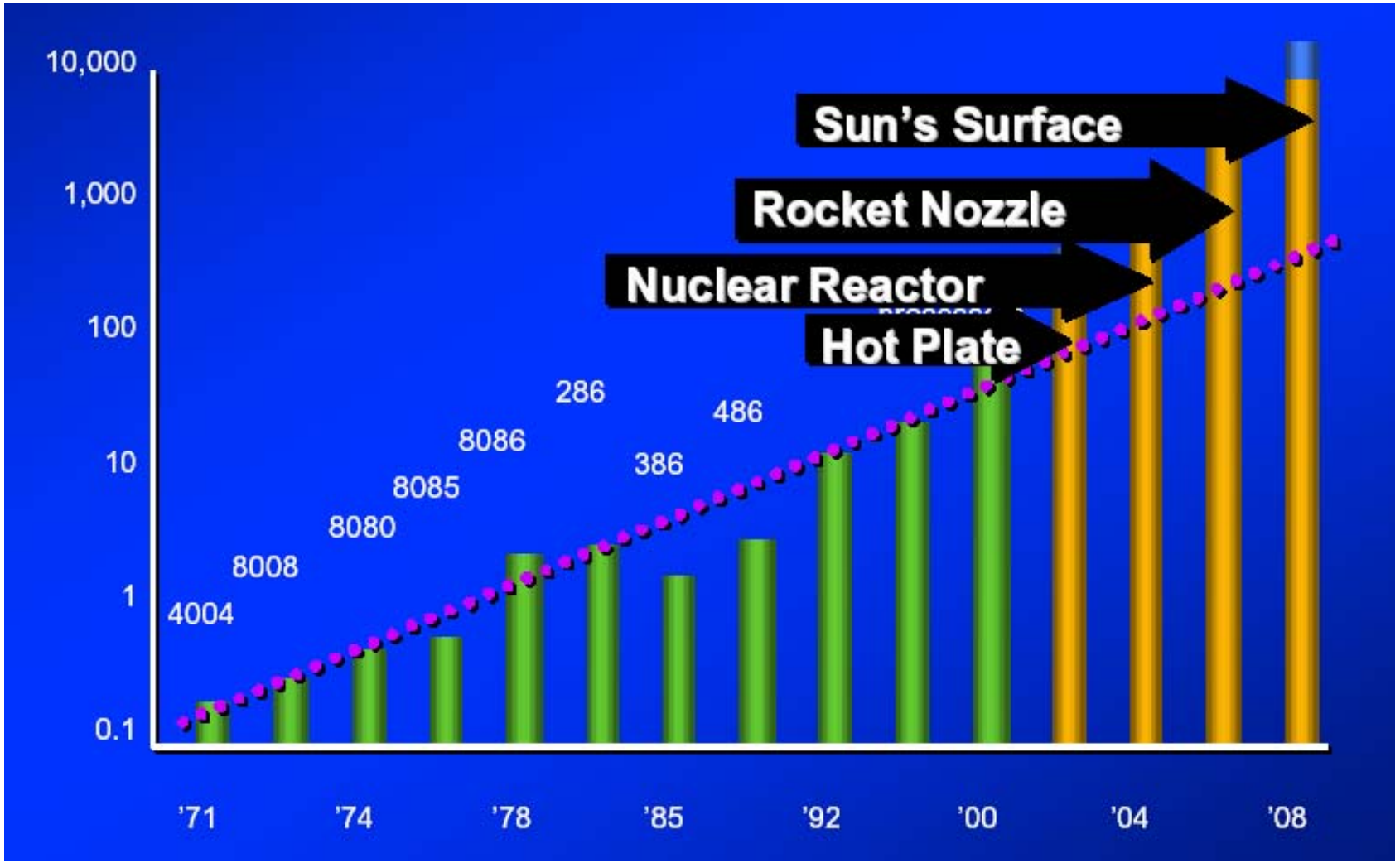
"**Moore**'s law": …and its consequences



…limited by power dissipation ???

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

“**Moore**’s law”: …and its consequences



Yes, if P continues exponentially !

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

“**Moore**’s law”: …not

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

ITRS Roadmap – Moore's Heirs

Started by Semiconductor Industry Association (SIA) in USA
1994: creation of an American style roadmap
The National Technology Roadmap for Semiconductors (NTRS)

1998, the SIA became closer to its European, Japanese, Korean and Taiwanese counterparts by creating the first global roadmap
The International Technology Roadmap for Semiconductors (ITRS).

Today: Over 1000 companies and research institutions
Teams for:

- System Drivers
- Design
- Test & Test Equipment
- Process Integration, Devices, & Structures
- RF and A/MS Technologies for Wireless Communications
- Emerging Research Devices
- Emerging Research Materials
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly & Packaging
- Environment, Safety, & Health
- Yield Enhancement
- Metrology
- Modeling & Simulation

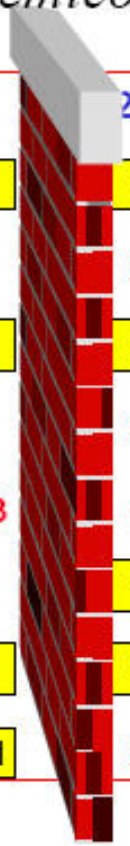
ITRS Roadmap

Moving Closer to the "Red Brick Wall"

2001 Results

Challenges/Opportunities for Semiconductor R&D

Year of Production:	2001	2003	2005	2007	2010	2016
DRAM Half-Pitch [nm]:	130	100	80	65	45	22
Overlay Accuracy [nm]:	46	35	28	23	18	9
MPU Gate Length [nm]:	90	65	45	35	25	13
CD Control [nm]:	8	5.5	3.9	3.1	2.2	1.1
T_{ox} (equivalent) [nm]:	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.5
Junction Depth [nm]:	48-95	33-66	24-47	18-37	13-26	7-13
Metal Cladding [nm]:	16	12	9	7	5	2.5
Inter-Metal Dielectric K:	3.0-3.6	3.0-3.6	2.6-3.1	2.3-2.7	2.1	1.8



2001 ITRS ITRS *IRC*

- Introduction to IH2655
- Brief historic overview
- Moore’s Law and the ITRS Roadmap
- MOS Transistor (re-cap)
- From Geometrical to Material-based scaling
- CMOS Process Flow

Long-channel MOSFETs

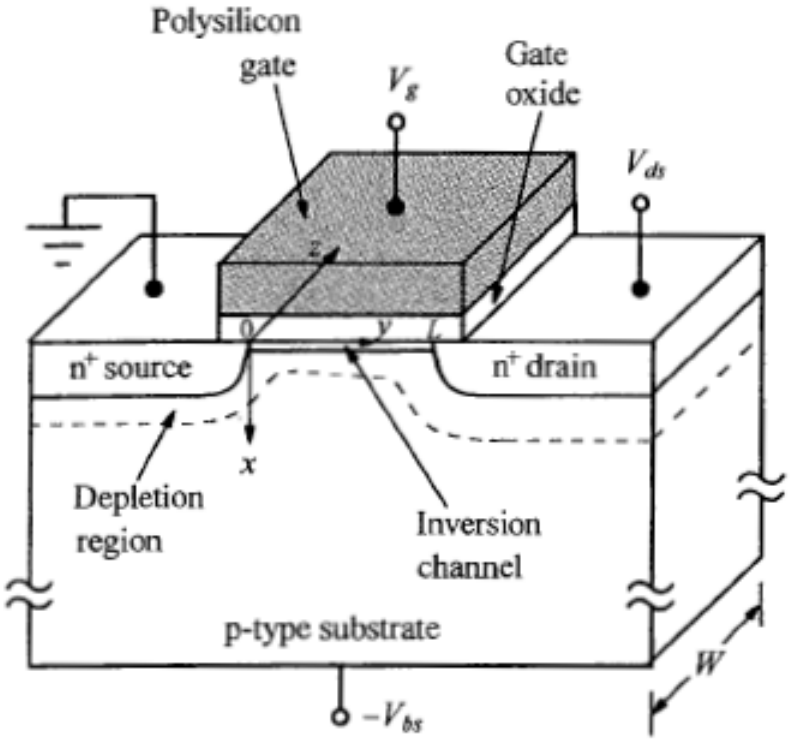


FIGURE 3.2. A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model.

MOSFET I-V characteristics

Linear region (small values of V_{ds}):

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \left(V_g - V_{fb} - 2\psi_B - \frac{\sqrt{4\varepsilon_{si} q N_a \psi_B}}{C_{ox}} \right) V_{ds}$$

$$= \mu_{eff} C_{ox} \frac{W}{L} (V_g - V_t) V_{ds},$$

$$V_t = V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{si} q N_a \psi_B}}{C_{ox}}.$$

$$V_t = V_{fb} + (2m - 1)\, 2\psi_B.$$

MOSFET I-V characteristics

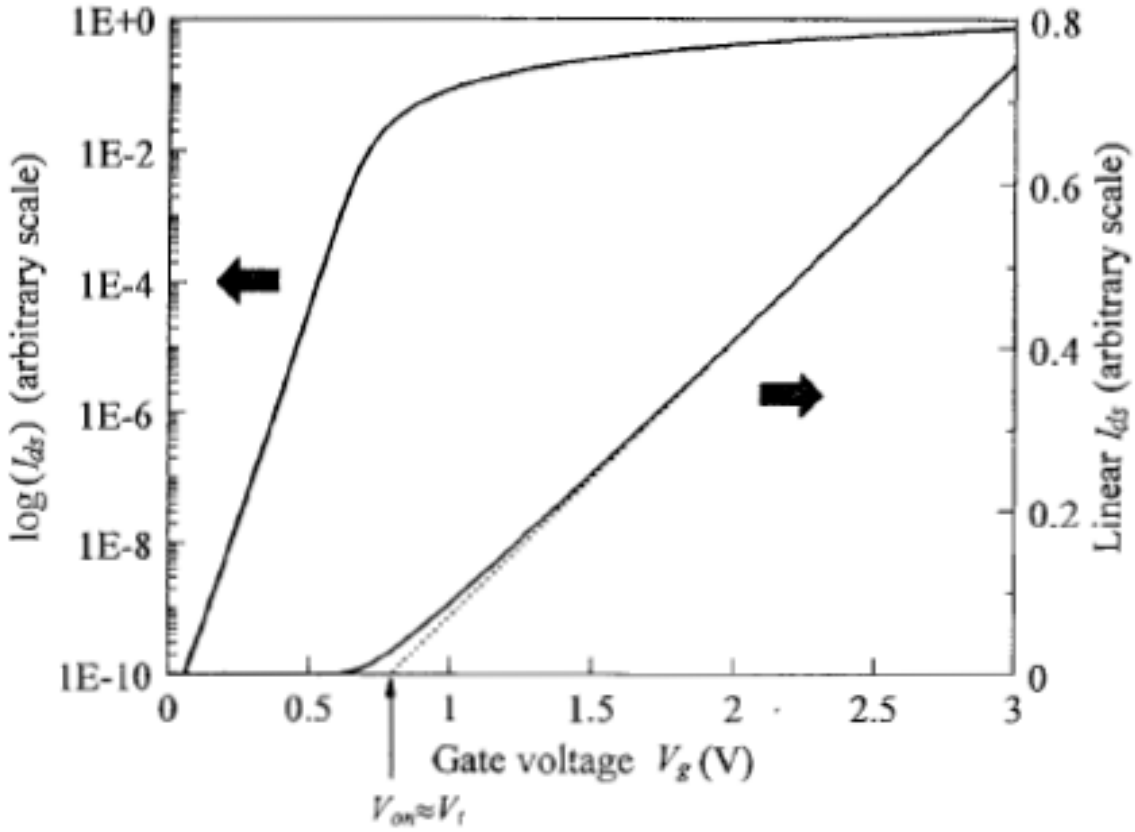


FIGURE 3.3. Typical MOSFET I_{ds}–V_g characteristics at low drain bias voltages. The same current is plotted on both linear and logarithmic scales. The dotted line illustrates the determination of the linearly extrapolated threshold voltage, V_{on}.

MOSFET I-V characteristics

Saturation region (V_{ds} larger than V_{dsat}):

$$I_{ds} = I_{dsat} = \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_g - V_t)^2}{2m}.$$

$$m = 1 + \frac{\sqrt{\varepsilon_{si} q N_a / 4\psi_B}}{C_{ox}} = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{3t_{ox}}{W_{dm}}$$

MOSFET I-V characteristics

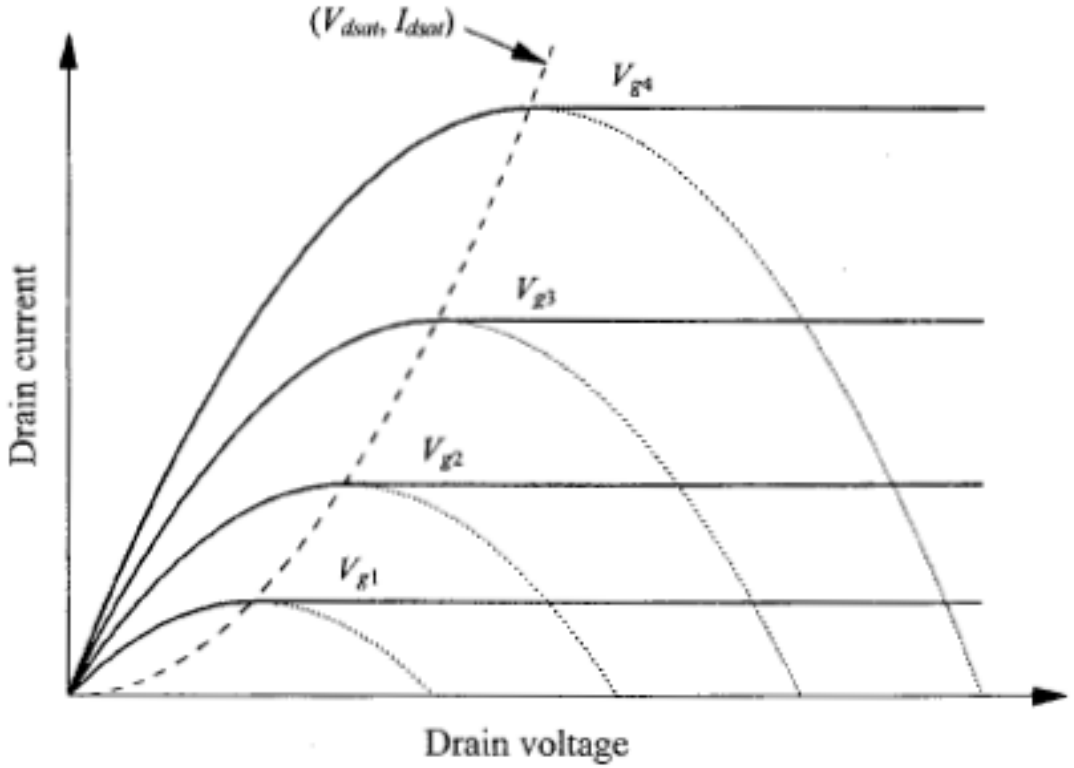


FIGURE 3.4. Long-channel MOSFET I_{ds}–V_{ds} characteristics (solid curves) for several different values of V_g. The dashed curve shows the trajectory of drain voltage beyond which the current saturates. The dotted curves help to illustrate the parabolic behavior of the characteristics before saturation.

MOSFET I-V characteristics

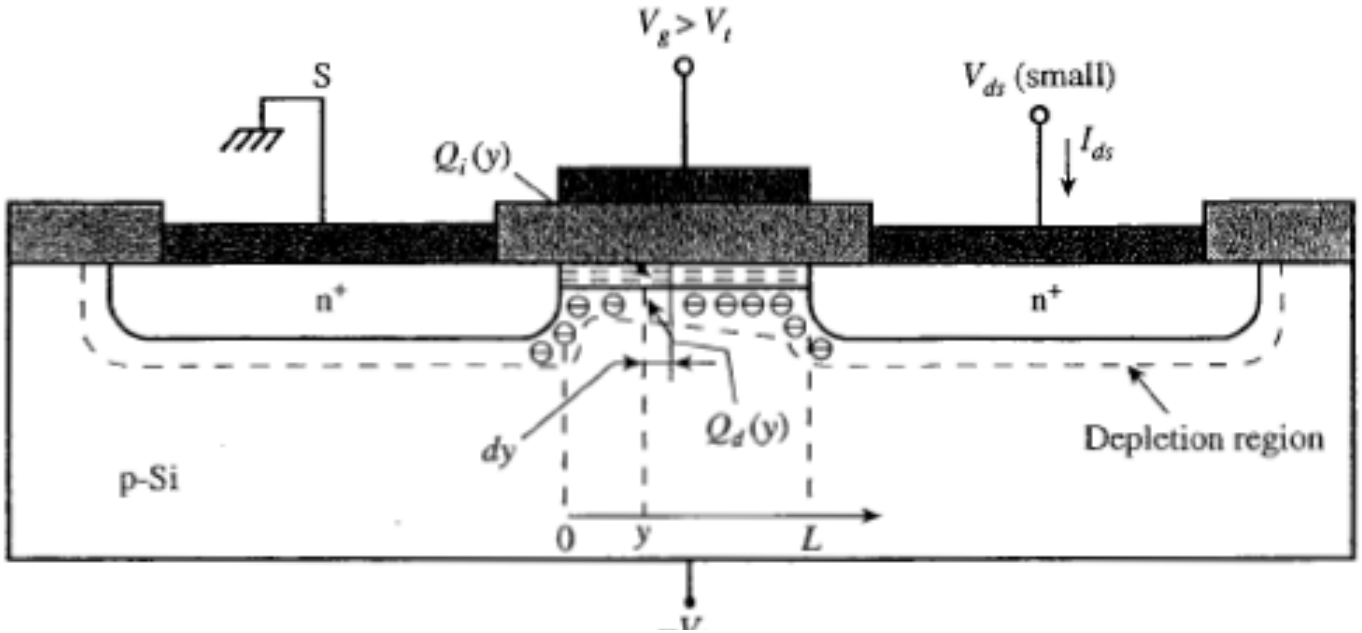
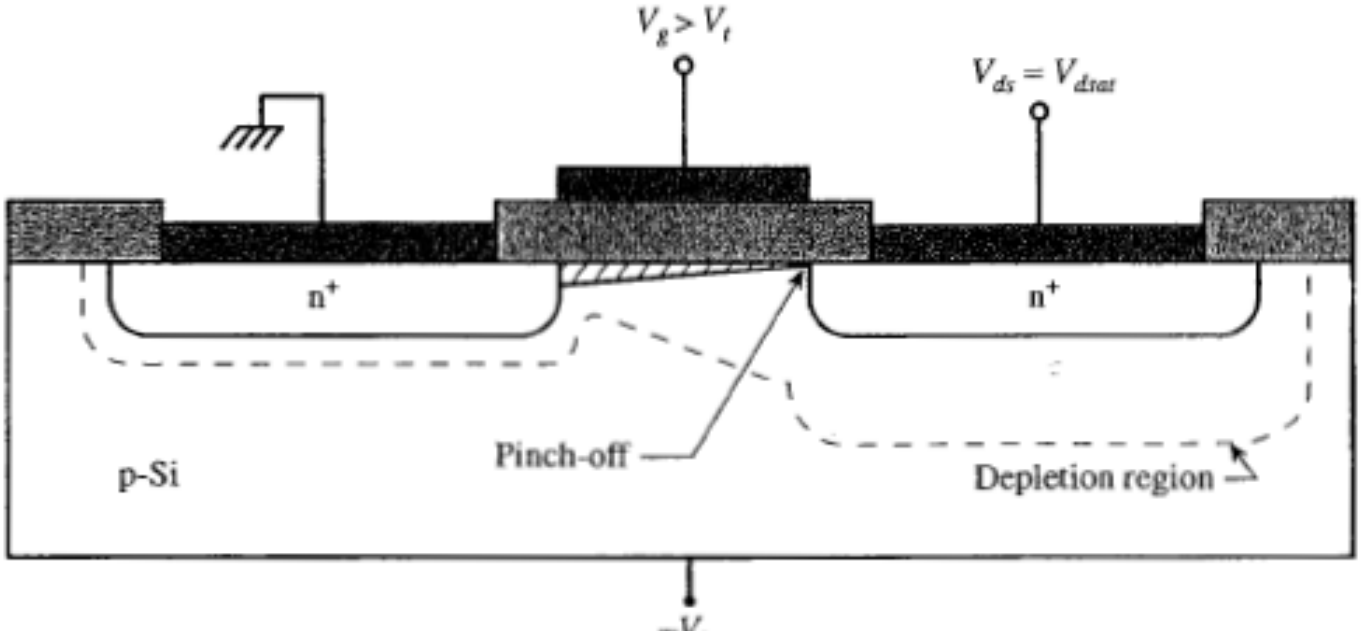


FIGURE 3.6. (a) MOSFET operated in the linear region (low drain voltage). (b) MOSFET operated at the onset of saturation. The pinch-off point is indicated by Y. (c) MOSFET operated beyond saturation where the channel length is reduced to L'. (After Sze, 1981.)

MOSFET I-V characteristics



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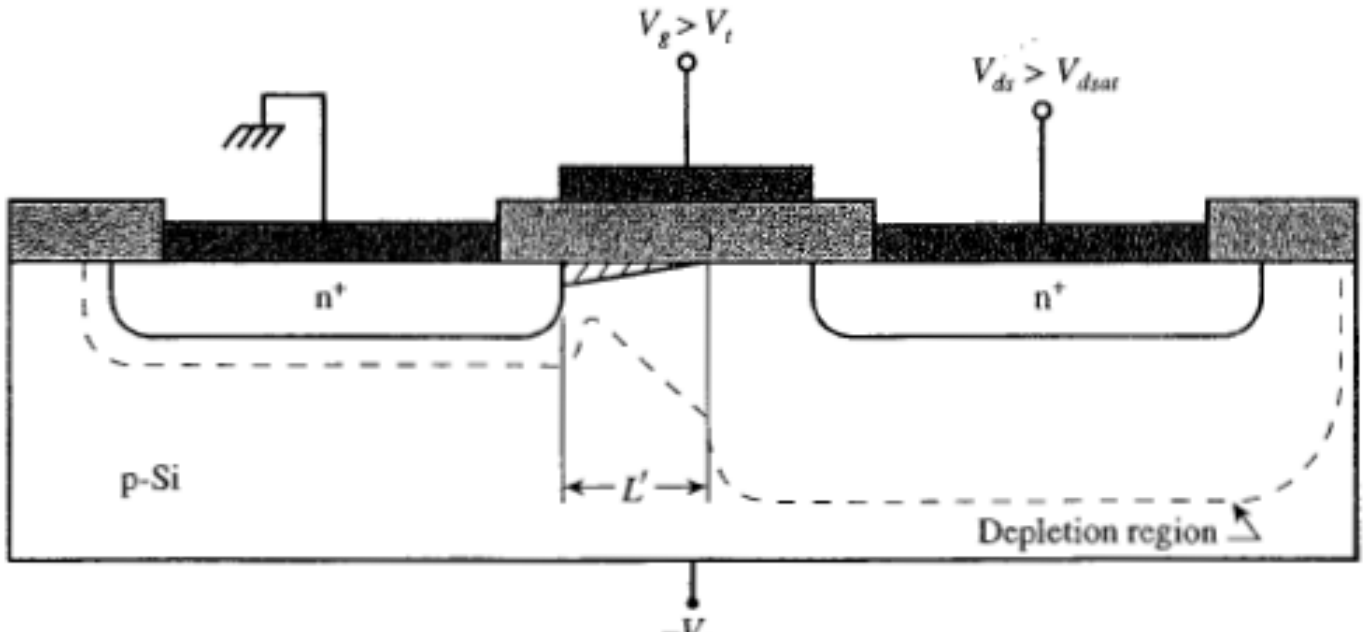
MOSFET I-V characteristics



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Subthreshold characteristics

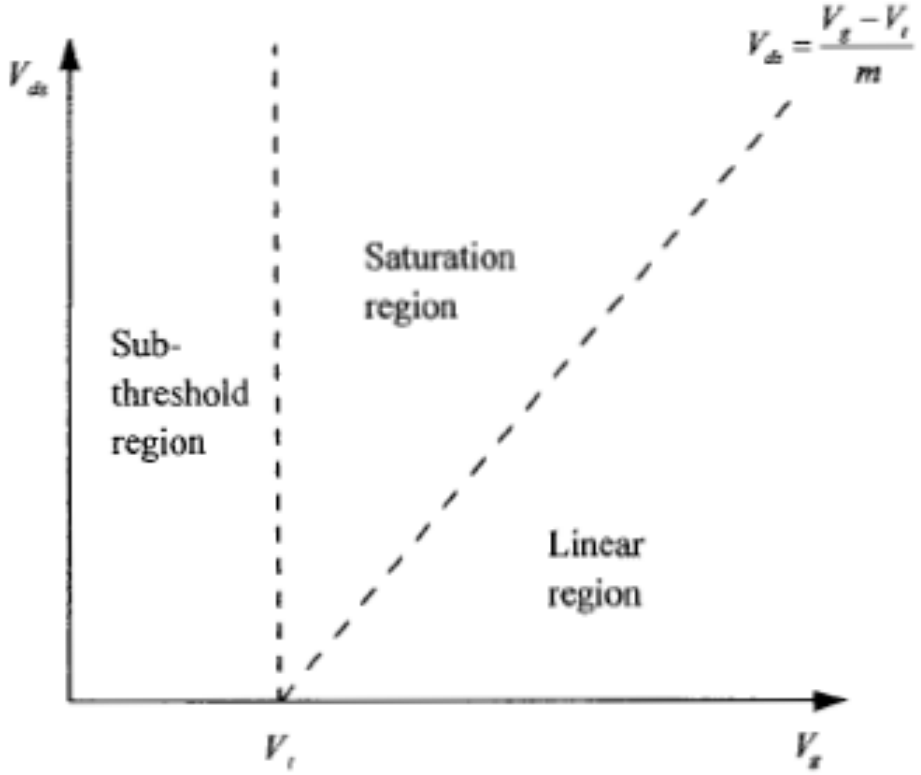


FIGURE 3.9. Three regions of MOSFET operation in the V_{ds}–V_g plane.

Subthreshold characteristics

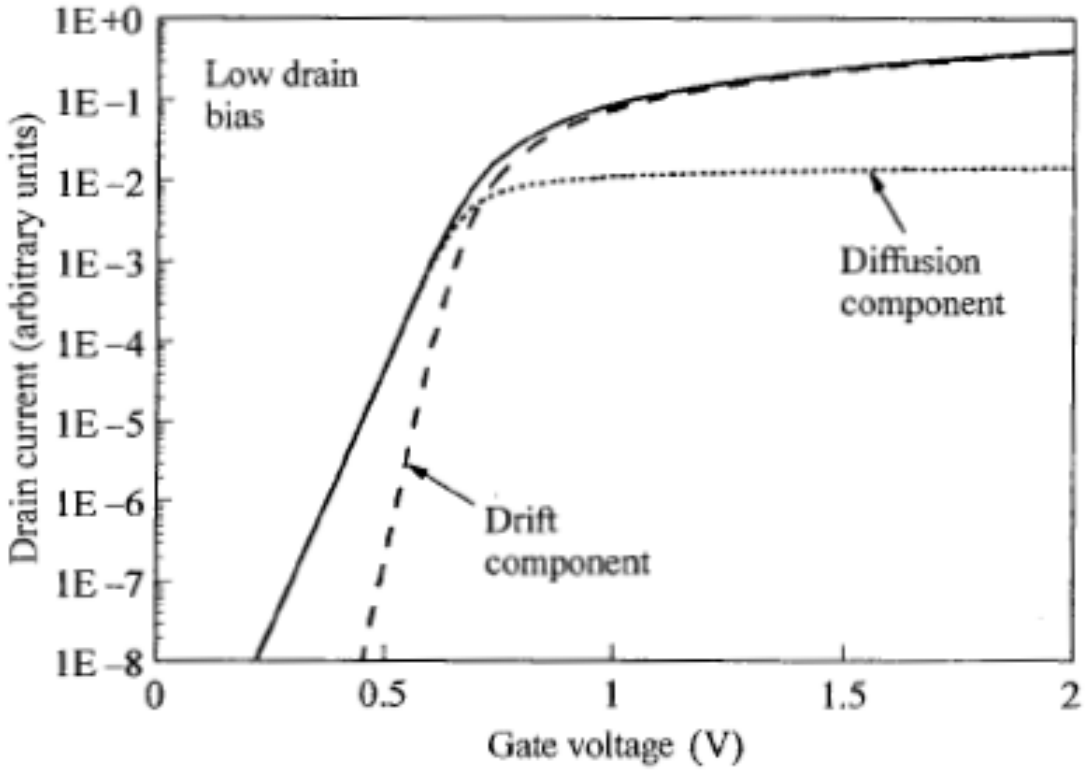


FIGURE 3.10. Drift and diffusion components of current in an I_{ds}–V_g plot. Their sum is the total current represented by the solid curve.

Subthreshold characteristics

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 e^{q(V_g - V_t)/mkT}(1 - e^{-qV_{ds}/kT}).$$

3.1.3.3 SUBTHRESHOLD SLOPE

The subthreshold current is independent of the drain voltage once V_{ds} is larger than a few kT/q, as would be expected for diffusion-dominated current transport. The dependence on gate voltage, on the other hand, is exponential with a *subthreshold slope* (Fig. 3.10),

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g}\right)^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right), \qquad (3.37)$$

of typically 70–100 mV/decade. Here $m = 1 + (C_{dm}/C_{ox})$ from Eq. (3.22).

Channel mobility

3.1.5.1 EFFECTIVE MOBILITY AND EFFECTIVE NORMAL FIELD

In Section 3.1.1, the channel mobility was treated as a constant by defining an effective mobility as

$$\mu_{eff} = \frac{\int_0^{x_i} \mu_n n(x)\,dx}{\int_0^{x_i} n(x)\,dx}, \tag{3.46}$$

which is essentially an average value weighted by the carrier concentration in the inversion layer. Empirically, it has been found that ***when μ_{eff} is plotted against an effective normal field $\mathscr{E}_{eff}$, there exists a universal relationship independent of the substrate bias, doping concentration, and gate oxide thickness***

Channel mobility

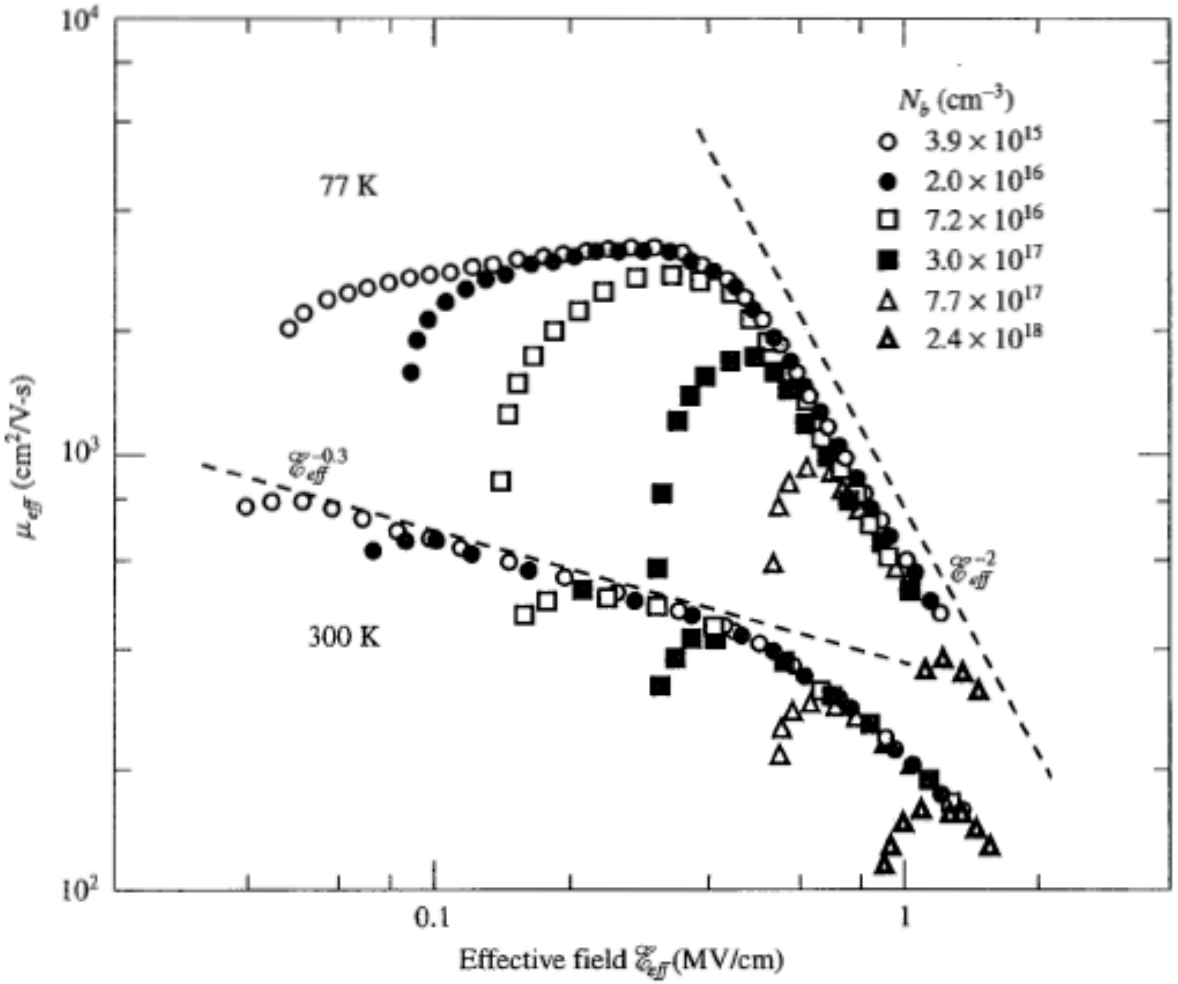


FIGURE 3.13. Measured electron mobility at 300 and 77 K versus effective normal field for several substrate doping concentrations. (After Takagi *et al.*, 1988).

Channel mobility

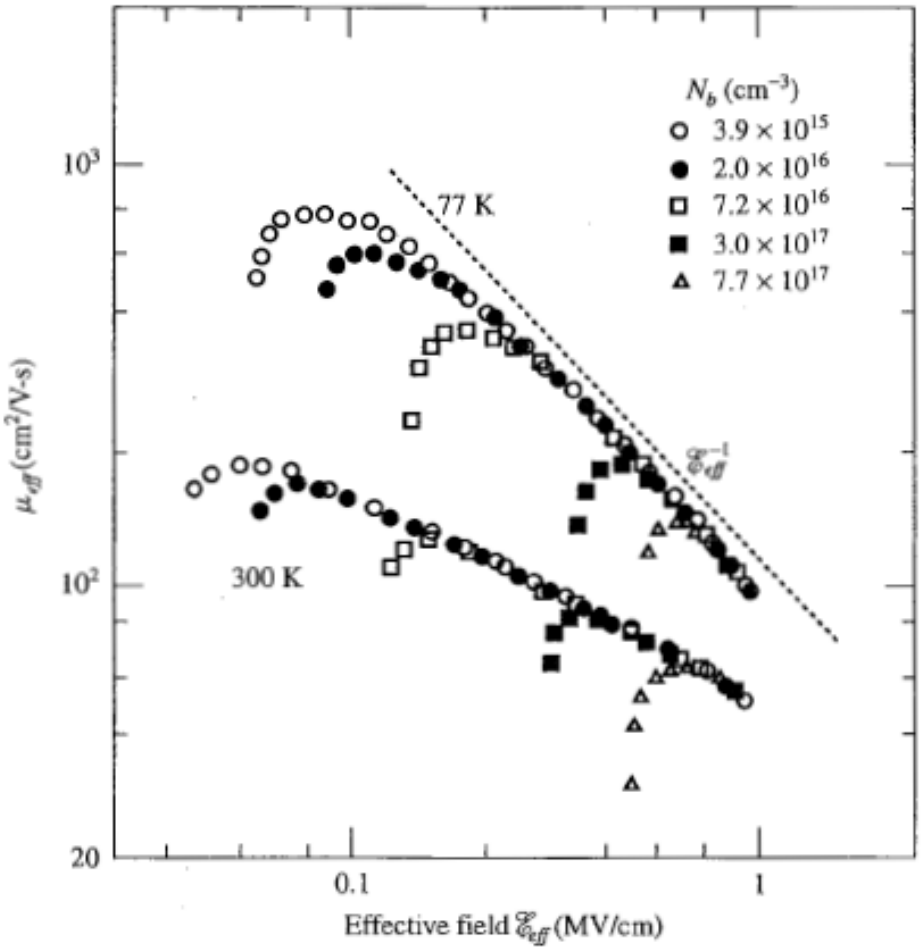


FIGURE 3.14. Measured hole mobility at 300 K and 77 K versus effective normal field (with a factor $\frac{1}{3}$) for several substrate doping concentrations. (After Takagi *et al.*, 1988).

Short-channel effect (SCE)

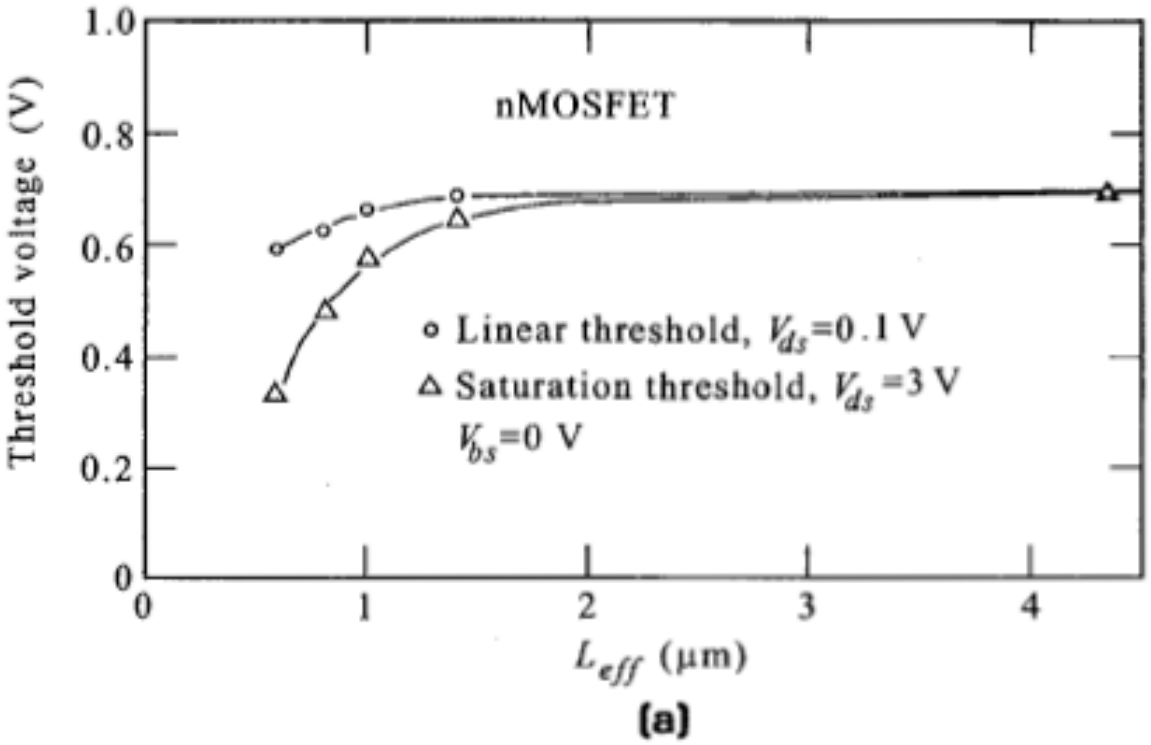


FIGURE 3.17. Short-channel threshold roll-off: Measured low- and high-drain threshold voltages of n- and p-MOSFETs versus channel length. (After Taur *et al.*, 1985.)

Short-channel effect (SCE)

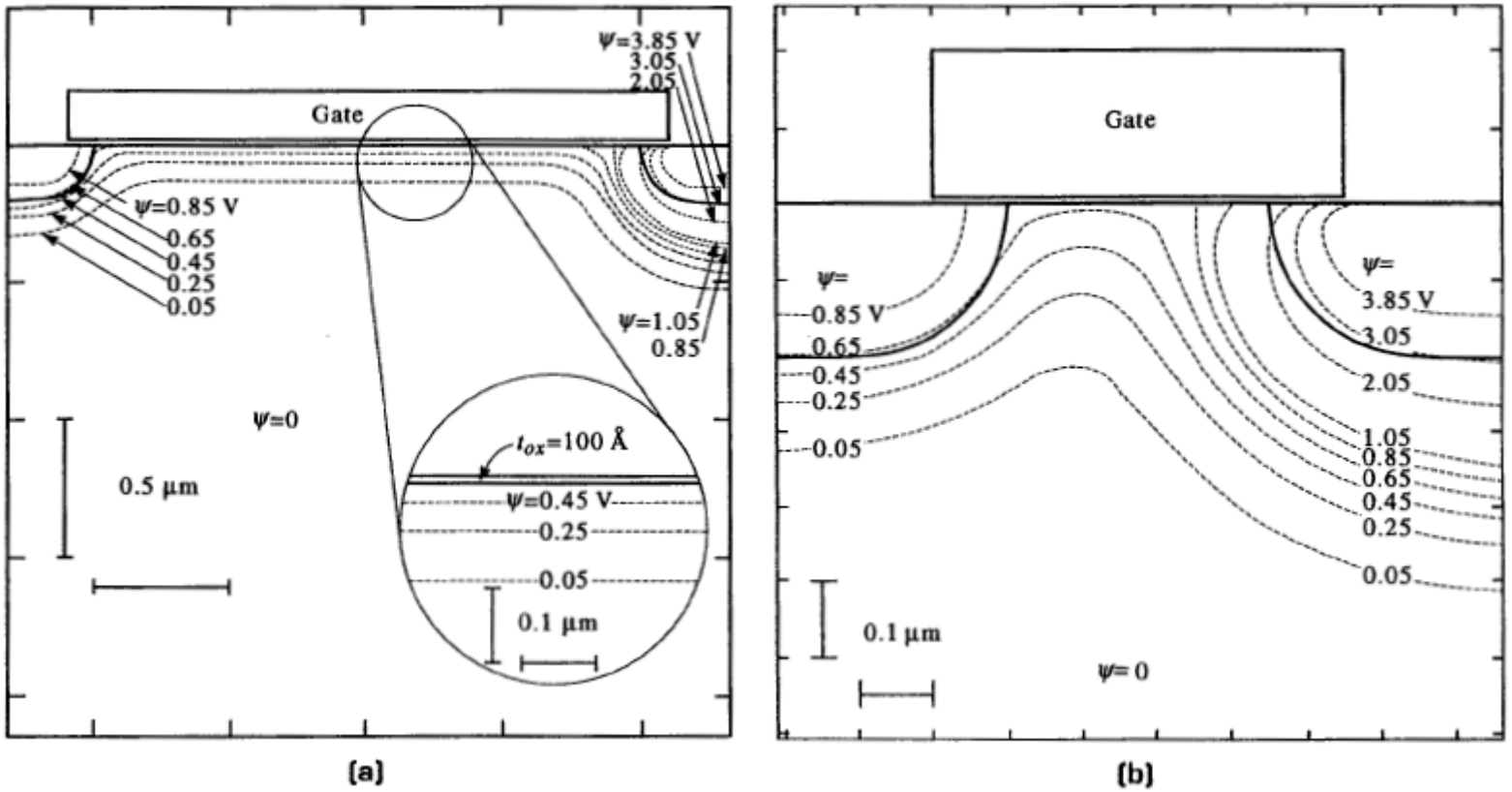


FIGURE 3.18. Simulated constant potential contours of (a) a long-channel and (b) a short-channel nMOSFET. The contours are labeled by the band bending with respect to the neutral p-type region. The solid lines indicate the location of the source and drain junctions (metallurgical). The drain is biased at 3.0 V. Both devices are biased at the same gate voltage slightly below the threshold.

Short-channel effect (SCE)

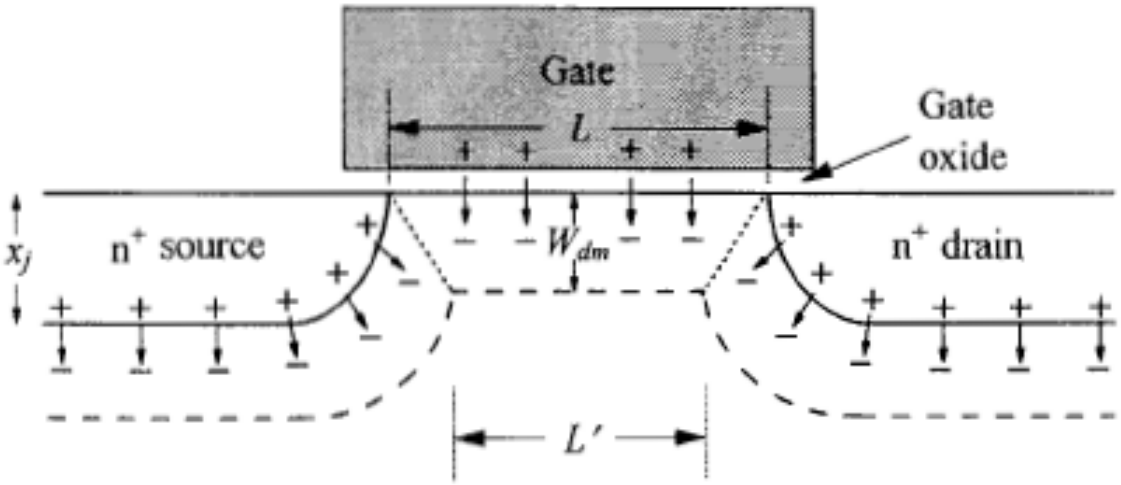


FIGURE 3.19. Schematic diagram of the charge-sharing model. The dashed lines indicate the boundary of the gate and source–drain depletion regions. The arrows represent electric field lines that originate from a positive charge and terminate on a negative charge. The dotted lines partition the depletion charge and form the two sides of the trapezoid discussed in the text. (After Yau, 1974.)

Constant-field scaling

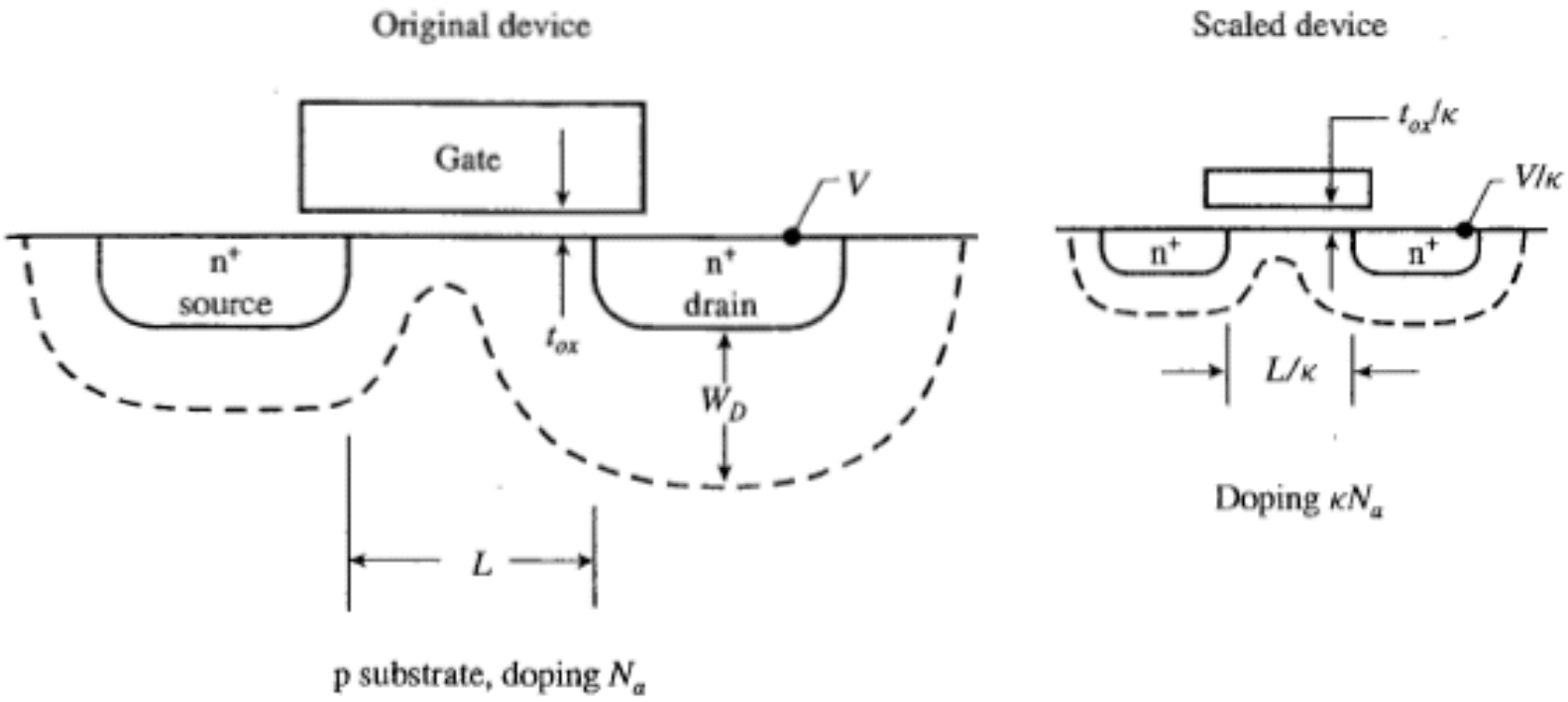


FIGURE 4.1. Principles of MOSFET constant-electric-field scaling. (After Dennard, 1986.)

Rules for constant-field scaling

TABLE 4.1 Scaling of MOSFET Device and Circuit Parameters

	MOSFET Device and Circuit Parameters	Multiplicative Factor ($\kappa > 1$)
Scaling assumptions	Device dimensions (t_{ox}, L, W, x_j)	$1/\kappa$
	Doping concentration (N_a, N_d)	κ
	Voltage (V)	$1/\kappa$
Derived scaling behavior of device parameters	Electric field ($\mathscr{E}$)	1
	Carrier velocity (v)	1
	Depletion-layer width (W_d)	$1/\kappa$
	Capacitance ($C = \varepsilon A/t$)	$1/\kappa$
	Inversion-layer charge density (Q_i)	1
	Current, drift (I)	$1/\kappa$
	Channel resistance (R_{ch})	1
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	$1/\kappa^2$
	Power–delay product per circuit ($P\tau$)	$1/\kappa^3$
	Circuit density ($\propto 1/A$)	κ^2
	Power density (P/A)	1

NOTE:
C_{ox} is F/cm^2

Rules for constant-field scaling

$$W_D = \sqrt{\frac{2\varepsilon_{si}(\psi_{bi} + V_{dd})}{qN_a}},$$

$$\frac{I_{drift}}{W} = Q_i v = Q_i \mu \mathscr{E},$$

$$I_{ds} = I_{dsat} = \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_g - V_t)^2}{2m}.$$

$$\frac{I_{diff}}{W} = D_n \frac{dQ_i}{dx} = \mu_n \frac{kT}{q} \frac{dQ_i}{dx},$$

Chapter 3

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 e^{q(V_g - V_t)/mkT} (1 - e^{-qV_{ds}/kT}).$$

$$V_t = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_{si} q N_a (2\psi_B + V_{bs})}}{C_{ox}},$$

Generalized scaling

TABLE 4.2 CMOS VLSI Technology Generations

Feature Size (μm)	Power-Supply Voltage (V)	Gate Oxide Thickness (Å)	Oxide Field (MV/cm)
2	5	350	1.4
1.2	5	250	2.0
0.8	5	180	2.8
0.5	3.3	120	2.8
0.35	3.3	100	3.3
0.25	2.5	70	3.6

Rules for generalized scaling

TABLE 4.3 Generalized MOSFET Scaling

	MOSFET Device and Circuit Parameters	Multiplicative Factor ($\kappa > 1$)	
Scaling assumptions	Device dimensions (t_{ox}, L, W, x_j)	$1/\kappa$	
	Doping concentration (N_a, N_d)	$\alpha\kappa$	
	Voltage (V)	α/κ	
Derived scaling behavior of device parameters	Electric field ($\mathscr{E}$)	α	
	Depletion-layer width (W_d)	$1/\kappa$	
	Capacitance ($C = \varepsilon A/t$)	$1/\kappa$	
	Inversion-layer charge density (Q_i)	α	
		Long Ch.	Vel. Sat.
	Carrier velocity (v)	α	1
	Current, drift (I)	α^2/κ	α/κ
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\alpha\kappa$	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	α^3/κ^2	α^2/κ^2
	Power–delay product per circuit ($P\tau$)	α^2/κ^3	
	Circuit density ($\propto 1/A$)	κ^2	
	Power density (P/A)	α^3	α^2

Nonscaling effects

Thermal voltage does not scale
=> subthreshold nonscaling

Bandgap does not scale
=> depletion layer does not scale

Voltage level not scaled (E increases)
=> mobility decreases

Higher electric field
=> higher power and lower reliability

Source/Drain doping can not be scaled
=> higher resistance

- Introduction to IH2655
- Brief historic overview
- Moore’s Law and the ITRS Roadmap
- MOS Transistor (re-cap)
- From Geometrical to Material-based scaling
- CMOS Process Flow

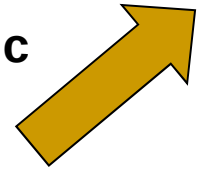
“**Moore**’s law”: scaling parameters

MOSFET metrics provide additional leverage: Materials

A simple model for I_{Don} is given by the MOSFET ***“Square-Law” Equation:***

$$\mathbf{I_{Don} = (W/L)\ (\mu\varepsilon_{ox}/t_{ox})\ (V_{GS} - V_T)^2}$$

geometric



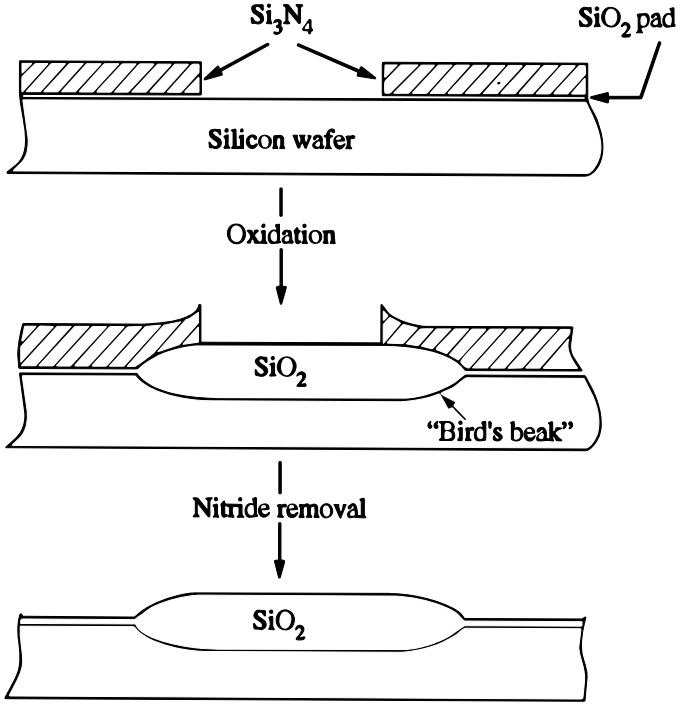
Gate length

Gate width

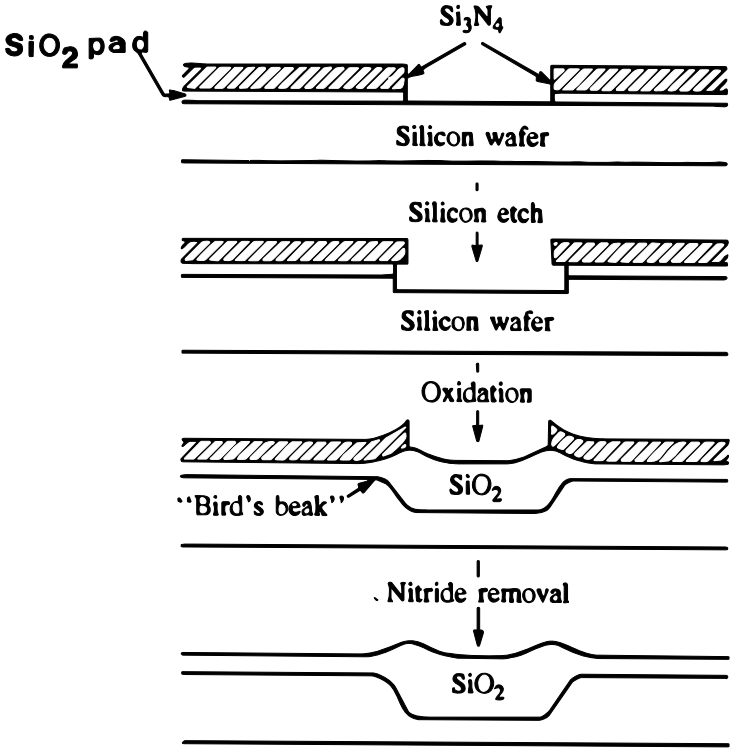
Geometric scaling is determined by improvements in process technology

Geometric Scaling: Isolation modules 1/2

LOCOS (semirecessed)



Recessed oxidation (ROX) (fully recessed)



Pros: **Improved geometric scalability**
Higher device density

Con: **Increased process complexity**

Geometric Scaling: Isolation modules 2/2

Bird's head and beak in LOCOS and ROX exhibit 0.6 –0.4 μm encroachment

Further process technology improvements

***Shallow Trench Isolation* (STI)**

- High-density plasma fills etched and liner-oxidixed trenches with SiO_2

Deep-trench isolation

- Trench isolation can be combined with silicon-on-insulator (SOI) wafers for nearly complete device isolation

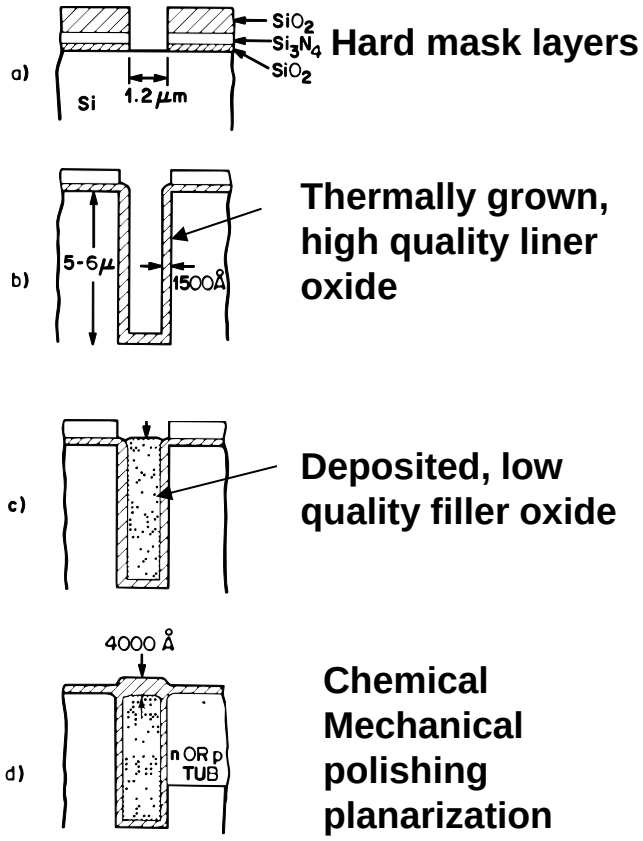
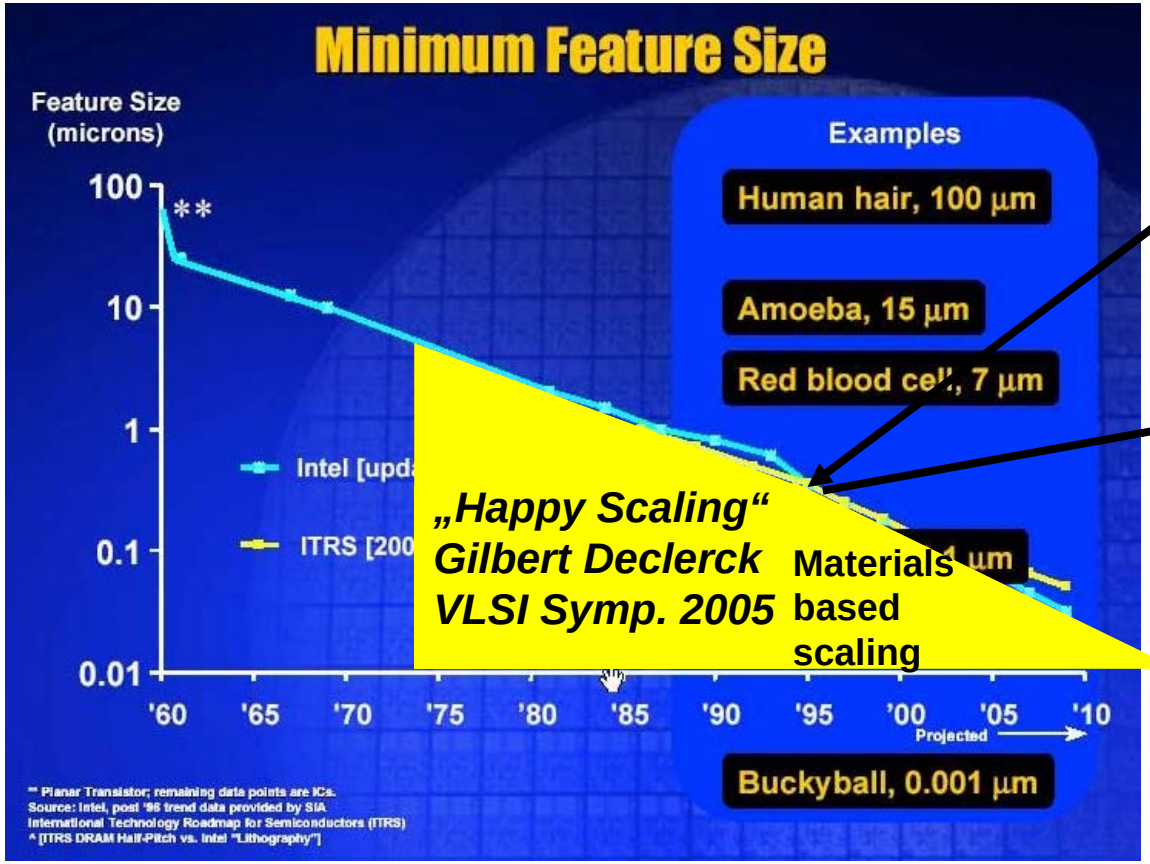


FIGURE 17
Process sequence for forming trench isolation structure for CMOS. (a) Trench mask patterning, (b) trench etching and oxide growth, (c) polysilicon deposition to fill trench, (d) oxide grown to cap trench. (*After Rung, Ref. 23.*)

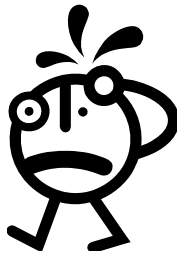
"**Moore**'s law": still going strong in 2010 – Why?



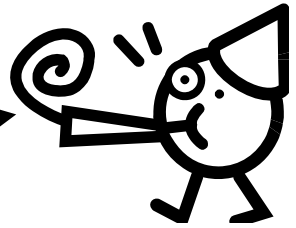
„Happy Scaling"
Gilbert Declerck
VLSI Symp. 2005

Materials based scaling

Industry guy



Researcher



- **SOI**
- **High-k**
- **Metal Gates**
- **Strained Silicon**
- **Germanium**
- **Carbon Nanotubes**
- **Graphene(!)**

Source: G.E. Moore, No exponential is forever…, ISSCC, February 2003

"**Moore**'s law": old & new scaling parameters

MOSFET metrics provide additional leverage: Materials

A simple model for I_{Don} is given by the MOSFET ***"Square-Law" Equation:***

$$I_{Don} = (W/L)\ (\mu\varepsilon_{ox}/t_{ox})\ (V_{GS} - V_T)^2$$

"old"

geometric

Gate length

Gate width

"new"

material

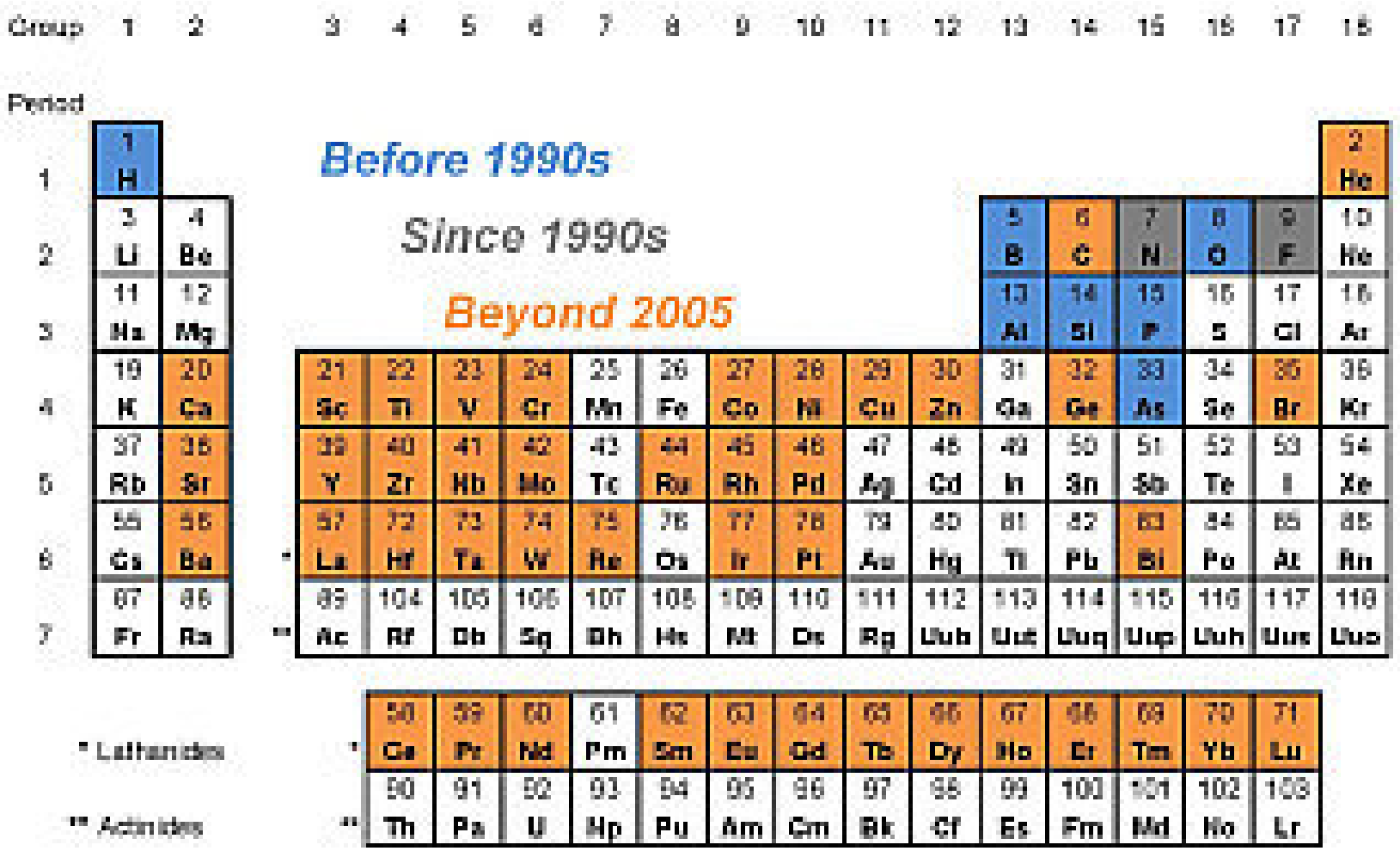
Mobility

Dielectric constant

Oxide thickness

All scaling parameters are determined by improvements in process technology

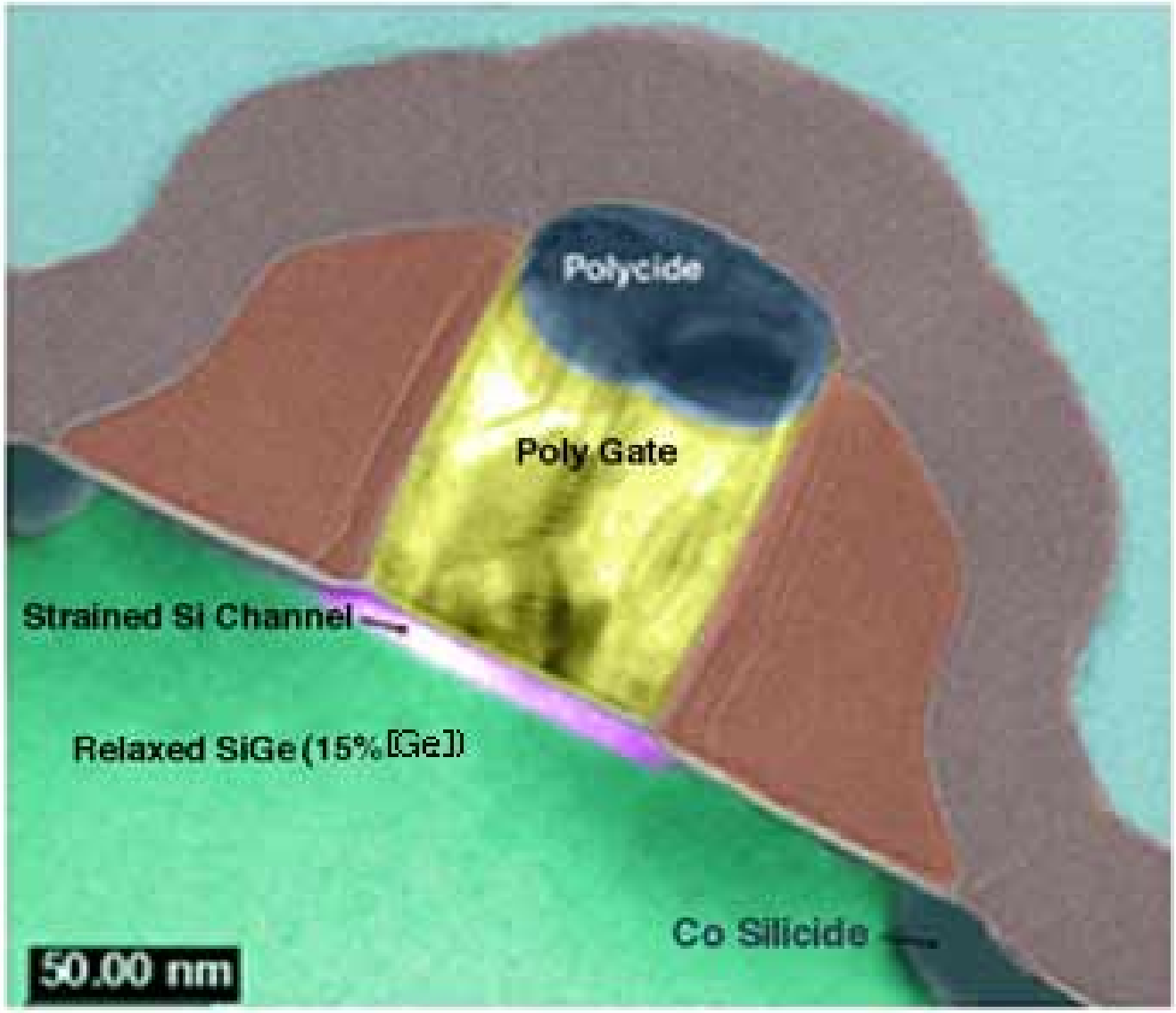
“**Moore**’s law”: still going strong in 2010 – Why?



Source: fabtech.org / Sigma Aldrich

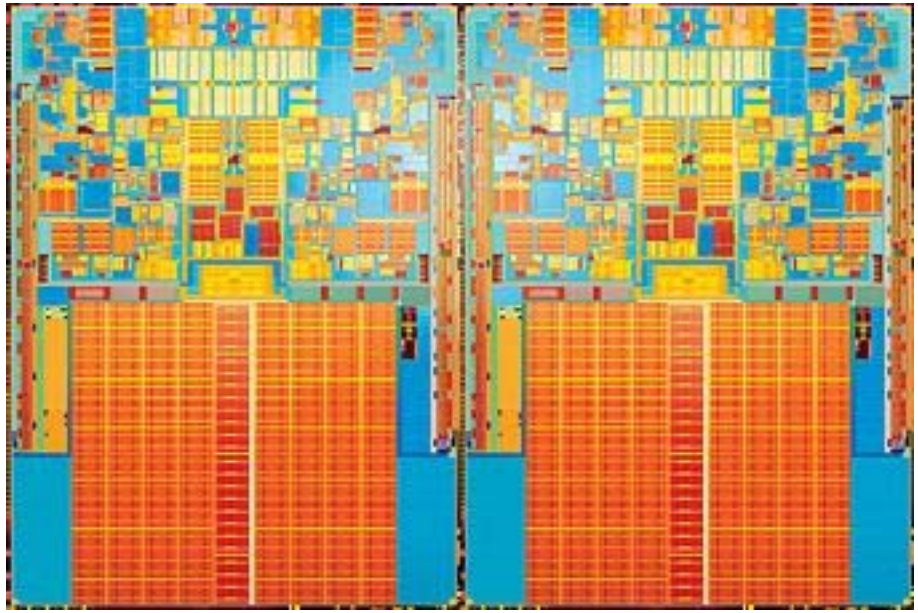
Today: New materials in connection with improvements in process technology

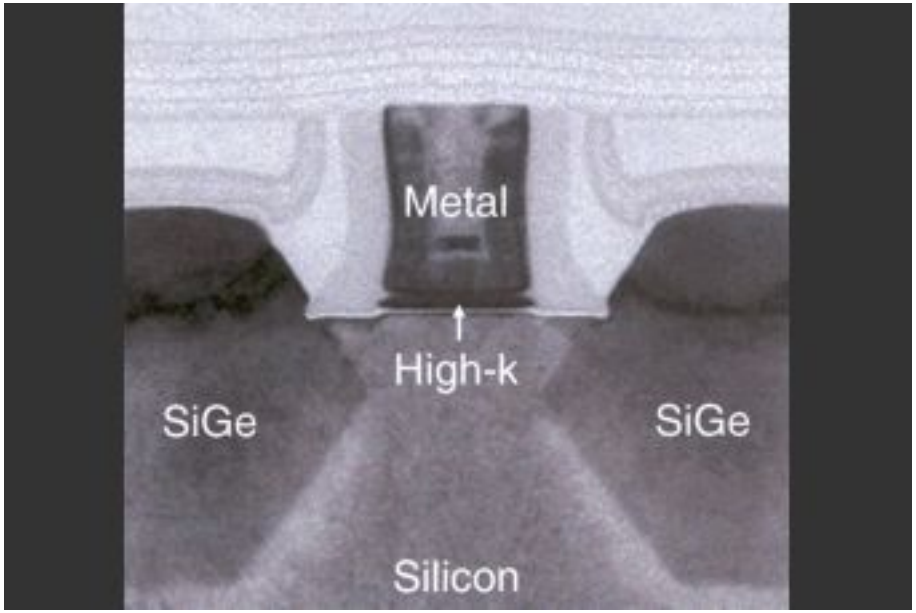
Strained silicon & SiGe



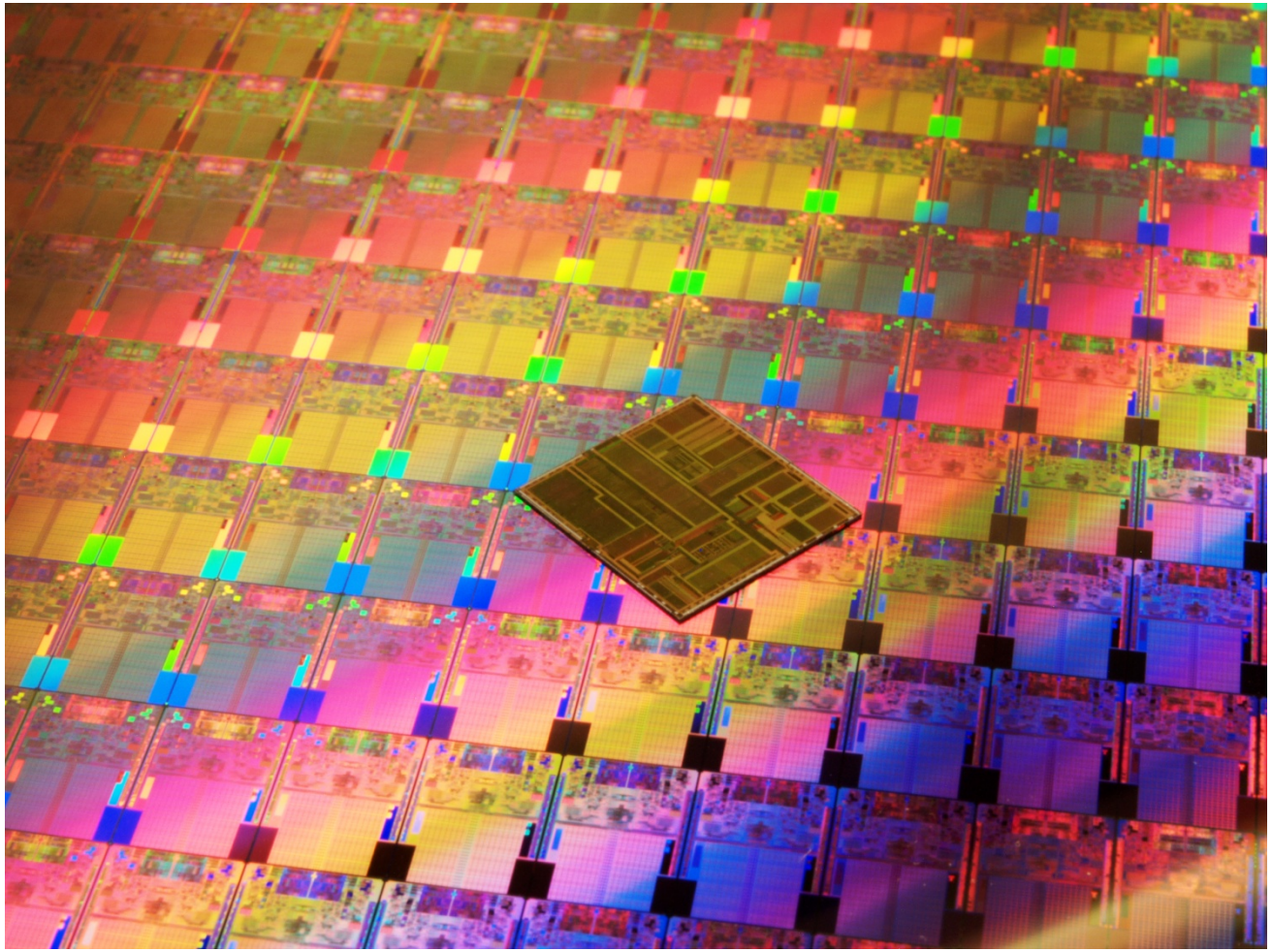
A transistor built with strained silicon. The silicon is “stretched out” because of the natural tendency for atoms inside compounds to align with one another. When is silicon is deposited on top of a substrate with atoms spaced farther apart, the atoms in silicon stretch to line up with the atoms beneath, stretching – “straining” – the silicon. In the strained silicon, electrons experience less resistance and flow up to 70 percent faster, which can lead to chips that are up to 35 percent faster – without having to shrink them. Image Reproduced with Permission of IBM Almaden Research Center, IBM.

Intel 45nm dual-core processor die





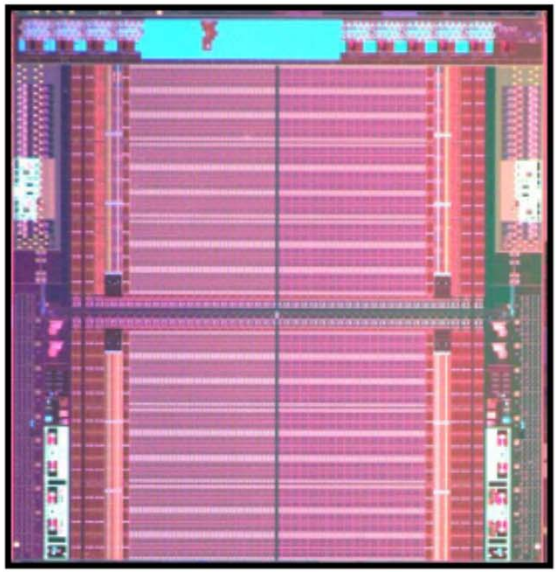
http://www.intel.com/pressroom/kits/45nm/photos.htm



Processors on an Intel 45nm Hafnium-based High-k Metal Gate "Penryn" Wafer photographed with an original Intel Pentium processor die. Using an entirely new transistor formula, the new processors incorporate 410 million transistors for each dual core chip, and 820 million for each quad core chip. The original Intel Pentium Processor only has 3.1 million transistors.

22 nm Tri-Gate Circuits

- 364 Mbit array size
- >2.9 billion transistors
- 3rd generation high-k + metal gate transistors
- Same transistor and interconnect features as on 22 nm CPUs



22 nm SRAM, Sept. '09

22 nm SRAMs using Tri-Gate transistors were first demonstrated in Sept. '09

Intel is now demonstrating the world's first 22 nm microprocessor (Ivy Bridge) and it uses revolutionary Tri-Gate transistors

intel

- Introduction to IH2655
- Brief historic overview
- Moore’s Law and the ITRS Roadmap
- From Geometrical to Material-based scaling
- CMOS Process Flow

CMOS structures

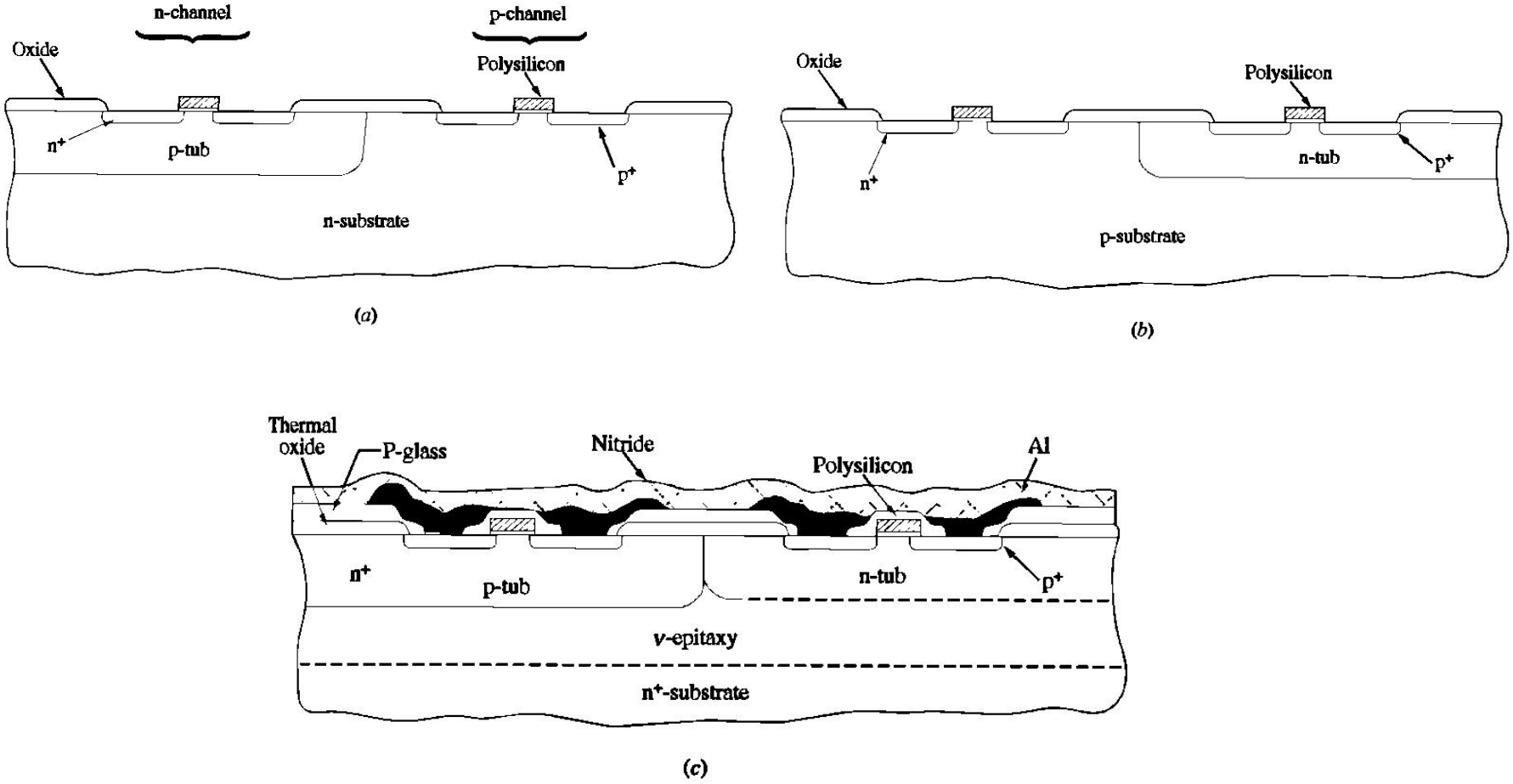
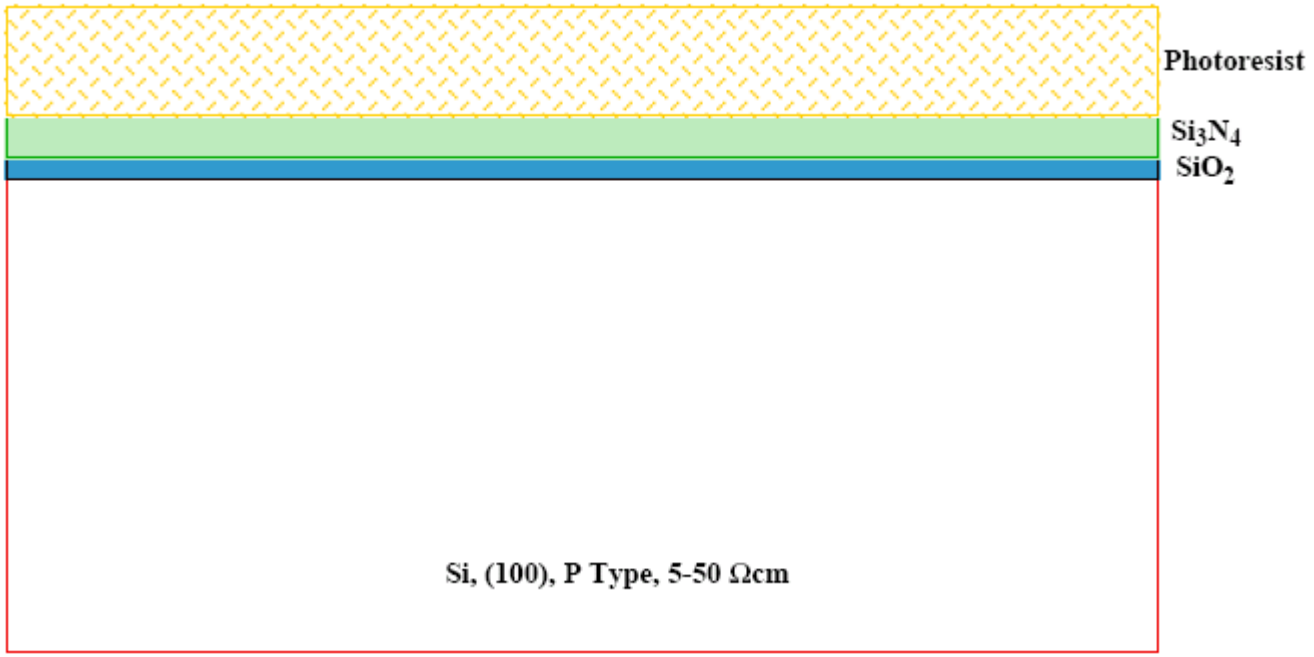


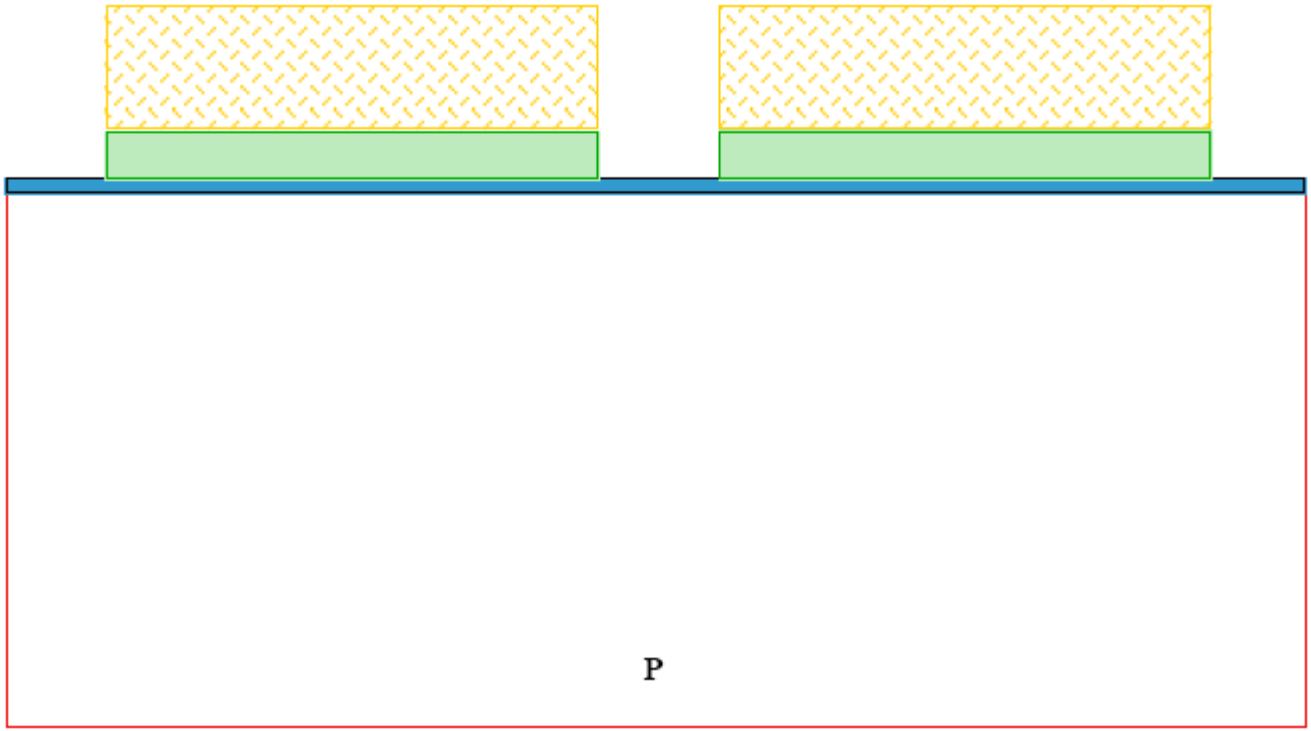
FIGURE 2
Various CMOS structures: (*a*) p-well, (*b*) n-well, (*c*) twin-well. (*After Parrillo et al., Ref. 4.* ©1980 IEEE.)

CMOS Process Flow



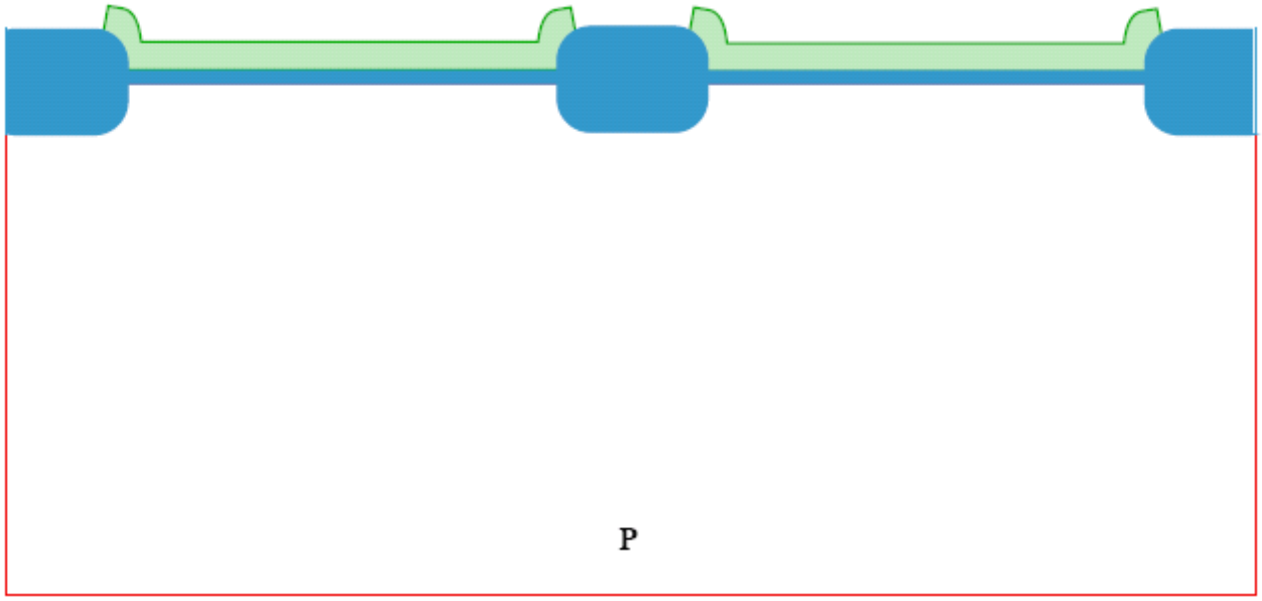
- Substrate selection: moderately high resistivity, (100) orientation, P type.
- Wafer cleaning
- Thermal oxidation (≈ 40 nm)
- Silicon Nitride LPCVD deposition (≈ 80 nm)
- Photoresist spinning and baking (≈ 0.5 - 1.0 μm)

CMOS Process Flow



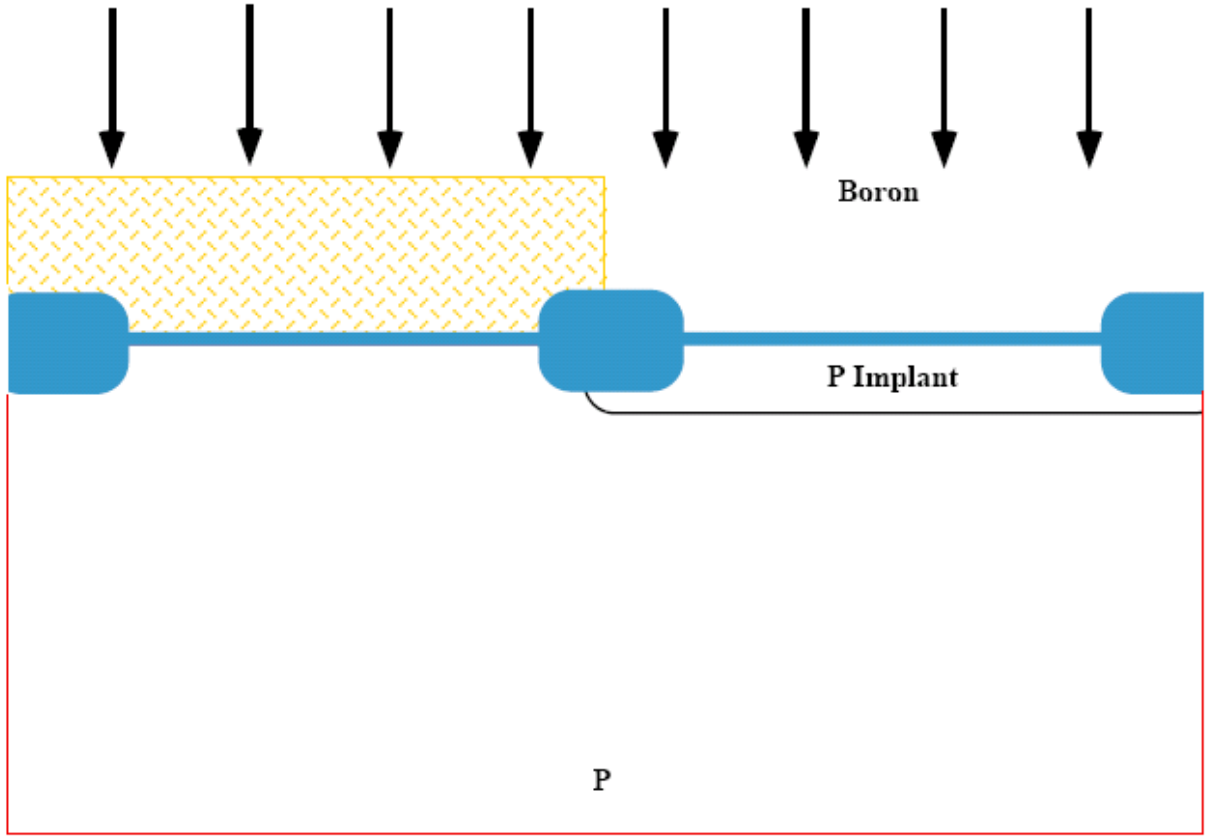
- Mask #1 patterns the active areas
- Silicon Nitride is dry etched
- Photoresist is stripped

CMOS Process Flow



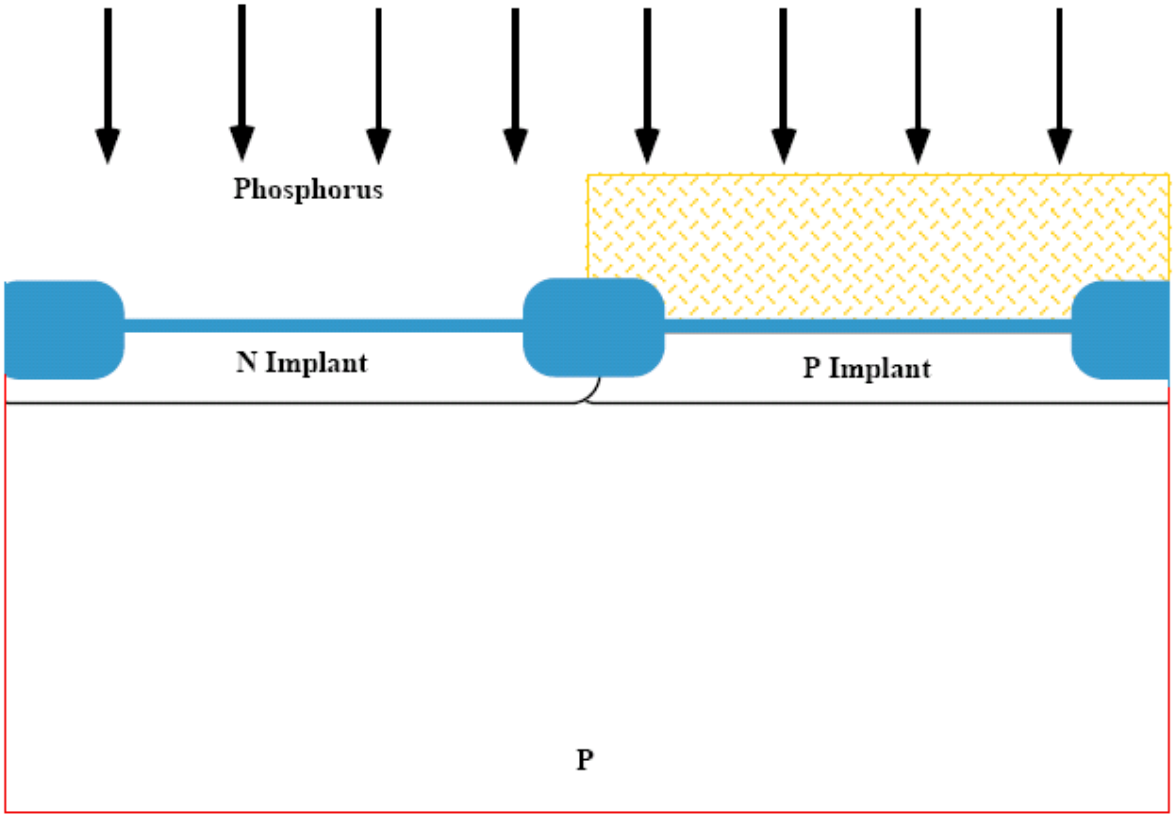
- Field oxide is grown using a LOCOS/ROX process
- Typically 90 min @ 1000 °C in H_2O grows ≈ 0.5 μm

CMOS Process Flow



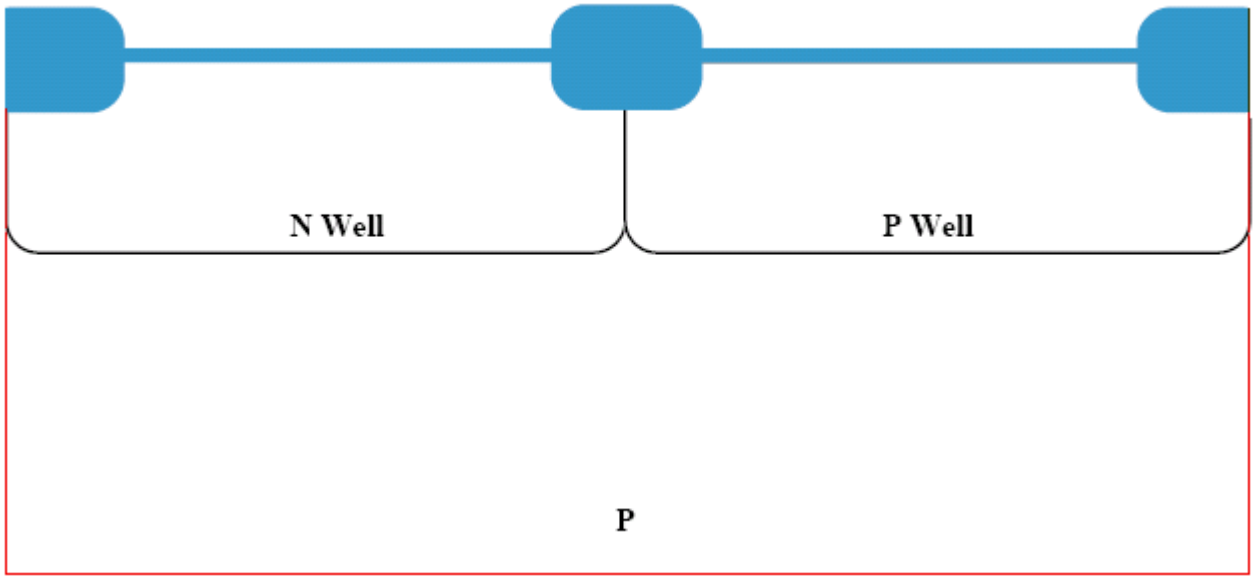
- Mask #2 blocks a B^+ implant to form the wells for the NMOS devices
- Typically 10^{13} cm^{-2} @ 150-200 KeV

CMOS Process Flow



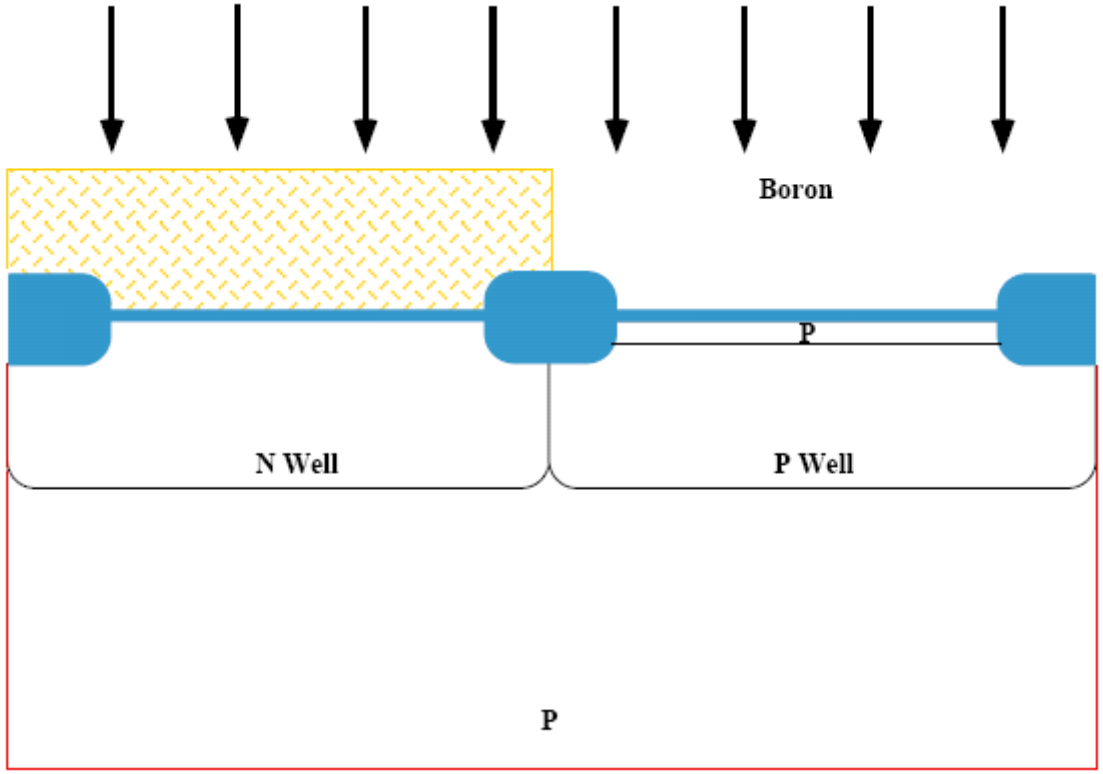
- Mask #3 blocks a P^+ implant to form the wells for the PMOS devices
- Typically 10^{13} cm^{-2} @ 300^+ KeV

CMOS Process Flow



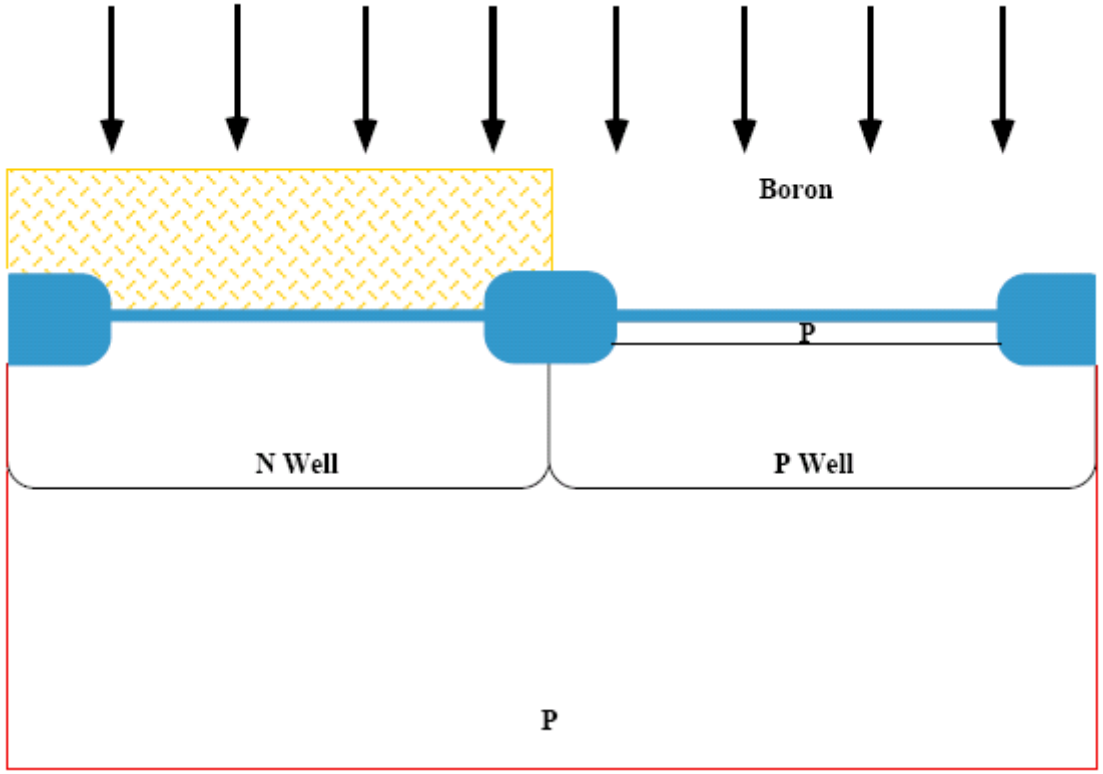
- ”Annealing”
- A high temperature drive-in produces the “final” well depths and repairs implant damage
- Typically 4-6 hours @ 1000 °C - 1100 °C

CMOS Process Flow



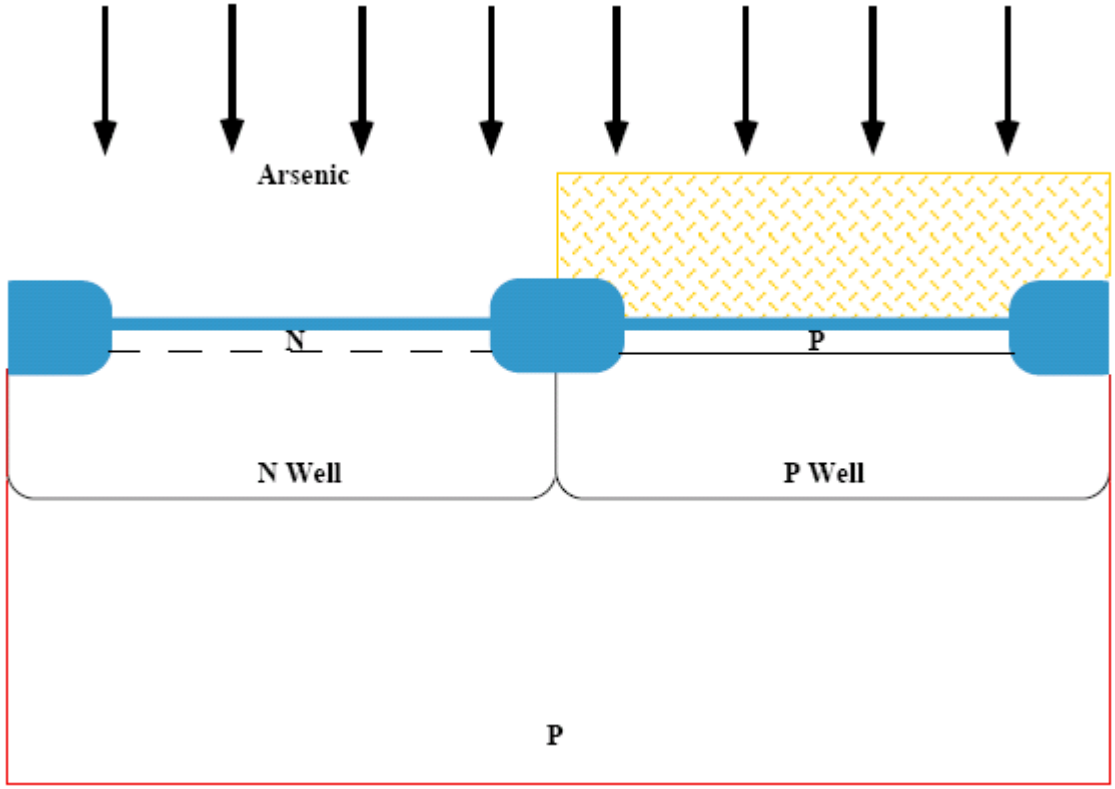
- Mask #4 is used to mask the PMOS devices
- An Implant is done on the NMOS devices
- Typically a 1-5 x 10^{12} cm^{-2} B^{+} implant @ 50 - 75 KeV

CMOS Process Flow



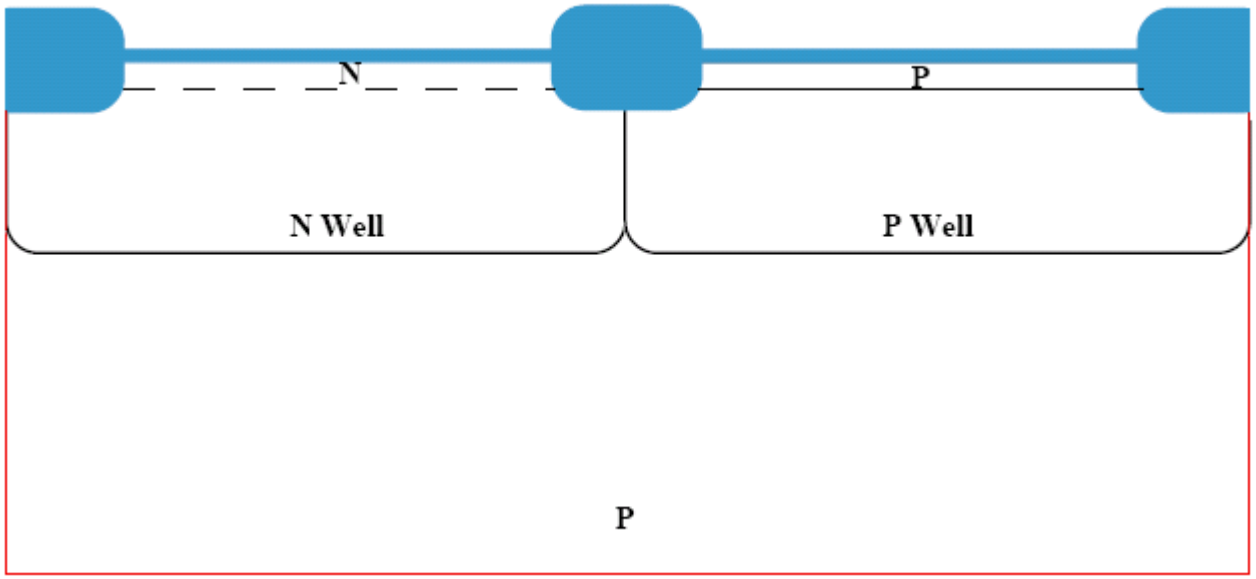
- Mask #4 is used to mask the PMOS devices
- A V_{TH} adjust implant is done on the NMOS devices
- Typically a 1-5 x 10^{12} cm^{-2} B^{+} implant @ 50 - 75 KeV

CMOS Process Flow



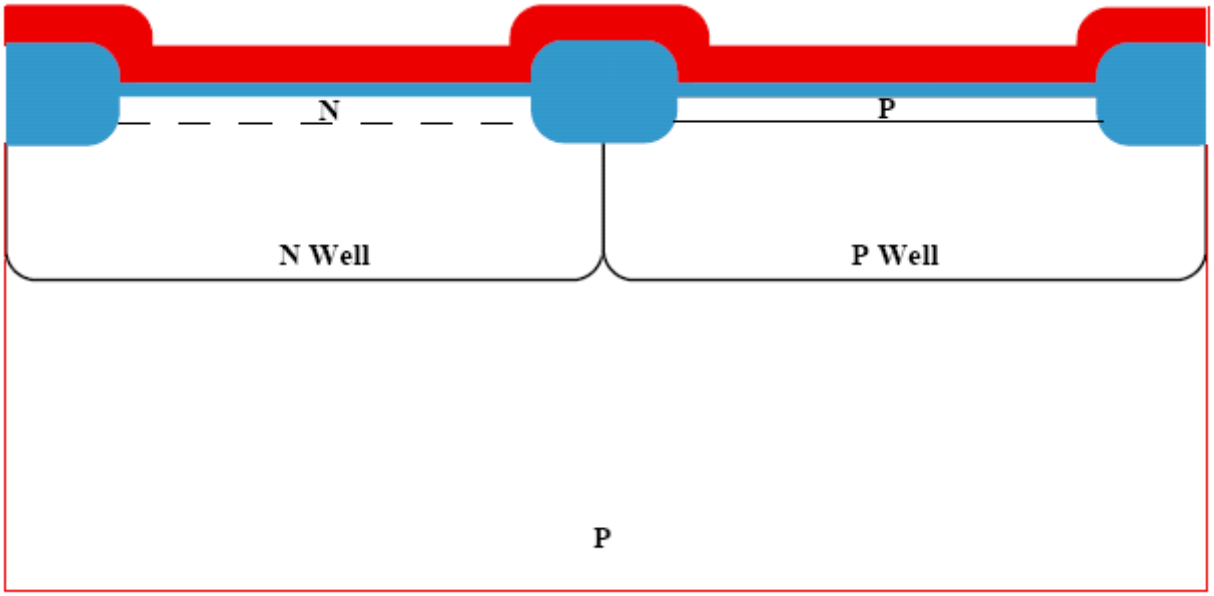
- Mask #5 is used to mask the NMOS devices
- A V_{TH} adjust implant is done on the PMOS devices,
- Typically 1-5 x 10^{12} cm^{-2} As^{+} implant @ 75 - 100 KeV.

CMOS Process Flow



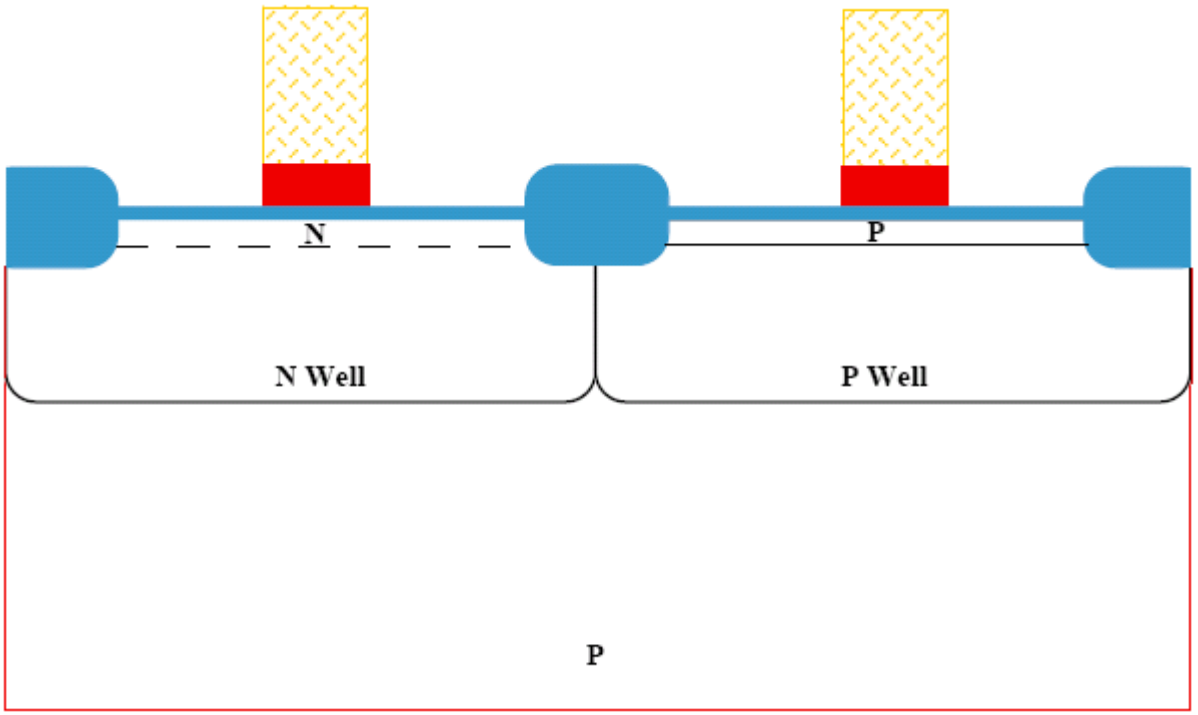
- The thin oxide over the active regions is stripped
- A high quality gate oxide grown
- Typically 3 - 5 nm, which could be grown in 0.5 - 1 hrs @ 800 °C in O_2
- Note: Today this could be entirely different for high end technology (high-k)

CMOS Process Flow



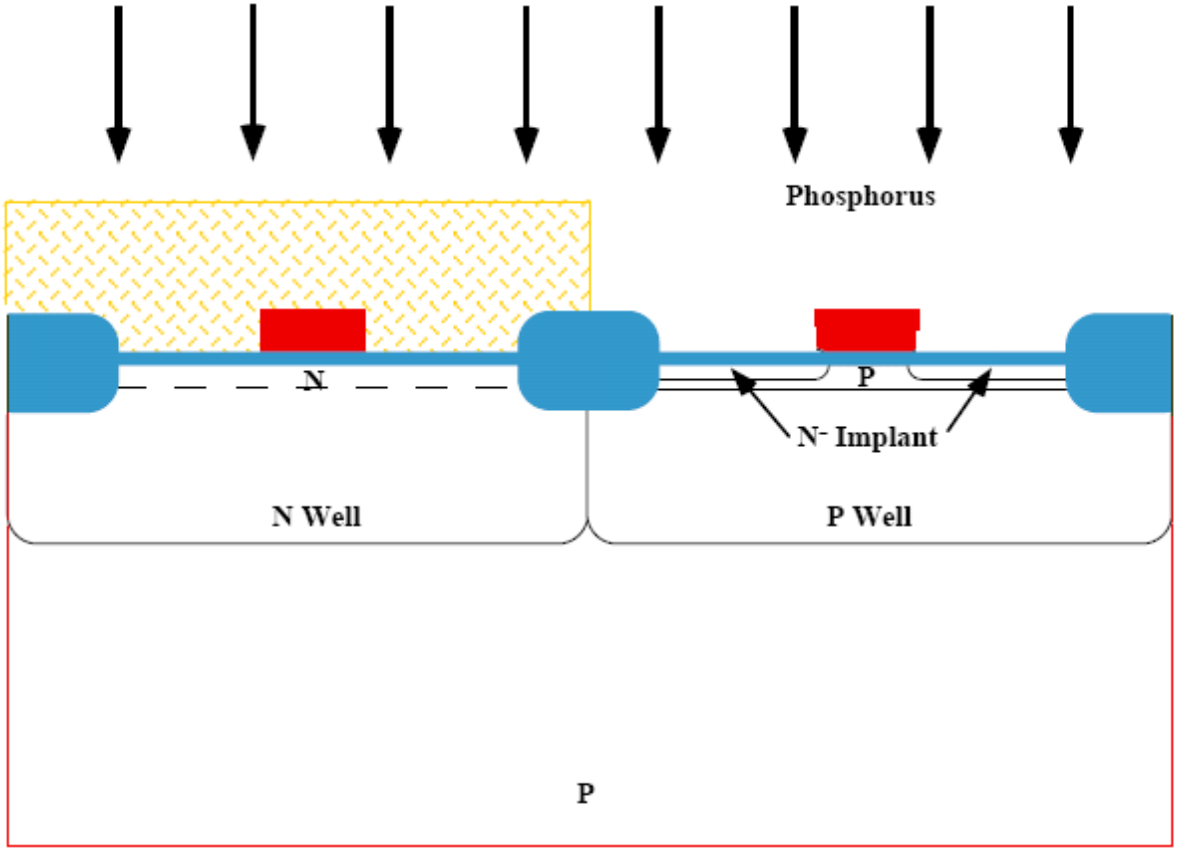
- Polysilicon is deposited by LPCVD (≈ 0.5 μm)
- An unmasked P^+ or As^+ implant dopes the poly (typically 5 x 10^{15} cm^{-2})
- Note: Today this could be a metal gate

CMOS Process Flow



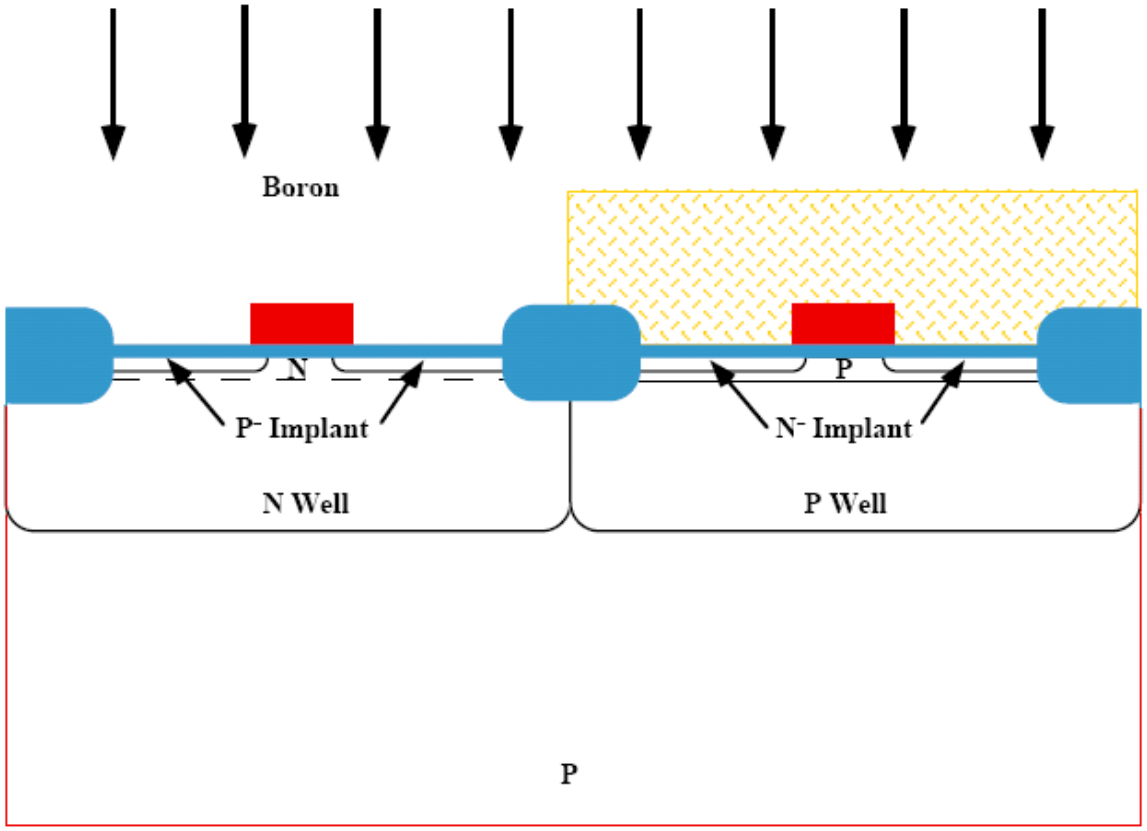
- Mask #6 is used to protect the MOS gates
- The poly is plasma etched using an anisotropic etch

CMOS Process Flow



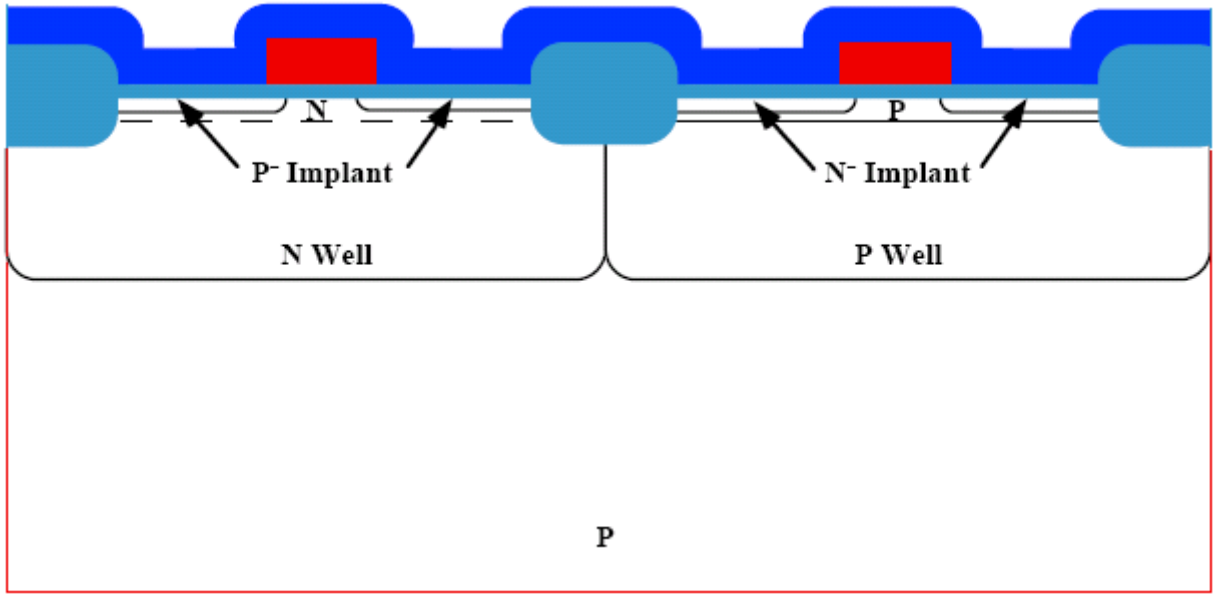
- Mask #7 protects the PMOS devices
- A P^+ implant forms the LDD regions in the NMOS devices
- Typically 5 x 10^{13} cm^{-2} @ 50 KeV

CMOS Process Flow



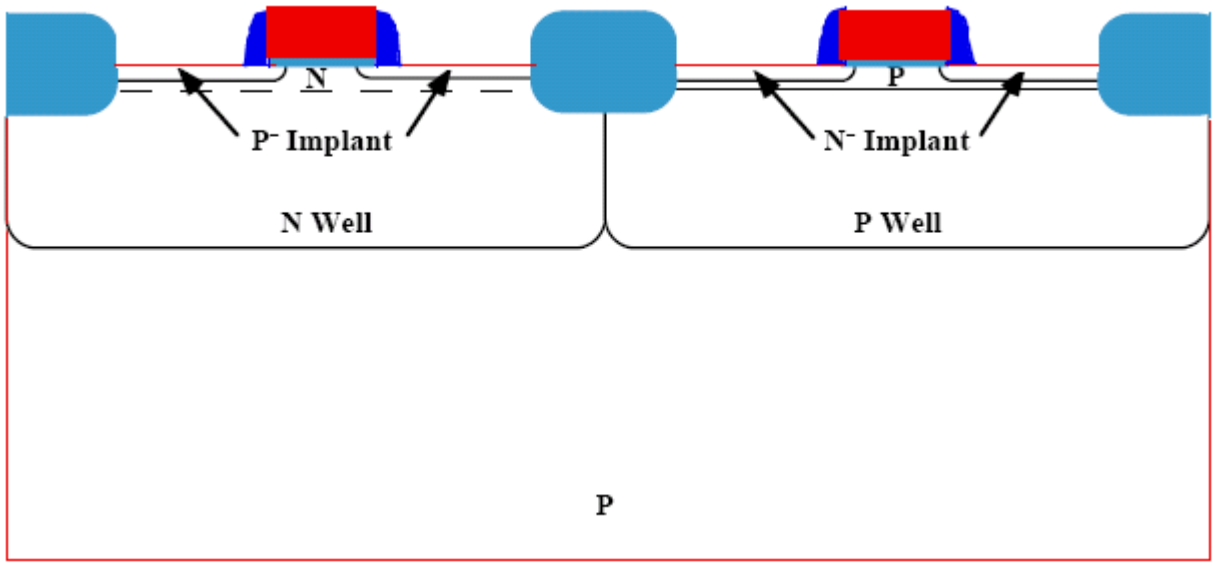
- Mask #8 protects the NMOS devices
- A B^+ implant forms the LDD regions in the PMOS devices
- Typically 5 x 10^{13} cm^{-2} @ 50 KeV

CMOS Process Flow



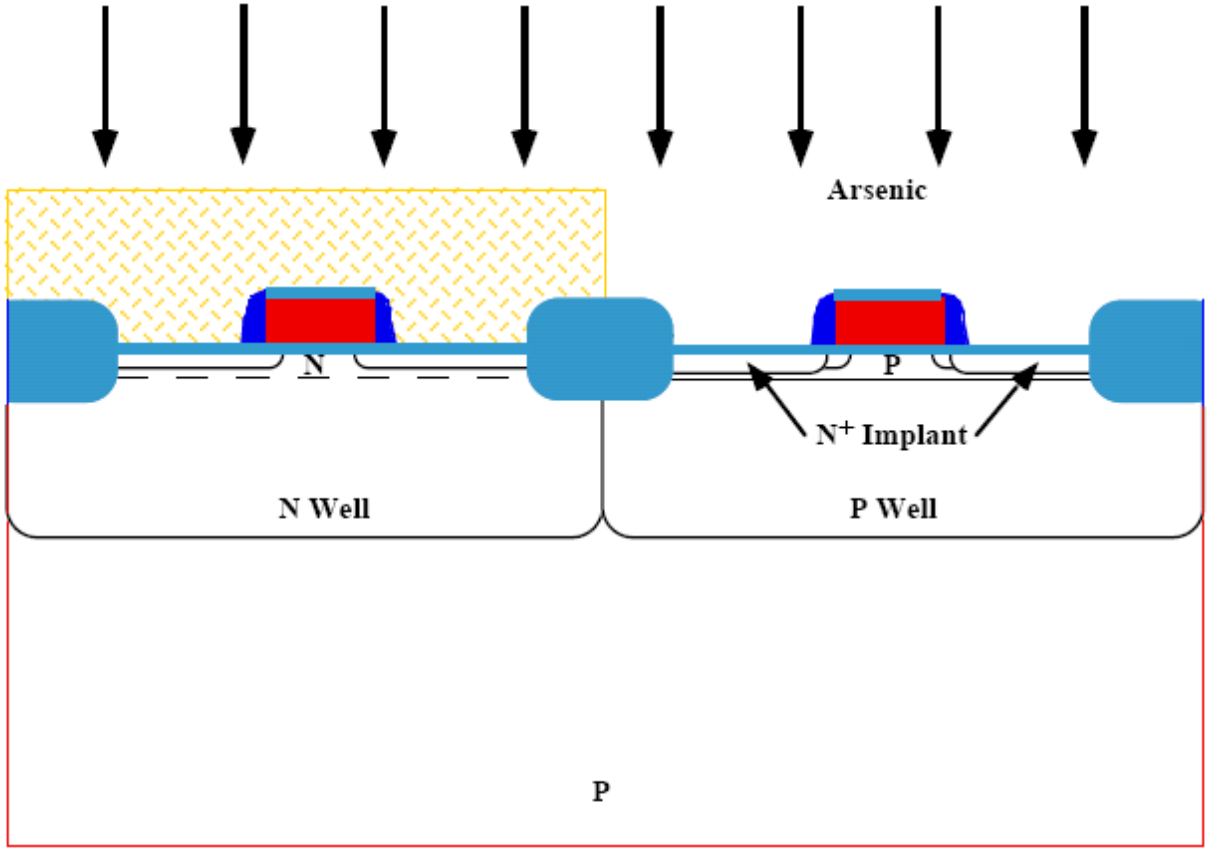
- Conformal layer of SiO_2 is deposited (typically 0.5 μm)

CMOS Process Flow



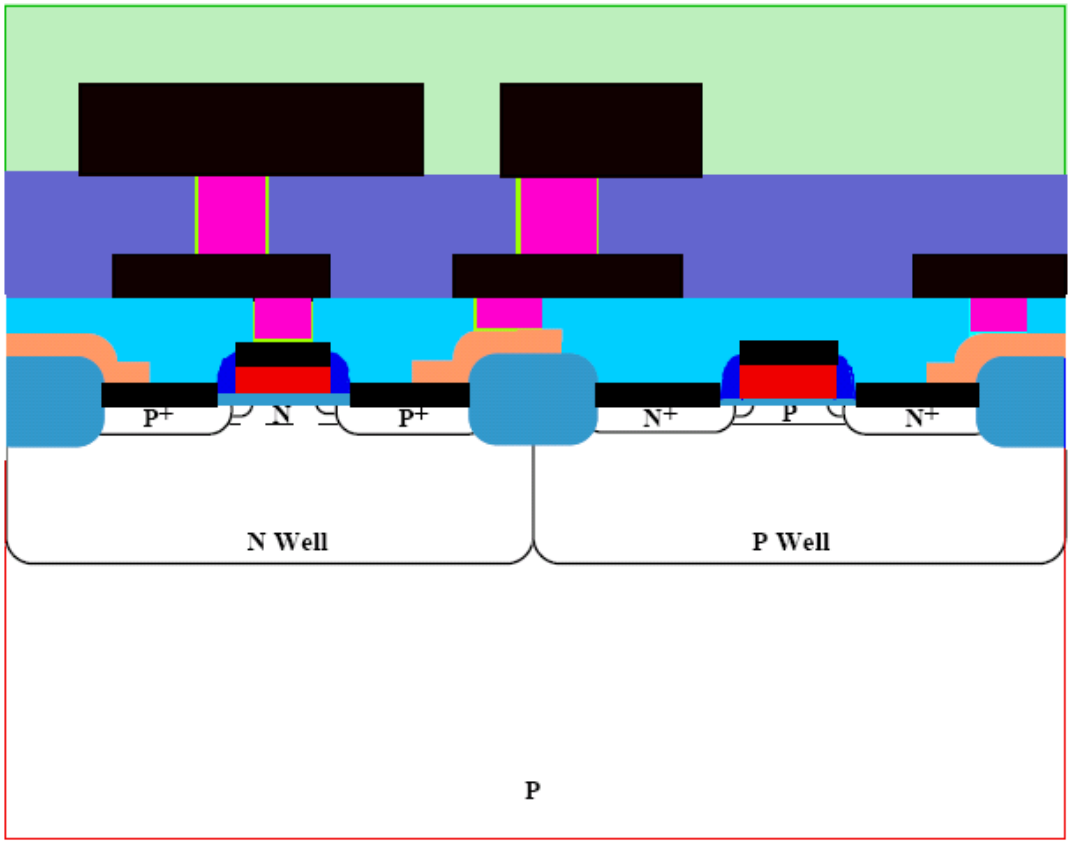
- Anisotropic etching leaves “sidewall spacers” along the edges of the poly gates

CMOS Process Flow



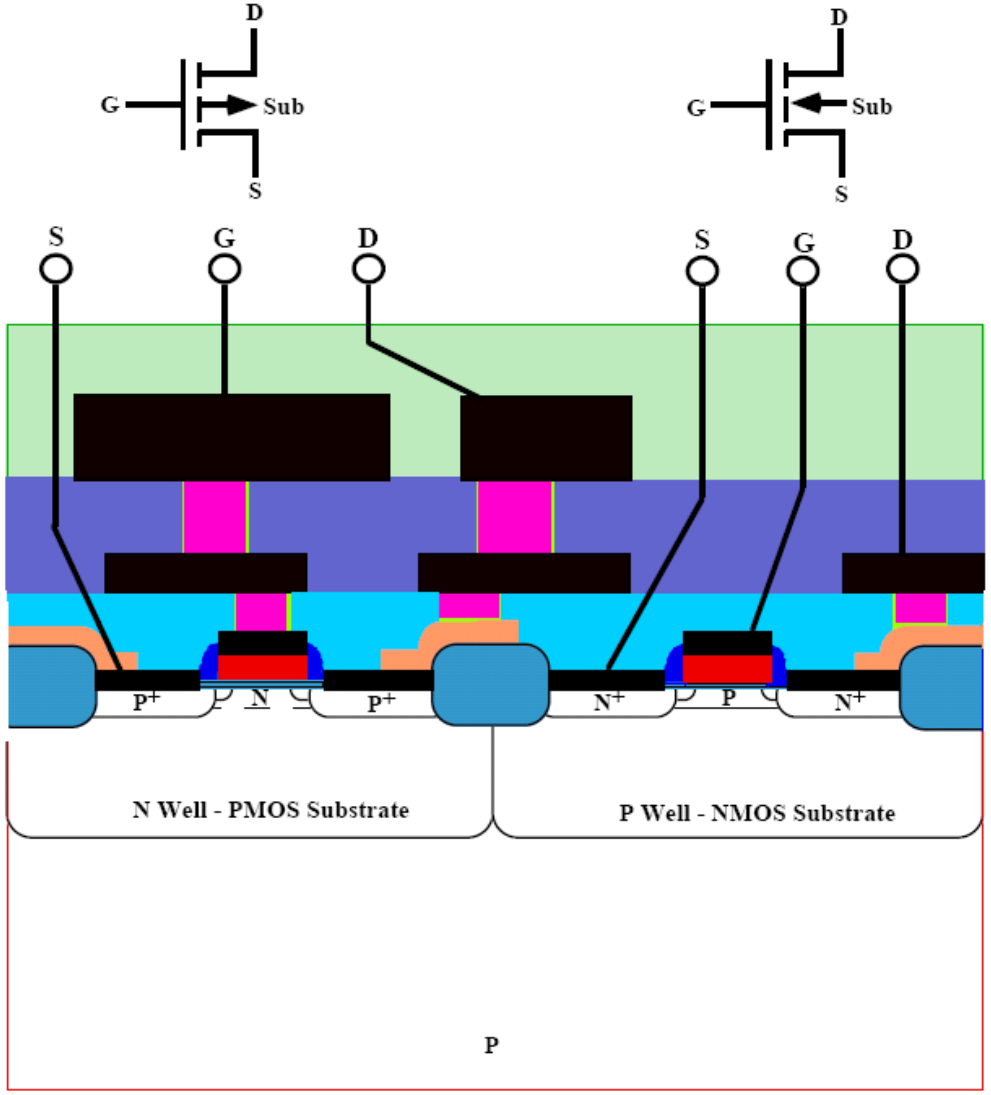
- Mask #9 protects the PMOS devices
- An As^{+} implant forms the NMOS source and drain regions
- Typically 2-4 x 10^{15} cm^{-2} @ 75 KeV

CMOS Process Flow



- Intermetal dielectric and second level metal are deposited and defined in the same way as level #1.
- Mask #14 is used to define contact vias and Mask #15 is used to define metal 2
- A final passivation layer of Si_3N_4 is deposited by PECVD and patterned with Mask #16
- This completes the CMOS structure

CMOS Process Flow



Final result of the process flow: One NMOS and one PMOS device, BUT...
They were made in parrallel and we can make 1 Billion other at the same time