Electrical characterization – process control for novel materials 2012

Laboratory exercise in IH2655 Design and Characterisation of Nano- and Microdevices

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Other instructors: Assoc. Prof. B.Gunnar Malm, gunta@kth.se, Phone 790 43 32

Location/Meeting place: Electrum building, elevator C, level 4, EKT lab, Isafjordsgatan 26.

Time: According to sign-up sheets distributed in class

Tasks

2. Individual theoretical task, emailed to gunta@kth.se at least **24 hours** before lab starts.
3. Lab exercise with instructor 3-4 hours, including 30 minutes of training
4. Individual report written and handed in within **1 week after completed lab.**

NOTE: STUDENTS WHICH HAVE NOT HANDED IN A WELL PREPARED THEORETICAL TASK WILL NOT BE ALLOWED TO ATTEND THE LAB.

NOTE: LAB REPORTS ARE DUE ONE WEEK AFTER THE LAB!
IF YOUR LAB REPORT IS LATE IT WILL NOT BE CONSIDERED FOR RAISING THE FINAL COURSE GRADE.

Theoretical task

In order to prepare for the lab you should write a first draft of the lab report. You will only have to write the Introduction part in this draft. Use about ½ page.

The draft should be written as a **continuous** text and cover these questions:

What is the purpose of these experiment?
What equipment is being used?
What are the main electrical characterization techniques used to analyze the materials/layers mentioned in the lab instruction.

The answers can be found in the instructions below, and the following chapters of the course book:

- 3.4.1.2 Sheet resistance on page 113
- 6.4.3 The MOS Capacitor on page 301
- 7.4.3-4 Sheet resistance & Capacitance-Voltage on page 398
- 11.4.2 Contact resistance/transfer length/oxide breakdown/accel. testing p.726

There is additional information available in the scanned pages from 'Schroder'

Background

We will use MOSFET test chips for process control of novel materials. The investigated devices in **Task 1, 2, and 3** have been fabricated in a so-called high-k/metal gate MOSFET process and additionally devices on strained substrates (**Task 4**) will be investigated. IV measurements of specific contact resistance and sheet resistance will be used to monitor the process uniformity. Standard MOSFET drain-current and gate current will also be measured to check the quality of the high-k gate insulator. An additional IV-characterization technique, charge pumping, can be used to characterize the number of states on the high-k oxide-to-channel interface and the interface of non-conventional substrates. The use of four-terminal techniques will be investigated for both low resistance and transistor measurements.

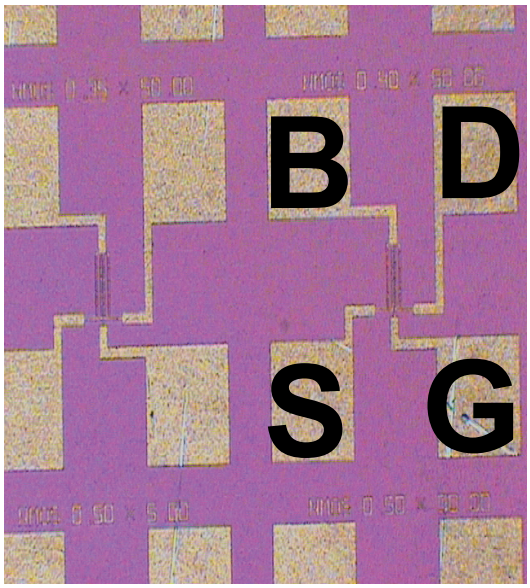


Figure 1. MOSFET test structure layout with probe pads for measurement.

In Fig 1 the layout of a MOSFET device is shown. The device is surrounded by the four probe pads, which are needed to connect gate, drain, source and body. Other common structures on a test chip are diodes, multi-terminal resistors (VDP and Kelvin type).

At the lab **complete layout maps and tables of test structure dimensions** will be handed out, for each of the investigated wafers. Since the layout is wafer dependent this information is not given in these instructions.

Set-up and DUT connections

A standard semiconductor parameter analyzer will be used. The device under test (DUT) is connected using four micro-positioners with sharp needles. Each connection has its own source/measurement unit (SMU) with better than 1 pA resolution. Totally 4 different units are available in this instrument. All units are remotely controlled by windows software, running on the instrument.

For IV-measurements on MOSFETs the connections are the gate terminal, source-and-drain and the bulk/substrate node. For 4-terminal resistance measurement one pair of connections is used for the test current and one pair of terminals is used to sense the voltage drop.
For charge pumping measurements a parameter analyzer with source/measurement units (SMUs) and a pulse generator will be connected. The pulse is applied to the gate and a base voltage is swept at the substrate node, while the source/drain junctions are reverse biased.

The first part of the lab is **dedicated to training** (about 30 minutes).The instructor will demonstrate the set-up for on wafer measurements. A shielded probe station is used. Small needles are placed on the 100x100 μm^2 contact pads by use of micromanipulators. Please be careful since the probe needles might bend or break!

Measurement task 1 – gate leakage current on high-k/metal gate samples

The first purpose is to check the current resolution of the set-up (instrument and cables). Measure the drain and gate current vs. gate voltage for a drain bias of 1.0 V. There are many different available gate areas. Basic test could be done using large devices (1x10 μm is suitable).

- Check if the noise level in the gate current can be reduced by changing the integration time (short/medium/long), also compare the case when the top cover of the shielding box is removed. Use the **reference sample** in Table 1.
- Repeat for another area and check that the current(s) scale with area as expected.
- Compare the gate leakage current for a fixed area for **two** of the samples mentioned in Table 1. Do the samples fulfil the ITRS roadmap requirements?

Table 1 Available samples for task 1,2 and 3

Wafer	*SiO_2 thickness nm*	*$LaLuO_3$ thickness nm*	*TiN thickness nm*
Reference	5	_	20
High-k 1	5	6	20
High-k 2	_	6	20
High-k 3	_	20	20

A second purpose is to check the dual (force/sense) cable Kelvin set-up, used to adjust the voltage close to the probe needle.

- Check this by directly measuring the potential on the source pad with and without the force /sense connection. To see this effect use a short length, large width device, to maximise the drive current!

Measurement task 2 – contact resistance to doped semiconductor and metallic layers

The purpose is to determine whether good ohmic (low-resistive) contacts have been formed to different metallic and doped semiconductor regions on a **nMOSFET**. Use the **reference sample** in Table 1.

For a nMOSFET the source and drain are highly n-type doped, the bulk node is p-type. Normally a self-aligned silicide (PtSi) is formed on the source and drain areas to reduce the sheet and contact resistance.
A metallic gate is used to set an appropriate work function. In this lab TiN (tungsten) gate devices will be measured.
The interconnect metallization, on top of the contacts, is a stack of TiW + Al in all cases.

- Examine the different type of contacts source/drain and gate and compare their performance. A good contact should exhibit linear IV-characteristics.
- Extra task 1: Verify that the 4-terminal measurement removes the influence of contact and cable resistance by comparison with a straightforward 2-terminal measurement on the same structures(s).
- Extra task 2: Try to determine the specific contact resistance by varying the contact area.

All necessary layout information is available at the lab!

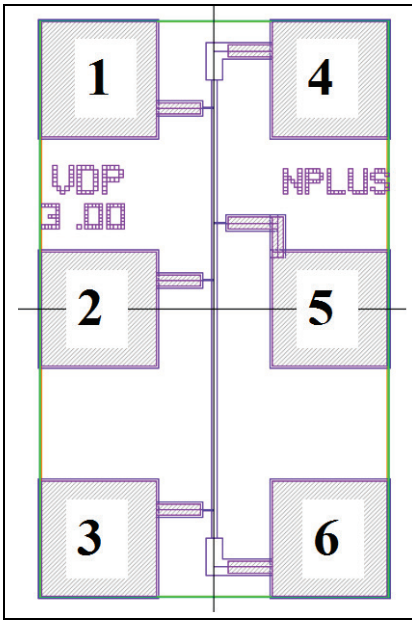
Measurement task 3 – sheet resistance

The purpose is to determine the sheet resistance of different metallic and doped semiconductor regions, see also task 2. Use the **reference sample** in Table 1.

- Examine the sheet resistance of the doped seminconductor and metallic layers on an nMOSFET using the Van der Pauw type of structure in a 4-terminal connection.
- Plot the resistance as a function of the length of structure (minimum 3 different lengths).

The VdP structure has 6 pads, see figure 2. Pads 4 and 6 are only used for driving current.
The pads 1, 2, 3, and 5 are used for measuring the voltage drop and are contacted with narrow lines.

All necessary layout information is available at the lab!



Distance

Pad 1	Pad 5	100 μm
Pad 1	Pad 2	150 μm
Pad 2	Pad 5	50 μm
Pad 3	Pad 5	250 μm
Pad 1	Pad 3	350 μm

Figure 2 Numbering and distances between pads in 6-terminal VdP layout

Measurement task 4 – interface state density

The purpose is to determine the interface state density (Dit) of the channel to gate insulator interface.

- Measure the charge pumping current (I_{CP}) for at least 3 different gate lengths. Try to vary the frequency.
- Verify that I_{CP} scales with frequency and gate length.
- Calculate the Dit of all samples from the measured charge pumping current.

NOTE: The instructor will provide you with samples with oxides grown under identical conditions on different wafer materials. Different from the samples used in task 1, 2, and 3.

Written report

The report should be written individually. Copying text in the report directly from the lab instructions or other sources is strictly forbidden. The report may not exceed 3 pages, following the structure:

a) Introduction (completed in preliminary version 24 h before start of the lab!!!)
b) Experimental set-up
c) Results
d) Conclusions

Number all figures and tables, use correct units. Do an error limit estimation of your reported values for at least one of the tasks 1-4.
Measurement data will be saved in ASCII format files and can be plotted and analyzed in EXCEL, MATLAB, Origin or similar programs.

Each section should be written as a **continuous text**. All questions should be answered in the report. They may not be given as a list of questions and answers, but instead, as a part of the discussion in the text.

The report will be graded Fail (F), Good (G) and Very Good (VG). If the report is not good enough to pass the student will have a chance to improve it. Only the grade VG can improve your final course grade.

The report is due 1 WEEK after the lab.