Lecture 4

Electrical Characterization

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Outline

- Measurement set-up, test-structures (samples/devices)
- Types of electrical measurements
- Real examples
- About the lab (sign-up, preparations)
- Summary

Outline continued

- Most of the Chapters in Plummer have a subsection called:
- Mesurement Methods
  - Electrical measurements
- 3.4.1.2 Sheet resistance on page 113
- 6.4.3 The MOS Capacitor on page 301
- 7.4.3-4 Sheet resistance & Capacitance-Voltage on page 398
- 11.4.2 Contact resistance/transfer length/oxide breakdown/accel. testing p.726

What do we want to measure?

1. Monitoring of process stability
   - Ultra-thin gate oxides, high-k dielectrics, sheet&contact resistance of doping and metal (silicides)
2. Performance of devices (MOSFETs) and circuits
3. Extract model parameters such as threshold voltage *(V_T)* or whole set of SPICE parameters

- This lecture mainly covers point 1

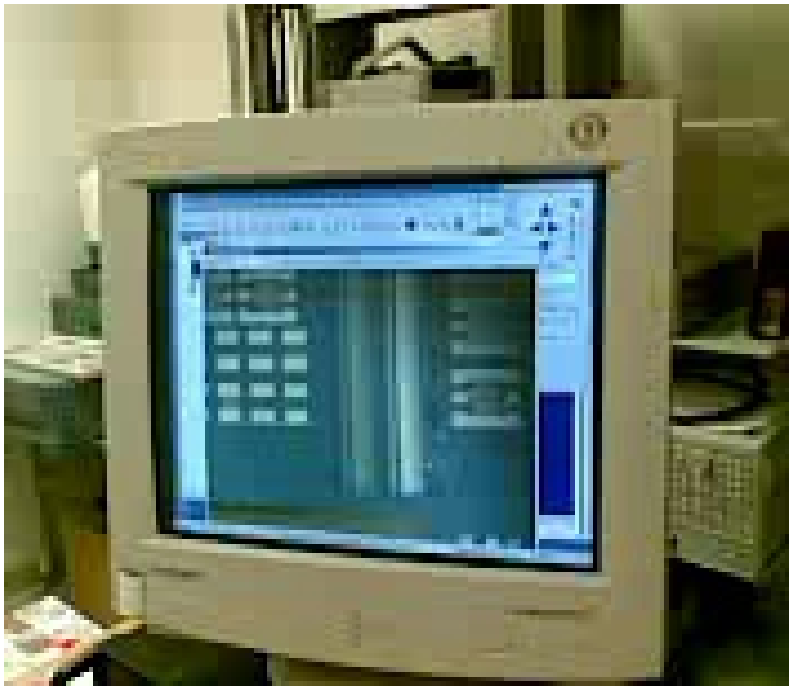
Test structures

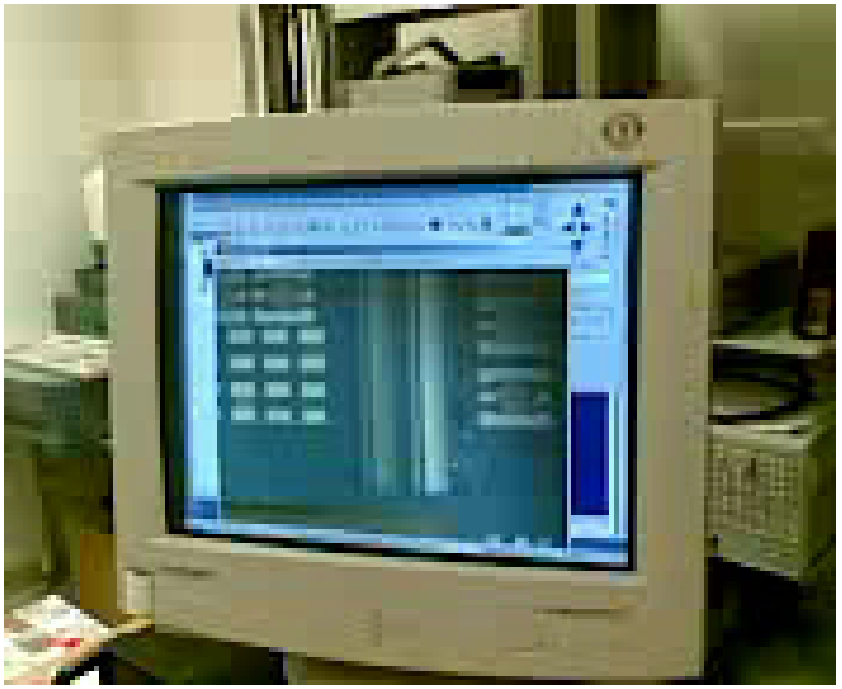
- All measurements are typically on a 200-300 mm inch wafer. Map statistics at selected locations.
- MOS capacitances (or split-CV) for oxide studies
- Different types of 4-terminal resistance structures
  - Van der Pauw for sheet resistance of metals, silicides, implanted/activated dopants
  - Cross Bridge Kelvin for contact resistance (metal-to-semiconductor)
- Different MOSFET transistor sizes, use that $I_{drain} \propto W/L$
- Arrays of structures for in-line probe-card measurement (PCM)

Measurement setup

- Automatic 200 mm wafer prober and manual 150 mm wafers
- Needle probes with micromanipulators
- Measurement equipment
  - 2 parameter analyzers (Keithley) with SMUs, pulse generator and coax-triax cables in Kelvin configuration)
  - CV impedance bridge (Agilent/Keithley) <10 MHz
- Optical or IR-emission microscope and digital cameras

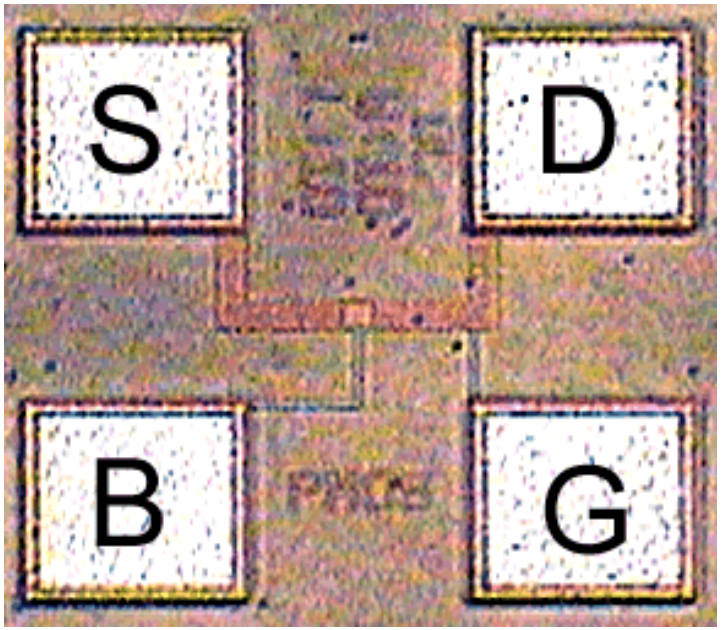
Measurement setup

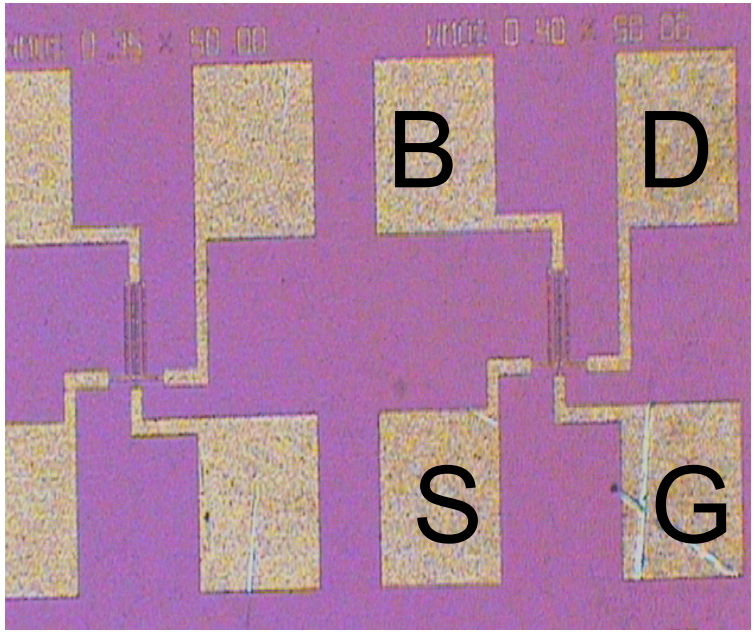




•Many different instruments, focus on ’semiconductor parameter analyzer’ and wafer mapping approach for IV type of measurements

Test-structure layout





- Transistors with different gate areas (W/L) contacted with 4 connection source, drain, gate, bulk/ground
- Typical probing area 80x80 μm, pitch μm 100
- Probe card and switching matrix used to connect multiple devices
- Acronyms: DUT (device under test), PCM (probe card measurement)

Characterization types

- IV/DC with source/measure units (SMUs), possibly preamplifiers below 1pA
  - High current (example small resistance of metal/silicide line or contact)
  - Low current (gate and junction leakage, charge pumping)
  - Pulsed to get information about defects and avoid self-heating
- AC: Impedance and C-V mainly for MOS gate oxide but also channel mobility

The 4-point principle (Kelvin)

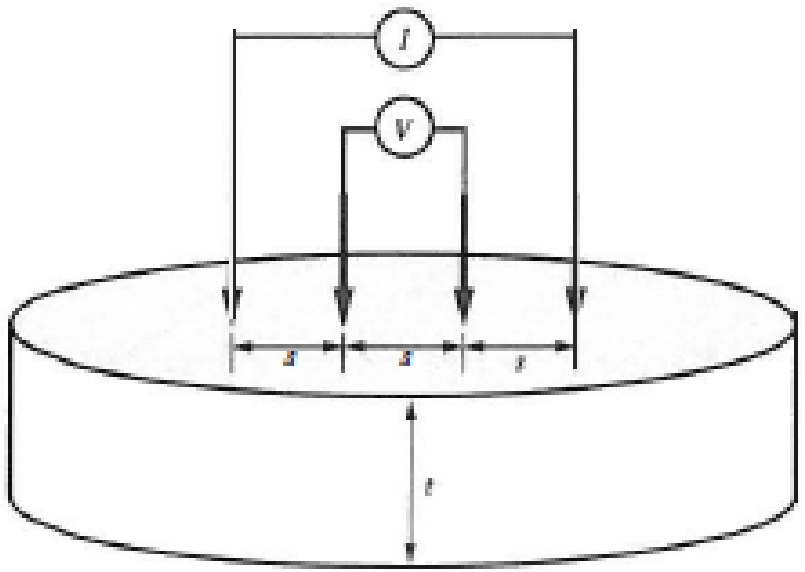
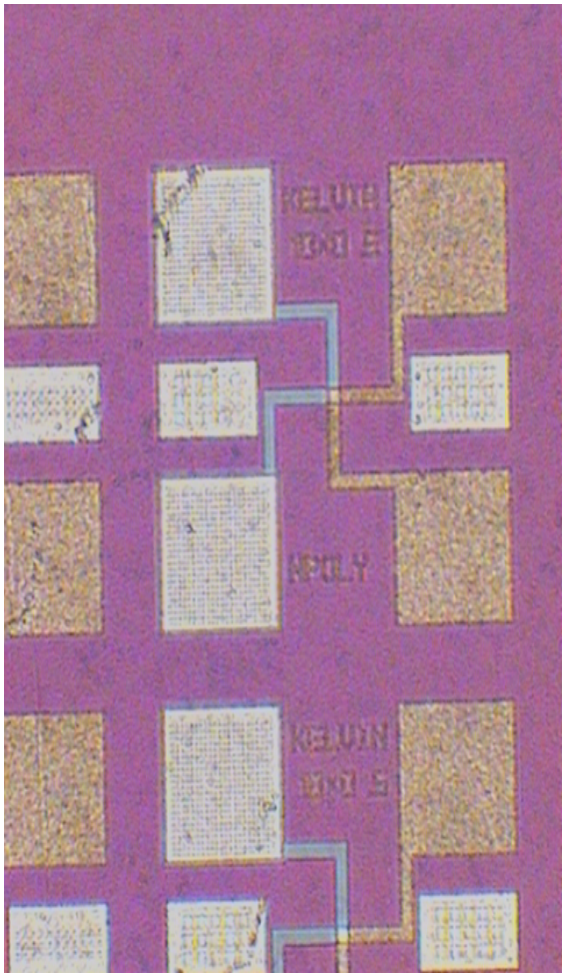


Figure 3–12 Four-point probe measurement method. The outer two probes force a current through the sample; the inner two probes measure the voltage drop.

- Separate voltage and current

Test-structure layout for resistance



- Cross-bridge Kelvin
- Contact resistance, metal to highly doped silicon or
- Metal to silicide

Test-structure layout for resistance

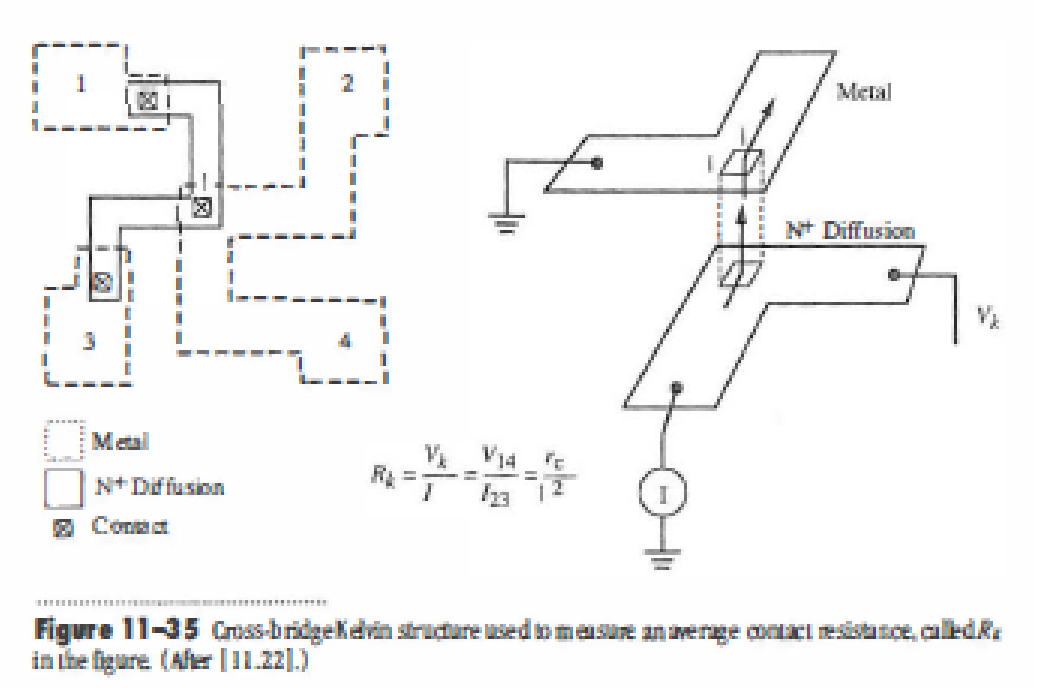
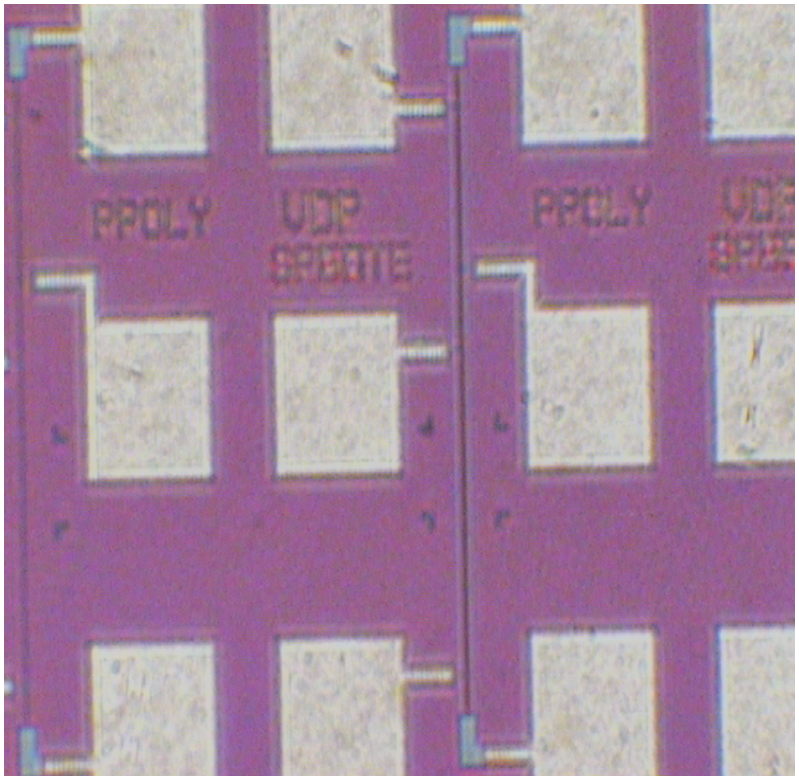


Figure 11–35 Cross-bridge Kelvin structure used to measure an average contact resistance, called R_k in the figure. (After [11.22].)

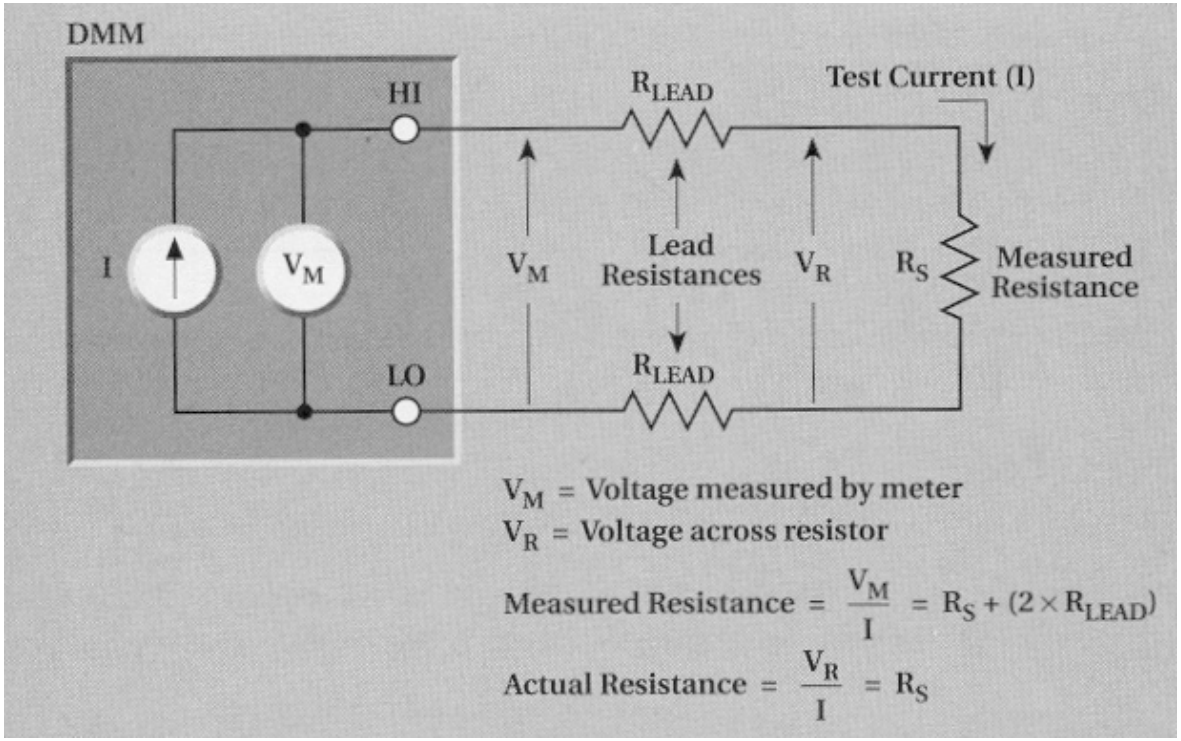
- Cross-bridge Kelvin

Test-structure layout for resistance



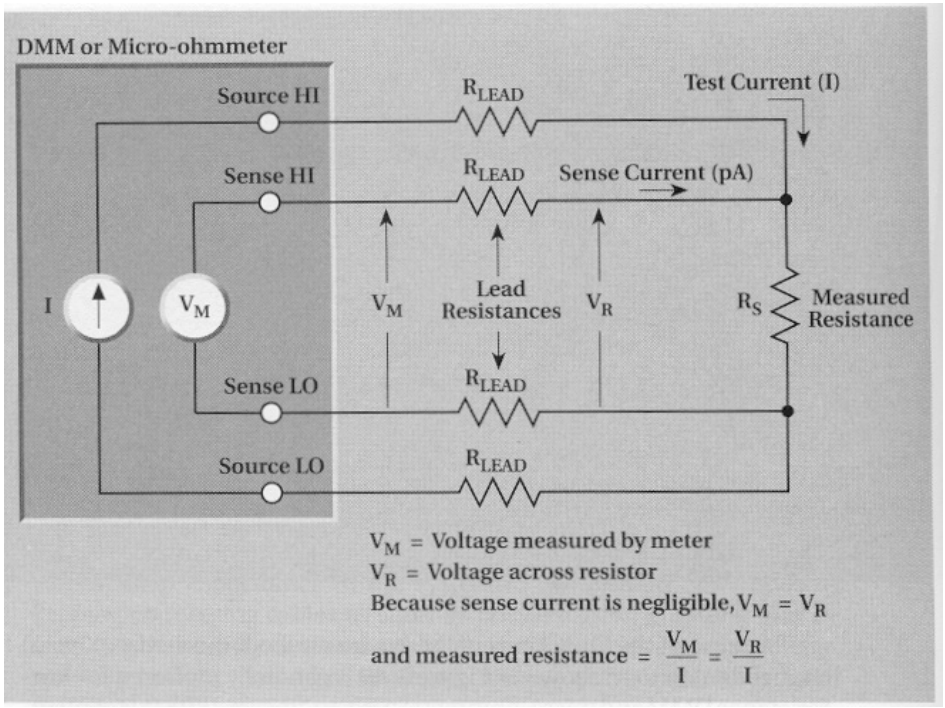
- Van der Pauw: 2 current terminals + 2 voltage sense terminals, different length of resistor lines
- Metal or metal silicide lines, approx 10 – 1000 Ω

High current measurements



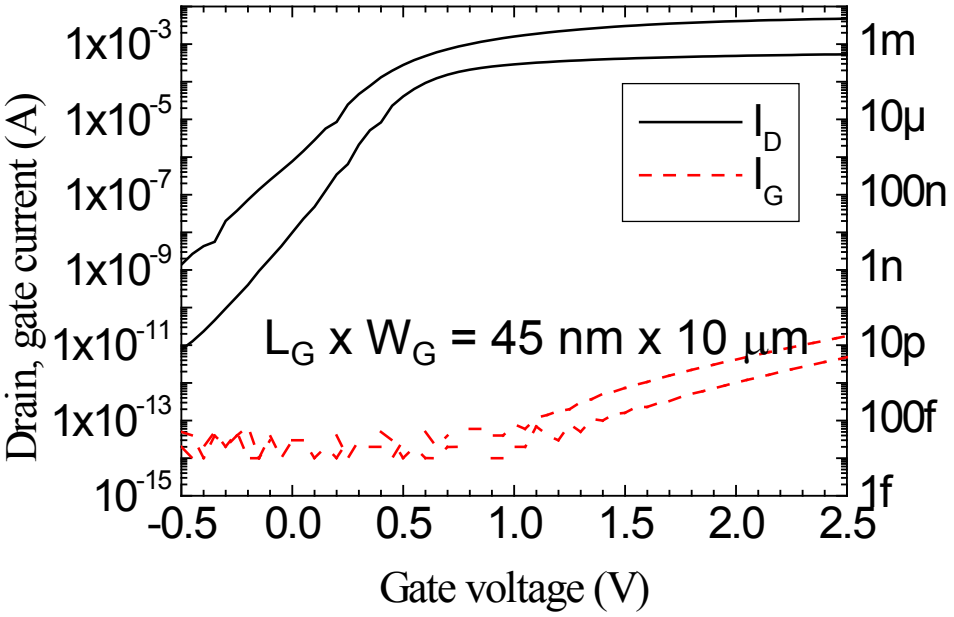
- Problem- resistance of cables and 'probe contacts' will be added to the actual device
- High current needed to get enough voltage drop over small resistor mΩ - 10 Ω range

High current measurements



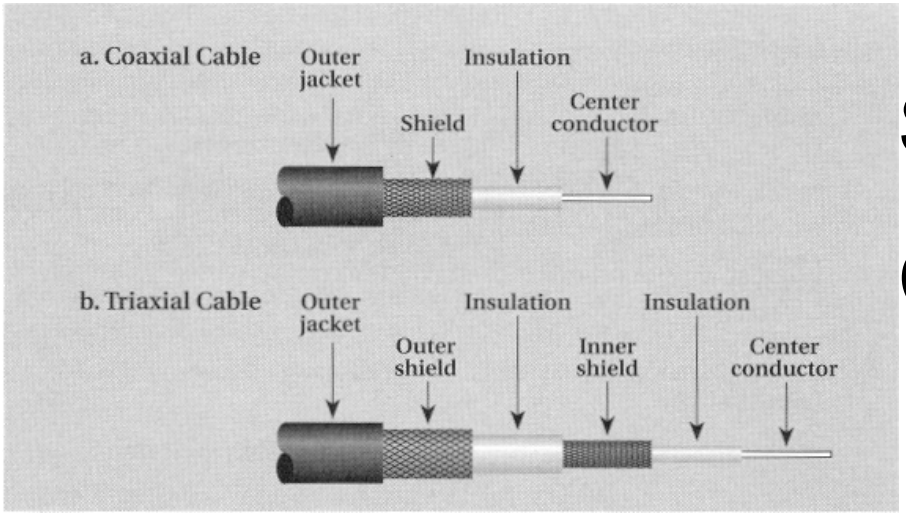
- Solution - use Kelvin connections for measurements below 100 Ω
- The sense current is as small as possible (pA)
- Special test-structure layout to do this on wafer

Low current measurements



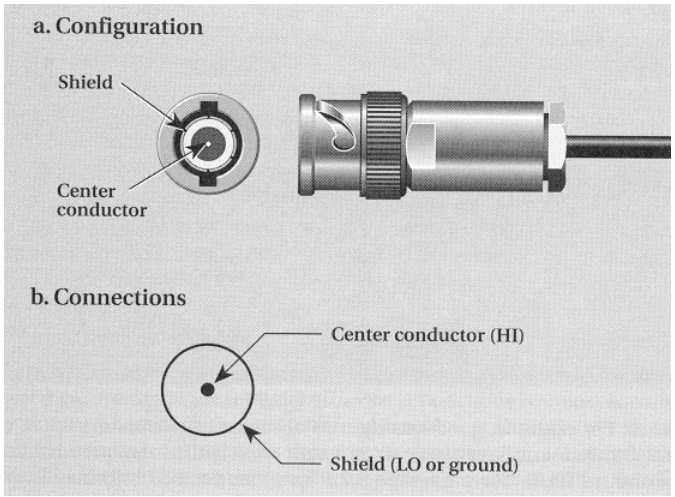
- Below 10 fA is possible with triax cables
- Voltage resolution of 1 μV
- Problems – leakage current in cables and outside interference (RF/noise)

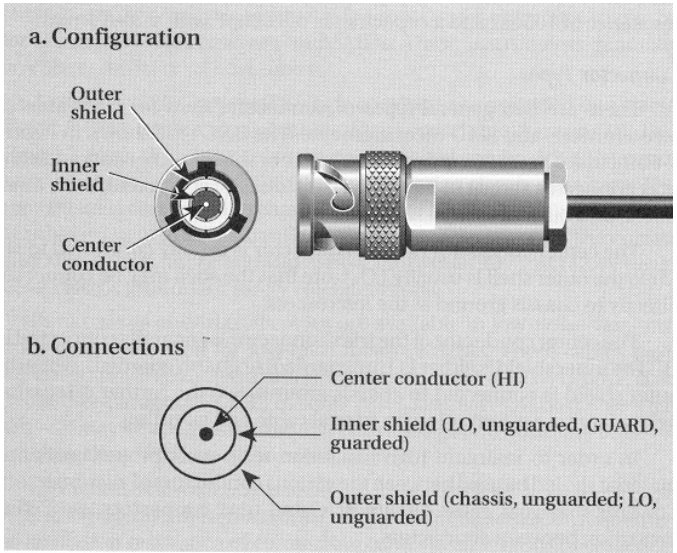
Low current measurements



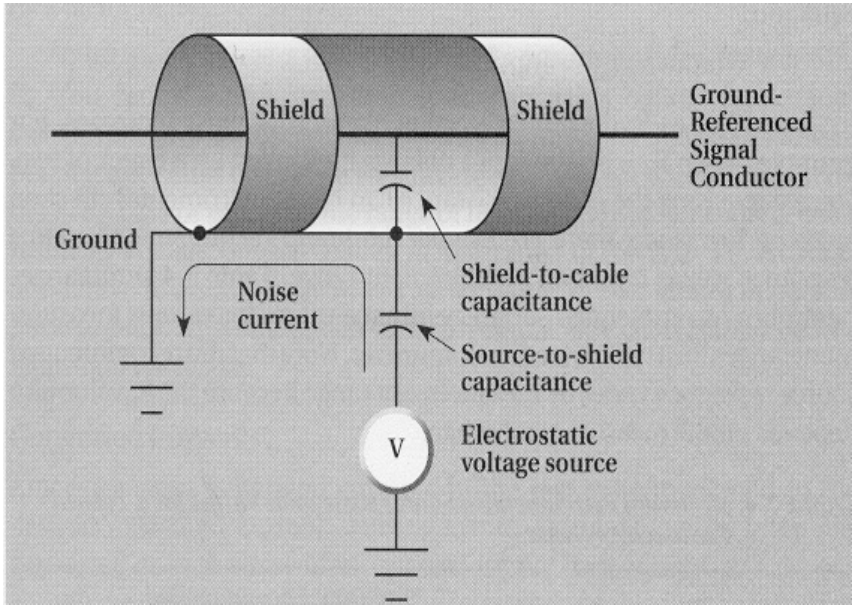
Shielded cable types

Coax & triax



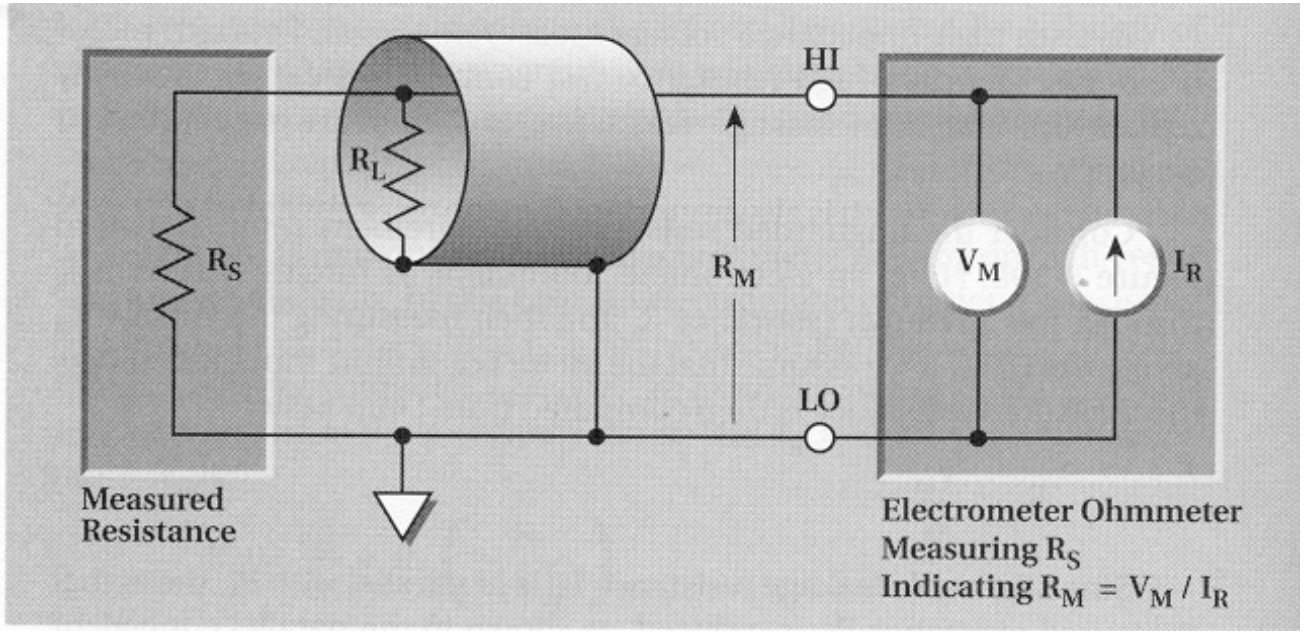


Low current measurements



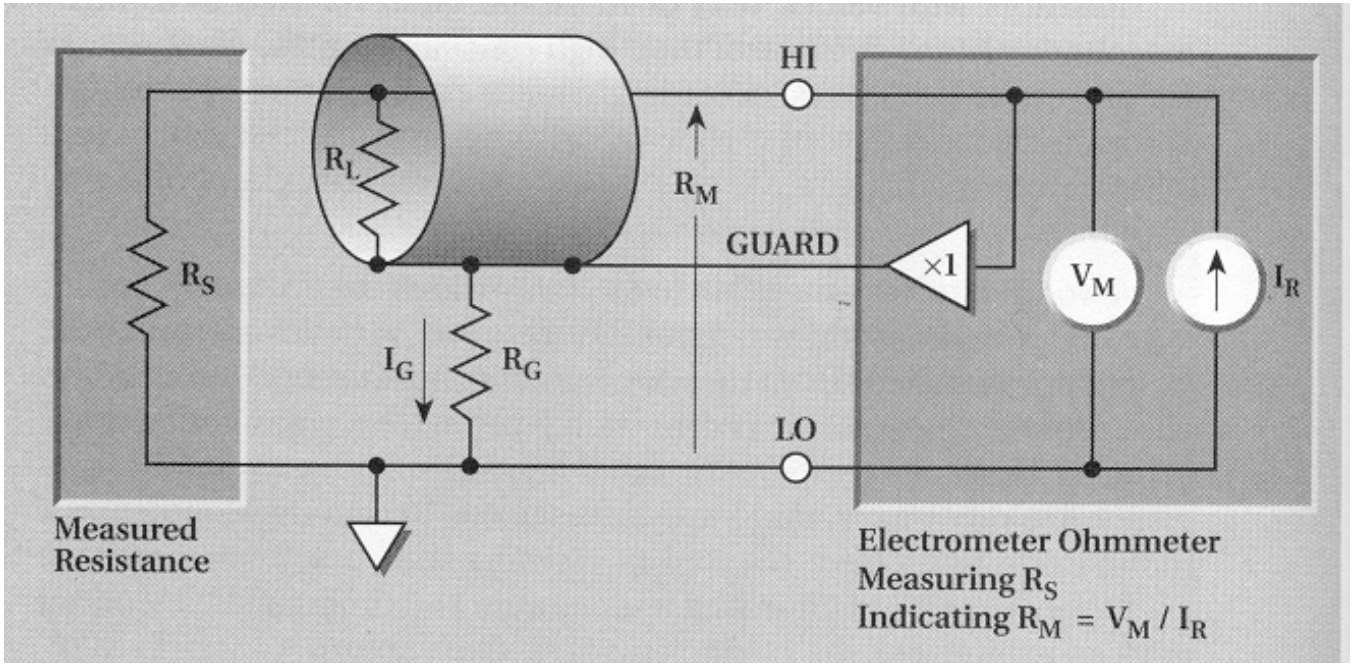
- Shielded cables reduce noise and interference
- Noise current is shunted to ground
- Voltage difference between signal conductor and grounded shield causes resistive leakage

Low current measurements



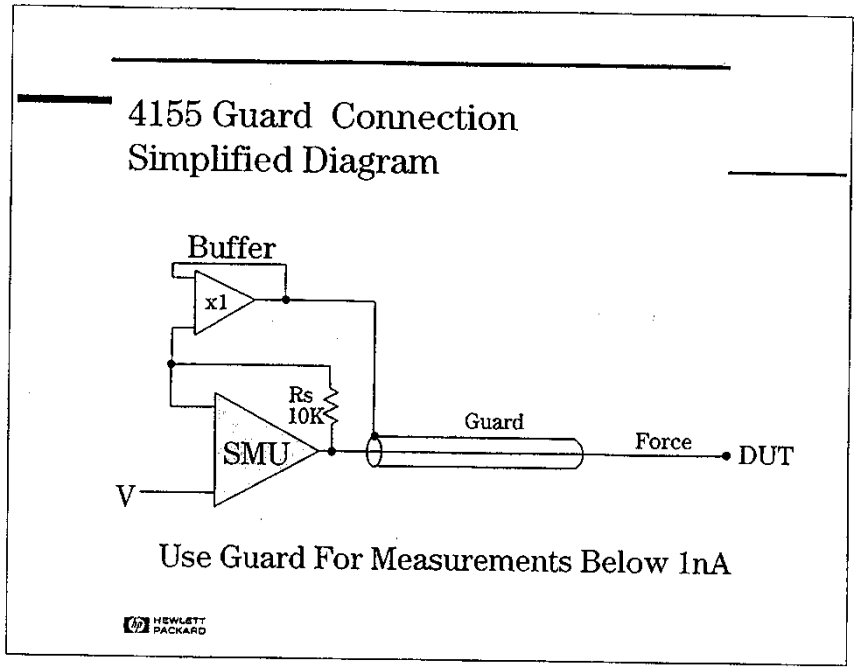
- Resistive leakage to shield around 1 nA, depends on applied voltage

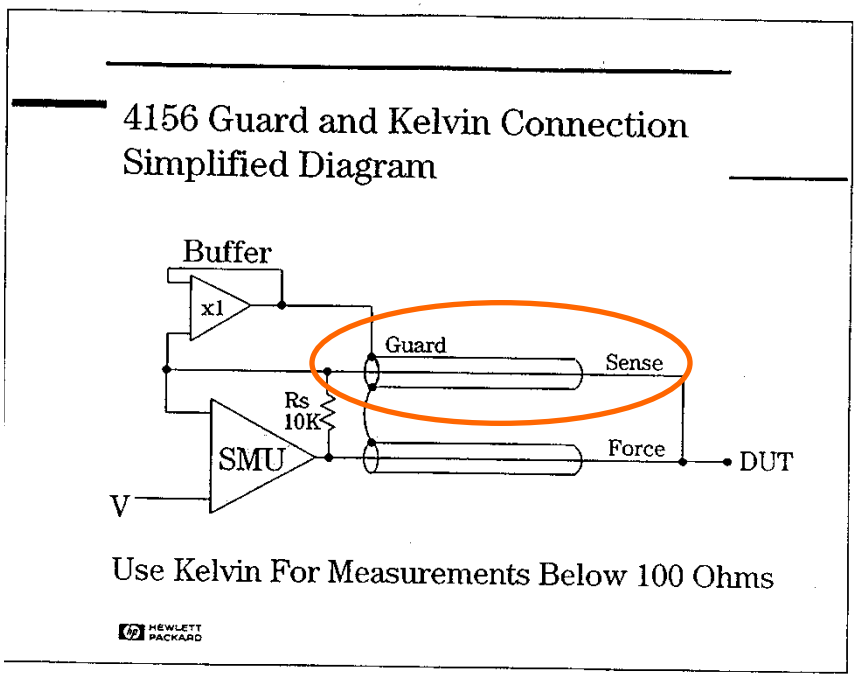
Low current measurements



- Use guard for measurements below 1 nA, solves problem of potential difference and resistive leakage
- Voltage buffer (x1 amplifier) sets the potential on the guard
- Leakage current flows between guard and ground potential

Low current measurements





- Special connection for guard potential using SENSE cable

Low current measurements

- The probe needle is also shielded, small radius 5 μm

L4: Electrical Characterization - Concept Test 4.1

4.1 Electrical characterization is an important step in the wafer fabrication flow: Which statements are true?

(One or more answers may be correct)

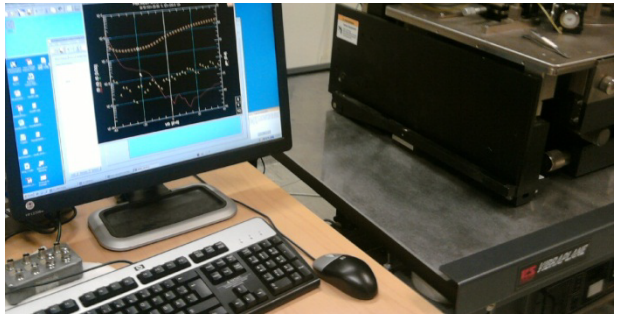
A. Measurements are usually done on completed wafers

B. Measurements are usually done during the process flow

C. Measurements are usually done on special test structures

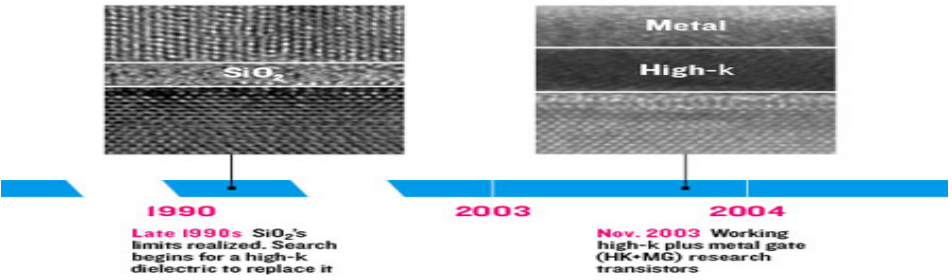
D. Measurements are usually done on transistors

E. None of the above.



Background – MOS gate oxide

Figure 1.3: Comparision between SiO_2 and *high-k* material



- New high-k material introduced to reduce gate leakage
- Thicker layer – lower leakage
- Bulk & interface decfects, long term stability, stress effects et.c. must be characterized

MOS gate oxide process stability

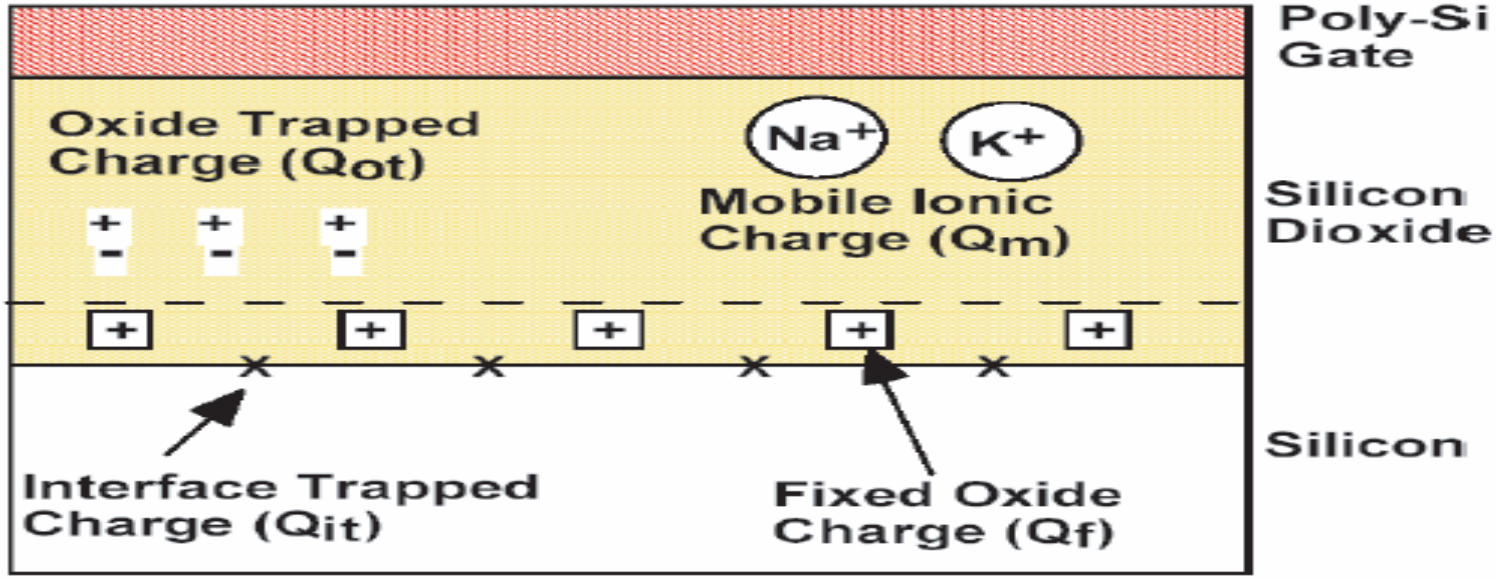


Figure 2.5: Types of charges and their distribution in the oxide

- Standard textbook picture of charge related oxide issues

MOS gate oxide process stability

- Gate oxide thickness and quality
- CV - thickness, trapped charge *(also VT-shift)*
- CP - interface states
- IV - oxide integrity, leakage current, breakdown field, charge-to-breakdown (QDB, TDDB) , hot-carrier injection (HCI), stress (NBTI)

CV /Impedance measurements

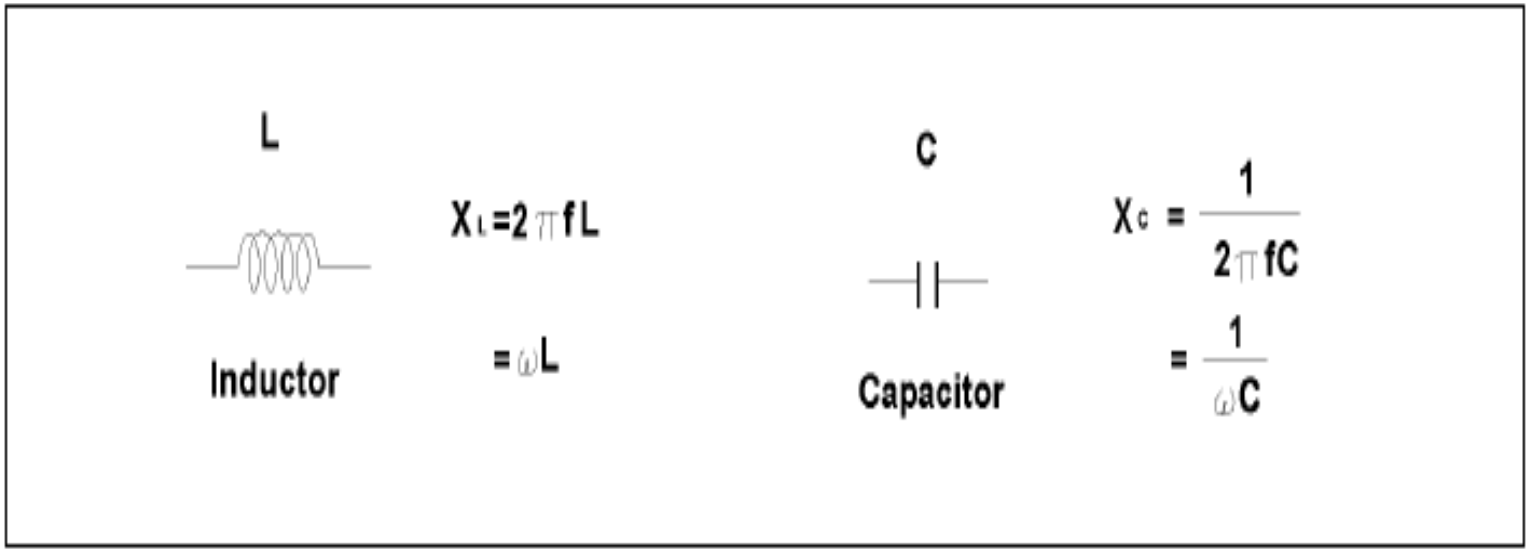


Figure 1-3. Reactance in two forms - inductive (X_L) and capacitive (Xc)

$$Z = \frac{1}{j\omega C} + j\omega L$$

CV applied to MOS

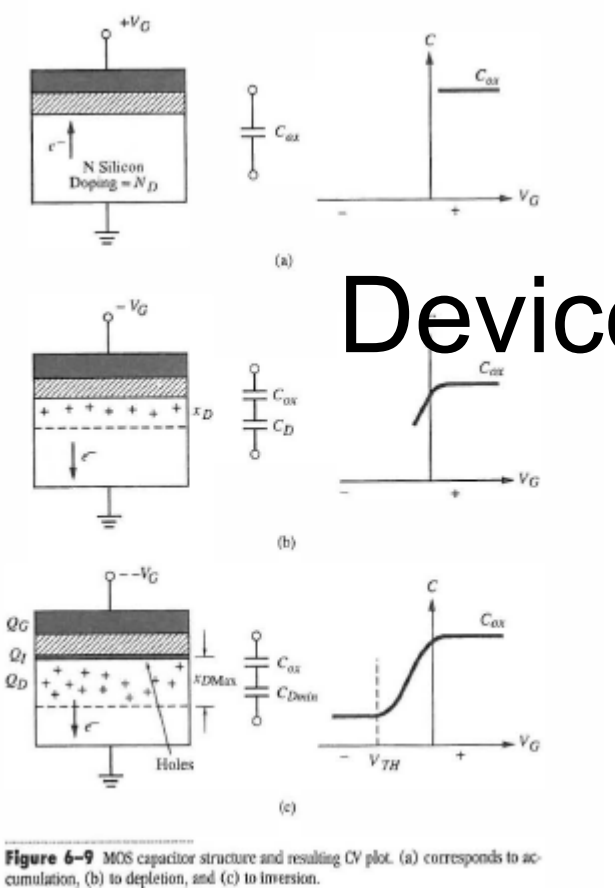


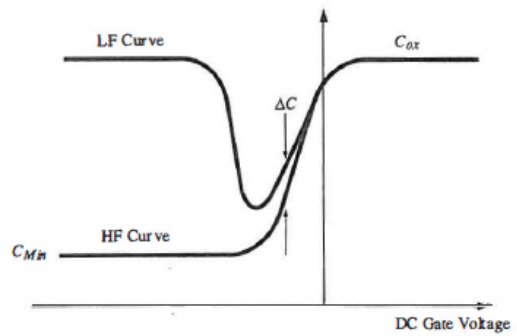
Figure 6–9 MOS capacitor structure and resulting CV plot. (a) corresponds to accumulation, (b) to depletion, and (c) to inversion.

The measured value is a sum of oxide and depletion capacitance

Device Physics!

$$Q_G = N_D x_D + Q_I$$

CV applied to MOS



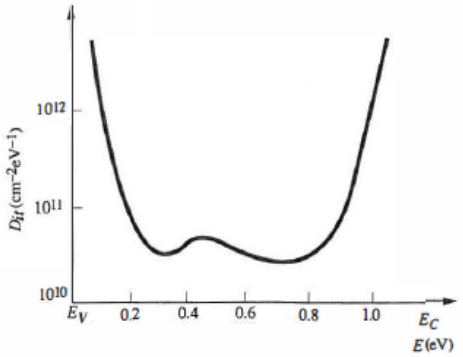


Figure 6–14 Typical experimental HF and LF CV curves used to extract the interface state density D_{it} as a function of energy in the bandgap. The D_{it} plot is typical of extracted data.

CV technique could be used to study defects, we focus on charge pumping later

CV applied to MOS

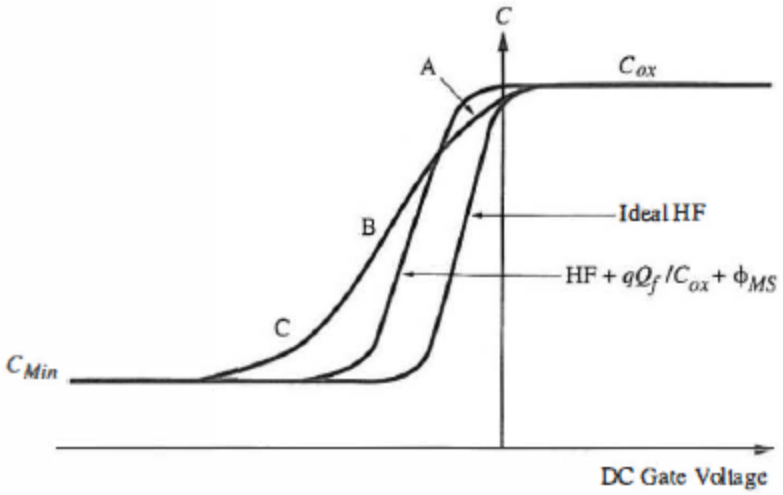


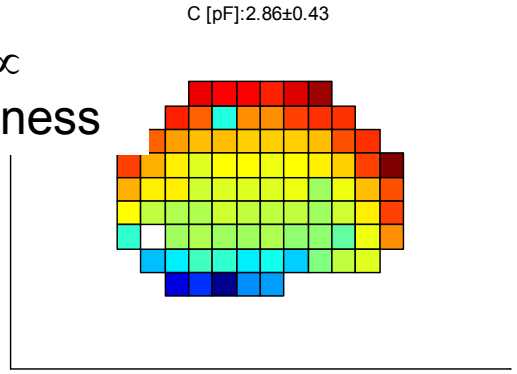
Figure 6–13 HF MOS CV curves illustrating some of the nonidealities that can be present in actual experimental structures. A, B, and C illustrate the effects of interface states with different energy levels in the silicon bandgap.

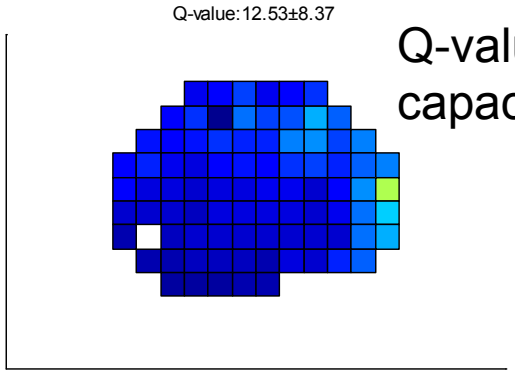
Real CV curves are non-ideal

MOS gate oxide process stability

- Gate oxide thickness and quality - 100 mm wafer map, metal-gate + high-k

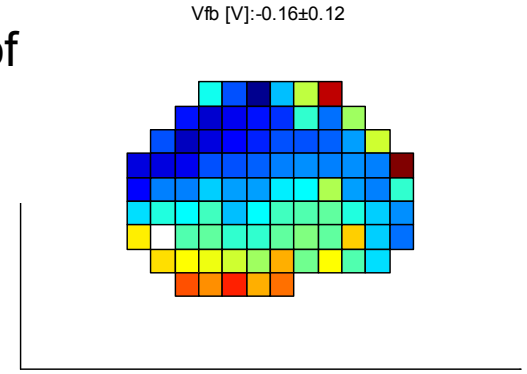
Capacitance ∝ 1/ oxide thickness

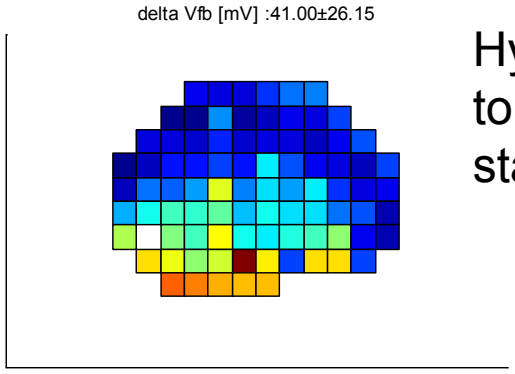




Q-value measure of capacitance/resistance

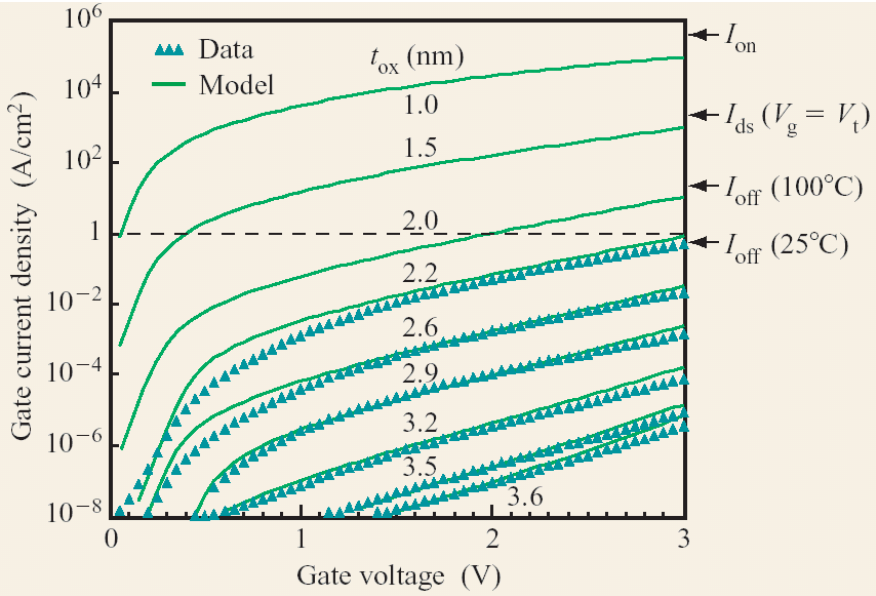
Influence of (trapped) charges





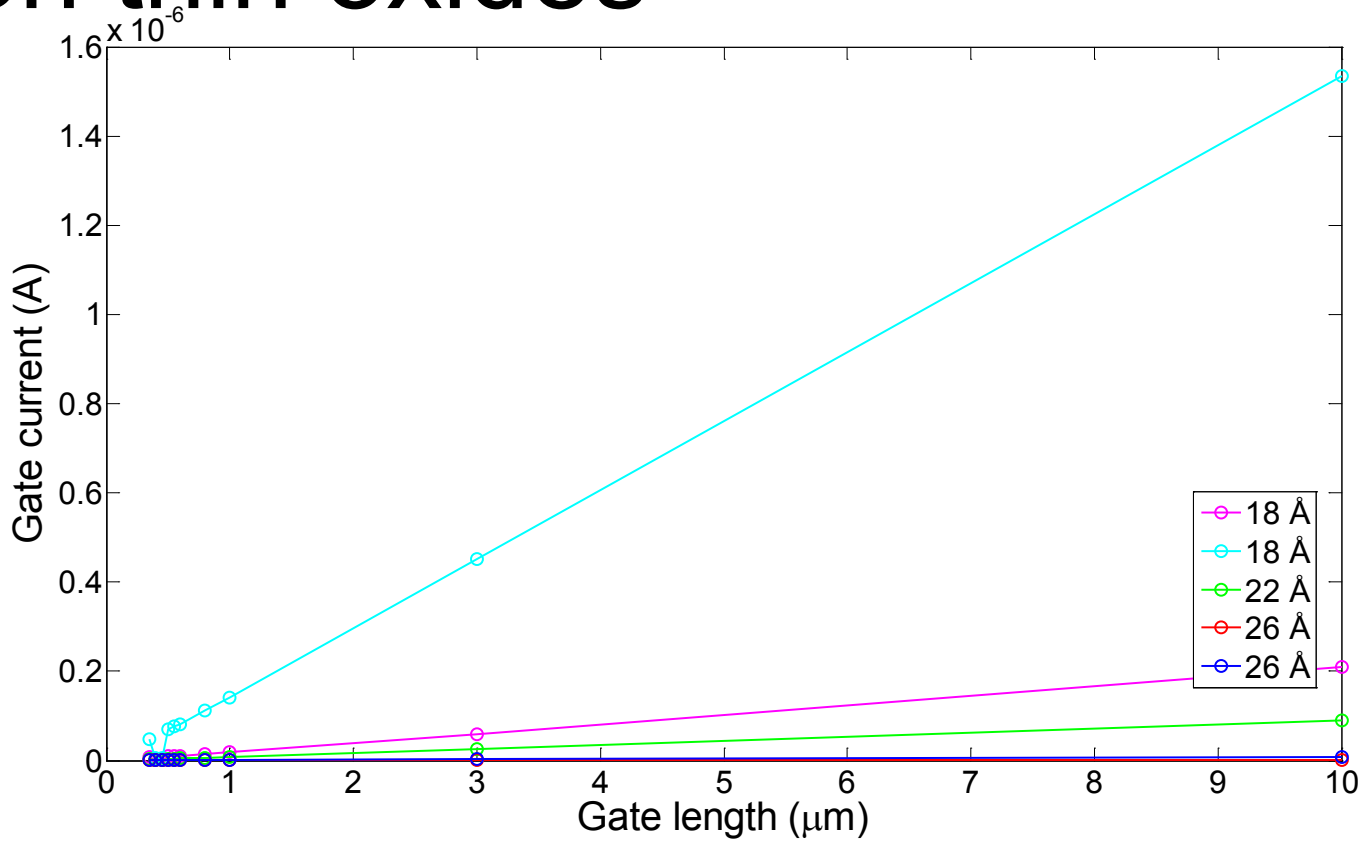
Hysteresis due to 'interface' states

MOS gate oxide process stability



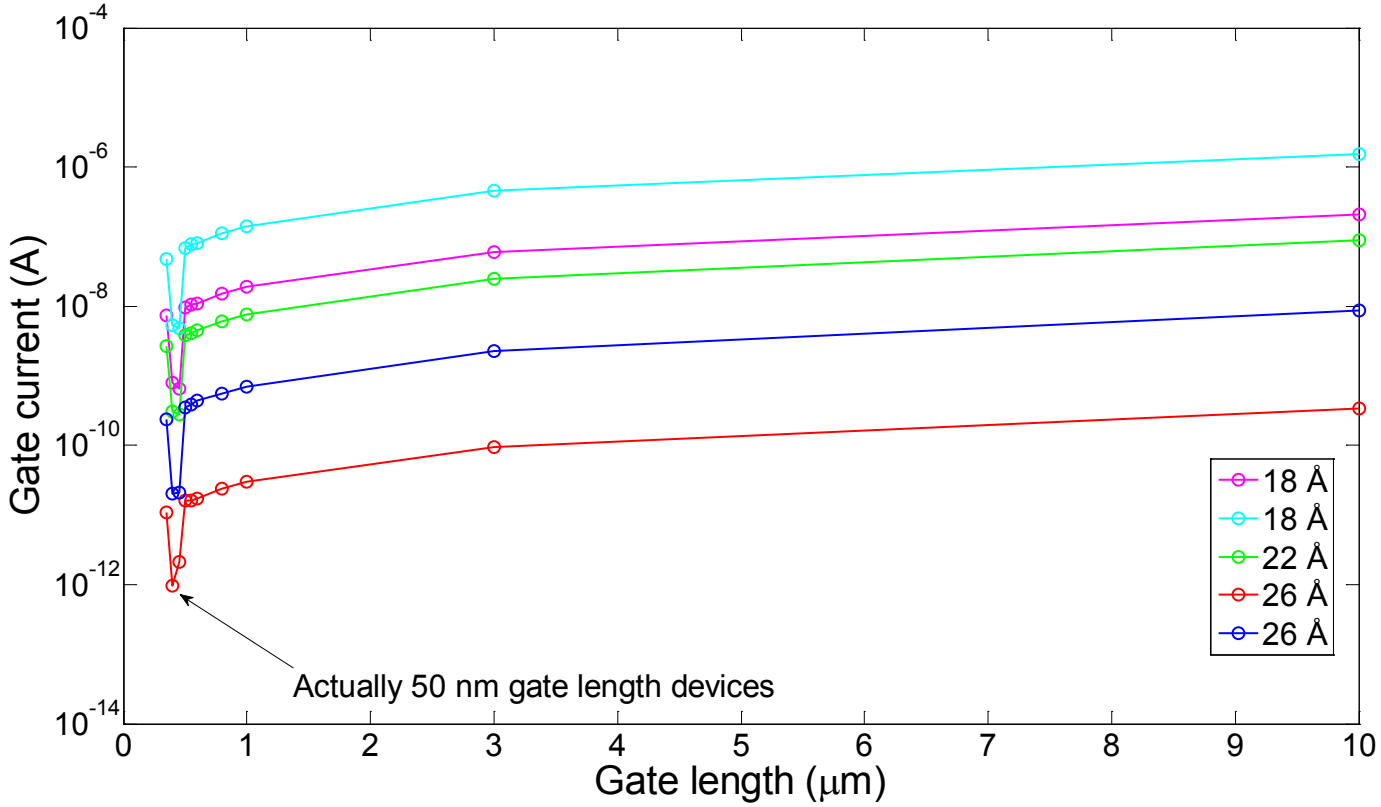
- Basic IV measurements of leakage current in thin gate oxides

IV on thin oxides



- Leakage strong function of oxide thickness => plot in log-scale

IV on thin oxides



- Leakage increased by 5 orders of magnitude by scaling oxide less than 50 %!
- Variation for nominally identical devices caused by?

MOS gate oxide process stability

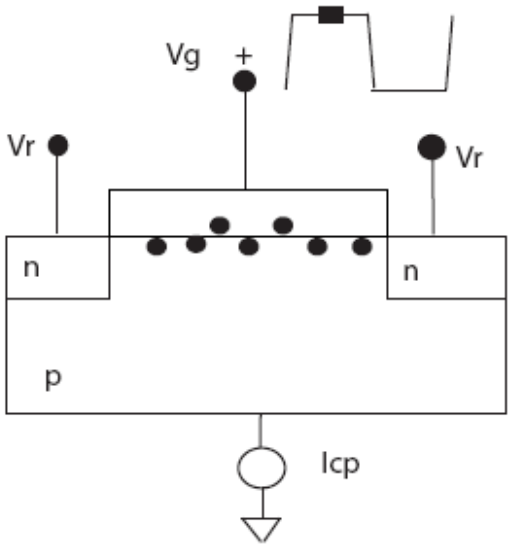
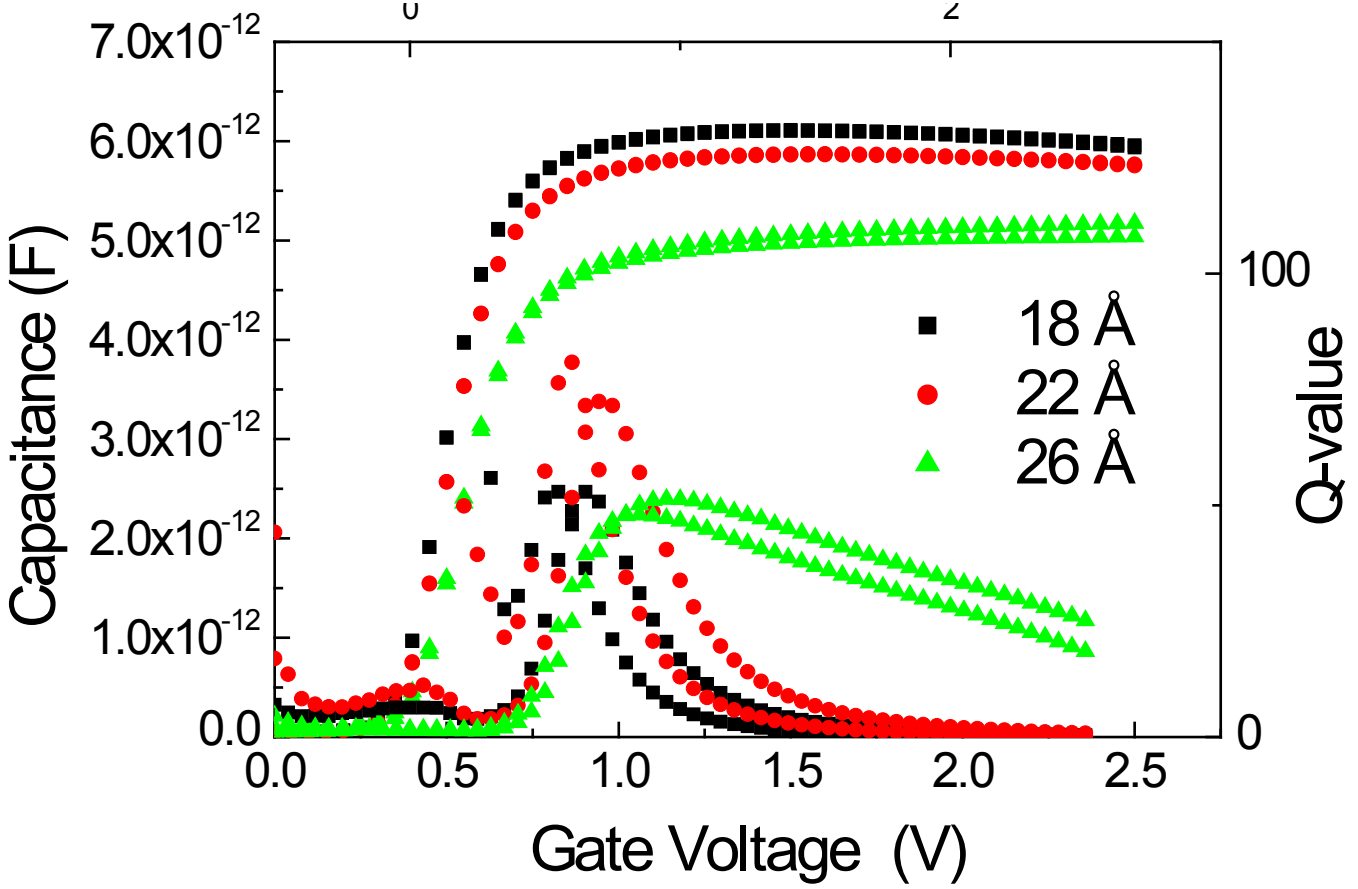


Figure 2.11: MOSFET used as test structure in inversion

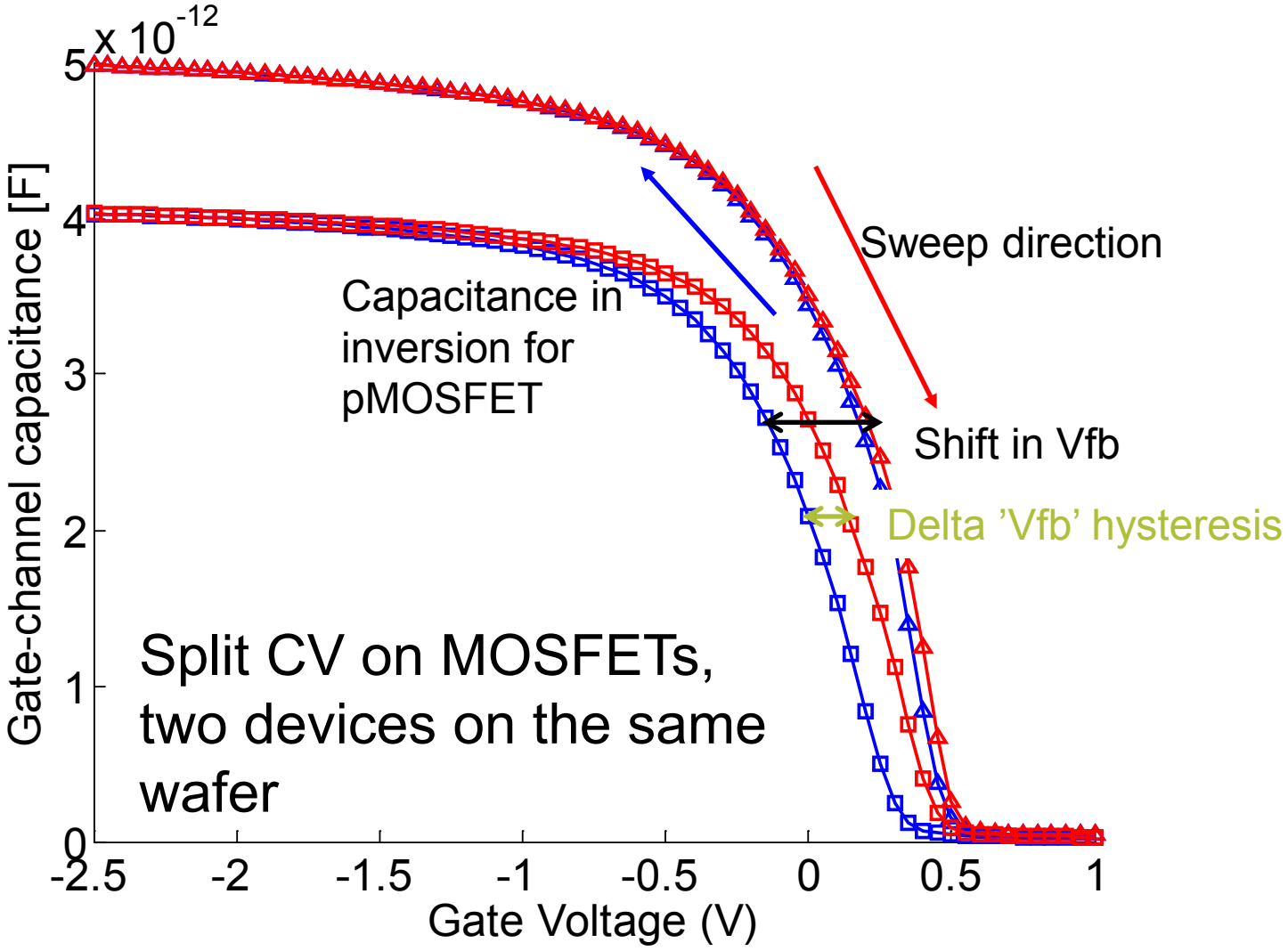
- Split CV on MOSFETs, source & drain reverse biased
- Use the actual device as a test-structure, measure the capacitance of the active carriers (electrons) in the channel inversion layer
- MOS capacitance probes the accumulated surface, using (holes)

CV on thin oxides

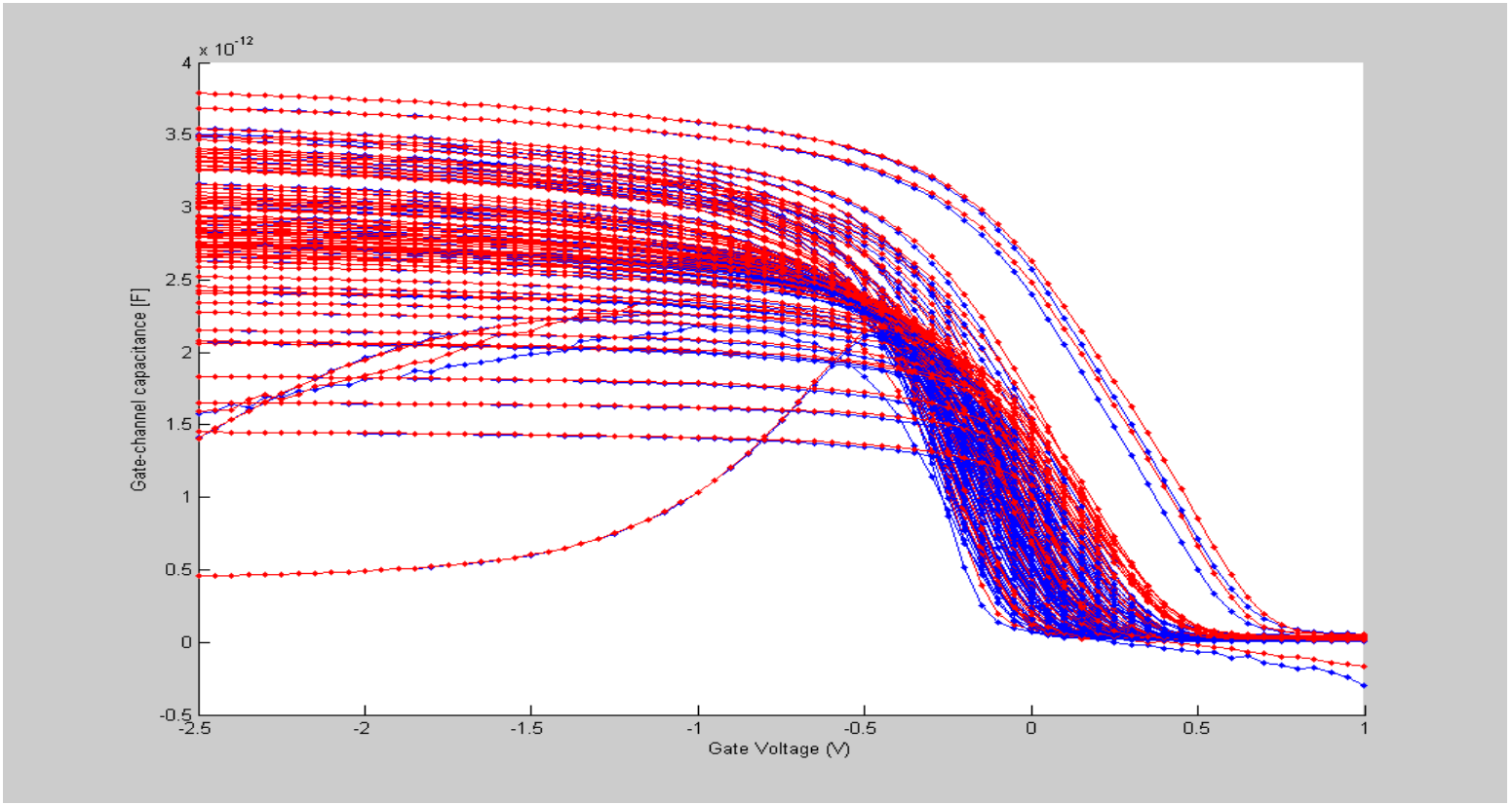


- Example of Q-value dependence on oxide thickness, frequency (100/300 kHz), and gate leakage current

MOS gate oxide process stability



MOS gate oxide process stability



- High-k HfO_2 based gate showed large variation over wafer

L4: Electrical Characterization - Concept Test 4.1

4.2 Electrical characterization is used to evaluate new materials: Which statements are true?

(One or more answers may be correct)

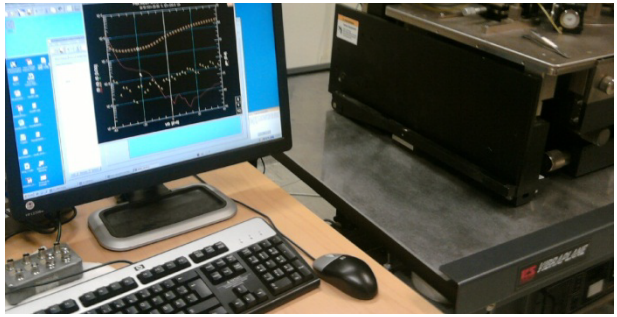
A. Capacitance-Voltage (CV) is the best technique to probe defects and thickness of thin oxides

B. Current-Voltage (IV) is the best technique to probe defects and thickness of thin oxides

C. Both IV and CV are needed to probe defects in thin oxides

D. Both IV and CV are needed to probe thickness of thin oxide

E. None of the above.



MOS gate oxide process stability

- 2 level charge pumping used to get 'response' from oxide/silicon interface states
- Carriers are trapped and released, for a pulsed gate voltage (V_G or V_{BASE}) , and the current (I_{CP}) is monitored

$$D_{it} = \frac{I_{cp}}{WLfq\Delta E}$$

$$\Delta E \approx 0.5 - 0.6\text{V}$$

$$2.7\times10^{11} \le D_{it} \le 5.2\times10^{11}\ [\text{cm}^{-2}\text{eV}^{-1}]$$

MOS gate oxide process stability

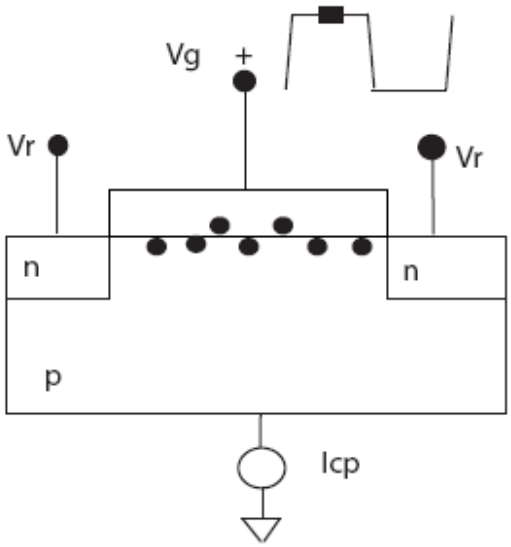
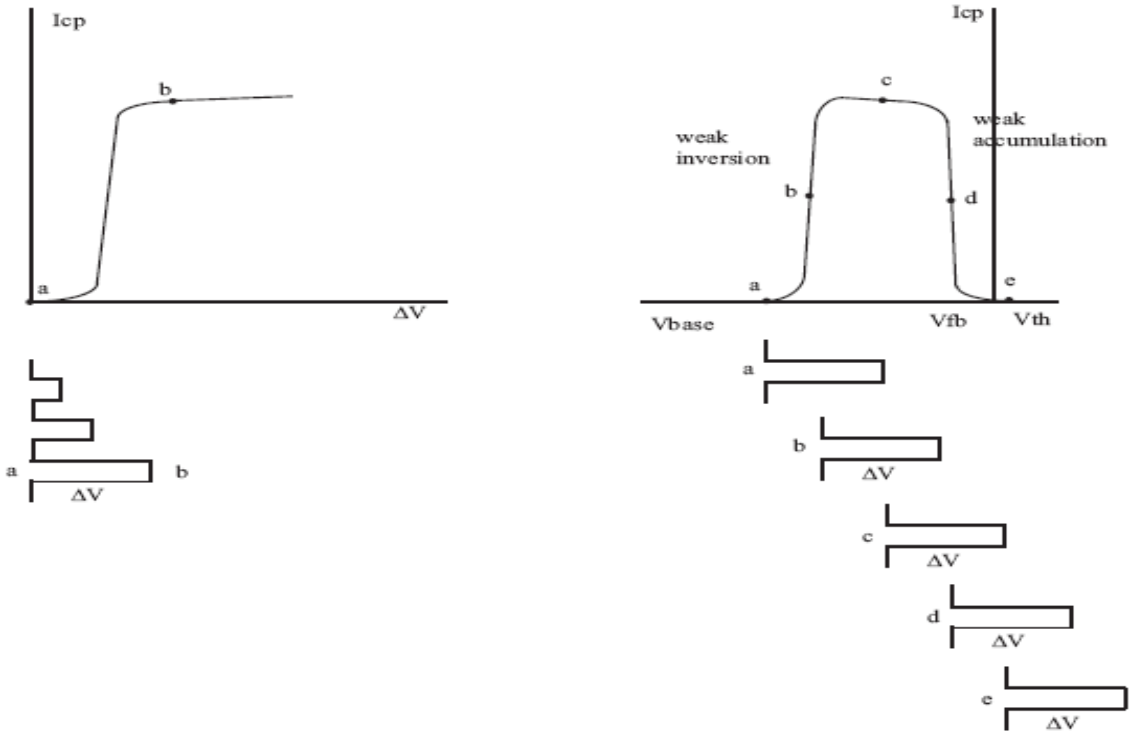


Figure 2.11: MOSFET used as test structure in inversion

- Trapped electrons at the interface recombine with holes supplied by the substrate node
- The net substrate substrate current is non-zero during a pulse period

MOS gate oxide process stability



- Sweeping base voltage V_{BASE} or amplitude $\Delta V$for the pulse
- Pulse generator with nanosecond rise/fall time needed

MOS gate oxide process stability

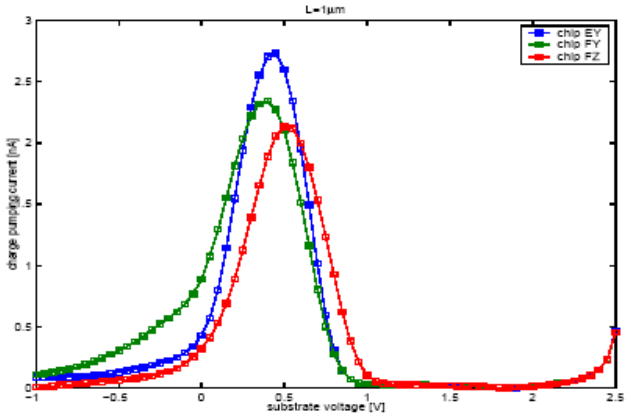


Figure 3.28: Charge pumping current versus substrate voltage

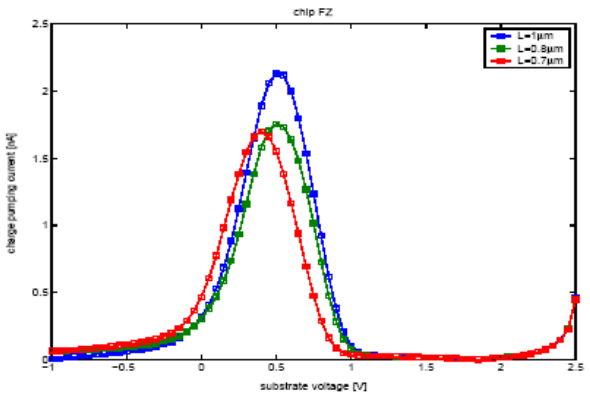


Figure 3.29: Charge pumping current versus substrate voltage for different pMOSFET gate lengths

- Maximum I_{CP} is a measure of D_{IT}
- I_{CP} should scale with gate length for short transistors according to equation

MOS gate oxide process stability

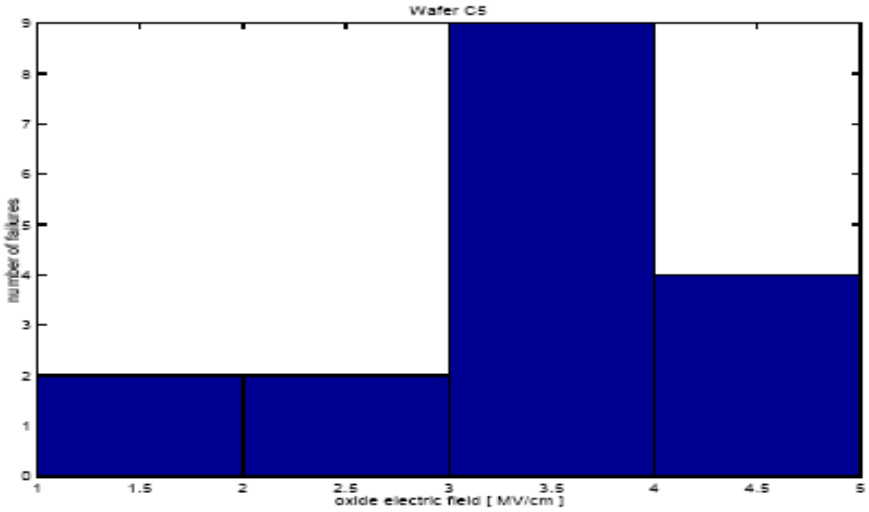


Figure 3.8: Number of failures versus oxide field for HfO_2 MOS capacitors on wafer C4

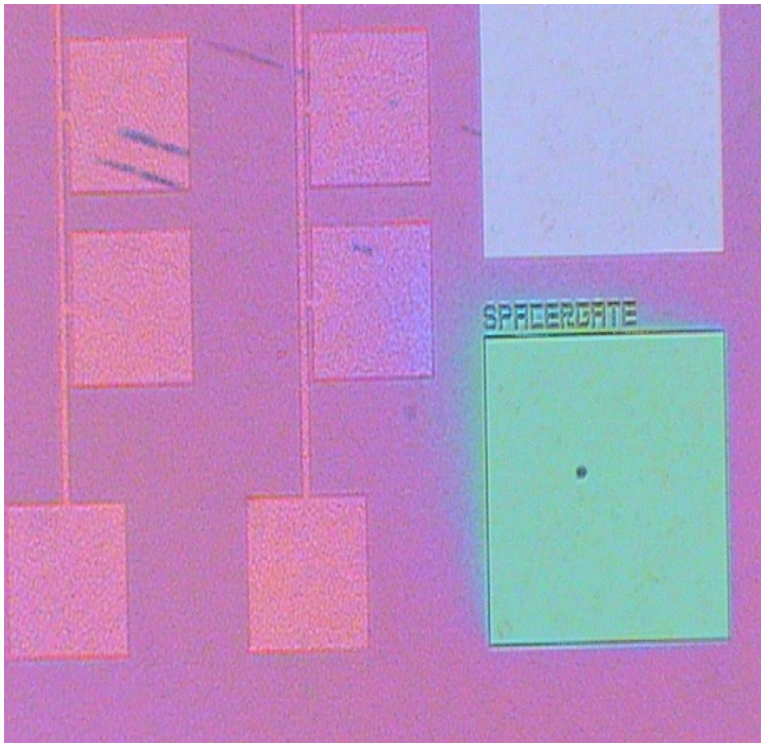
Oxide integrity can be tested by applying high field

Destructive – sweep until hard breakdown

Non-destructive – soft breakdown, inject charges into oxide by constant field/voltage/current stress, measure charge-to-breakdown

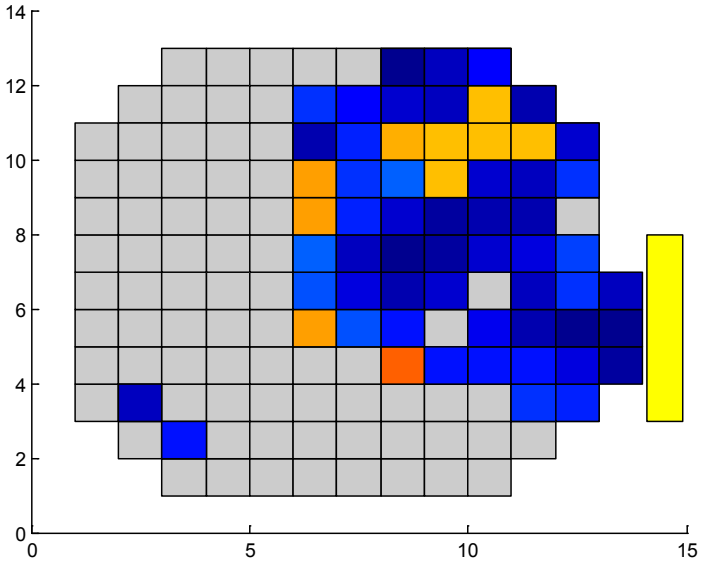
Useful acronyms: QBD, TDDB, HCI, NBTI, ...

Monitoring of process stability



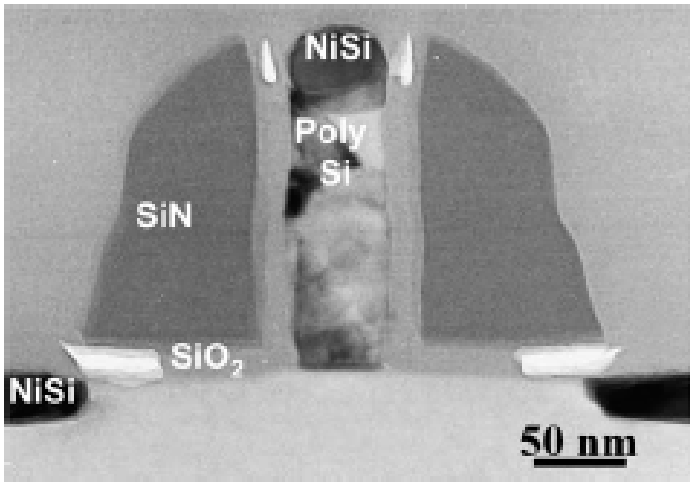
- Sheet-resistance measurements
- Uniformity of metal-silicide formation (resistance) across wafer
- Color shift (bluish to red) indicates problem!

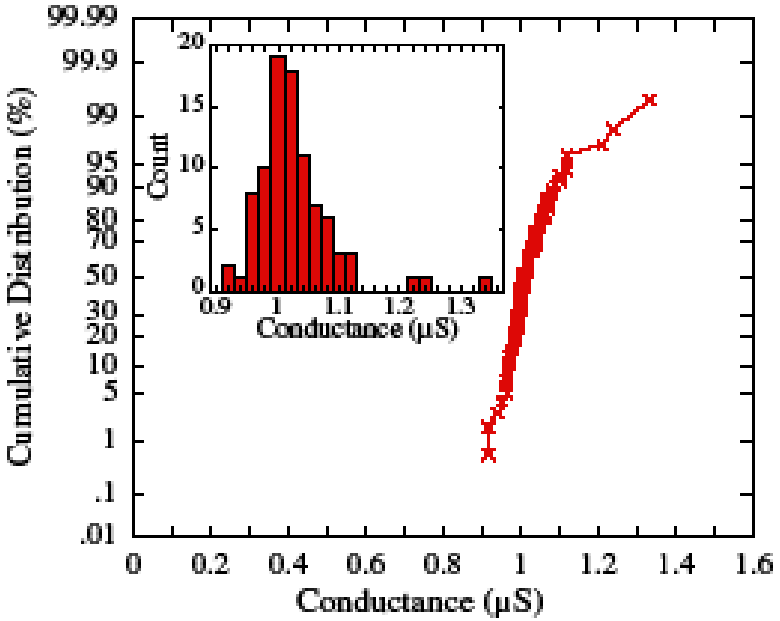
Monitoring of process stability



- Silicide formation on thin (10-20) nm SOI substrate (contacts for MOSFET source/drain)
- Problem – to much silicon is consumed before contact formation

Monitoring of process stability





- Gate length variation - critical dimension (CD) control
- Monitor gate electrode in 4-point resistor configuration across wafer, plot in Weibull graph!

About the lab

- Sign-up sheets distributed in class
- Mandatory preparation 48 h in advance, email to: vaziri@kth.se
- PREL Instructions for 2013 available from today, general theme IV measurement of high-k/metal gate wafers see above, also high mobility substrates
- Report due 1 week after completed lab, submit by email.

Summary

- Combination of IV, CV, chargepumping needed to characterize wafer mainly after completed process flow
- Low-level measurements use special shielding techniques and/or calibration
- Special layout of test structures for challenging measurements – sometimes the transistor is the test structure

Sources

- IEEE Spectrum, ”The high-k solution,” online, Oct, 2007.
- Keithley – Low level measurements 6th ed
- Keithley – Overcoming the Measurement Challenges of Advance Semiconductor Technologies 1st ed
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- Schroder – Semiconductor Material and Device Characterization
- Plummer et al – Silicon VLSI Technology
- Buono, Master Thesis, KTH, 2007