Deposition of dielectrics and metal gate stacks
(CVD, ALD)
Thin Film Deposition Requirements

Many films, made of many different materials are deposited during a standard CMOS process.

- Gate Electrodes (poly and metal)
- Vias
- Interconnects
- Interconnect insulators
- Shallow Trench Isolation (ATI)
- Dielectrics (High-k, DRAM)
- Diffusion barriers

Requirements or desirable traits for deposition:

1. Desired composition, low contaminates, good electrical and mechanical properties
2. Uniform thickness across wafer, and wafer-to-wafer
3. Good step coverage (“conformal coverage”)
4. Good filling of spaces
5. Planarized films
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CVD and ALD of polysilicon and dielectric thin films

- Chemical Vapor Deposition (CVD)
  - Basic definitions
  - Reactor designs
  - Examples
    - Polysilicon CVD
    - Silicon Dioxide CVD
    - Silicon Nitride CVD
  - Modeling
- Atomic Layer Deposition (ALD)
  - Basic Definitions
  - Reactor Designs
  - Example
    - Aluminum Oxide ALD
Chemical vapor deposition (CVD) - Definition

Constituents of the films are delivered through the gas phase. For CVD reactant gases are introduced into the deposition chamber and chemical reactions are used to deposit a thin film on the wafer surface.

Energy for this reaction can origin from heat, radiation or from a plasma.

Typical pressure range: 0.01 to 1 bar

Good film quality and step coverage.
CVD Process (compare L2)

1. Transport of reactants to the deposition region
2. Transport of reactants by diffusion from the main gas stream through the boundary layer to the wafer surface
3. Adsorption of reactants on the wafer surface
4. Surface processes: migration, decomposition, reaction, site incorporation
5. Desorption of byproducts from surface
6. Transport of byproducts through the boundary layer
7. Transport of byproducts from the deposition region
CVD Process (compare L2)

Growth limited by mass-transfer or surface reaction

\[ F_1 = h_g (C_g - C_s) \]
\[ F_2 = k_s C_s \]

- \( F_1, F_2 \): flux of reactant species to the wafer / of reactant consumed at surface
- \( h_g \): mass transfer coefficient (cm/s)
- \( C_g, C_s \): concentration of reactant species in gas / at surface
- \( K_s \): surface reaction constant

(Plummer 9-6, p.515)
The Grove Model for Epitaxial Growth
Growth limited by mass-transfer or surface reaction

\[ C_g = y C_t \]

\[ \Rightarrow k_s \left( \frac{C_t}{C_a} \right) y ; \quad C_s \rightarrow C_g \]

\[ \Rightarrow h_g \left( \frac{C_t}{C_a} \right) y ; \quad C_s \rightarrow 0 \]

\( k_s \): surface reaction constant
\( h_g \): vapor mass transfer coefficient (cm/s)

**Figure 9-7** Arrhenius plot of growth velocity (or deposition rate) vs. \( 1/T \) for CVD process. The net growth velocity is the result of the surface reaction and gas-phase mass transfer processes acting in series so that the slower of the two dominates at any temperature.

(Plummer Fig 9-7)
The Grove Model for Epitaxial Growth
Growth limited by mass-transfer or surface reaction

\[ C_g = y C_t \] where \( y \) is the mole fraction and \( C_t \) is the total number of gas molec/cm\(^3\) →

\[ v = \frac{F}{N} = \frac{k_s h_g}{k_s + h_g} \left( \frac{C_t}{C_a} \right) y \]

\[ v \approx k_s \left( \frac{C_t}{C_a} \right) y \]

\[ v \approx h_g \left( \frac{C_t}{C_a} \right) y \]

---

*(Figure 9-7)* Arrhenius plot of growth velocity (or deposition rate) vs. \( 1/T \) for CVD process. The net growth velocity is the result of the surface reaction and gas-phase mass transfer processes acting in series so that the slower of the two dominates at any temperature.

(Plummer Fig 9-7)
Chemical vapor deposition (CVD) - Methods

Thermal CVD typically between 400-900°C:
Low-pressure CVD (LPCVD): 0.1-1 torr
Atmospheric-pressure CVD (APCVD)

Lower temperature budget by:
Plasma-enhanced CVD (PECVD)
Photon-induced CVD: Photon generation by UV or laser.

Present CVD trends:
Rapid Thermal CVD (RTCVD) > 10 torr
High-density PECVD (HDPCVD)

CVD parameters important for film properties:
Reactor design
Temperature
Pressure
Fundamental CVD Aspects

Compare Lecture 2: CVD Epitaxy!

• Thermodynamics and kinetics
• Transport phenomena
• Nucleation and thin film growth

Effect of supersaturation* and temperature on thin film structure:

*Vapor that has higher partial pressure than its equilibrium vapor pressure is supersaturated
CVD and ALD of polysilicon and dielectric thin films

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    - Aluminum Oxide ALD
CVD basic reactor design

Hot wall

Cold wall

Trend is from hot-wall batch reactors to cold-wall single-wafer tools
**Thermal CVD**

LPCVD hot-wall. Most common in production. Both horizontal and vertical design.

APCVD. Not very common today.

(Fig. 6.1 VLSI Techn. p. 236)
The LPCVD workhorse system for Si$_3$N$_4$, silicon oxide and polysilicon
Plasma Enhanced CVD (PECVD)

• Non-thermal energy to enhance processes at lower temperatures.
• Plasma consists of electrons, ionized molecules, neutral molecules, neutral and ionized fragments of broken-up molecules, excited molecules and free radicals.
• Free radicals are electrically neutral species that have incomplete bonding and are extremely reactive. (e.g. SiO, SiH3, F)
• The net result from the fragmentation, the free radicals, and the ion bombardment is that the surface processes and deposition occur at much lower temperatures than in non-plasma systems.

Details on plasma reactors: see Lecture 7.1 Etching

(Plummer 9-14, p.528)
High Density Plasma CVD (HDPCVD)

Properties

• Extension of PECVD
• Remote high density plasma with independent RF substrate bias
• Allows simultaneous deposition and sputtering for better planarization and void-free films
• Mostly used for SiO$_2$ deposition in backend of the line (BEOL) processes
Modern RTCVD process

Deposition module in cluster tool

Similar to LT epi process:

Single-wafer system > 10 torr
Hydrogen as carrier gas
In situ doping
In situ cleaning (HCl or NF₃)
## Characteristics of various CVD processes

<table>
<thead>
<tr>
<th>PROCESS</th>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
<th>APPLICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>APCVD</td>
<td>Simple Reactor, Fast Deposition, Low Temperature</td>
<td>Poor Step Coverage, Particle Contamination</td>
<td>Low Temperature Oxides, both doped and undoped</td>
</tr>
<tr>
<td>(Low Temperature)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPCVD</td>
<td>Excellent Purity and Uniformity, Conformal Step Coverage, Large Wafer Capacity</td>
<td>High Temperature Low Deposition Rate</td>
<td>High Temperature Oxides, both doped and undoped, Silicon Nitride, Poly-Si, W, WSi₂</td>
</tr>
<tr>
<td>PECVD</td>
<td>Low Temperature, Fast Deposition, Good Step Coverage</td>
<td>Chemical (e.g. H₂) and Particulate Contamination</td>
<td>Low Temperature Insulators over Metals, Passivation (Nitride)</td>
</tr>
</tbody>
</table>

(Table 1. ULSI Technology p. 211)
CVD and ALD of polysilicon and dielectric thin films

• Chemical Vapor Deposition (CVD)
  • Basic definitions
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    • Polysilicon CVD
    • Silicon Dioxide CVD
    • Silicon Nitride CVD
  • Modeling

• Atomic Layer Deposition (ALD)
  • Basic Definitions
  • Reactor Designs
  • Example
    • Aluminum Oxide ALD
Polysilicon

Used in VLSI for:
- n+ or p+ gate electrode material in CMOS (see below)
- n+ emitter contact in BIP (see below), so-called polysilicon emitter technology
- Diffusion source (double-poly bipolar process for formation of E and B) (see below)
- Local interconnects
- Deep-trench filling (see below)
- Resistances

Also poly-SiGe of interest as common p+-gate electrode in CMOS (so-called mid bandgap material)
Example: Polysilicon CVD

Application

• n⁺ or p⁺ gate electrode material in CMOS (see below)
• n⁺ emitter contact in BIP (“polysilicon emitter technology”)
• poly-SiGe of interest as common p+-gate electrode in CMOS (mid bandgap material)
• Diffusion source (double-poly bipolar process for formation of E and B)
• Local interconnects
• Deep-trench filling
• Resistances
• Solar cells
• Thin Film Transistors (TFTs)

…
**CMOS structure with poly gate electrode:**

![CMOS structure diagram]

**Double-poly bipolar structure:**

![Double-poly bipolar structure diagram]

Also many other applications of polysilicon: Solar cells, TFTs etc
Conventional LPCVD process

Polysilicon deposition using silane at 600-650°C

\[ \text{SiH}_4 \leftrightarrow \text{SiH}_2 + \text{H}_2 \]
\[ \text{SiH}_2 \leftrightarrow \text{Si} + \text{H}_2 \]

Alternative: \( \text{Si}_2\text{H}_6 \) (disilane). Permits lower deposition temperatures.

**FIGURE 5**
The effect of silane concentration on the polysilicon deposition rate.

(VLSI Tech. Fig. 5 p. 243)
Arrhenius plot of SiH$_4$ deposition at different partial pressures of SiH$_4$

Activation energy of 1.7 eV

(VLSI Tech. Fig. 5 p. 240)
**Microstructure of polysilicon**

- **T > 625°C**: Columnar growth. Preferential (110) orient.
- **T < 575°C**: Amorphous
- **T ~ 600°C**: Microcrystalline polysilicon

Exact microstructure depends on a number of factors: Pressure, dopants, temperature, thickness, recrystallization etc

Grain growth important for final electrical properties

---

Fig. 4. Average crystallite size $\bar{s}$ for LPCVD Si-layers, as-grown (○: interface, ●: surface) and annealed at 1000°C (■: interface, ■: surface) as a function of $T_d$.

Growth and Physical Properties of LPCVD Polycrystalline Silicon Films, G. Harbeke, SOLID-STATE SCIENCE AND TECHNOLOGY 1984
Example: Polysilicon CVD

Temperature and Pressure Dependence

Poly-Silicon:
- 620 °C
- 160 mTorr

α-Silicon:
- 580 °C
- 400 mTorr

- grain size >> functional structure
- surface roughness complicates etch stop
- smooth surface
- gas phase nucleation
- recrystalization after annealing
Microstructure of polysilicon

T > 625°C  Columnar growth. Preferential (110) orient.
T < 575°C  Amorphous
T ~ 600°C  Microcrystalline polysilicon

Exact microstructure depends on a number of factors: Pressure, dopants, temperature, thickness, recrystallization etc

Grain growth important for final electrical properties

Figure 9-32  TEM cross sections of CVD polycrystalline films deposited at 625°C: (a) as-deposited, undoped film, showing the thin grains in a columnar structure; (b) as-deposited phosphorus-doped film, showing much larger grain size; (c) annealed (1000°C), undoped film, showing little grain growth as compared to (a); (d) annealed (1000°C), phosphorus-doped film, showing evidence of grain growth as compared to (b). Reprinted with permission of the Electrochemical Society [9.19].

(Plummer Fig 9-32 p. 560)
Doping of polysilicon

Doping by diffusion, ion implant or in situ during CVD deposition

\[ \rightarrow \text{resistivity} < 1 \ \text{mWcm after annealing} \]

Ion implantation most common today

Ion implantation most common today (VLSI Techn, Fig. 8 p. 245)

- Dopant diffusion is typically around 1000x faster in grain boundaries than inside the grains
- Complex behavior of dopants in polysilicon during subsequent processing:
  - Segregation of Ph and As (but not B) to the grain boundaries
  - Dopant diffusion is typically around 1000x faster in grain boundaries than inside the grains

(VLSI Techn, Fig. 8 p. 245)
In situ doping of polysilicon

Difficult process in batch furnace, in particular during n-type doping. Non-uniformities and very low deposition rates. Requires quartz cage for wafers in LPCVD tube. Preferably deposited in amorphous phase and subsequently crystallized.

FIGURE 6
The effect of dopants on the polysilicon deposition rate at 610°C. (VLSI Techn, Fig. 6 p. 243)
Example: SiO₂ CVD

Application
Isolation in active devices as well as between metal layers

Essential reactions for SiO₂ depositions:

**LPCVD:**
Tetraethylorthosilicate (TEOS): (liquid source!)
\[ \text{Si(OC}_2\text{H}_5)_4 \] 650-750°C

Low-temperature oxide (LTO):
\[ \text{SiH}_4 + \text{O}_2 \] 400-450°C

Note: Dichlorosilane (DCS): \( \text{SiCl}_2\text{H}_2 + \text{N}_2\text{O} \) uncommon today

**PECVD:**
\[ \text{SiH}_4 + 2\text{N}_2\text{O} \] 200 - 350°C
\[ \text{Plasma TEOS} \] 300 - 360°C
Sub-atmospheric CVD (SACVD):

TEOS + O₃  

300-550°C

Typically TEOS results in porous films which may need densification. Also C in films!

PECVD films generally contains a lot of H or N

Christoph Henkel / Mikael Östling
Comparison of TEOS and LTO: Arrhenius plots

FIGURE 12
Arrhenius plots for the low-pressure deposition of SiO₂. (After Adams and Capio, Ref. 30, for the TEOS data and after Learn, Ref. 29, for the silane-oxygen data.)

(VLSI Techn. p.252)
Example: SiO$_2$ CVD

Comparison of TEOS and LTO: Step coverage

(a) typical for TEOS  
(c) typical for LTO

Difference rather due to different sticking than surface transport  
(sticking of TEOS lower than for LTO)
Example: SiO₂ CVD

Phosphosilicate Glass (PSG)

Phosphorous introduced in SiO₂
  • Gettering of impurities in intermetallic dielectric
  • Permitting glass flow at high temperature around 1000-1100°C

Glass flow improves poor step coverage of LTO:

By adding B → B-PSG = BPSG

B will help to reduce softening point to 800°C
Silicon nitride

Applications:

For mask in LOCOS process (barrier against oxygen diffusion)
Passivation layer: (barrier against $\text{H}_2\text{O}$, sodium)

**LPCVD**

$$3\text{SiH}_2\text{Cl}_2 + 4\text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 6\text{HCl} + 6\text{H}_2 \quad 650-800^\circ\text{C}$$

(most common)

$$3\text{SiH}_4 + 4\text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12\text{H}_2 \quad 700-900^\circ\text{C}$$

Excess of $\text{NH}_3$ used in reaction!

**PECVD**

$\text{Si}_3\text{N}_4$ used for passivation using silane and $\text{NH}_3$ at 200-400$^\circ\text{C}$
Contains much H! Usually non-stoichiometric!
Stress can be tuned by plasma parameters
New trend: High-density plasma systems
Properties of silicon nitride

Large tensile stress.

Typically max 2000 Å Si₃N₄ can be deposited on Si

<table>
<thead>
<tr>
<th>TABLE 4 Properties of silicon nitride</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition</td>
</tr>
<tr>
<td>Temperature (°C)</td>
</tr>
<tr>
<td>Composition</td>
</tr>
<tr>
<td>Si/N ratio</td>
</tr>
<tr>
<td>Atom % H</td>
</tr>
<tr>
<td>Refractive index</td>
</tr>
<tr>
<td>Density (g/cm³)</td>
</tr>
<tr>
<td>Dielectric constant</td>
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<tr>
<td>Resistivity (ohm·cm)</td>
</tr>
<tr>
<td>Dielectric strength (10⁶ V/cm)</td>
</tr>
<tr>
<td>Energy gap (eV)</td>
</tr>
<tr>
<td>Stress (10⁹ dyne/cm²)</td>
</tr>
</tbody>
</table>

(VLSI Techn. p. 263)
CVD and ALD of polysilicon and dielectric thin films

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    • Silicon Nitride CVD
  • Modeling

• Atomic Layer Deposition (ALD)
  • Basic Definitions
  • Reactor Designs
  • Example
    • Aluminum Oxide (Al₂O₃) ALD
Atomic Layer Deposition (ALD)

**Definition:**
- CVD-based deposition mode
- But: Gases introduced sequentially
- But: Self-limiting surface reaction

<table>
<thead>
<tr>
<th></th>
<th>ALD</th>
<th>MBE</th>
<th>PVD</th>
<th>CVD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step coverage</td>
<td>Excellent</td>
<td>Poor</td>
<td>Poor</td>
<td>Varies</td>
</tr>
<tr>
<td>Deposition rate</td>
<td>Acceptable</td>
<td>Acceptable</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>Thickness uniformity</td>
<td>Excellent</td>
<td>Acceptable</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>Material availability</td>
<td>Acceptable</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Acceptable</td>
</tr>
<tr>
<td>Defects</td>
<td>Acceptable</td>
<td>Excellent</td>
<td>Poor</td>
<td>Acceptable</td>
</tr>
</tbody>
</table>
Atomic Layer Deposition (ALD)

**Definition:**
- CVD-based deposition mode
- But: Gases introduced sequentially
- But: Self-limiting surface reaction

**Application:**
- Thin films from 1-500 nm
- High aspect / 3D structures
- Good film quality
- Most viable sub-5 nm deposition technique
Precursor desorption

Precursor decomposition

Typical: RT to 400°C

Insufficient reactivity

Surface sites

Ideal ALD

Atomic Layer Deposition (ALD)

The principle of ALD is based on sequential pulsing of chemical precursor vapors, forming one atomic layer during each pulse sequence.

- Precise control of depositions down to the atomic scale
- Deposit nanometer thin films with special properties
- Pinhole free coatings, extremely uniform in thickness
- Deposition deep inside pores, trenches, and cavities
- A wide variety of thin films can be deposited (dielectrics and metals)
- A wide range of precursors available (gas, liquid or solid)
- Described in terms of “cycles”, a cycle consists of four basic steps

System in Electrum at KTH used in electronics, MEMS…
ALD: Reactor Designs

Thermal ALD
- Chemistry relies on substrate temperature
- Radiative heating or direct heat transfer
- Traveling wave cross-flow reactors and perpendicular flow (showerhead)
- Limited pressure range 1-10 Torr
- Single wafer or batch configuration commercially available from ASM, Picosun, Beneq, Cambridge Nanotech, etc.

Radical enhanced ALD
- Chemistry thermally activated for one of the precursors
- Radical source is attached to reactor or the reactor consists of radical beams in UHV
- Reactors based on this concept are so far not commercially available, but separate radical sources are, such as the MKS R*Evolution

ALD: Reactor Designs

Direct plasma ALD
- Precursor injection through a showerhead or in the background (due to low pressure (1-10 mTorr))
- Ion bombardment (ion energy > ~100 eV) is an issue when depositing on sensitive substrates
- Reactors commercially available from ASM etc.

Remote plasma ALD
- ICP plasma source most common
- Wide pressure range (1-1000 mTorr)
- Low ion bombardment (energy < ~20 eV)
- Commercially available from Oxford Instruments, Cambridge Nanotech etc.

Basic Principle of Atomic Layer Deposition

- $\text{CH}_3\text{AlCH}_3$
- $\text{H}_3\text{C}$
- $\text{CH}_3$
- $\text{Al}$
- $\text{H}_2\text{O}$

Diagram showing pulse and purge times ($t_{\text{pulse}}$, $t_{\text{purge}}$) with N$_2$ flow and TMA (Tributylaluminium).
Basic Principle of Atomic Layer Deposition

Byproduct

$\text{CH}_3$ $\text{CH}_3$

$\text{Al}$

$\text{H}_3\text{C}$

$\text{H}_4\text{C}$

$\text{H}_3\text{O}$ $\text{H}_3\text{O}$ $\text{H}_3\text{O}$ $\text{H}_3\text{O}$

$\text{Al}$

$\text{CH}_4$

$\text{H}_3\text{C}$ $\text{CH}_3$

TMA

$\text{N}_2$ flow

$\text{t}_{\text{Pulse}}$ $\text{t}_{\text{Purge}}$

$\text{t}$

Chopped Henkel / Mikael Östling KTH
Basic Principle of Atomic Layer Deposition

Byproduct

Excess of precursor

N₂ flow

TMA

Pressure

Time

$\text{CH}_3$ $\text{Al}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$

$\text{H}_3\text{C}$

$\text{CH}_3$
Basic Principle of Atomic Layer Deposition

The diagram illustrates the process of atomic layer deposition (ALD) with the following components:

- **Chemical Reagents**:
  - TMA (Trimethylaluminum) $\text{H}_3\text{C} \text{CH}_3 \text{Al}$
  - Water $\text{H}_2\text{O}$

- **Gas Flow**:
  - Nitrogen ($\text{N}_2$) flow

- **Time Phases**:
  - Pulse ($t_{\text{Pulse}}$)
  - Purge ($t_{\text{Purge}}$)

- **Temperature**:
  - Thermal ALD process
    - La-precuror @ 140°C
    - Zr-precuror @ 75°C
  - Heated substrate holder (250 or 300 °C)

- **Device**:
  - MFC (Mass Flow Controller)

This process is characterized by sequential pulses of precursor gases and purges of inert gas, leading to the deposition of thin, uniform layers on the substrate.
Basic Principle of Atomic Layer Deposition

Byproduct

\[ \text{CH}_4 \]

\[ \text{Al} \]

\[ \text{H}_2\text{O} \]

Byproduct

Moisture
Basic Principle of Atomic Layer Deposition

H₂O deposition cycle

CH₄ byproduct

N₂ flow

t_Pulse t_Purge t_Pulse t_Purge t

TMA H₂O deposition cycle
Basic Principle of Atomic Layer Deposition

Al₂O₃ on fluorinated W surface

R.W. Wind, JAP 105, 074309 (2009)
Basic Principle of Atomic Layer Deposition

Si, H-terminated surface
Atomic Layer Deposition (ALD)

Properties and Applications

• High-k dielectrics

<table>
<thead>
<tr>
<th>ALD Film</th>
<th>Min. Deposition Temperature °C</th>
<th>Dielectric Constant (k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃</td>
<td>&gt;25</td>
<td>6-9</td>
</tr>
<tr>
<td>SiO₂</td>
<td>&gt;100</td>
<td>3.9</td>
</tr>
<tr>
<td>HfO₂</td>
<td>&gt;80</td>
<td>&gt;15</td>
</tr>
<tr>
<td>TiO₂</td>
<td>&gt;80</td>
<td>&gt;20</td>
</tr>
<tr>
<td>Ta₂O₅</td>
<td>&gt;100</td>
<td>&gt;22</td>
</tr>
<tr>
<td>ZrO₂</td>
<td>&gt;80</td>
<td>&gt;14</td>
</tr>
</tbody>
</table>
• Metal Gate eliminate poly-Si depletion effects
• Solve pinning of $V_T$ of poly-Si on high-k dielectrics
• High aspect ratios and 3D structures

Plasma Enhanced ALD TiN + ALD HfSiO

And references therein.
• High aspect ratios and 3D structures

Atomic Layer Deposition (ALD) - Advantages

**Perfect films:**
- Thickness control to atomic level (deposited one atomic layer at a time)
- Pinhole free films, even over very large areas
- Excellent repeatability
- Wide process windows: ALD is not sensitive to temperature or precursor dose variations
- Amorphous or crystalline depending on substrate and temperature
- Digital control of sandwiches, heterostructures, nanolaminates, mixed oxides, graded index layers and doping
- Oxides, nitrides, metals, semiconductors possible
- 100% film density guarantees ideal material properties (n, E_{bd}, k, etc)

**Conformal Coating:**
- Perfect 3D conformality, 100% step coverage: uniform coatings on flat, inside porous and around particle samples
- Atomically flat and smooth coating
- Large area thickness uniformity

**Challenging Substrates:**
- Gentle deposition process for sensitive substrates, no plasma needed (though it is available as an option)
- Low temperature deposition possible (RT-400 °C)
- Coats on everything, even on teflon
- Excellent adhesion due to chemical bonds at the first layer
- Low stress because of molecular self assembly