Nanofabrication Lab – Process Development for High-k Dielectrics

Each lab group consists of 4 to 5 students.

The dates of these Labs are:

Lab 1

Date 14.02.2013

Time: 8-12 am

Lab 2

Date 14.02.2013

Time: 1-5 pm

Lab 3

Date 15.02.2013

Time: 8-12 am

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Nanofabrication Lab – Process Development for High-k Dielectrics

Laboratory exercise in IH2655 Design and Characterization of Nano- and Microdevices

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Location/Meeting place: Electrum building, in front of restaurant, Isafjordsgatan 26

Time: According to sign-up in the Lecture

Tasks

1. Individual theoretical task, emailed to chenkel@kth.se at least **24 hours** before lab starts.
2. Lab exercise with instructor 3-4 hours
3. Individual report written and handed in within **1 week** after the lab exercise

NOTE: STUDENTS WHICH HAVE NOT HANDED IN A WELL PREPARED THEORETICAL TASKS WILL NOT BE ALLOWED TO ATTEND THE LAB.

NOTE: LAB REPORTS ARE DUE ONE WEEK AFTER THE LAB!

IF YOUR LAB REPORT IS LATE IT WILL NOT BE CONSIDERED FOR RAISING THE FINAL COURSE GRADE.

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Theoretical task

In order to prepare for the lab you should write a first draft of the lab report. You will only have to write the introduction part of the report in this draft. Use 300-400 words. The draft should be written as a **continuous** text and cover these questions:

- What is the purpose of this experiment?
- What type of equipment is being used?
- What are the main issues regarding the scaling of gate oxides in MOS transistors and how are we trying to solve them?

The pre-reading material includes answers to the above and below questions.

Part of it can be downloaded on the course webpage:

1. Overview of Atomic Layer Deposition: Leskelä and Ritala, "Atomic Layer Deposition Chemistry: Recent Developments and Future Challenges", Angew. Chem. Int. Ed., 42, 5548 –5554, 2003 (Nanofab_Leskela_Atomic_Layer_Deposition.pdf)
2. Overview High-k Materials (suggested reading: first 8 pages): Wilk et al, "High-k gate dielectrics: Current status and materials properties considerations" J. Appl. Phys., 89(10), 2001, (Nanofab_Wilk_High_K_Gate_Dielectrics.pdf)

The following Plummer chapters are also relevant:

- Chapter 10.2.2, Plasma Etching, pages 619-628
- Chapter 5.2.2 and 5.2.3, Lithography, pages 208-230

Also, take a quick look at the virtual lab tour:
http://www.it.kth.se/courses/2B1242/index.htm?tour.htm

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Introduction

Continuous scaling of MOS transistors has led to the replacement of SiO_2 as the gate dielectric with new materials, generically referred to as ***high-k dielectrics***, which provide a higher permittivity ε than silicon dioxide. This allows increasing the gate capacitance C_{ox} without having to use extremely thin oxides, which would lead to intolerably high leakage currents by means of direct tunneling. This can be understood using equation 1,

$$C_{ox} = (\varepsilon_{ox} A) / t_{ox} \qquad (1)$$

where A is the area of the capacitor and t_{ox} is the gate oxide thickness. ***Please elaborate in your report!***

While variants of hafnium oxides are currently used in industry, they are not expected to sustain further scaling and new materials are actively investigated. This research includes surface treatments prior to oxide deposition as well as gate electrode materials, since new gate oxides require a new design of the gate stack (i.e. combination of the transistor channel, the gate oxide and the gate electrode). Finally, substantial research is invested in understanding the effects of these new materials on carrier transport in the transistor channel.

In this lab we will conduct an experiment to develop a process for depositing a high-k/metal gate stack with suitable characteristics for MOS transistors. The experiment will be carried out in the Electrum cleanroom laboratory. Here, an atomic layer deposition (ALD) system will be used in order to deposit a thin layer of Titanium Oxide (TiO_2). The aim of the lab is to use this system to realize MOS capacitors with different variants of Ti-based gate stacks in order to evaluate the influence of process parameters on the quality of the resulting devices.

Each group will start with one 4 inch (100) Si wafer and will deposit both a gate dielectric and a titanium-nitride (TiN) gate electrode layer using the ALD system. Different parameters such as pressure, gas flow, temperature and number of cycles will be varied among the groups. The wafers will be masked with a pattern by optical lithography and then etched by reactive ion etching (RIE). Electrical data from these MOS capacitors will be discussed and evaluated in the workshop.

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Security

The lab assistant will go through the security protocol with the group before entering the cleanroom.

The basic rules are as follows:

- Security glasses should be worn at all times (You will get them before you enter the cleanroom)
- All use of equipment must be done under supervision of the lab assistant
- Handling of corrosive chemicals must be done with rubber gloves and a visor
- There are four different types of alarms: red, yellow/blue, yellow, and blue. If a red or yellow/blue alarm is sounded proceed immediately to the nearest emergency exit and go to the appointed meeting place.

Lab instructions

The questions below will have to be answered during the respective process steps and will be discussed during the lab. You should be prepared to answer them on your own.

High-k/metal gate formation by ALD

A Silicon substrate is cleaned with a standard cleaning procedure and loaded in the ALD system, where the gate stack is deposited. The relevant ALD process parameters are varied according to the experimental plan provided by the instructor during the lab.

- Clean wafer
- Load wafer through a load-lock chamber
- Adjust process parameters and start deposition process

Questions (will be asked during the Lab and you should be able to answer them):

- What is the basic principle of ALD?
- What prerequisites should a high-k dielectric have? (Think about band-gap, dielectric constant, band-offsets, ...)
- Is the interface towards Si better with TiO_2 or SiO_2?
- Are metals better or worse than poly-Silicon as a gate electrode? What metal would you choose in case of p-doped substrates?

Lithography

The wafer is exposed using a lithography stepper. The mask used is a standard metallization mask for MOSFET processing, providing square contact pads which will be used to define the capacitor area.

- Spin on positive photoresist 700-1.2
- Expose the wafer in the stepper
- Develop the wafer
- Hard-bake the wafer at 110 °C for 20 minutes
- Using an optical microscope, measure the resolution of the pattern defined by the lithography

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Questions:

- Why is the lithography room yellow?
- What is the target thickness of the resist?
- What is the mask size reduction ratio for the stepper?
- What is the resolution of the lithography?

TiN etch and resist removal

The titanium nitride gate electrode is etched in a RIE system and the resist is subsequently removed in an O_2 barrel etcher.

- Etch TiN in RIE tool
- Remove photoresist in barrel etcher.

Questions:

- What chemical reaction happens during the O_2 plasma etch?
- What is the etch rate of TiN, assuming its thickness is 60 nm?

Written report

The report should be written individually. Copying text in the report directly from the lab instructions or other sources is strictly forbidden. The report may not exceed 3 pages, following the structure:

a) Introduction (completed in preliminary version 24 h before start of the lab!!!)

b) Experimental details

c) Conclusions

Each section should be written as a **continuous text**. All questions stated above should be answered in the report. They may not be given as a list of questions and answers, but instead, as a part of the discussion in the text. Also, number all figures and tables. Use appropriate units.

The report will be graded Fail (F), Good (G) and Very Good (VG). If the report is not good enough to pass the student will have a chance to improve it. The grade VG can improve your final course grade.

The report is due 1 WEEK after the lab.

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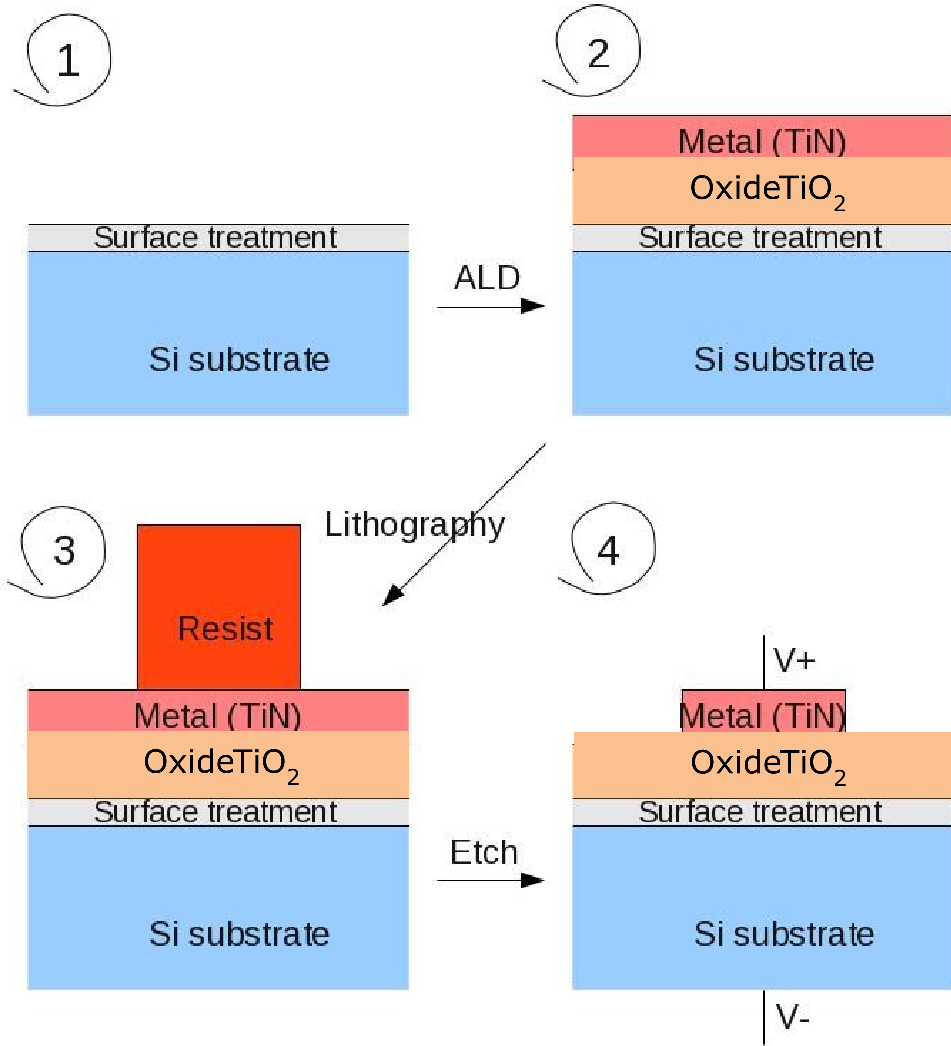
Schematic process flow



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