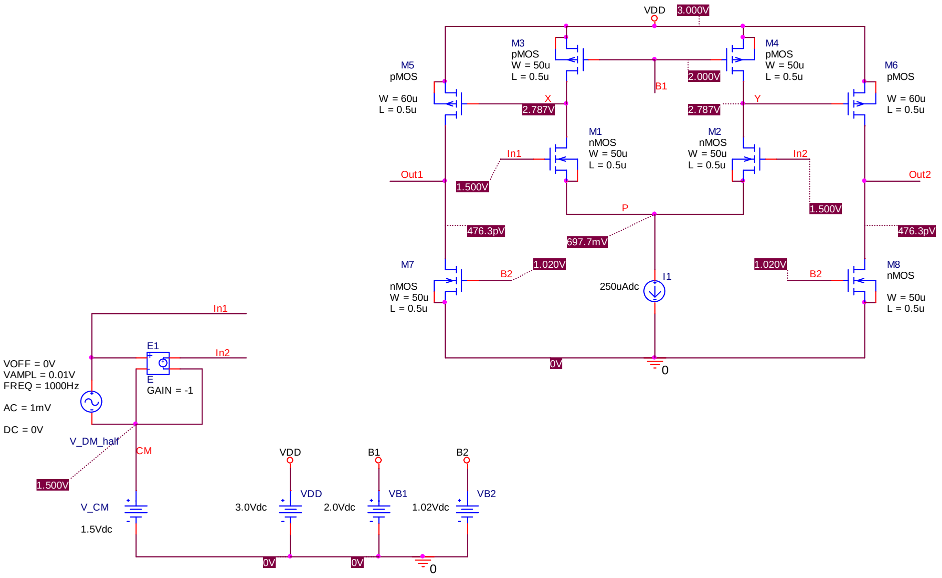
Problem 10.11

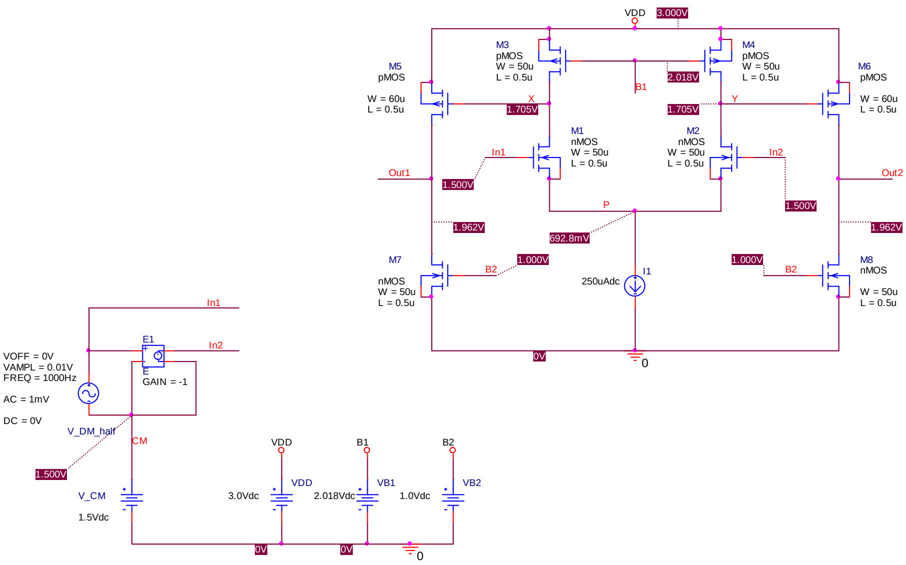
Based on the circuit for problem 10.11 but more of a discussion than an exact solution to that problem.

First calculations, this is not exactly the same bias as in problem



Voltage is too high in node X, Y turning M5, M6 off!

The effect of channel length modulation λ has not been considered. In this circuit one current source is balanced by PMOS current source M3, M4. This is a demonstration that common mode feedback is needed in this kind of amplifier. For the simulation I continue to find a bias that get close to calculated and brings the transistors into saturation region.



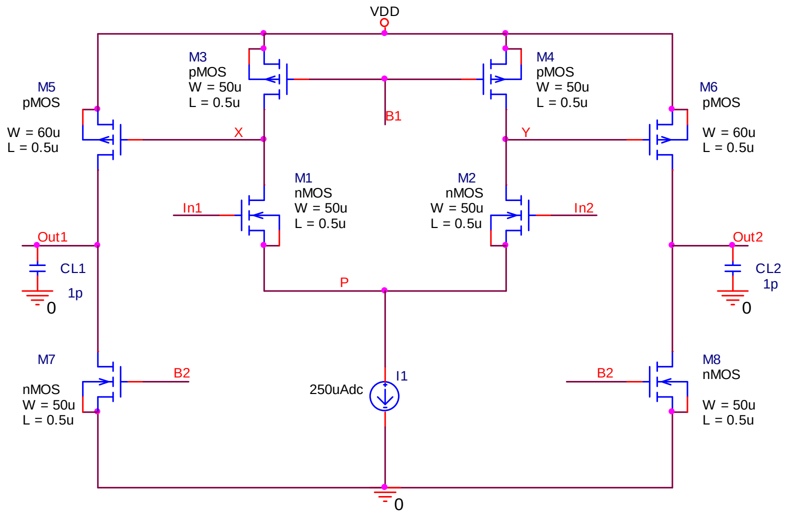
Increasing bias voltage slightly at B1 and a small decrease at B2 bias all transistors in saturation. This is of course not a good design if we need to bias voltage with high accuracy.

NAME	M_M5	M_M4	M_M7	M_M2	M_M8
MODEL	pMOS	pMOS	nMOS	nMOS	nMOS
ID	-1.06E-03	-1.25E-04	1.06E-03	1.25E-04	1.06E-03
VGS	-1.29E+00	-9.82E-01	1.00E+00	8.07E-01	1.00E+00
VDS	-1.04E+00	-1.29E+00	1.96E+00	1.01E+00	1.96E+00
VBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
VTH	-8.00E-01	-8.00E-01	7.00E-01	7.00E-01	7.00E-01
VDSAT	-4.95E-01	-1.82E-01	3.00E-01	1.07E-01	3.00E-01
GM	4.30E-03	1.37E-03	7.09E-03	2.33E-03	7.09E-03
GDS	1.76E-04	1.99E-05	8.89E-05	1.14E-05	8.89E-05
GMB	9.61E-04	3.07E-04	1.68E-03	5.53E-04	1.68E-03
CBD	5.80E-14	4.54E-14	2.52E-14	3.02E-14	2.52E-14
CBS	8.50E-14	7.08E-14	4.24E-14	4.24E-14	4.24E-14
CGSOV	1.80E-14	1.50E-14	2.00E-14	2.00E-14	2.00E-14
CGDOV	1.80E-14	1.50E-14	2.00E-14	2.00E-14	2.00E-14
CGBOV	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGS	4.91E-14	4.09E-14	4.35E-14	4.35E-14	4.35E-14
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

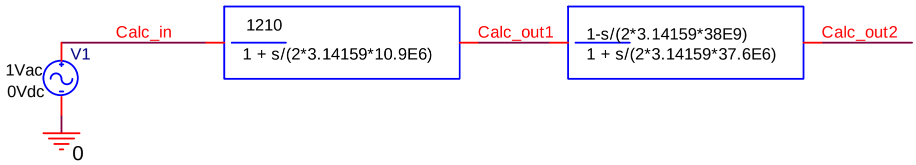
NAME	M_M3	M_M1	M_M6
MODEL	pMOS	nMOS	pMOS
ID	-1.25E-04	1.25E-04	-1.06E-03
VGS	-9.82E-01	8.07E-01	-1.29E+00
VDS	-1.29E+00	1.01E+00	-1.04E+00
VBS	0.00E+00	0.00E+00	0.00E+00
VTH	-8.00E-01	7.00E-01	-8.00E-01
VDSAT	-1.82E-01	1.07E-01	-4.95E-01
GM	1.37E-03	2.33E-03	4.30E-03
GDS	1.99E-05	1.14E-05	1.76E-04
GMB	3.07E-04	5.53E-04	9.61E-04
CBD	4.54E-14	3.02E-14	5.80E-14
CBS	7.08E-14	4.24E-14	8.50E-14
CGSOV	1.50E-14	2.00E-14	1.80E-14
CGDOV	1.50E-14	2.00E-14	1.80E-14
CGBOV	0.00E+00	0.00E+00	0.00E+00
CGS	4.09E-14	4.35E-14	4.91E-14
CGD	0.00E+00	0.00E+00	0.00E+00
CGB	0.00E+00	0.00E+00	0.00E+00

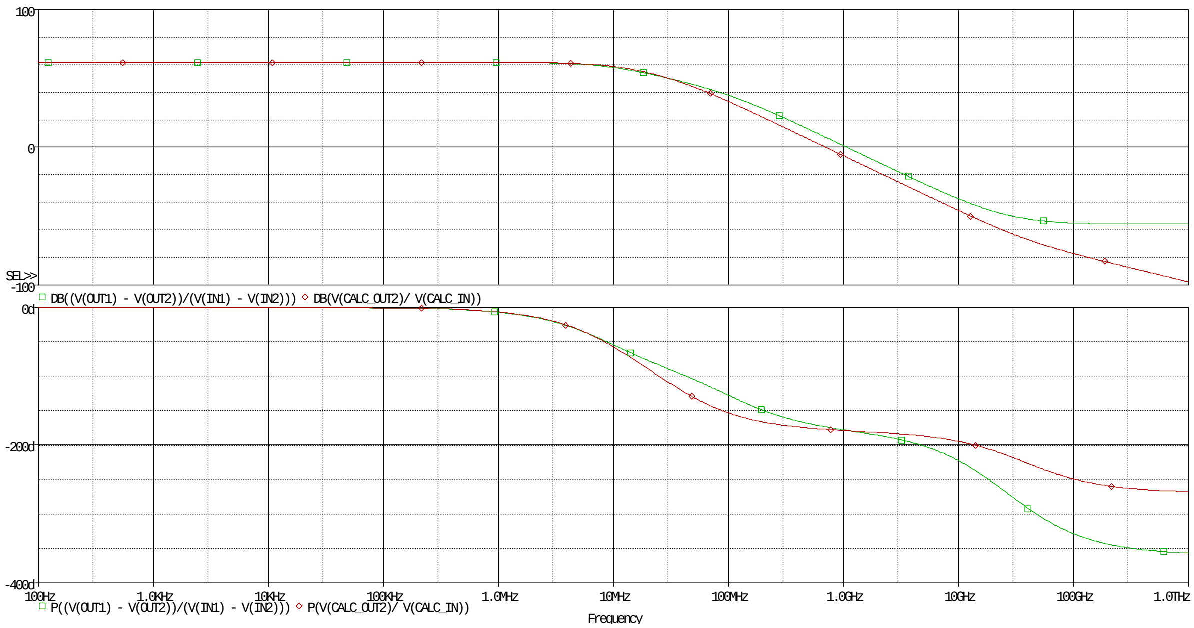
I will use these values in calculation.

Calculated poles are at 10.9 MHz and 37.6 MHz. Calculated zero is at 38 GHz. Let's check this with simulation.



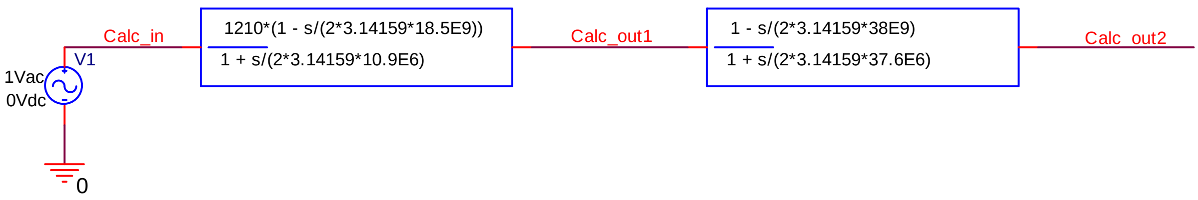
To compare circuit to hand calculated results I use symbol LAPLACE from ABM library (Analog Behavioral Modeling). I put this schematic in a schematic page that is simulated at the same time as the circuit. Red plot is calculated and green plot is circuit.

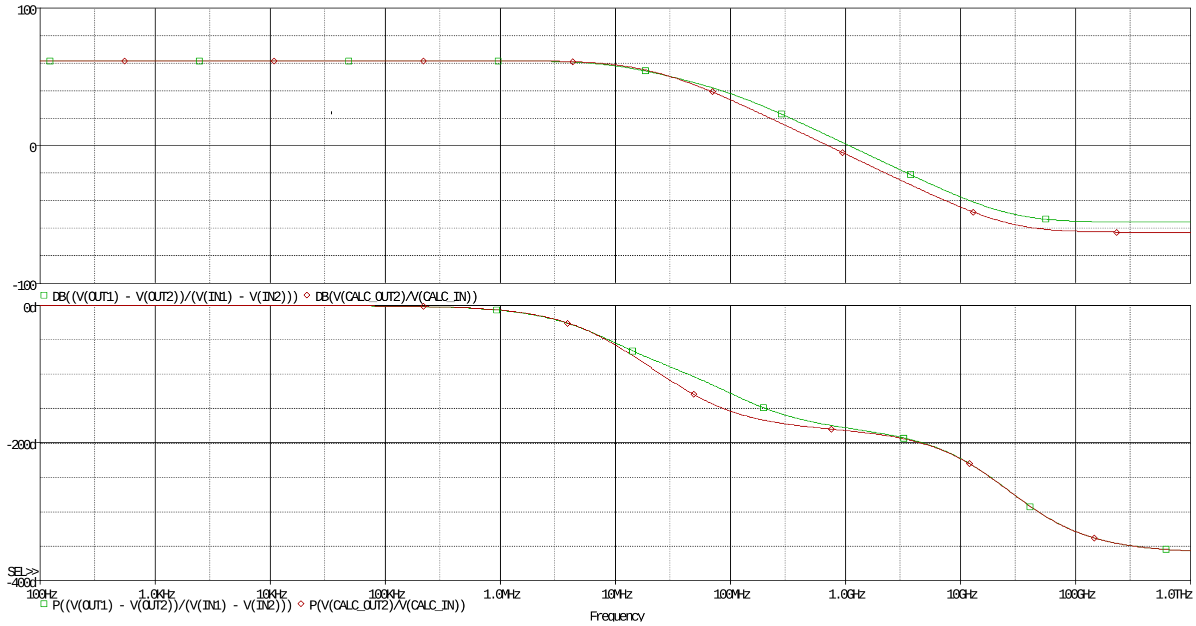




Conclusion: The first pole seems to be OK. The second pole seems to be higher than the calculated value. Also there seem to be one more zero. This will be in the first stage and the calculated value for that zero is 18.5 GHz.

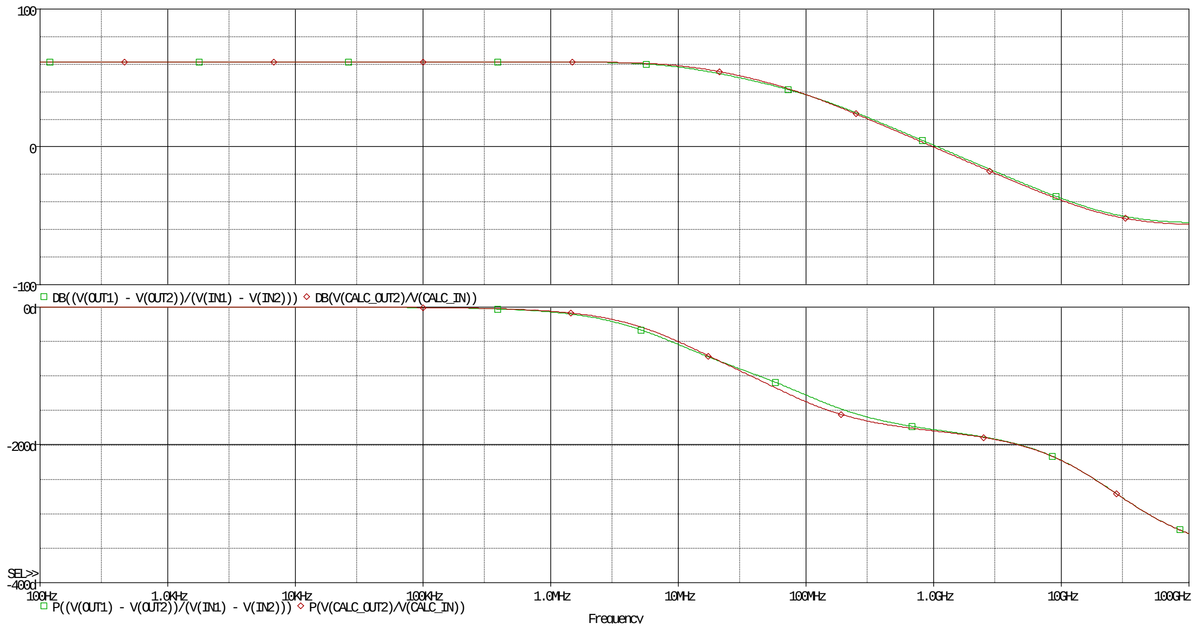
Adding the zero of first stage to simulation of calculated values



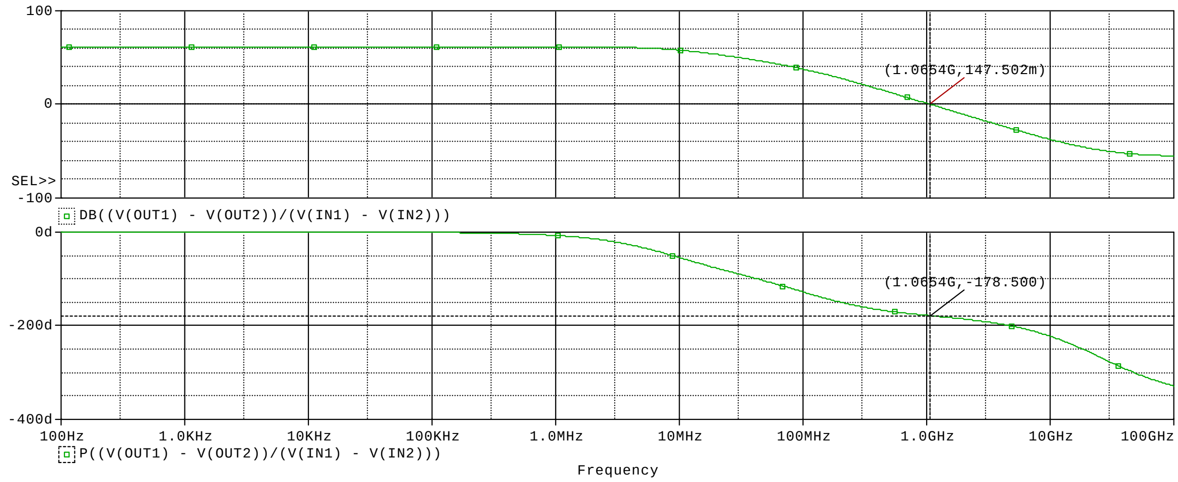


As we can see the curves are pretty close except for the second pole that is lower in the calculated values.

If I change the value of the second pole to 75 MHz I get good agreement. The second pole seems to be twice as high as calculated. Factor 2! Hmmm….. Have I done something wrong or is it the approximation to associate poles to nodes that is not correct? See the plot below.

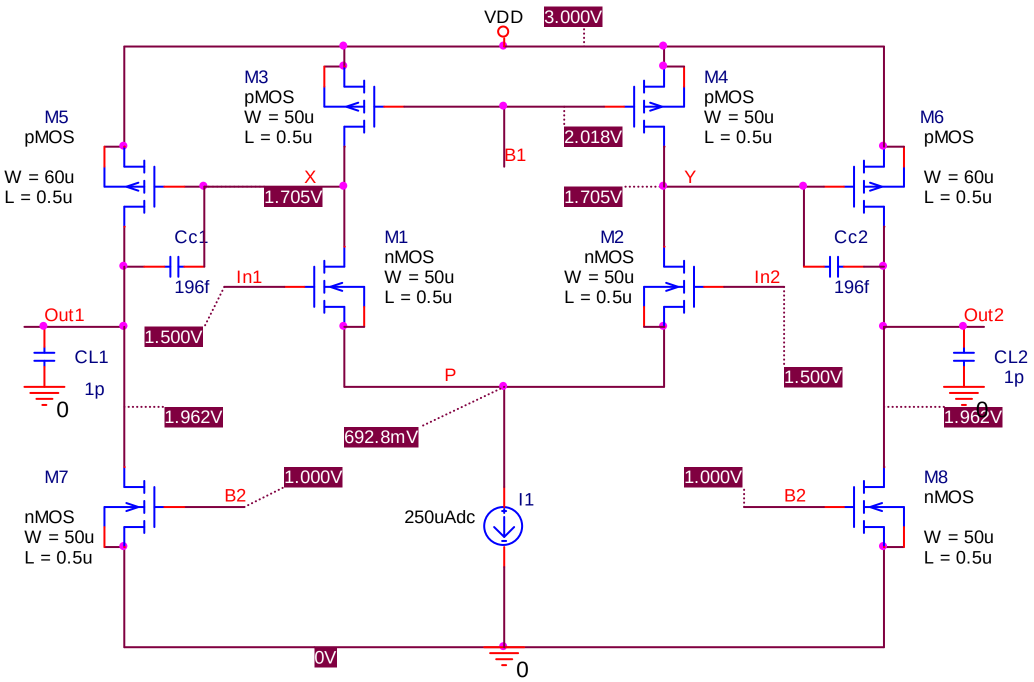


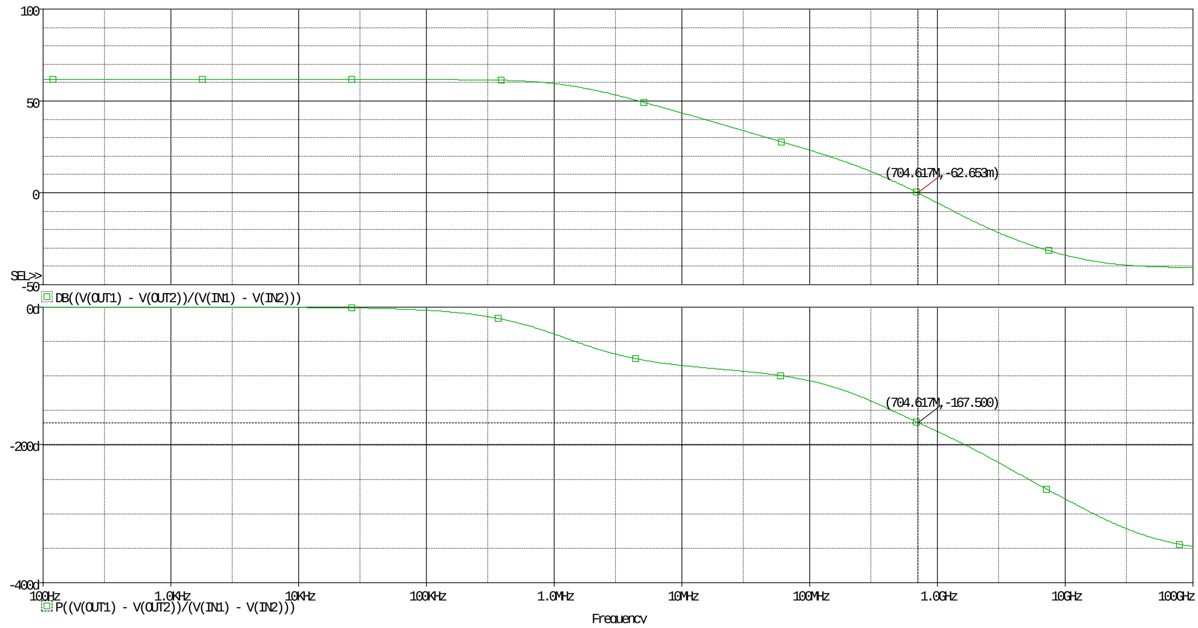
Checking phase margin



Phase margin without compensation is 1.5° so it is nearly instable.

Compensating with Cc = 196 fF (p 7 in calculations), splitting poles to 1.3 MHz and 2.77 GHz.

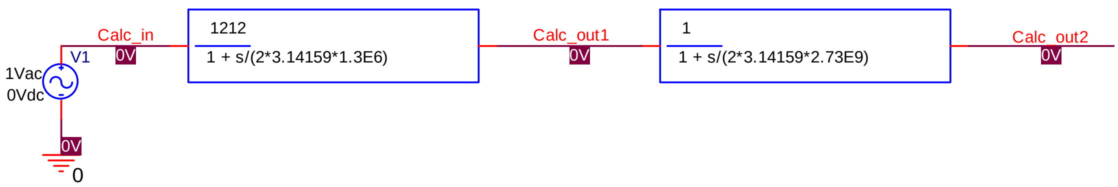


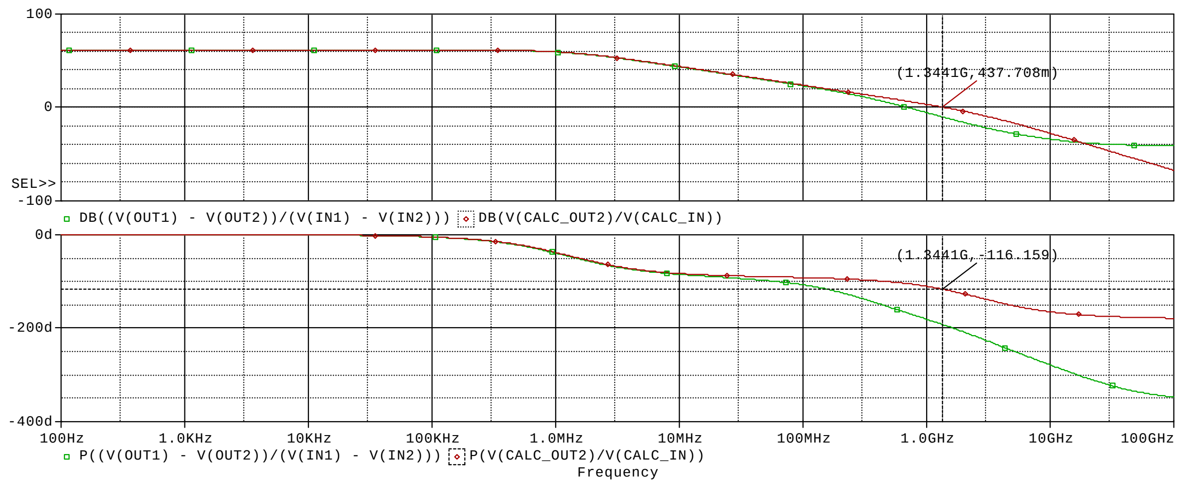


Phase margin is now 12.5°.

Checking poles: First pole is at 1.26 MHz, which is close to expected 1.3 MHz.

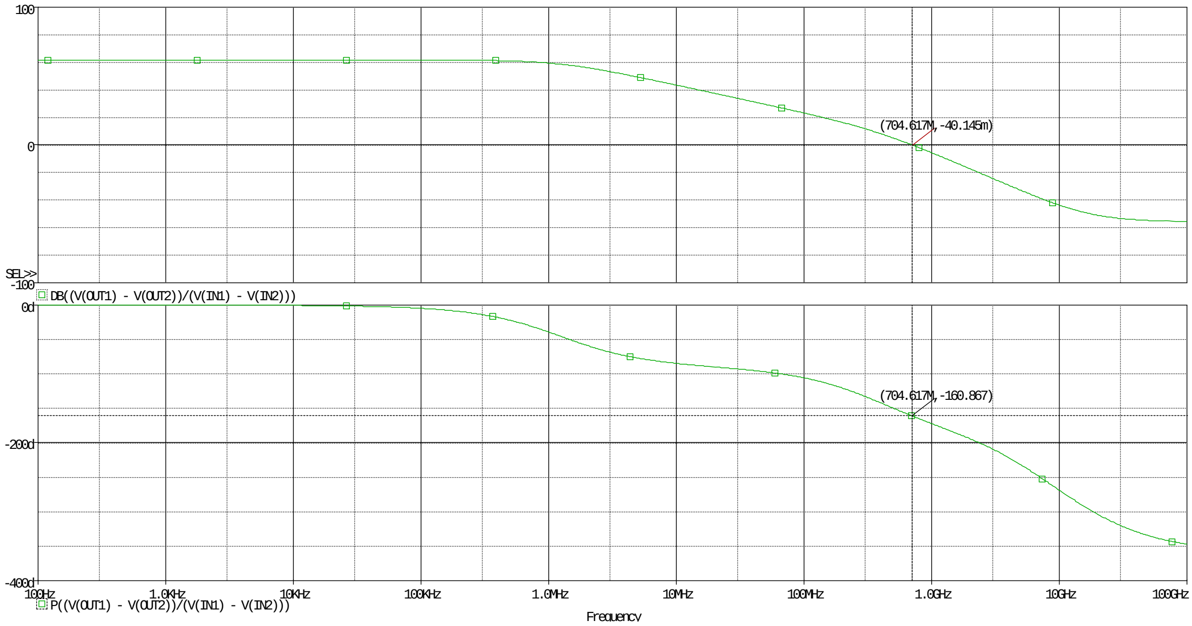
Next step is to check if the moving of the two poles is as expected, so lets simulate only the two calculated poles.



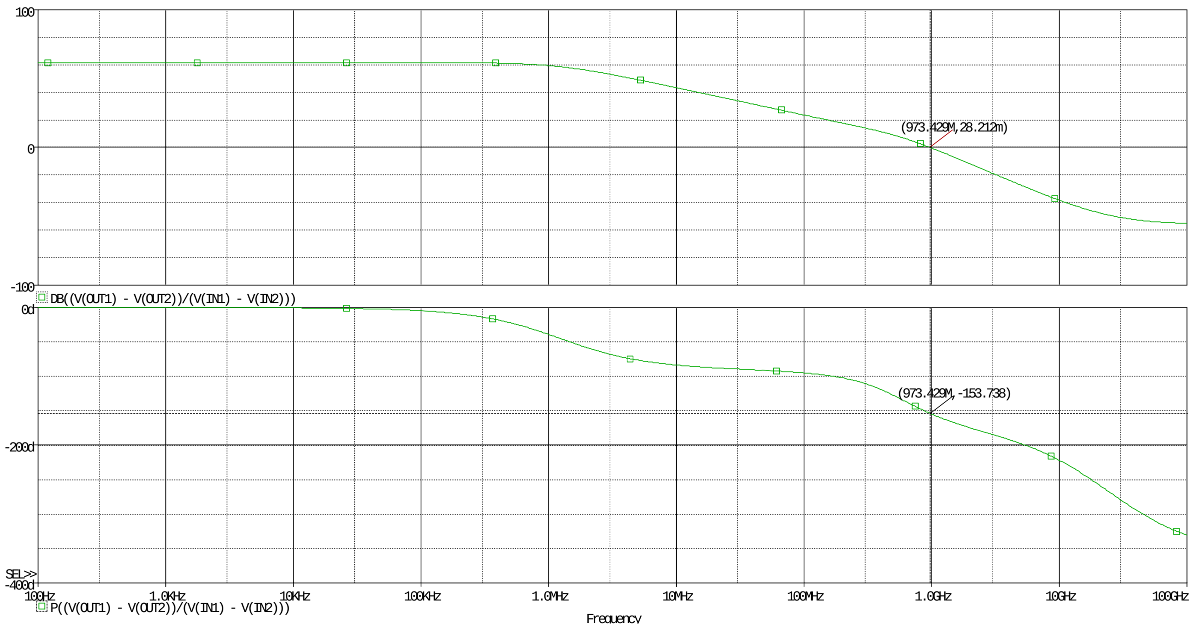


Phase margin from the two poles is 63°, well in agreement with calculation. It is the two zeroes in the circuit that destroys the phase margin.

Moving zero in second stage to infinity by R_z = 233 Ω in series with Cc = 196 fF. Phase margin is now 19°.

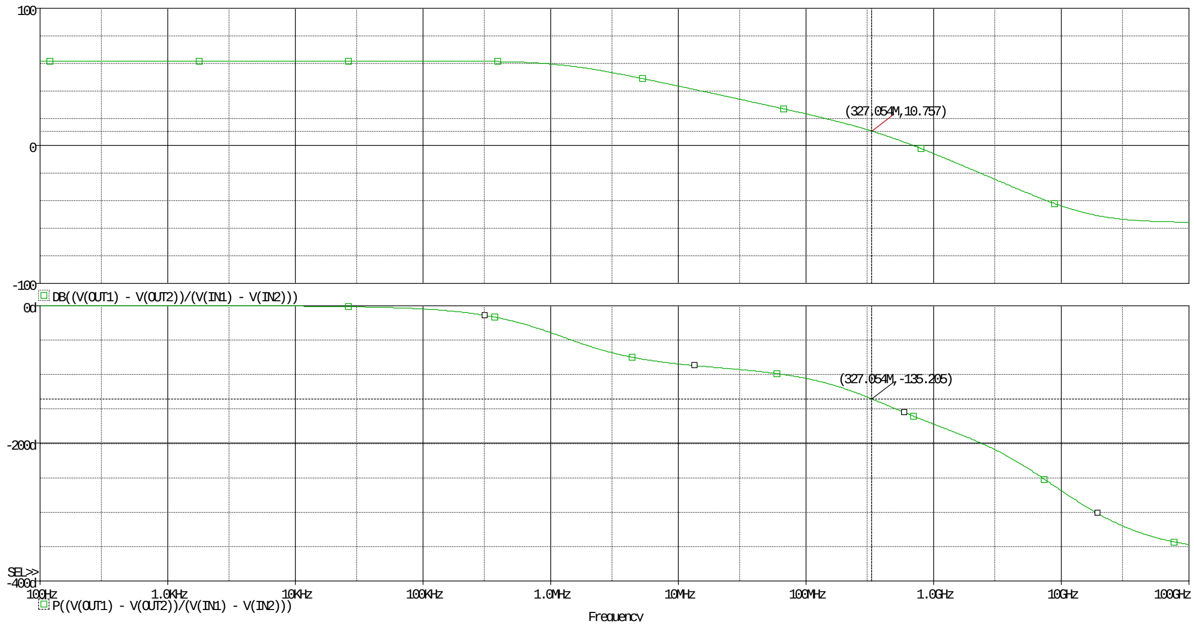


Trying to cancel the second pole by placing the zero atop. R_z = 2.1 kΩ in series with Cc = 196 fF. Phase margin is now 26°.

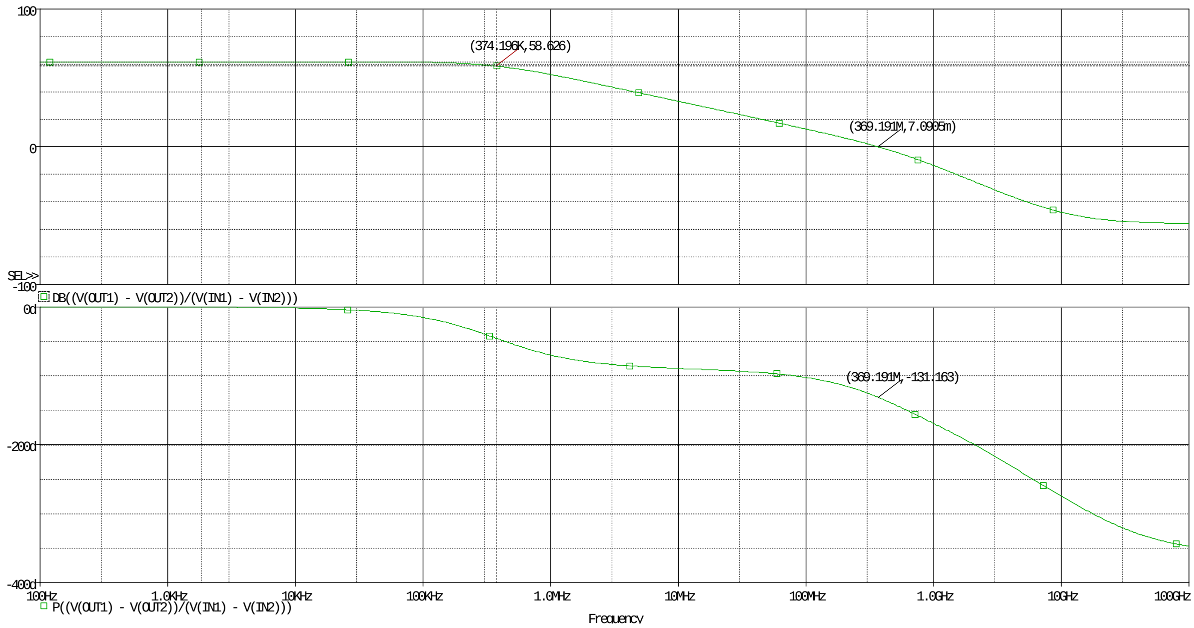


Trying to make the circuit more stable. What is the magnitude when there is 45° left to -180° ?

Simulating with Rz = 233 Ω (zero moved to infinity). Cc= 196 fF

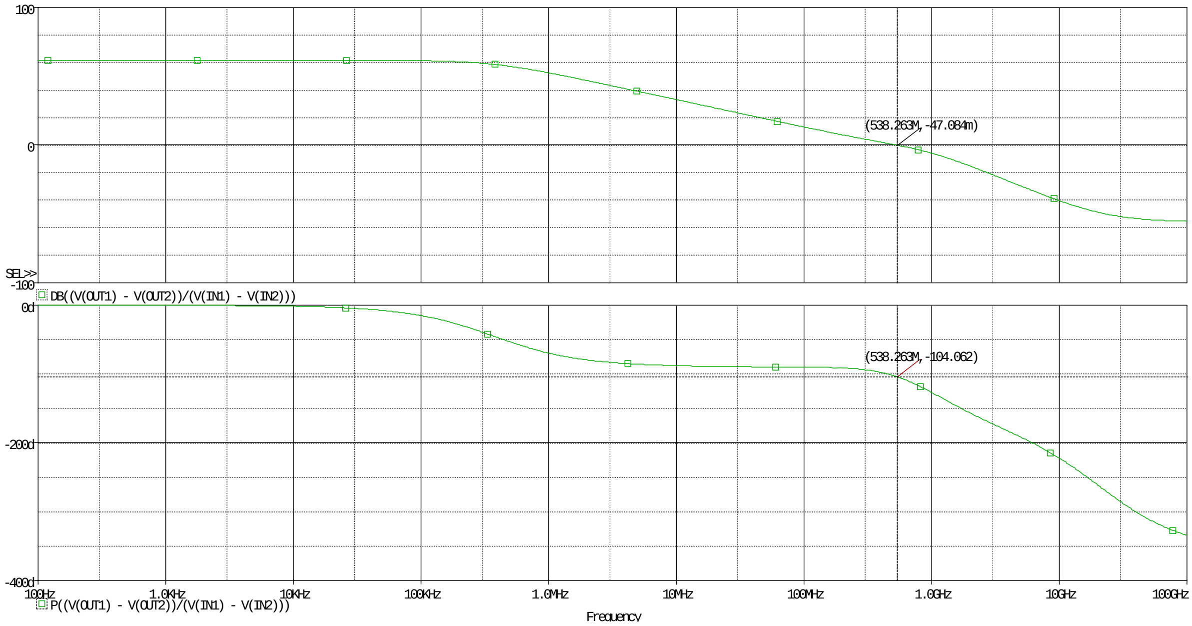


Lowering the magnitude plot -10.7 dB (1/3.43) at phase -135° will give phase margin 45°. To lower the plot the dominating pole is moved to a lower frequency. Cc = 736 fF, Rz = 233 Ω

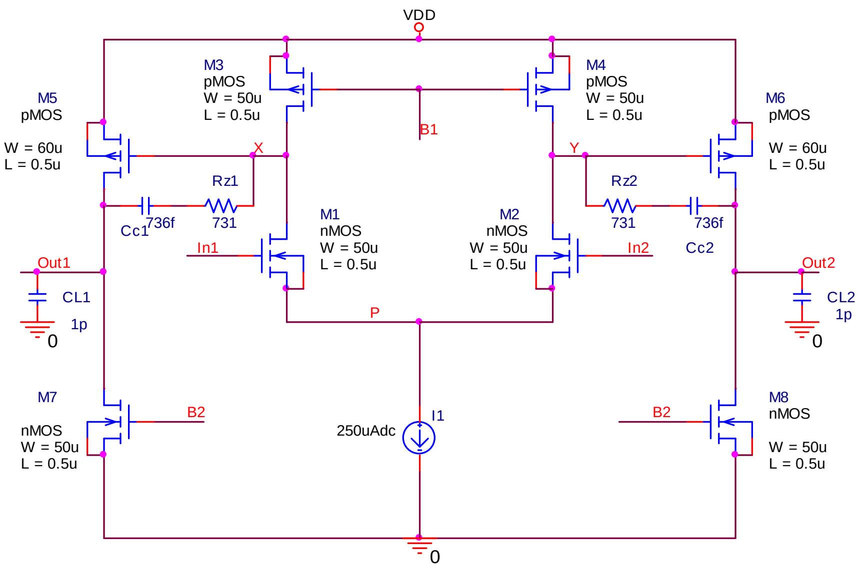


From simulation phase margin 49°, which is an acceptable value.

Moving the zero atop second pole. Cc = 736 fF, Rz = 731 Ω



Now the phase margin is 76°, so it should be possible to increase dominating pole and increase bandwidth and find a more optimal solution.



What still confuses me is that the phase plot goes to -360° at high frequencies. If I have managed to cancel the second pole by moving the right half plane zero into the left half plane and place it on top of the second pole then the phase should go to -180° at high frequencies.

So if anyone can solve that mystery I would be grateful.