

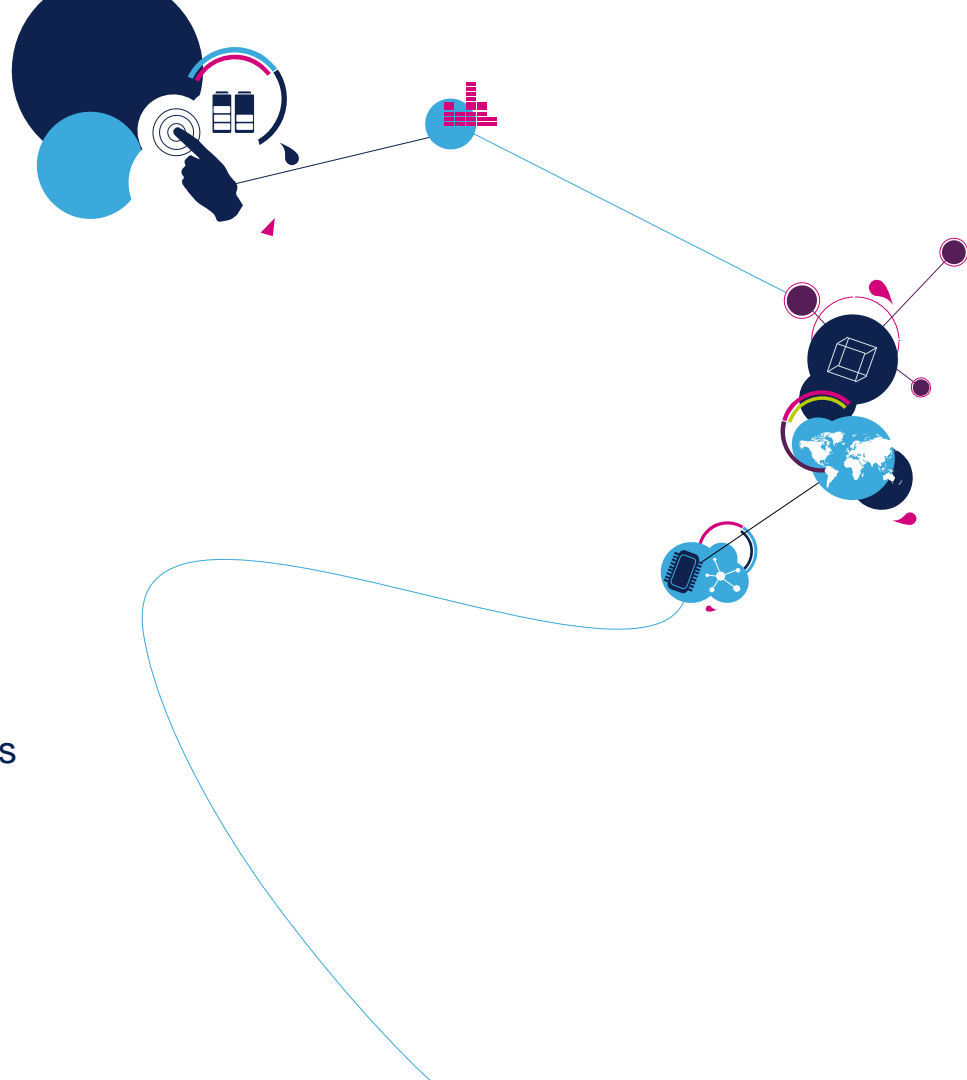
# Microcontrollers

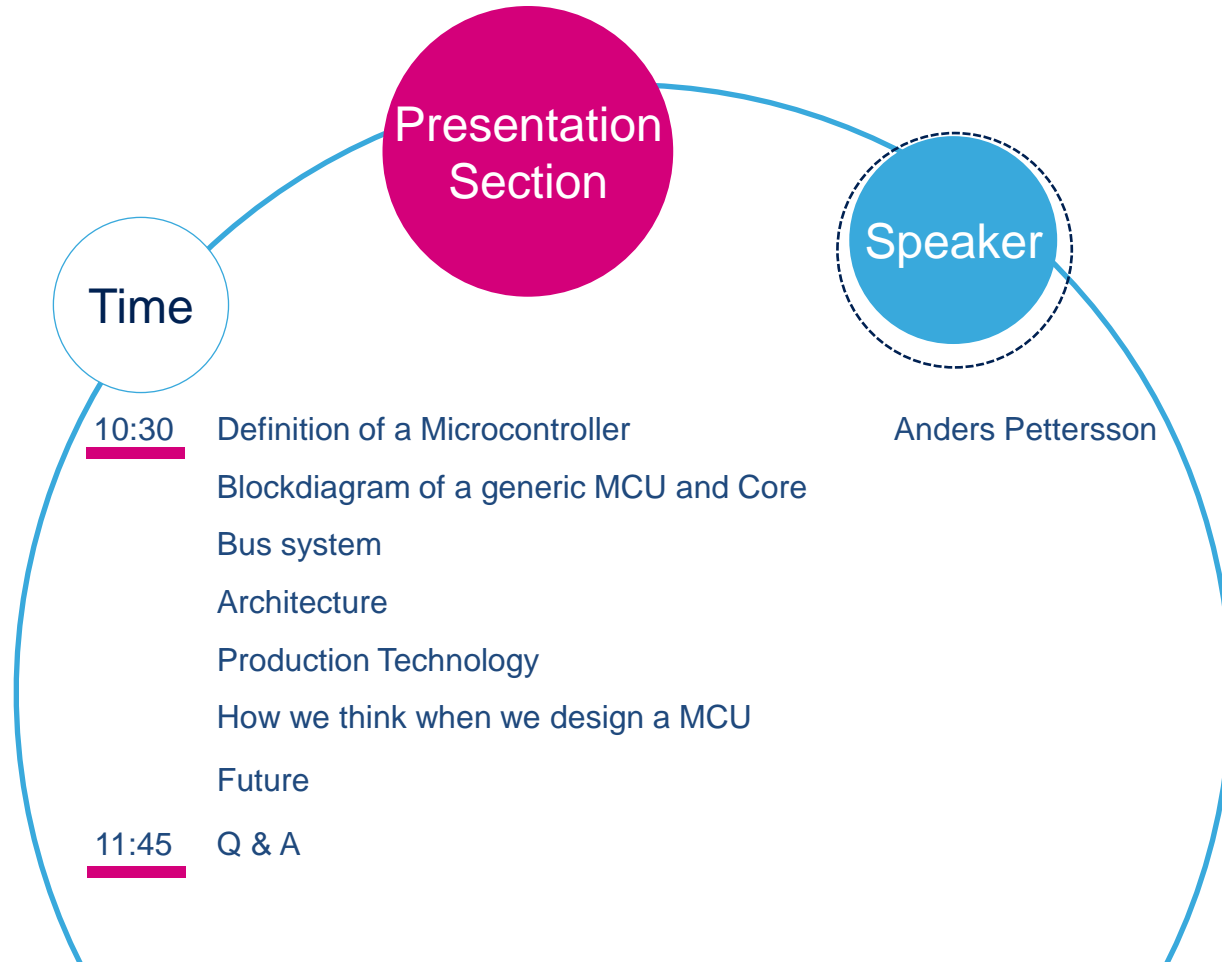
-Definition, Basics and Trends

Anders Pettersson

Technical Marketing Manager Microcontrollers

Nordic and Baltic





# After the session you should have learnt..

3

- Know the difference between a MCU, MPU and CPU.
- Differences between a 8 bit and 32 bit MCU.
- Differences between RISC and CISC architecture
- Differences between Harvard and Von Neuman Architecture
- Temporary production technologies



# Definition of a Microcontroller

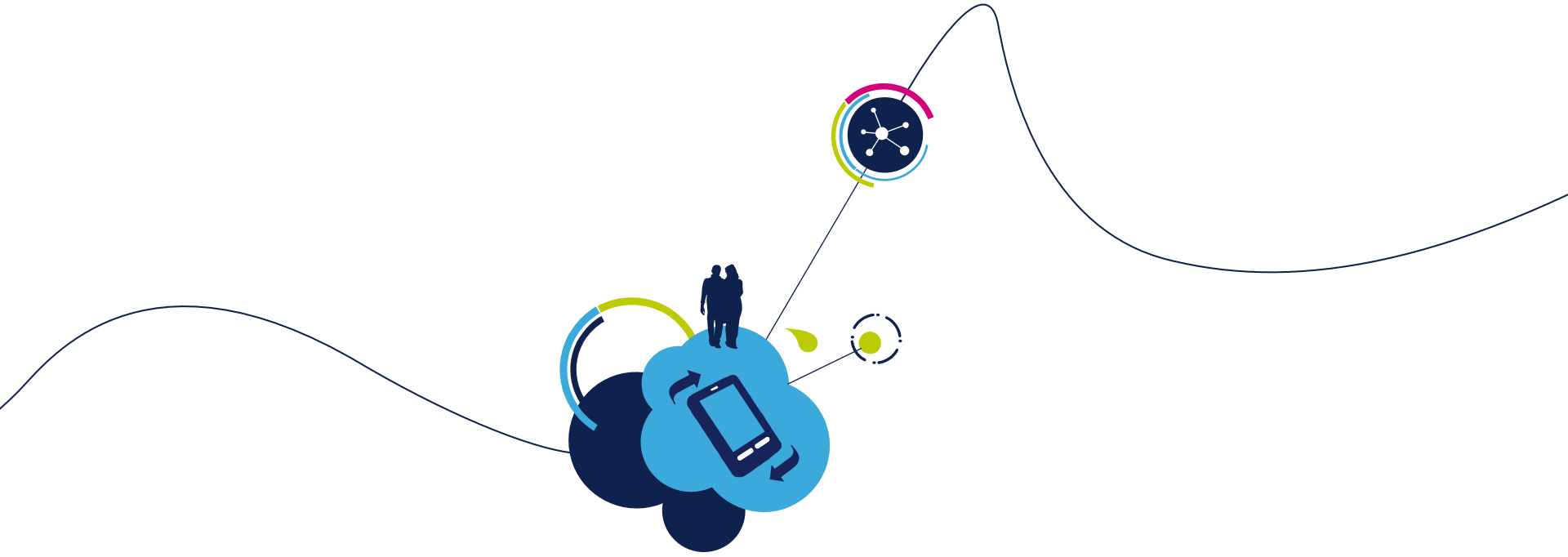
# Definition of a Microcontroller

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- What is the Definition of a Microcontroller?
- There is no absolute definition...

A **microcontroller** (sometimes abbreviated **μC**, **uC** or **MCU**) is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals. Program memory in the form of NOR flash or OTP ROM is also often included on chip, as well as a typically small amount of RAM. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications.

....from Wikipedia



# Architecture

CISC and RISC

# CISC vs RISC

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## CISC

- Emphasis on HW
- Includes Multi-clock complex instructions
- Memory-to-memory: "LOAD" and "STORE" incorporated in instructions
- Small code sizes, high cycles per second
- Transistors used for storing complex instructions

## RISC

- Emphasis on SW
- Single-clock, reduced instructions only
- Register-to-register: "LOAD" and "STORE" and independent from instructions
- Low cycles per second, larger code size
- Spends more transistors on memory registers

Example: Multiply (MULT) , considered as a complex instruction

CISC: MULT 2:3, 5:2

RISC: LOAD A, 2:3  
LOAD B, 5:2  
PROD A, B  
STORE 2:3, A

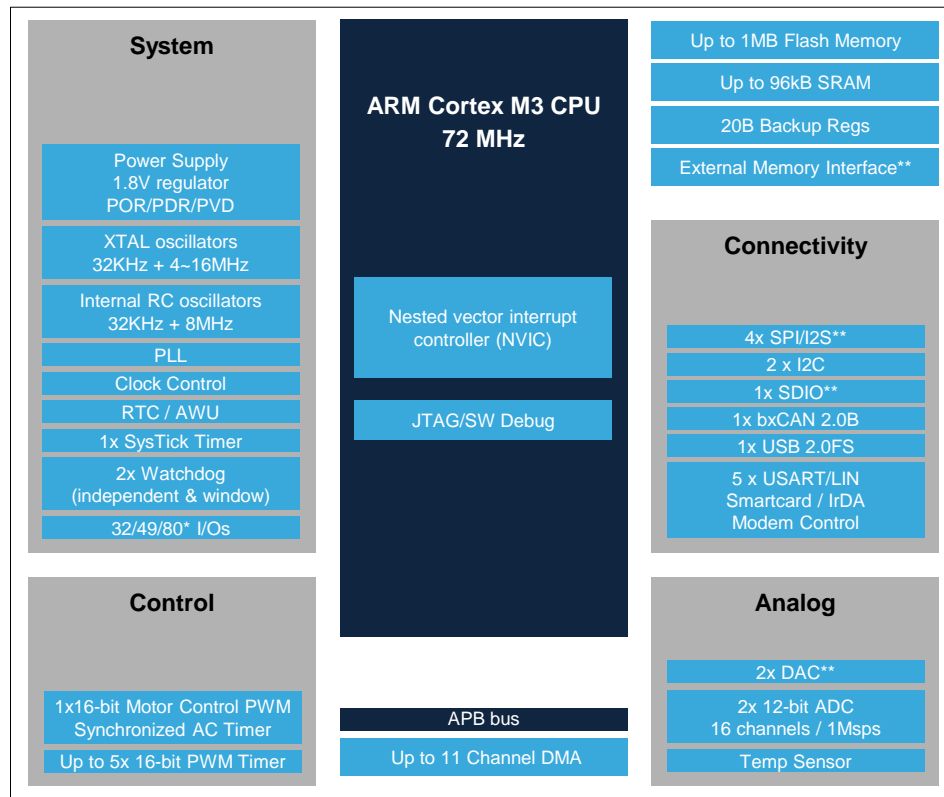


# Block diagram and the Core



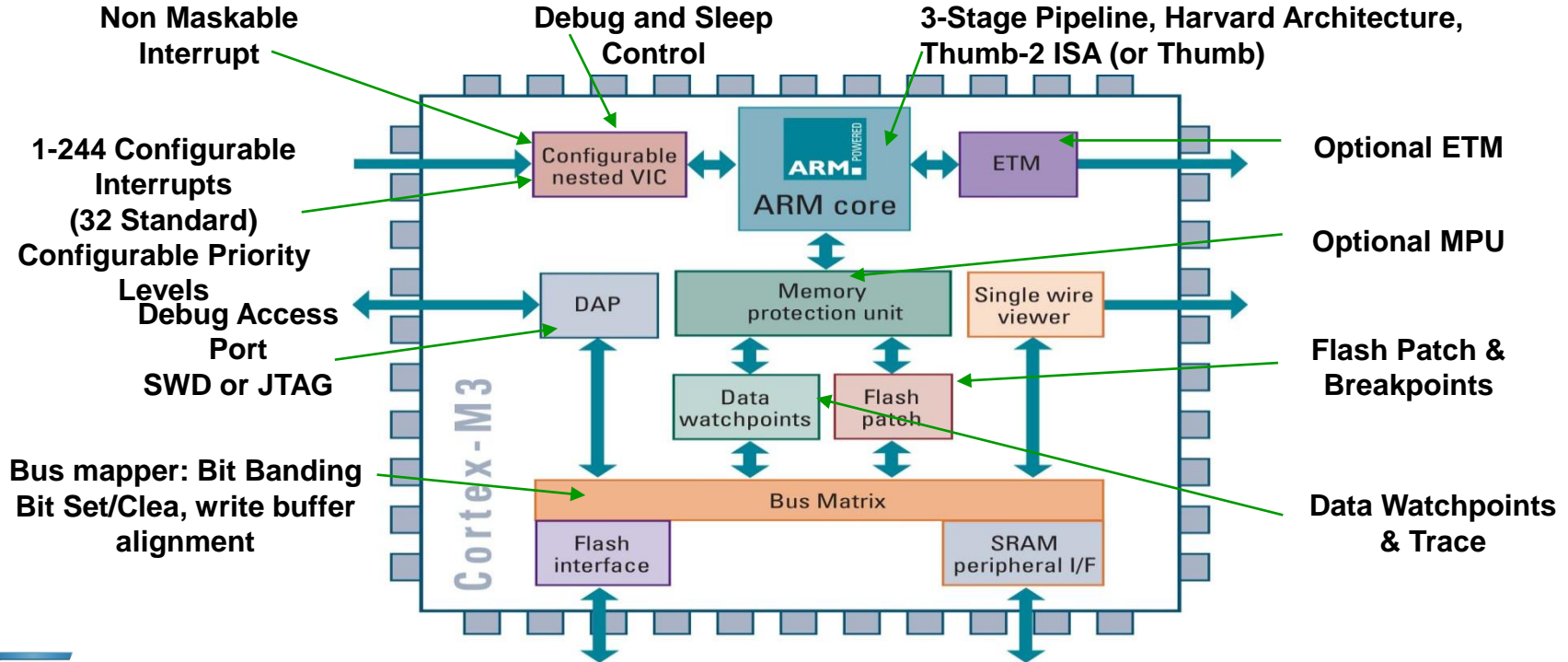
# Essential block diagram of a MCU

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# Cortex-M3 Microprocessor

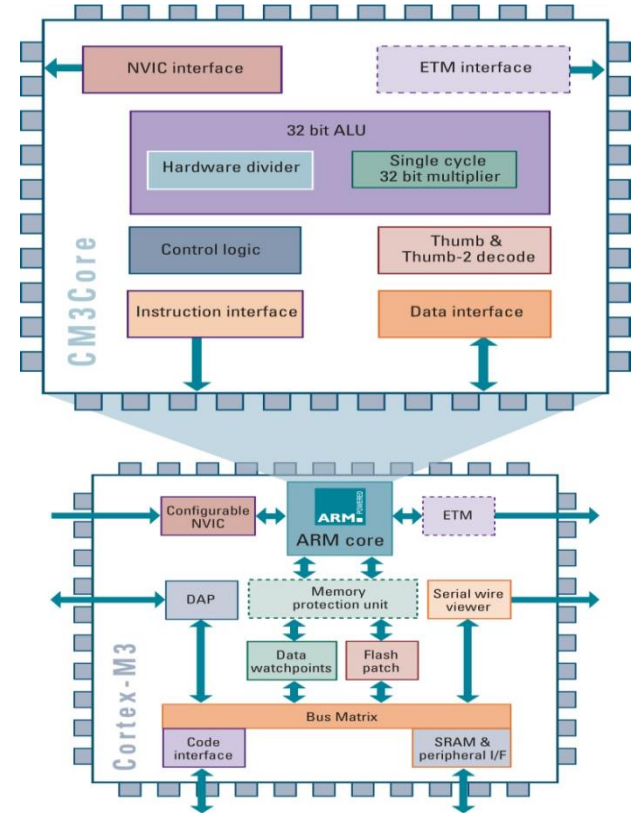
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# Cortex-M3 Microprocessor

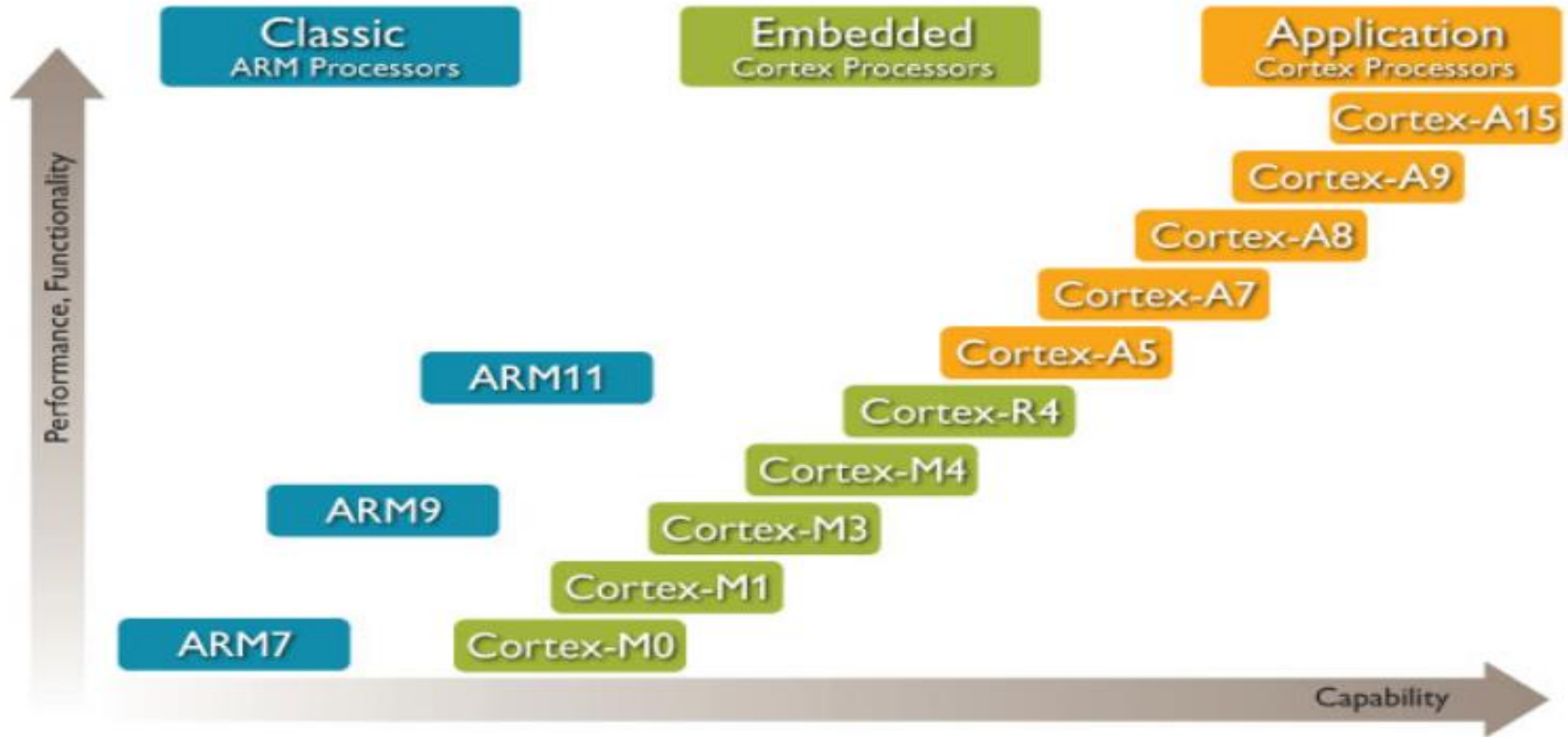
11

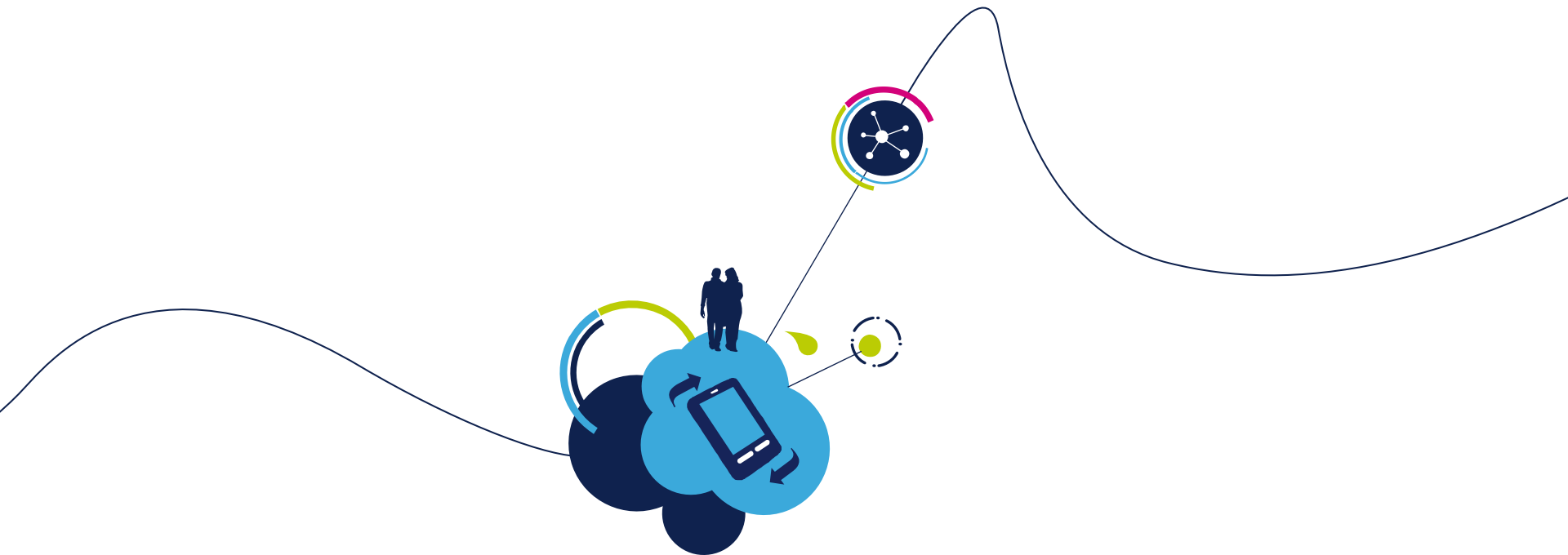
- Hierarchical processor integrating core and advanced system peripherals
- Cortex-M3 core
  - Harvard architecture
  - 3-stage pipeline w. branch speculation
  - Thumb®-2 and traditional Thumb
  - ALU w. H/W divide and single cycle multiply
- Cortex-M3 Processor
  - Cortex-M3 core
  - Configurable interrupt controller
  - Bus matrix
  - Advanced debug components
  - Optional MPU & ETM (Not available in STM32F10x)



# Processors for All Applications

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# Bus system

# Architecture of the bus

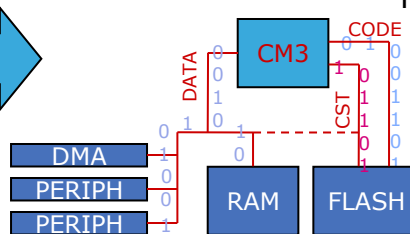
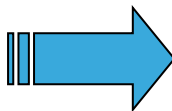
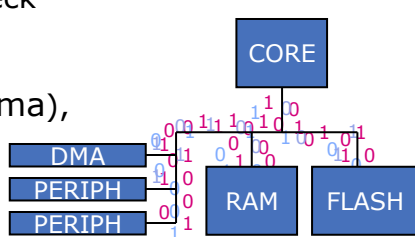
14

 Cortex M3 Architecture: Harvard benefits with Von Neumann single memory space

Von Neumann "bottleneck"

Single 32bit bus for:

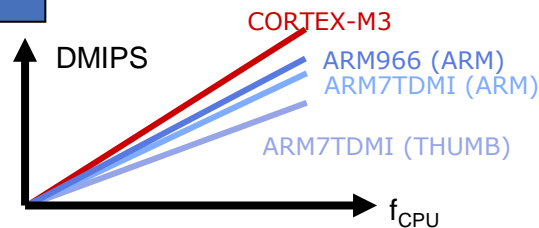
- ♦ code execution,
- ♦ data transfer (core/dma),
- ♦ peripheral control




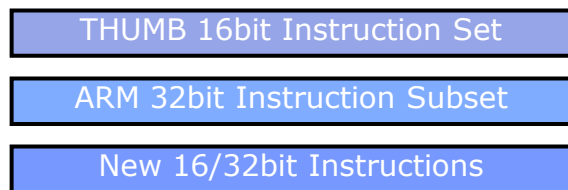
Three 32bit buses for a parallel

- ♦ code execution,
- ♦ data transfer (core/dma),
- ♦ peripheral control

 Outstanding efficiency of 1.25 DMIPS/MHz



 THUMB2 instruction set provides 32bit performance with 16bit code density



Full THUMB compatibility

Complete ARM instruction set for better performance

1 cycle MAC and Hardware Divide  
Unaligned data, Bit banding

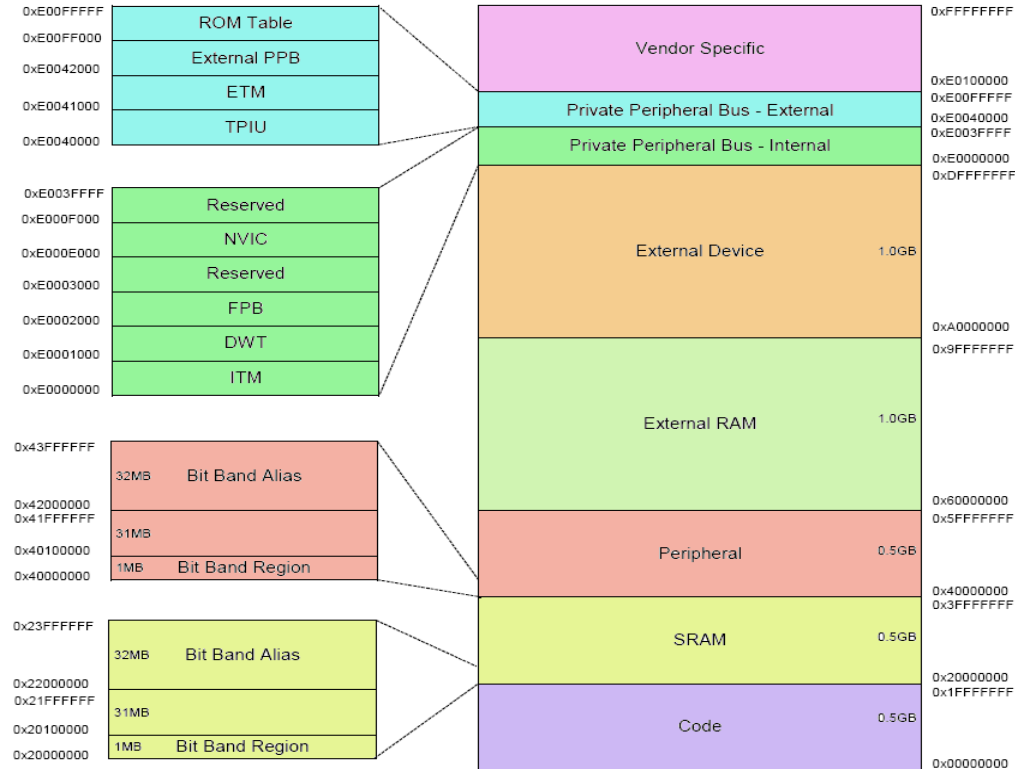
**THUMB-2**

- ♦ Single POWERFUL instruction set → No more mode switching
- ♦ 25% smaller code
- ♦ 25% lower RAM requirement

# Cortex-M3 Memory Map

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- **Vendor Specific (0.5GB)**
  - Set aside to enable vendors to implement peripheral compatibility with previous systems
- **Private Peripheral Bus (1M)**
  - Address space for system components (CoreSight, NVIC etc.)
- **External Device (1GB).**
  - Intended for external devices and/or shared memory that needs ordering/non-buffered
- **External RAM (1GB)**
  - Intended for off chip memory
- **Peripheral (0.5G)**
  - Intended for normal peripherals. The bottom 1MB of the 32MB peripheral address space (0x40000000 – 0x400FFFFFF) is reserved for bit-band accesses. Accesses to the peripheral 32MB bit band alias region (0x42000000 – 0x43FFFFFFF) are remapped to this 1MB
- **SRAM (0.5GB)**
  - Intended for on-chip SRAM. The bottom 1MB of the SRAM address space (0x20000000 - 0x200FFFFFF) is reserved for bit-band accesses. Accesses to the SRAM 32MB bit band alias region (0x22000000 – 0x23FFFFFFF) are remapped to this 1MB address space.
- **Code(0.5GB)**
  - Reserved for code memory (flash, SRAM). This region is accessed via the Cortex-M3 ICode and DCode busses.





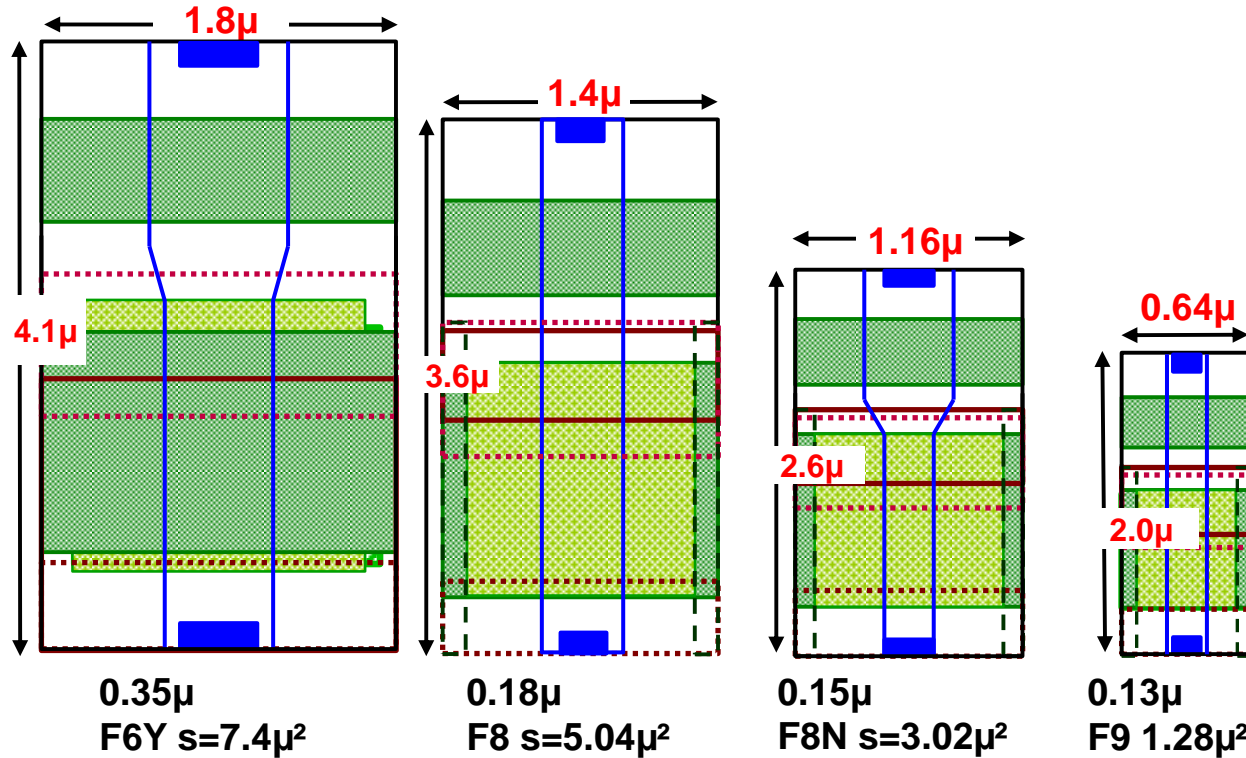
# Production Technologies

- The road to success...



# CMOSF9 eEEPROM Technology History

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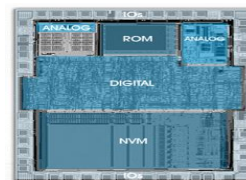
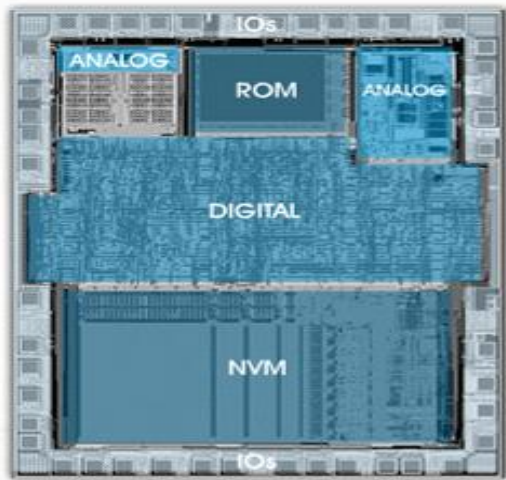
# Technology to Break Price Barriers

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- Technology driving 8-bit evolution
- Breakthrough with 130nm lithography
- E<sup>2</sup> non-volatile memory, analog and digital peripherals

0,4μM

0,13μm



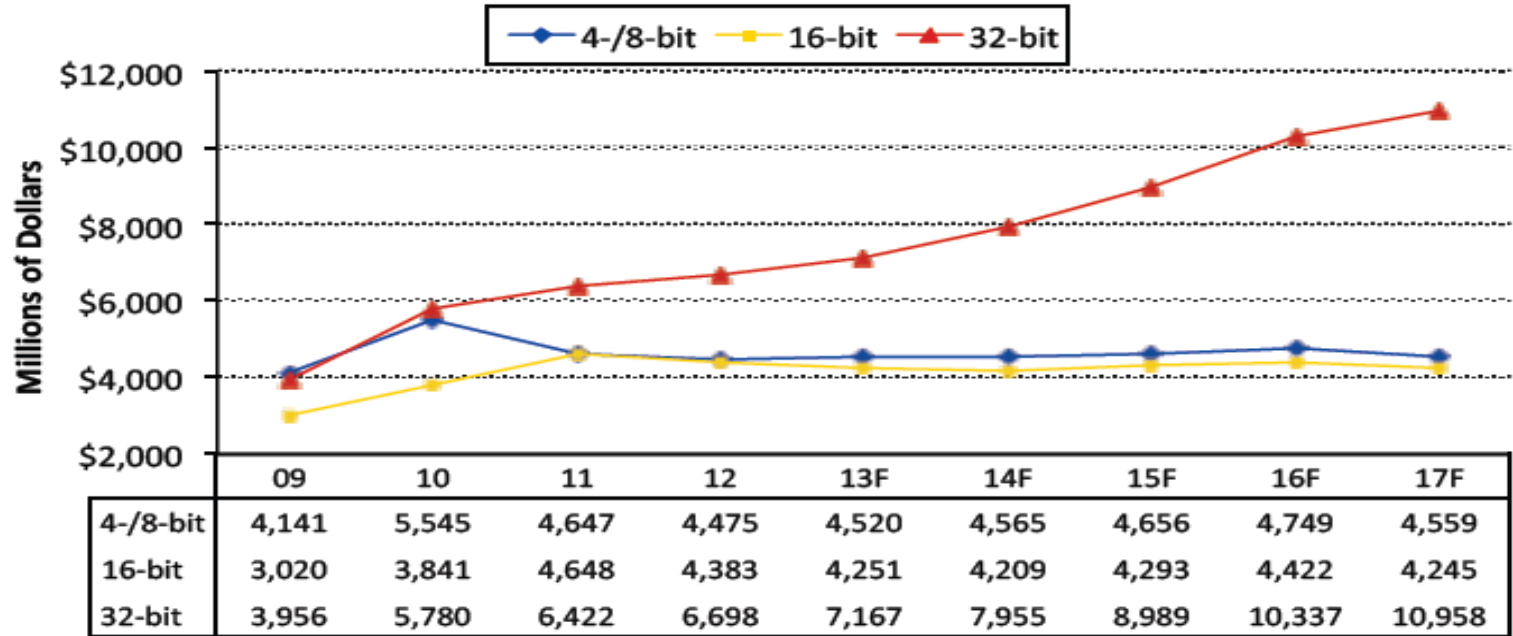


# How do we think when we design a MCU?

# MCU market forecast

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## MCU Sales by Category (2009-2017)



Source: IC Insights

# ST has licensed all Cortex-M processors

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- Forget traditional 8/16/32-bit classifications and get
  - Seamless architecture across all applications
  - Every product optimized for ultra-low power and ease of use

**Cortex-M0**

8/16-bit applications

**Cortex-M3**

16/32-bit applications

**Cortex-M4**

32-bit/DSC applications

Binary and tool compatible



# Cortex-M Powerful & scalable instruction set

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Floating Point Unit

DSP (SIMD, fast MAC)

Advanced data processing  
Bit field manipulations

General data processing  
I/O control tasks

VABS	VADD	VCMP	VCMP	VCVT	VCVTR	VDIV	VLDM
VLDR	VMLA	VMLS	VMOV	VMRS	VMSR	VMUL	VNEG
VNMLA	VNMLS	VNMUL	VPOP	VPUSH	VSQRT	VSTM	VSTR
VSUB	VFMA	VFMS	VFNMA	VFNMS			
Cortex-M4 FPU							
PKH	QADD	QADD16	QADD8	QASX	QDADD	QDSUB	QSAX
QSUB	QSUB16	QSUB8	SADD16	SASX		SEL	SHADD16
SHADD8	SHASX	SHSAX	SHSUB16	SHSUB8	SMLABB	SMLABT	SMLATB
SMLATT	SMLAD	SMLALBB	SMLALBT	SMLALTB	SMLALTT	SMLALD	SMLAWB
SMLAWT	SMLS	SMLS	SMMLA	SMMLS	SMMUL	SMUAD	SMULBB
ADC	ADD	ADR	AND	ASR	B	SMULBT	SMULTT
CLZ	BFC	BFI	BIC	CDP	CLREX	SMULTB	SMULWT
CBNZ	CBZ	CMN	CMP	DBG	EOR	LD	SSAT16
LD	LD	LD	LD	LD	LD	SSAT16	SSAX
LDREX	LDREXB	LDREXH	LDREX	LDREX	LDREX	SSUB16	SSUB8
LD	LD	LD	LD	LD	LD	SXTAB	SXTAB16
LSR	MCRR	MLS	MLA	MOV	MOVT	SXTAH	SXTB16
MRC	MRR	MUL	MVN	NOP	ORN	UADD16	UADD8
ORR	PLD	PLDW	PLI	POP	PUSH	UASX	UHADD16
RBIT	REV	REV16	REYSH	ROR	ROR	UHADD8	UHASX
BKPT	BLX	ADC	ADD	ADR		UHSAX	UHSUB16
BX	CPS	AND	ASR	B		UHSUB8	UMAAL
DMB		BL	BIC			UQADD16	UQADD8
DSB	CMN	CMP	EOR			UQASX	UQASX
ISB	LDR	LDRB	LDM			UQSUB16	UQSUB8
MRS	LDRH	LDRSB	LDRSH			USAD8	USADA8
MSR	LSL	LSR	MOV			USAT16	USAX
NOP	REV	MUL	MVN	ORR		USUB16	USUB8
REV16	REVSH	POP	PUSH	ROR		UXTAB	UXTAB16
SEV	SXTB	RSB	SBC	STM		UXTAH	UXTB16
SXTH	UXTB	STR	STRB	STRH			
UXTH	WFE	SUB	SVC	TST			
WFI	YIELD			WFI			
Cortex-M0/M0+/M1				Cortex-M3		Cortex-M4	

# Minimal External Components

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- **Built-in Supervisor reduces need for external components**
  - Filtered reset input, Power-On reset, Low-Voltage Detect, Brown-Out Detect, Watchdog Timer with independent clock
- **One main crystal drives entire system (with help from PLL)**
  - Inexpensive 4-16 MHz crystal drives CPU, USB, all peripherals
- **Embedded 8 MHz RC can be used as main clock**
  - Optional 32 kHz crystal needed additionally for RTC, can run on internal 40 kHz RC
- **Only 7 external passive components for base system on LQFP100 package!!**



# STM32 – 6 product series

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Common core peripherals  
and architecture:

Communication peripherals: USART, SPI, I <sup>2</sup> C
Multiple general-purpose timers
Integrated reset and brown-out warning
Multiple DMA
2x watchdogs Real-time clock
Integrated regulator PLL and clock circuit
Up to 3x 12-bit DAC
Up to 4x 12-bit ADC (Up to 5 MSPS)
Main oscillator and 32 kHz oscillator
Low-speed and high-speed internal RC oscillators
-40 to +85 °C and up to 105 °C operating temperature range
Low voltage 2.0 to 3.6 V or 1.65/1.7 to 3.6 V (depending on series)
Temperature sensor

STM32 F4 series - High performance with DSP (STM32F401/405/415/407/417/427/437/429/439)

Up to 180 MHz Cortex-M4 DSP/FPU	Up to 2-Mbyte Flash	Up to 256-Kbyte SRAM	2x USB 2.0 OTG FS/HS	3-phase MC timer	2x CAN 2.0B	SDIO 2x I <sup>2</sup> S audio Camera IF	Ethernet IEEE 1588	LCD-TFT SDRAM I/F
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STM32 F3 series - Mixed-signal with DSP (STM32F302/303/313/373/383)

72 MHz Cortex-M4 with DSP and FPU	Up to 256-Kbyte Flash	Up to 48-Kbyte SRAM & CCM-SRAM	USB 2.0 FS	2x 3-phase MC timer (144 MHz)	CAN 2.0B	Up to 7x comparator	3x 16-bit $\Sigma\Delta$ ADC	4x PGA
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STM32 F2 series - High performance (STM32F205/215/207/217)

120 MHz Cortex-M3 CPU	Up to 1-Mbyte Flash	Up to 128-Kbyte SRAM	2x USB 2.0 OTG FS/HS	3-phase MC timer	2x CAN 2.0B	SDIO 2x I <sup>2</sup> S audio Camera IF	Ethernet IEEE 1588	Crypto
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STM32 F1 series - Mainstream - 5 product lines (STM32F100/101/102/103 and 105/107)

Up to 72 MHz Cortex-M3 CPU	Up to 1-Mbyte Flash	Up to 96-Kbyte SRAM	USB 2.0 OTG FS	3-phase MC timer	Up to 2x CAN 2.0B	SDIO 2x I <sup>2</sup> S audio	Ethernet IEEE 1588
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STM32 F0 series – Entry level (STM32F030/50/051)

48 MHz Cortex-M0 CPU	Up to 64-Kbyte Flash	Up to 8-Kbyte SRAM	3-phase MC timer	Comparator	CEC
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STM32 L1 series - Ultra-low-power (STM32L100/151/152/162)

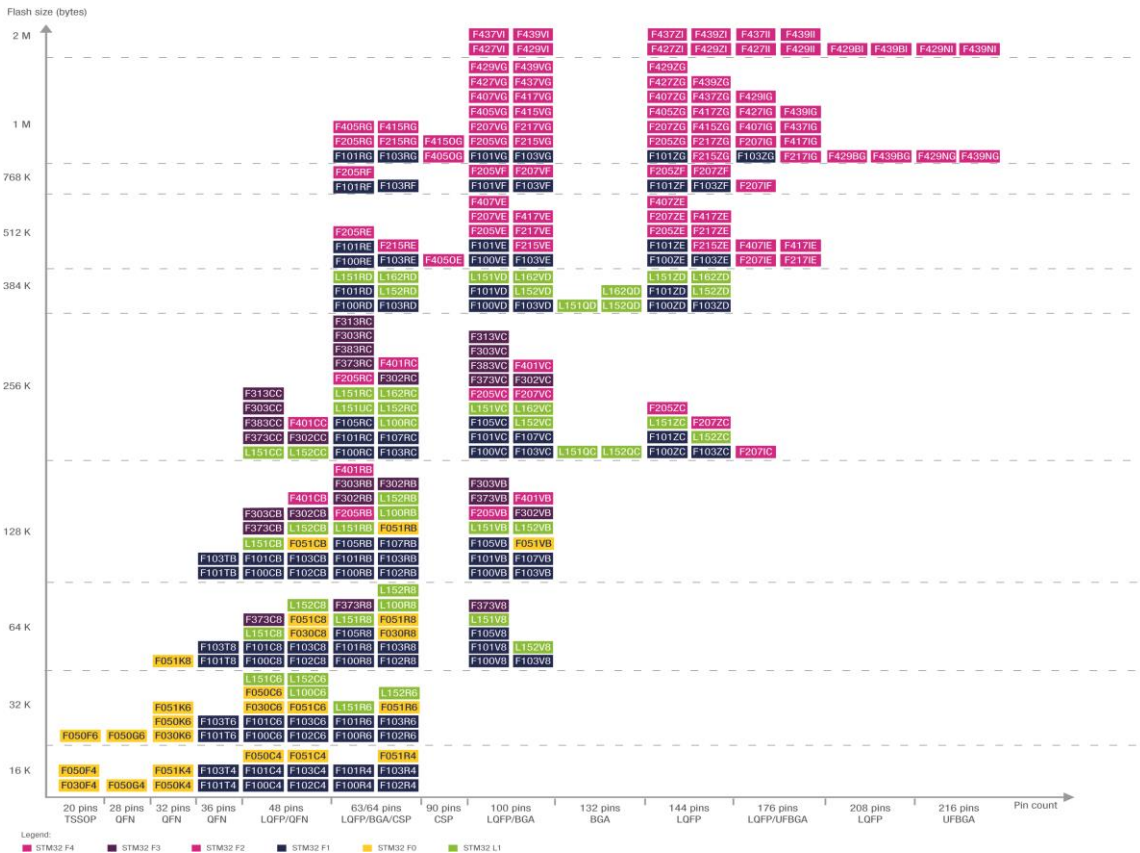
32 MHz Cortex-M3 CPU	Up to 384-Kbyte Flash	Up to 48-Kbyte SRAM	USB FS device	Up to 12-Kbyte EEPROM	LCD 8x40 4x44	Op-amps Comparator	BOR MSI VScal	AES 128-bit
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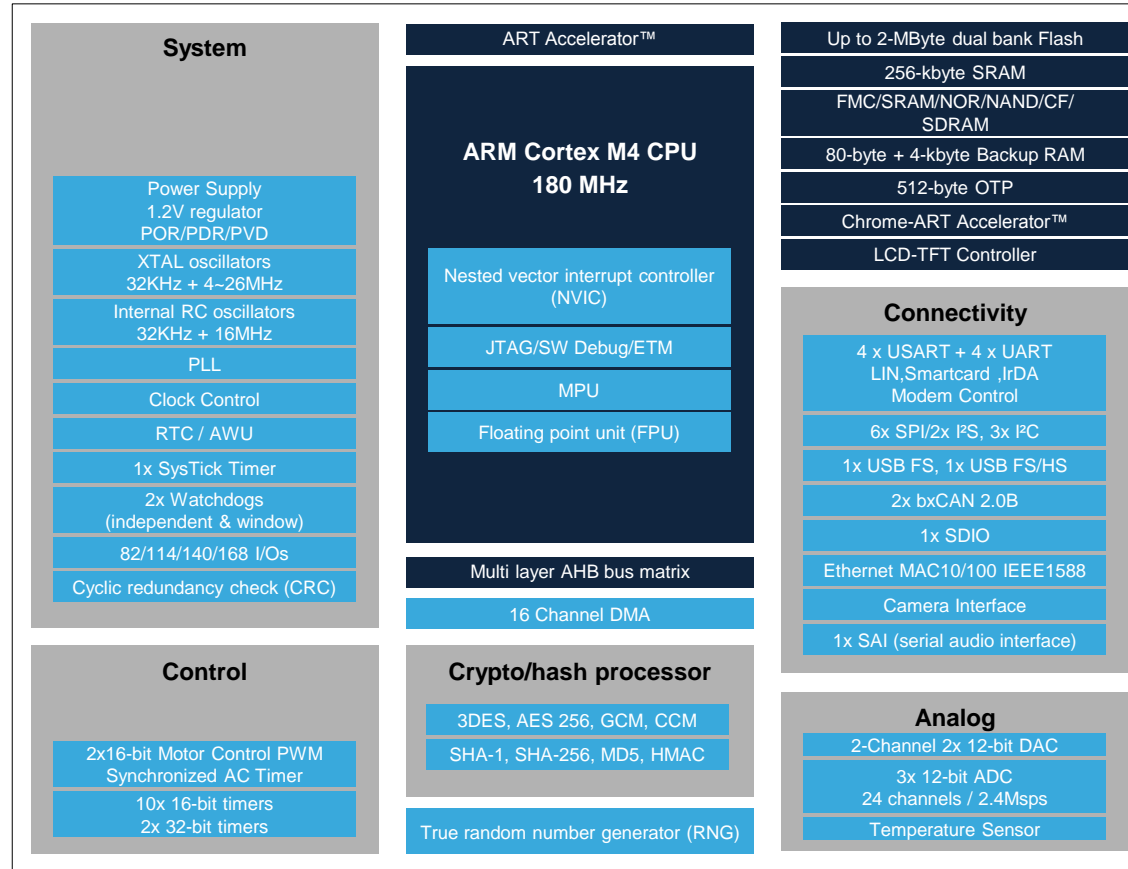


# STM32 – Large compatible portfolio

29

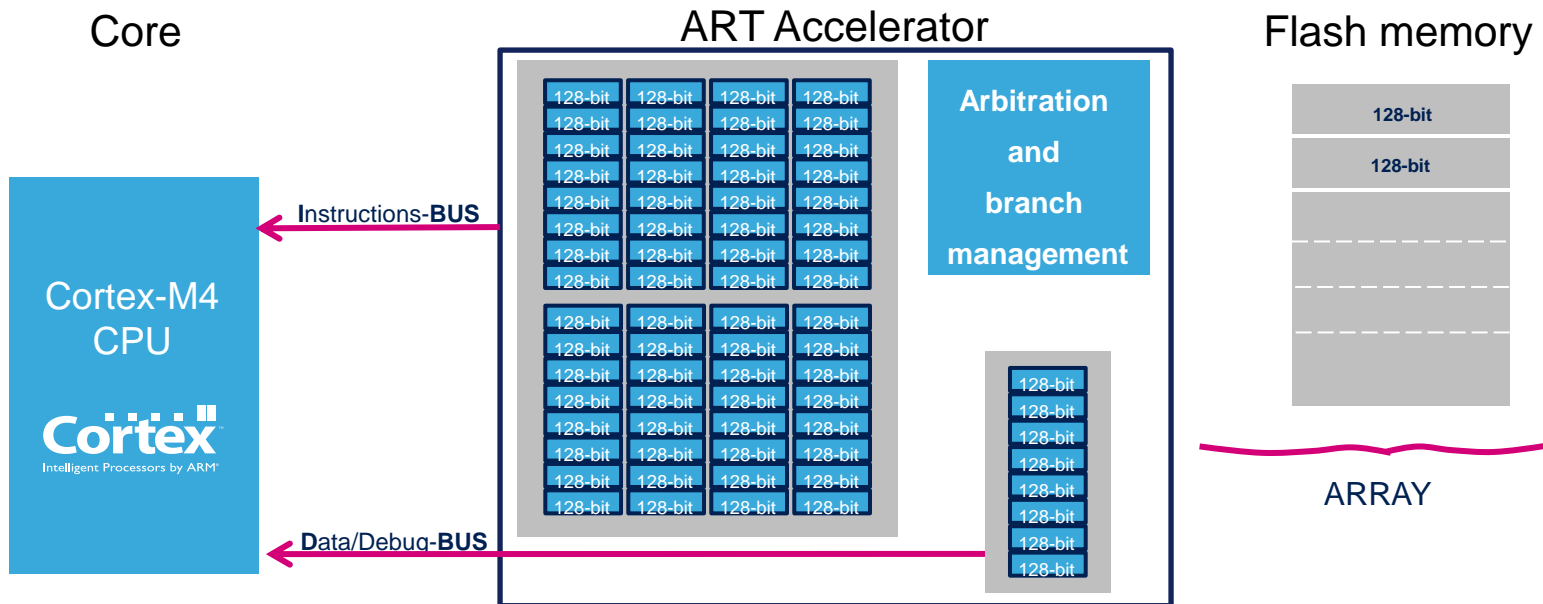


More than  
450 compatible  
devices



# Processing performance

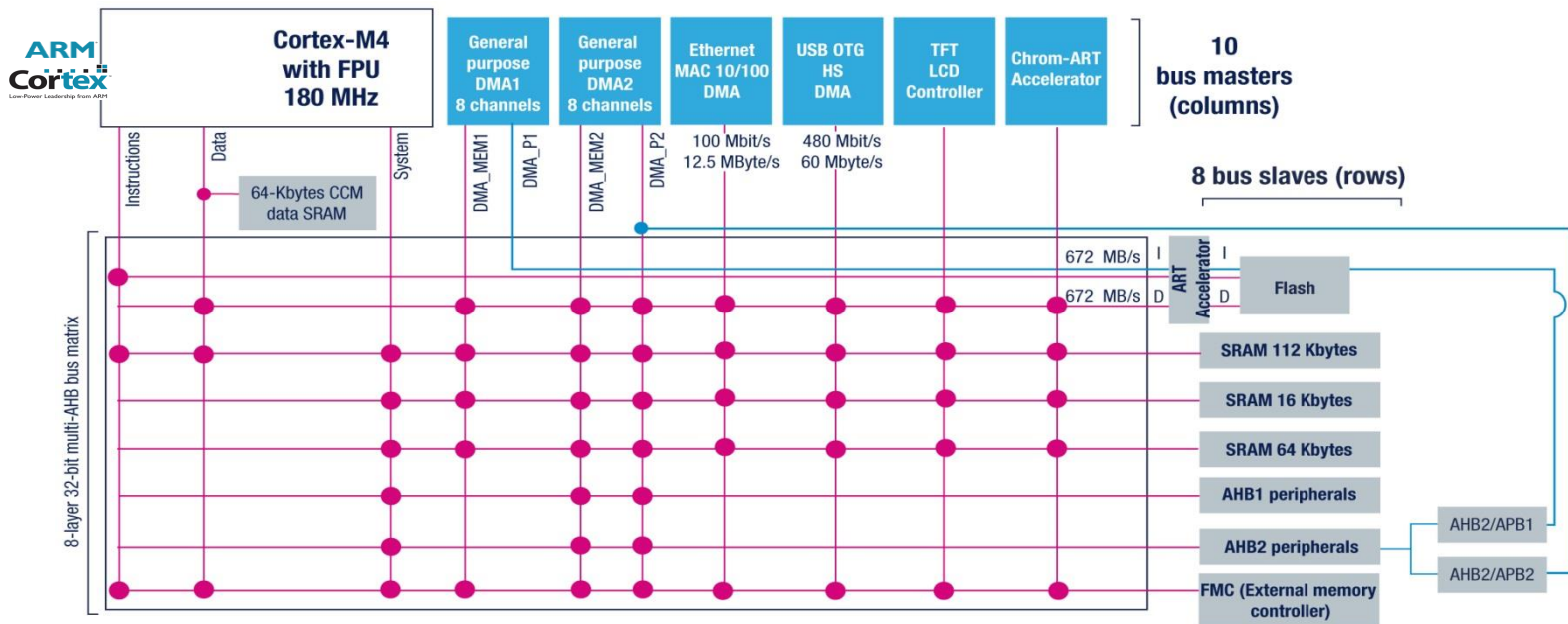
- ART Accelerator™ for F4 series
  - The ART (Adaptive Real-Time) memory accelerator unleashes processing performance equivalent to 0-wait state Flash execution up to 180 MHz for F4 series



# System performance

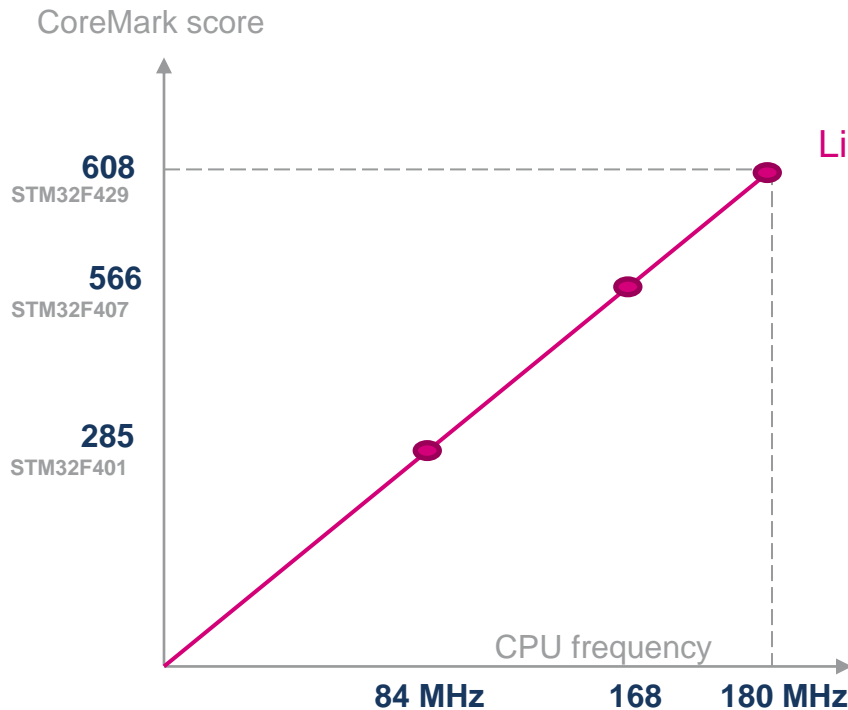
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## 32-bit multi-AHB bus matrix





## Providing more performance



Linear execution performance from Flash

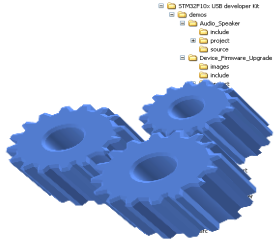
- **Up to 180 MHz/ 225 DMIPS** with ART Accelerator™
- **Up to 608 CoreMark Result**
- ARM Cortex-M4 with floating-point unit (FPU)

Press release:

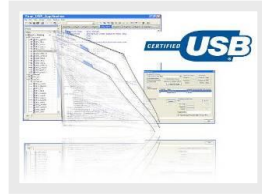
<http://www.st.com/web/en/press/en/p3393>

# Free software solutions from ST

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**Standard Peripheral Library**



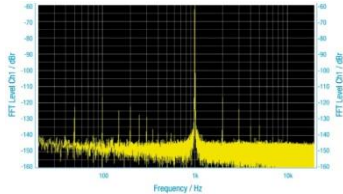
**USB device library  
USB Host Library**



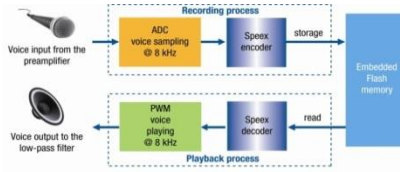
**Motor Control Library**



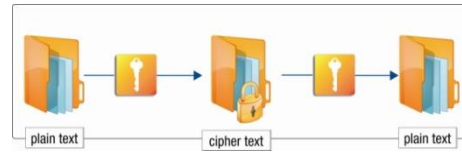
**Self-test routines for  
EN/IEC 60335-1 Class B**



**DSP Library**



**SPEEX Codec**



**Encryption Library**



**STM32 Audio Engine**

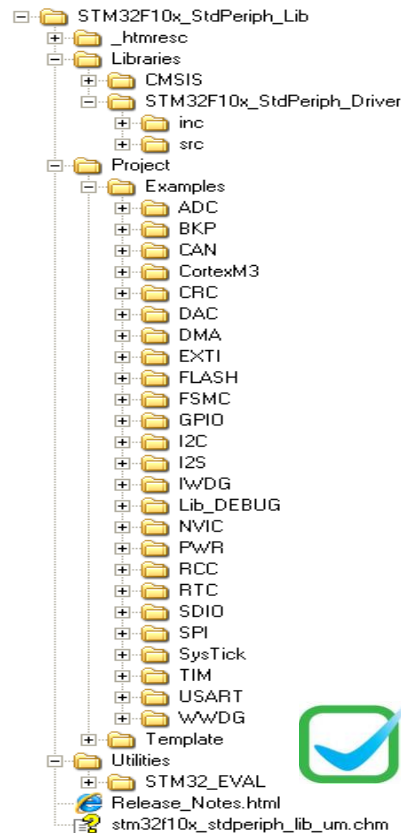
# Software libraries – speed time to market

35

- **ST software libraries free at [www.st.com/mcu](http://www.st.com/mcu)**

C source code for easy implementation of all STM32 peripherals in any application

- **Standard library** – source code for implementation of all standard peripherals; code implemented in demos for STM32 evaluation board
- **Motor control library** – sensorless vector control for 3-phase brushless motors
- **USB Device Library** – Supporting HID, CDC, Audio, Mass Storage, DFU...
- **USB Host Library** – Supporting Mass Storage and HID
- **DSP Library** – PID, IIR, FFT, FIR
- **Graphics Library** – Drop down menus, radio buttons, sliders, ...
- **Software Solutions for**
  - Ethernet TCP/IP
  - Bluetooth
  - SpeexCodec
  - And many others.



- Evaluation board for full product feature evaluation

- **Hardware evaluation platform for all interfaces**
- **Connection to all I/Os and all peripherals**



**STM32303C-EVAL**

**STM32373C-EVAL**

**Available in Q4-2012**

(For any support before please contact our local ST office)



**STM32F3DISCOVERY**

**Available End Q3-2012**

(For any support before please contact our local ST office)

- Discovery kit for cost-effective evaluation and prototyping
- Large choice of IDE solutions from the STM32 and ARM ecosystem:

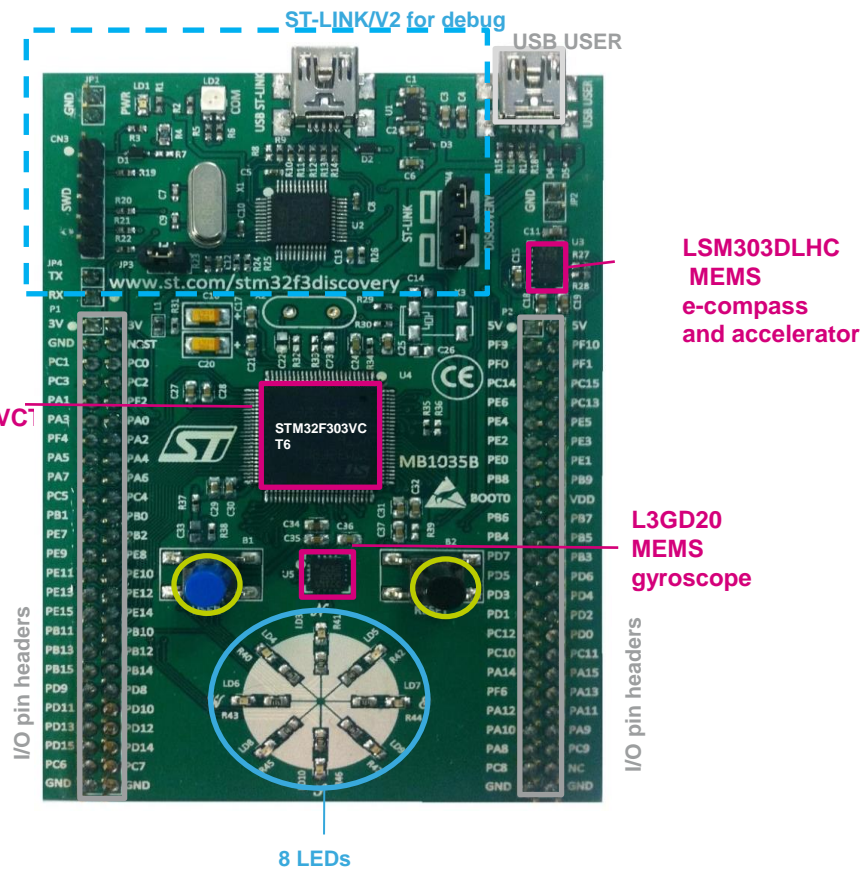




# STM32F3-Discovery kit

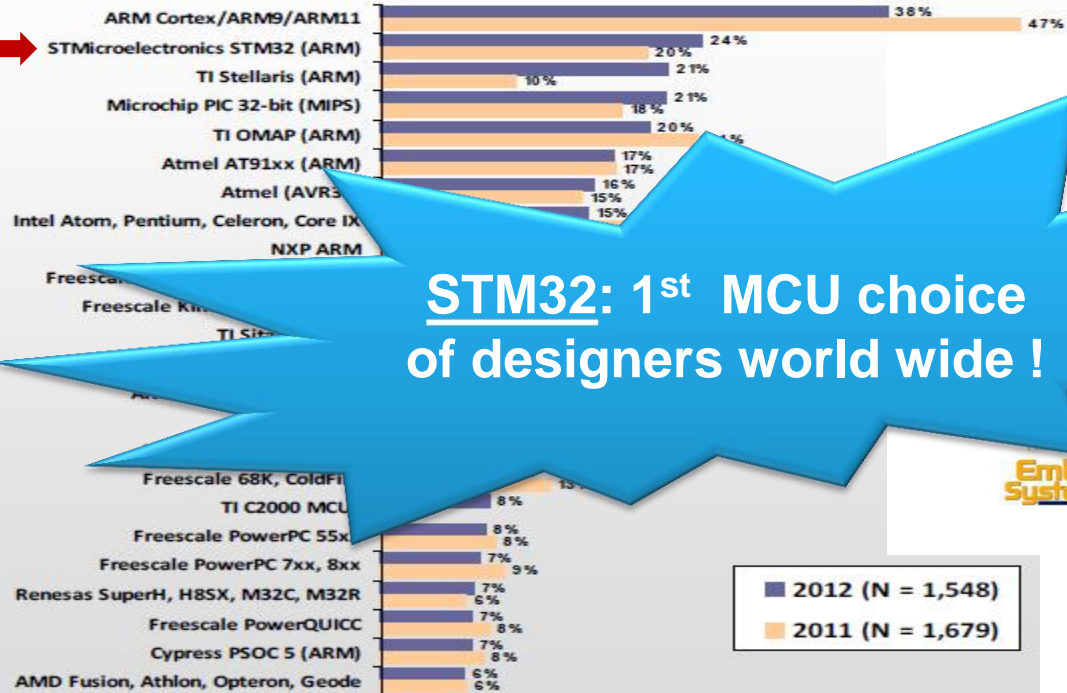
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- Includes everything for a quick start with the STM32F3 for less than \$11
- Ideal for evaluation, learning, prototyping
- The kit combines ST's STM32 F3 MCU with 9-axis MEMS sensors (gyroscope and e-compass), ready for 3D motion-sensing application development
- Dedicated web page: [www.st.com/stm32f3discovery](http://www.st.com/stm32f3discovery) with SW example and documents



## 2012 Embedded Market Study

Which of the following 32-bit chip families would you consider for your next embedded project?



**STM32: 1<sup>st</sup> MCU choice of designers world wide !**



*Years serving the embedded community!*

2012

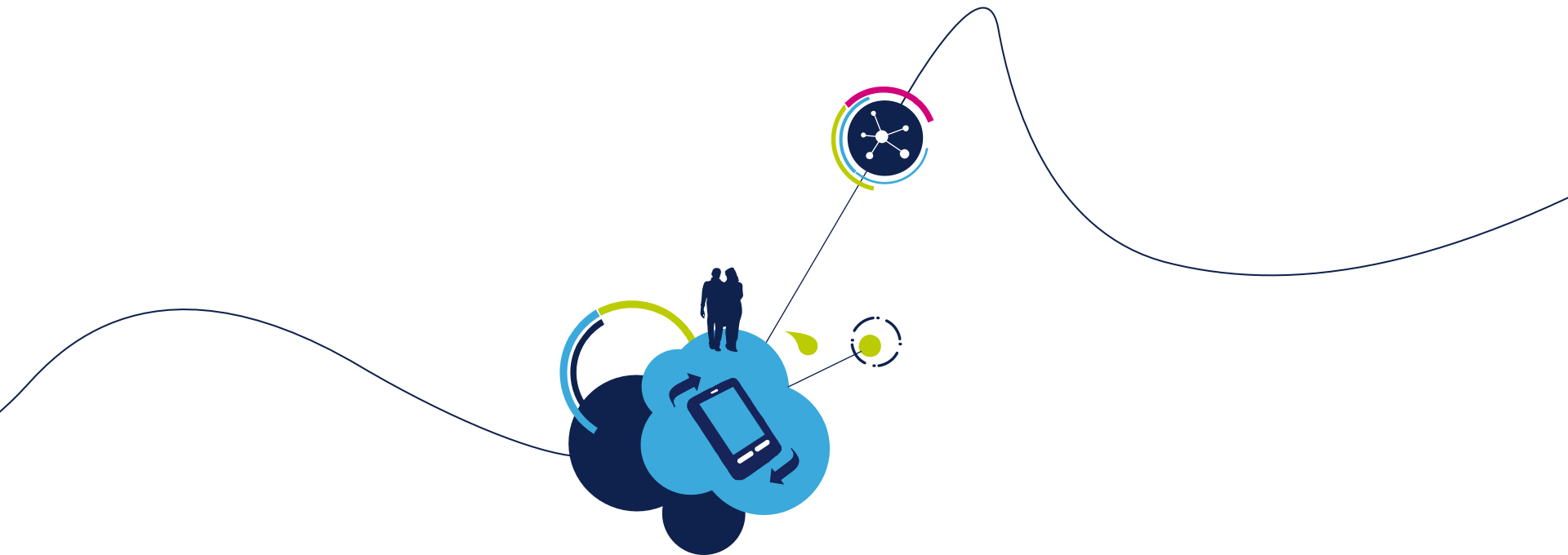
MARKET STUDY

Times

Embedded Systems Design

ESD  
Embedded.com  
The Official Site of the Embedded Development Community

**1700 MCU&DSP Developers questioned WW**

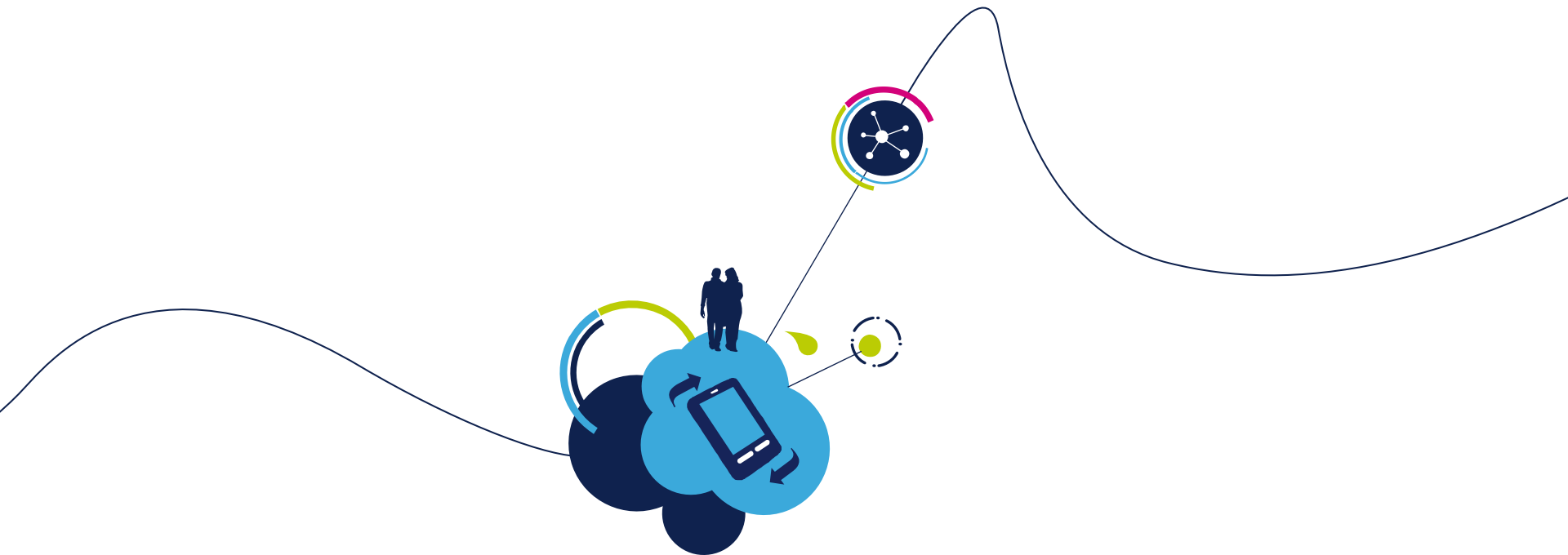


# Future

# MCU Trends – a selection of topics

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- Price → Technology
- Performance → Low Power and MIPS
- Memory size → Larger flash and RAM
- Peripheral Integration → analog, RF
- Industry standard cores → Cortex Mx
- Advanced Peripherals → USB Ethernet LCD SDRAM
- Predefined Libraries + RTOS → Abstraction from the hardware



Q & A

# After the session you should have learnt..

42

- Know the difference between a MCU and a MPU and a CPU.
- Differences between a 8 bit and 32 bit MCU.
- Differences between Risc and Cisc architecture
- Differences between Harvard and Von Neuman Architecture
- Temporary production technologies

# Thank you

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