Lecture 3, January 28, 2014

Electrical Characterization,B. Gunnar Malm
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Outline

- Measurement set-up, test-structures (samples/devices)
- Types of electrical measurements
- Real examples
- About the lab (sign-up, preparations)
- Summary

Outline Continued

•Most of the Chapters in Plummer have a subsection called:

•Mesurement Methods

• Electrical measurements

•3.4.1.2 Sheet resistance on page 113

•6.4.3 The MOS Capacitor on page 301

•7.4.3-4 Sheet resistance & Capacitance-Voltage on page 398

•11.4.2 Contact resistance/transfer length/oxide breakdown/accel. testing p.726

Other material

Well known book ”Semiconductor Material and Device Characteriztion, 3ed,” by Schroder covers electrical, physical and optical characterization methods

What do we want to measure?

1. Monitoring of process stability
   - Ultra-thin gate oxides, high-k dielectrics, sheet&contact resistance of doping and metal (silicides)
2. Performance of devices (MOSFETs) and circuits
3. Extract model parameters such as threshold voltage *(V_T)* or whole set of SPICE parameters

- This lecture mainly covers point 1

Test structures

- All measurements are typically on a 200-300 mm inch wafer. Map statistics at selected locations.
- MOS capacitances (or split-CV) for oxide studies
- Different types of 4-terminal resistance structures
  - Van der Pauw for sheet resistance of metals, silicides, implanted/activated dopants
  - Cross Bridge Kelvin for contact resistance (metal-to-semiconductor)
- Different MOSFET transistor sizes, use that $I_{drain} \propto W/L$

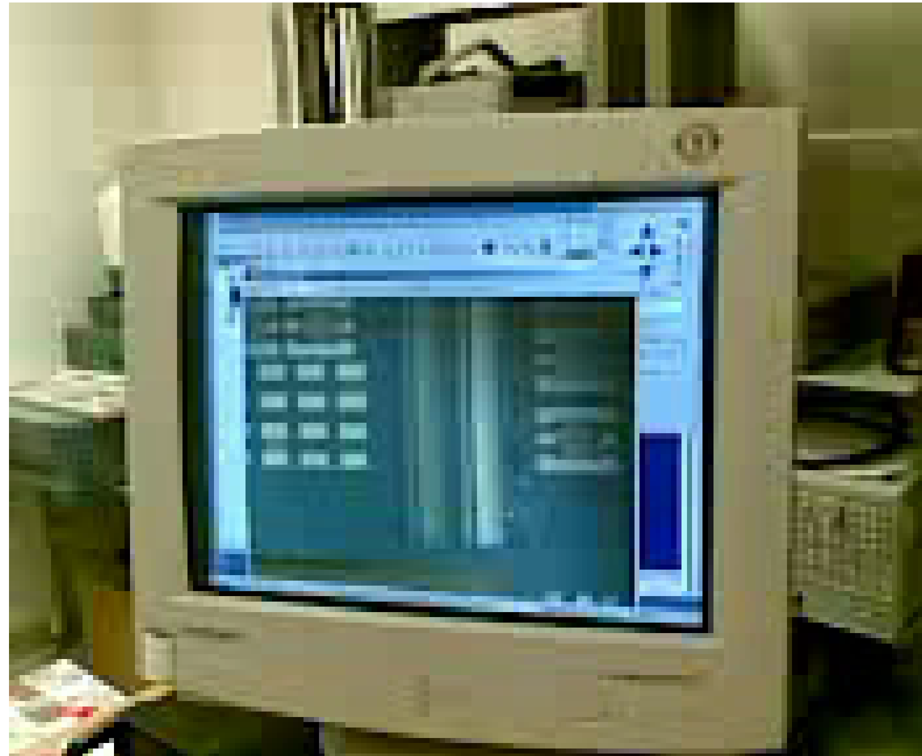
■Arrays of structures for in-line probe-card measurement (PCM)

Measurement setup

- Automatic 200 mm wafer prober and manual 150 mm wafers
  http://www.kth.se/ict/forskning/ickretsar/kiselbaserade-kompontenter

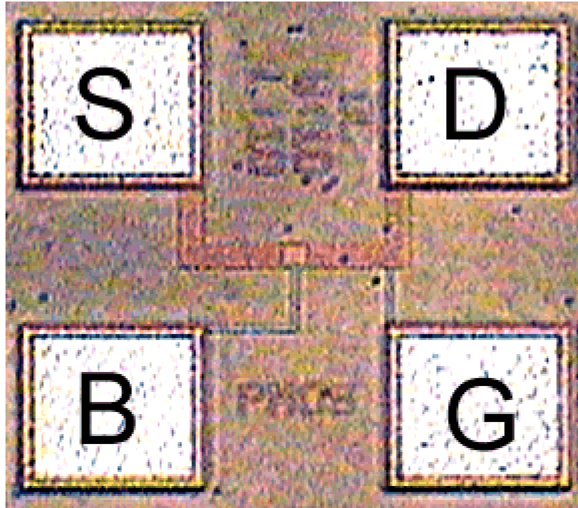
- Needle probes with micromanipulators
- Measurement equipment
  - 2 parameter analyzers (Keithley) with SMUs, pulse generator and coax-triax cables in Kelvin configuration)CV impedance bridge (Agilent/Keithley) <10 MHz
- Optical or IR-emission microscope and digital cameras

Measurement setup

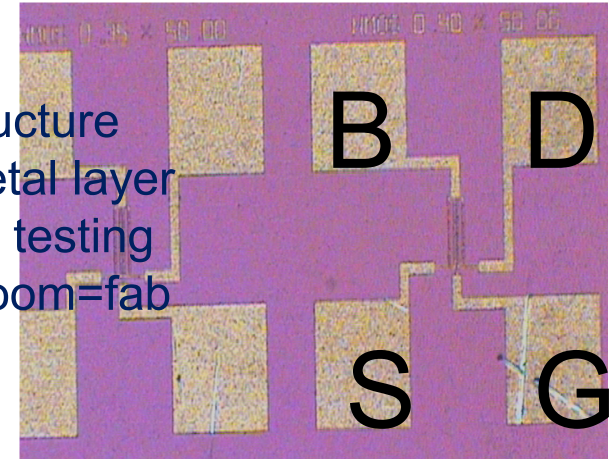


Test-structure layout

5-10 metal layers for interconnects. Top layer thick and soft metal (Al few microns)



Basic structure with 1 metal layer for in-line testing in cleanroom=fab



- Transistors with different gate areas (W/L) contacted with 4 connection source, drain, gate, bulk/ground
- Typical probing area 80x80 μm, pitch μm 100
- Probe card and switching matrix used to connect multiple devices
- Acronyms: DUT (device under test), PCM (probe card measurement)

Characterization types

- IV/DC with source/measure units (SMUs), possibly preamplifiers below 1pA
  - High current (example small resistance of metal/silicide line or contact)
  - Low current (gate and junction leakage, charge pumping)
  - Pulsed to get information about defects and avoid self-heating
- AC: Impedance and C-V mainly for MOS gate oxide but also channel mobility

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The 4-point principle (Kelvin)

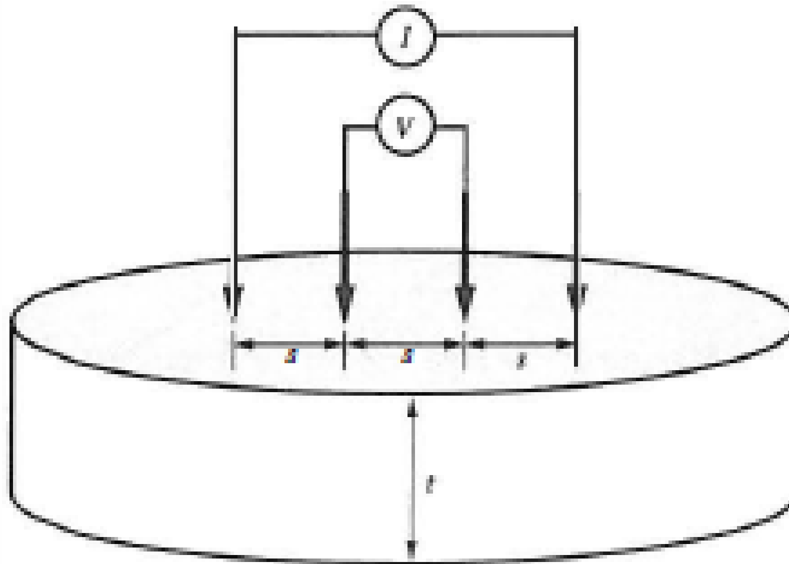
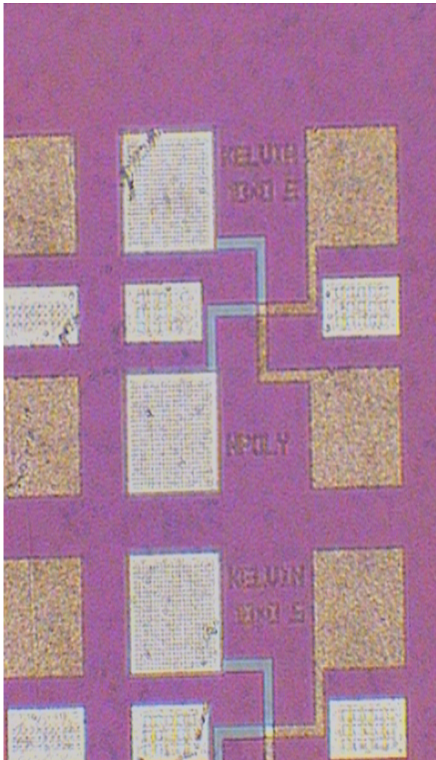


Figure 3–12 Four-point probe measurement method. The outer two probes force a current through the sample; the inner two probes measure the voltage drop.

Test-structure layout for resistance



- Cross-bridge Kelvin
- Contact resistance, metal to highly doped silicon or
- Metal to silicide

Test-structure layout for resistance

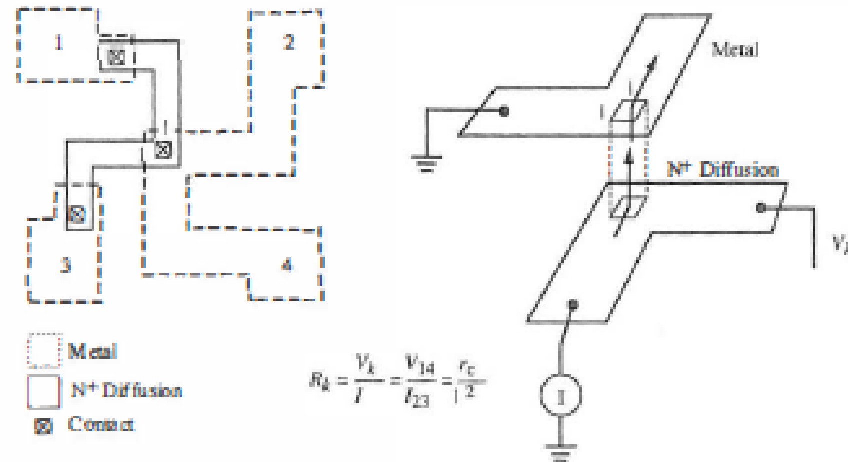
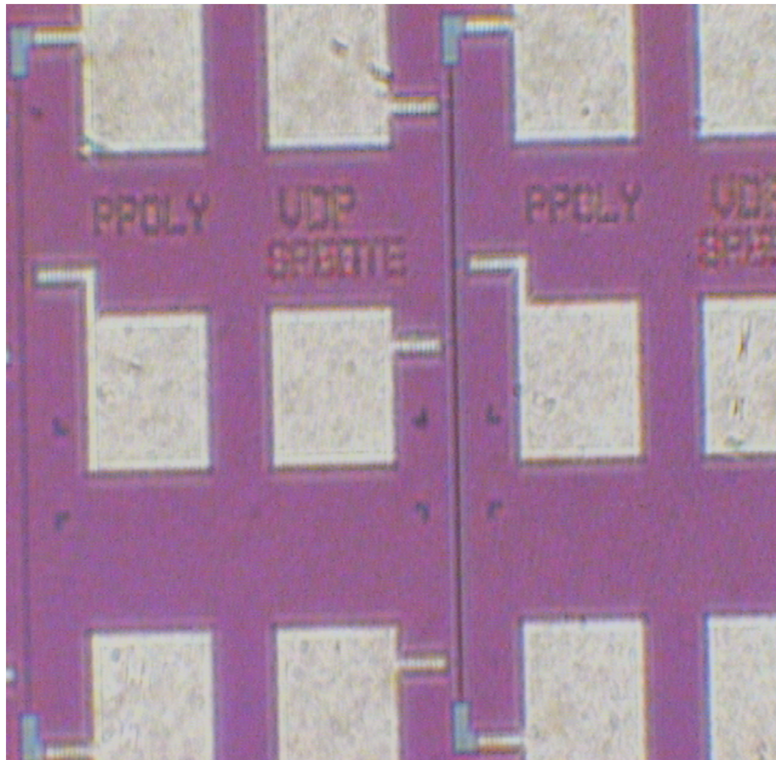


Figure 11–35 Cross-bridge Kelvin structure used to measure an average contact resistance, called R_k in the figure. (After [11.22].)

- Cross-bridge Kelvin

Test-structure layout for resistance



- Van der Pauw: 2 current terminals + 2 voltage sense terminals, different length of resistor lines
- Metal or metal silicide lines, approx 10 – 1000 Ω

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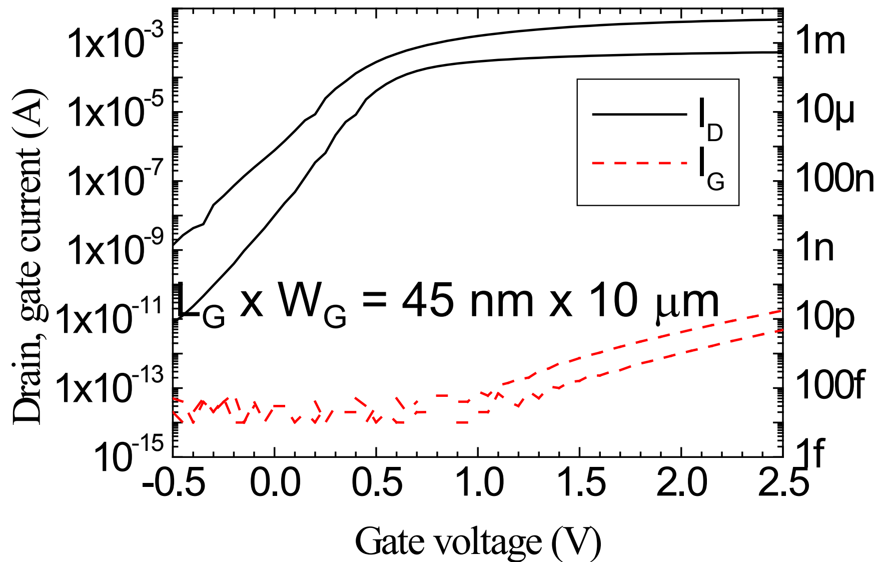
Low current measurements



- Below 10 fA is possible with triax cables
- Voltage resolution of 1 µV
- Problems – leakage current in cables and outside interference (RF/noise)

L3: Electrical Characterization - Concept Test 3.1

3.1 Electrical characterization is an important step in the wafer fabrication flow: Which statements are true?

(One or more answers may be correct)

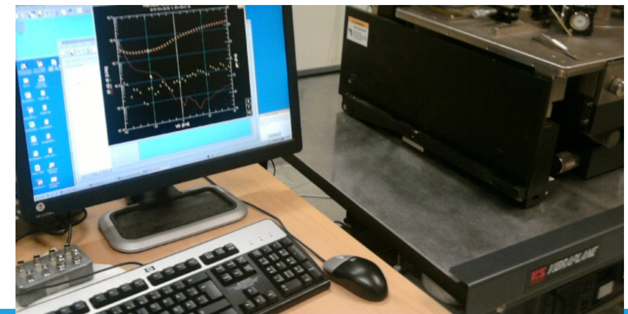
A. Measurements are usually done on completed wafers

B. Measurements are usually done during the process flow

C. Measurements are usually done on special test structures

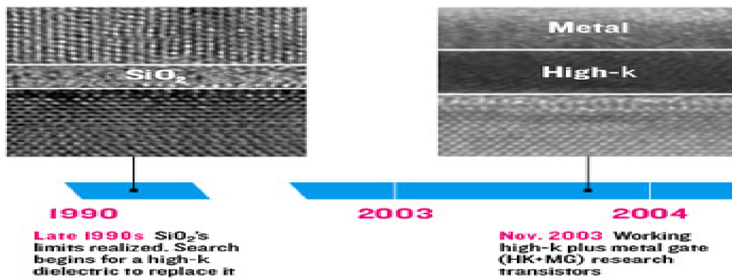
D. Measurements are usually done on transistors

E. None of the above.



MOS gate oxide – stability in focus

Figure 1.3: Comparision between SiO_2 and *high-k* material



- New high-k material introduced to reduce gate leakage
- Thicker layer – lower leakage
- Bulk & interface decfects, long term stability, stress effects et.c. must be characterized

MOS gate oxide process stability

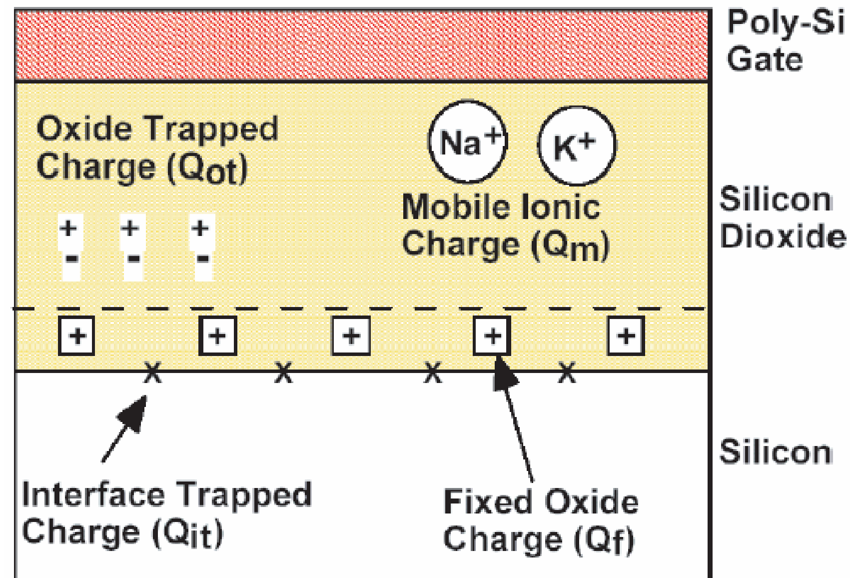


Figure 2.5: Types of charges and their distribution in the oxide

- Standard textbook picture of charge related oxide issues (inside bulk and at interface to channel region)

MOS gate oxide process stability

- Gate oxide thickness and quality
- CV - thickness, trapped charge *(also VT-shift)*
- CP - interface states
- IV - oxide integrity, leakage current, breakdown field, charge-to-breakdown (QDB, TDDB) , hot-carrier injection (HCI), stress (NBTI)

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Interpretation of real life MOS CV data

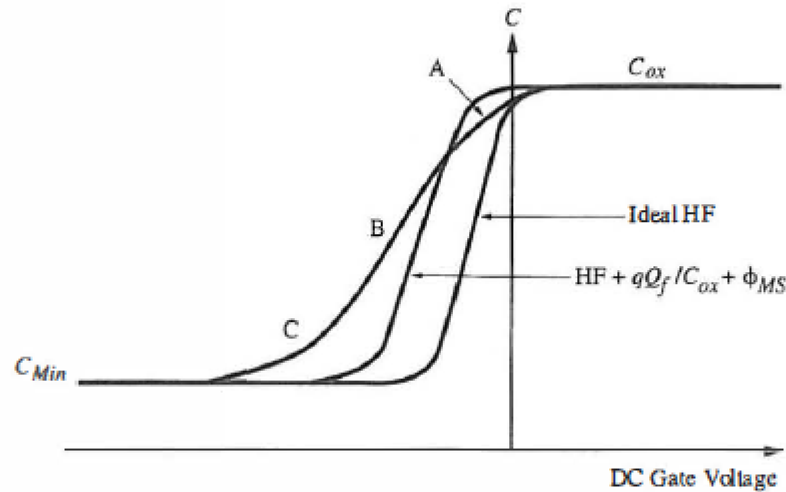
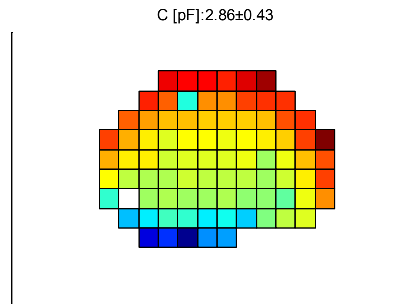


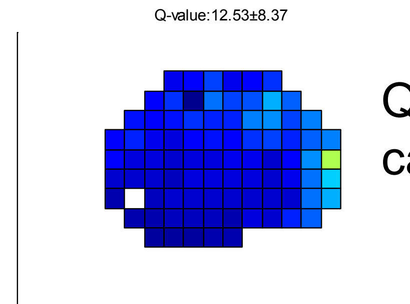
Figure 6–13 HF MOS CV curves illustrating some of the nonidealities that can be present in actual experimental structures. A, B, and C illustrate the effects of interface states with different energy levels in the silicon bandgap.

The set of CV curves from a wafer contains information about the charge in traps and interface states. Shift with respect to ideal curve shows the type of effect present.

MOS gate oxide process stability

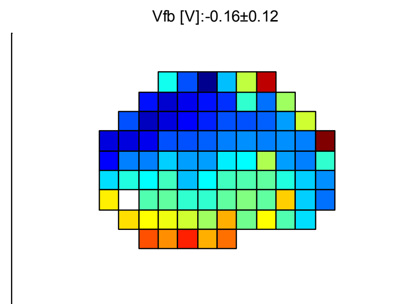
Capacitance ∝ 1/ oxide thickness

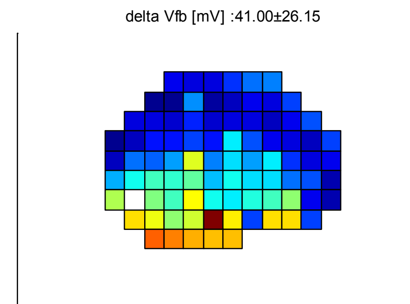




Q-value measure of capacitance/resistance

Influence of (trapped) charges

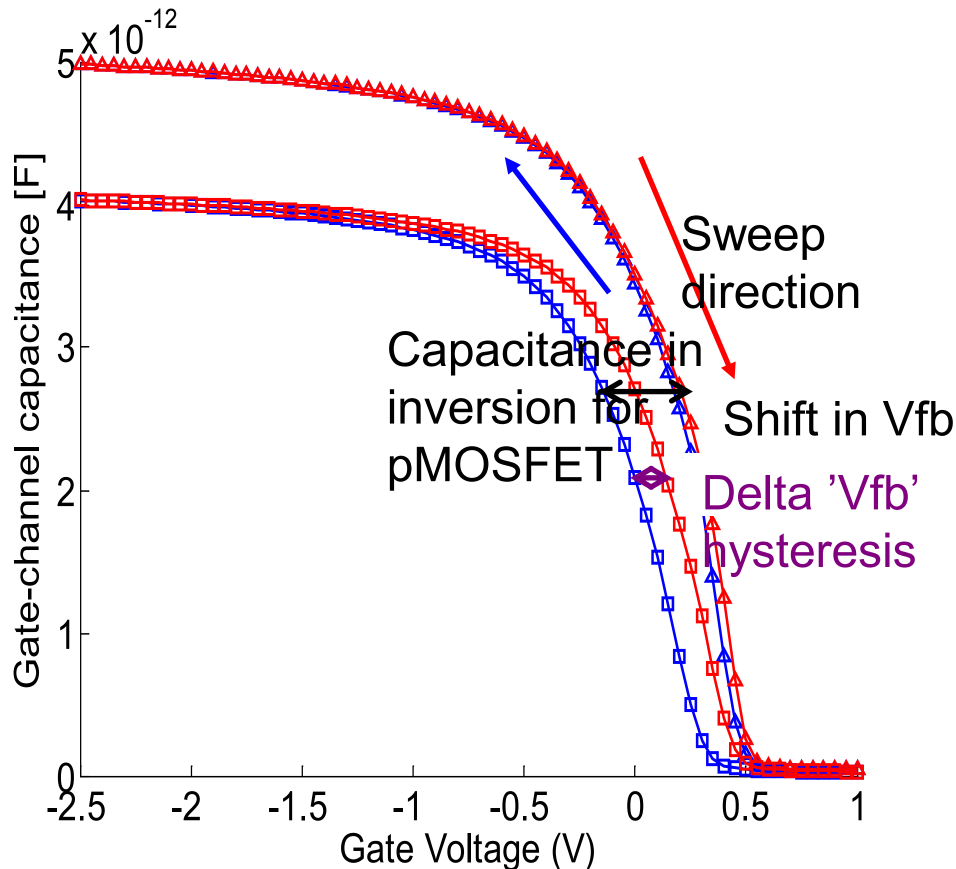




Hysteresis due to 'interface' states

- Gate oxide thickness and quality - 100 mm wafer map, metal-gate + high-k

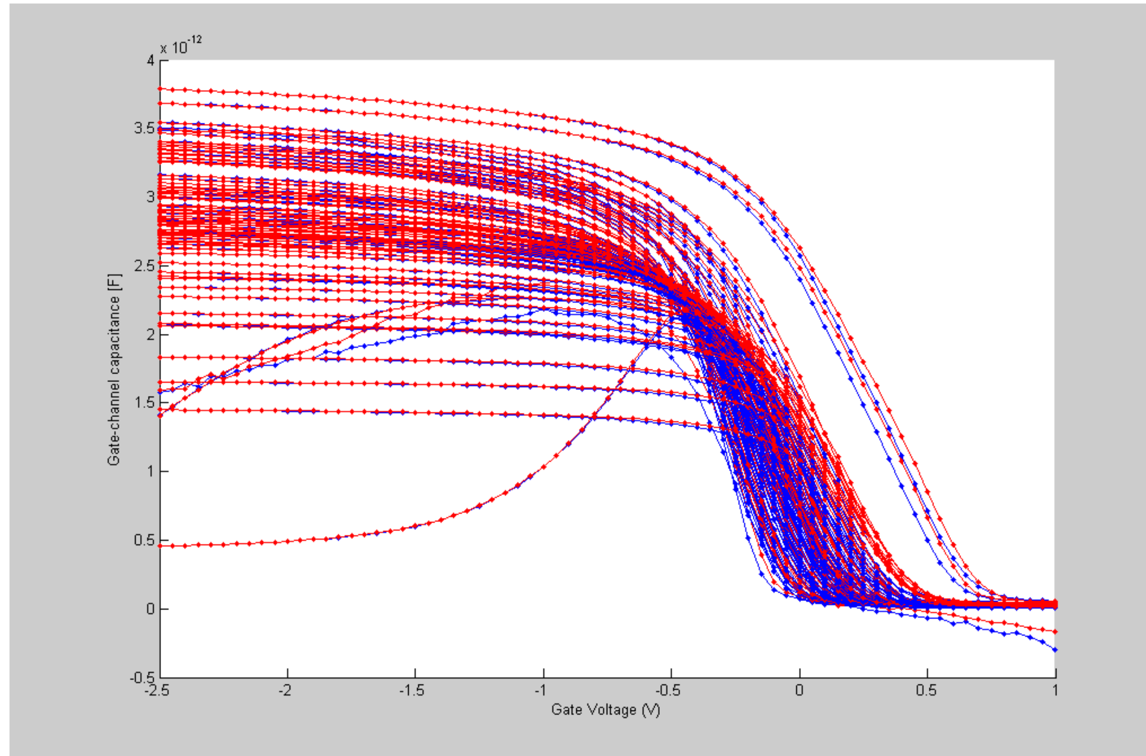
MOS gate oxide process stability



Split CV on MOSFETs, two devices on the same wafer

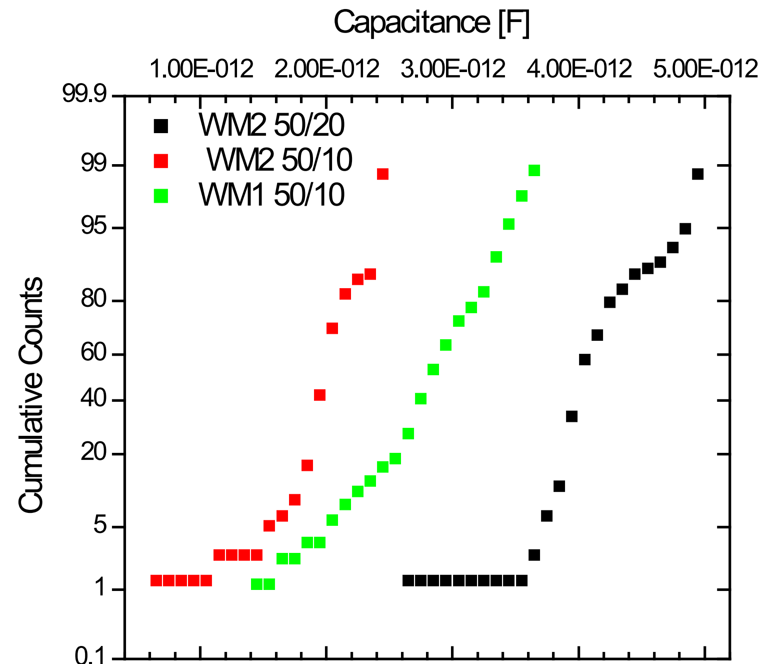
Capacitance in inversion for pMOSFET

MOS gate oxide process stability



- High-k HfO_2 based gate showed large variation over wafer

MOS gate oxide process stability



- Weibull distribution plots of capacitance, 2 different wafers/ 2 device gate areas
- Large slope = tight distribution = good sample

L4: Electrical Characterization - Concept Test 4.2

4.2 Electrical characterization is used to evaluate new materials: Which statements are true?

(One or more answers may be correct)

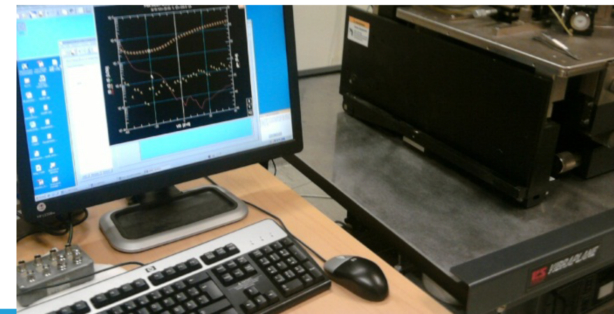
A. Capacitance-Voltage (CV) is the best technique to probe defects and thickness of thin oxides

B. Current-Voltage (IV) is the best technique to probe defects and thickness of thin oxides

C. Both IV and CV are needed to probe defects in thin oxides

D. Both IV and CV are needed to probe thickness of thin oxide

E. None of the above.



MOS gate oxide process stability

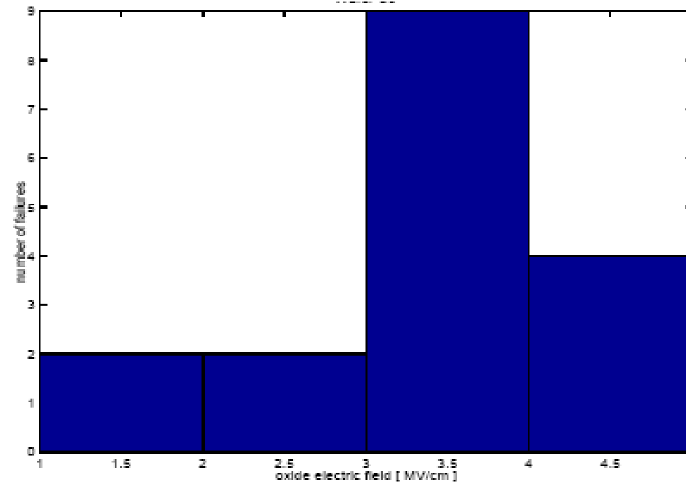
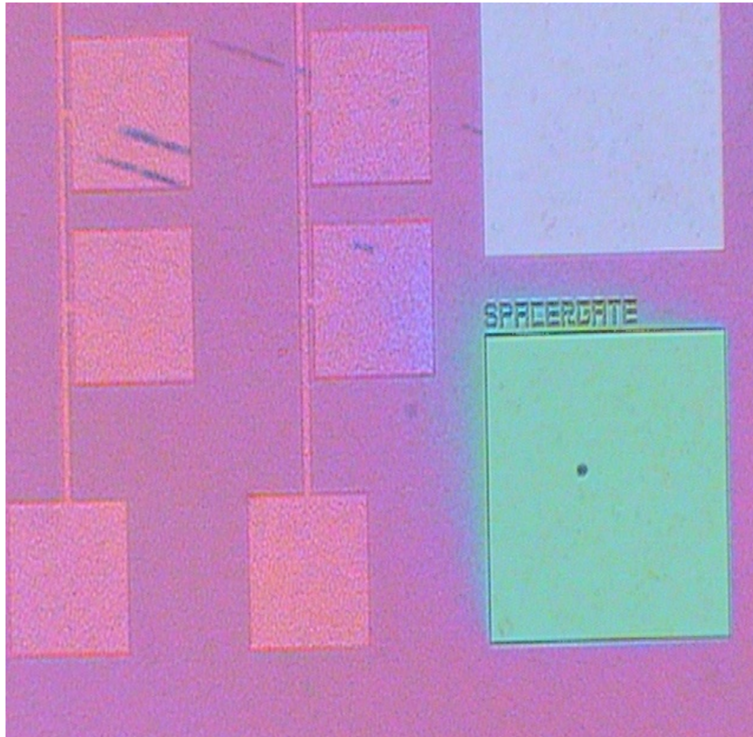


Figure 3.8: Number of failures versus oxide field for HfO_2 MOS capacitors on wafer C4

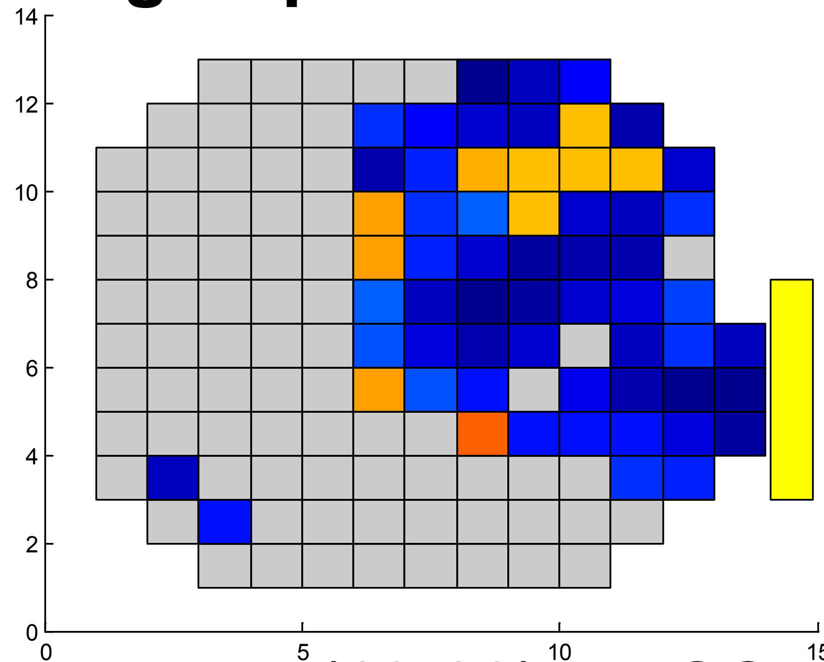
- Oxide integrity can be tested by applying high field
- Destructive – sweep until hard breakdown
- Non-destructive – soft breakdown, inject charges into oxide by constant field/voltage/current stress, measure charge-to-breakdown
- Useful acronyms: QBD, TDDB, HCI, NBTI, ...

Monitoring of process stability



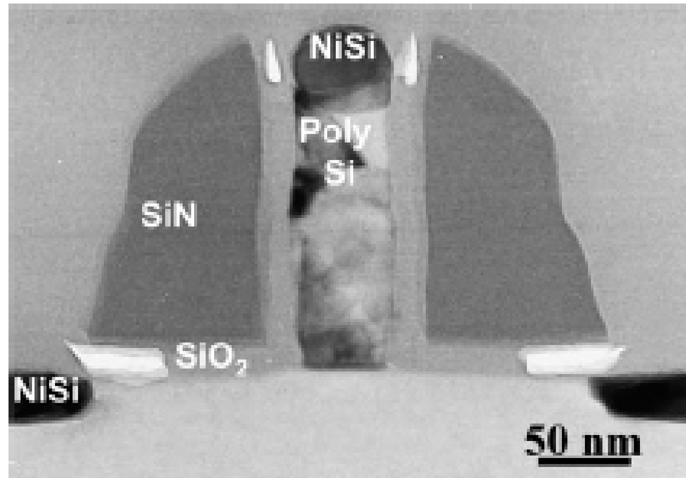
- Sheet-resistance measurements
- Uniformity of metal-silicide formation (resistance) across wafer
- Color shift (bluish to red) indicates problem!

Monitoring of process stability



- Silicide formation on thin (10-20) nm SOI substrate (contacts for MOSFET source/drain)
- Problem – to much silicon is consumed before contact formation

Monitoring of process stability



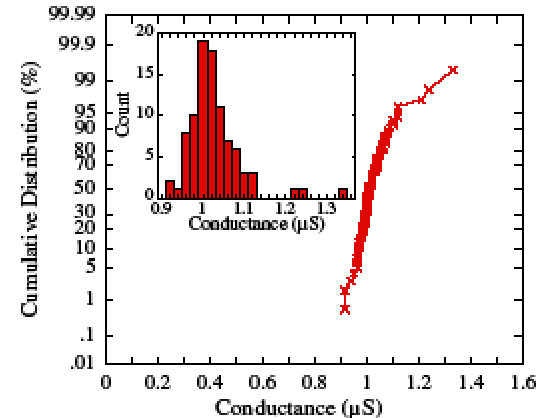


Fig. 7. Cumulative distribution of measured conductance across a wafer (90 dies). The poly-Si lines were 200 µm long and 40 nm wide.

- Gate length variation - critical dimension (CD) control
- Monitor gate electrode in 4-point resistor configuration across wafer, plot in Weibull graph

About the lab

- Sign-up sheets distributed in class
- Mandatory preparation 48 h in advance, email to: smedfors@kth.se
- PREL Instructions for 2014 available online, general theme IV measurement of high-k/metal gate wafers see above, also high mobility substrates
- Report due 1 week after completed lab, submit by email.

Summary

- Combination of IV, CV, and pulsed techniques needed to characterize wafer mainly after completed process flow but also in-line in the cleanroom
- Low-level measurements use special shielding techniques and/or calibration
- Special layout of test structures for challenging measurements – sometimes the transistor is the test structure
- Wafer mapping reveals trends and pinpoint process stability issues
- Recommended text by Schroder in addition to Plummer book

Sources

- IEEE Spectrum, ”The high-k solution,” online, Oct, 2007.
- Keithley – Low level measurements 6th ed
- Keithley – Overcoming the Measurement Challenges of Advance Semiconductor Technologies 1st ed
- Agilent Technologies Impedance Measurement Handbook 2003 (Online)
- Schroder – Semiconductor Material and Device Characterization
- Plummer et al – Silicon VLSI Technology
- Buono, Master Thesis, KTH, 2007