Mobility enhancement by integration of TmSiO IL in 0.65nm EOT high-k/metal gate MOSFETs

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Outline

- **Introduction**
  - EOT-mobility tradeoff
  - Advantages of high-k interfacial layers

- **Device fabrication**
  - TmSiO formation
  - Integration in a realistic gate stack

- **Results**
  - Electrical characterization of N- and P-MOSFETs
  - Mobility improvement compared to SiO$_x$/HfO$_2$ stacks

- **Conclusion**
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Introduction: IL scavenging

- High-k/metal gate technology suffers from EOT-mobility tradeoff
- The main factor is the thickness of the interfacial layer (IL)

[Ando 2012]

[Ando 2009]
Introduction: LaSiO IL

- IL thickness trade-off can be overcome by increasing $\kappa$
- La diffusion from capping layer can form a silicate IL with lower EOT

$$La_2O_3 \quad HfO_2 \quad SiO_x \quad Si$$

Activation anneal, $\sim 1000^\circ C$

Compatible with:
- N-MOSFET
- Gate-first
Introduction: high-k IL

Direct integration of a high-k IL can be designed to achieve:

- Compatibility with any gate stack (N and P)
- Compatibility with gate-first and gate-last integration
- Improvement of the EOT-mobility tradeoff curve

The silicate should be chosen as to provide:

- High $\kappa$ (>10)
- Good electrical quality of the interface with Si
- Compatibility with Hf-based gate stacks
Introduction: TmSiO

- Silicates can be formed from many lanthanide oxides

- Requirements:
  - Low reactivity with Si and H₂O -> High atomic number
  - k of the oxide > 15
  - E₇ of the oxide > 5 eV
  - Conduction and valence band offsets > 1 eV

- Tm₂O₃ is a good candidate: k=16, E₇=5.5 eV, CBO/VBO >2eV [Wang 2012]
- TmSiO has similar dielectric constant to LaSiO (k=10-12)
- TmSiO IL has been shown to provide good electrical properties [Denti Litta et al., IEEE Trans. Electr. Dev., Early access, 2013]
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Device fabrication

- Thulium silicate IL module is integrated with HfO$_2$/TiN stack
- Gate-last CMOS process
Device fabrication

- Starting substrate with pre-formed source/drain
- Surface clean in $\text{H}_2\text{SO}_4$:$\text{H}_2\text{O}_2$ and 5% HF
- Deposition of $\text{Tm}_2\text{O}_3$ by ALD

- **System:**
  - Beneq TFS 200
- **Precursors:**
  - $\text{TmCp}_3$ and $\text{H}_2\text{O}$
- **Deposition temperature:**
  - 250 °C
Device fabrication

- Post deposition anneal in N\textsubscript{2} for 60s
- TmSiO thickness is controlled by PDA temperature [Dentoni Litta et al., ULIS 2013]
- PDA at 500 °C yields 0.8±0.1 nm
Device fabrication

- $\text{Tm}_2\text{O}_3$ needs to be removed selectively
- Etching solution needs to be CMOS-compatible
- $\text{H}_2\text{SO}_4$ etches $\text{Tm}_2\text{O}_3$ with > 23:1 selectivity toward $\text{TmSiO}$
Device fabrication

- Deposition of HfO$_2$ by ALD (2 nm)
- Deposition of TiN by reactive sputtering (15 nm)
- Post metallization anneal (N$_2$, 425 °C, 5 min)
Device fabrication

- Gate patterning
- PECVD SiO\(_2\) passivation
- Ti/TiW/Al metallization
- Forming gas anneal

**Layer Details:**
- TiN (15 nm)
- HfO\(_2\) (2 nm)
- TmSiO (0.8 nm)
- Si
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Results: C-V characterization

- 30 N-FETs and 30 P-FETs measured on 100 mm wafer
- Low hysteresis:
  N: 0-50 mV, P: 0-20 mV
- EOT extracted by CVC fitting [Hauser 1998]:
  N: 0.65-1.1 nm  P: 0.8-1.2 nm
- Perfect agreement with CET values:
  N: 1.0-1.6 nm  P: 1.25-1.6 nm
Results: I-V characterization

- $I_DV_G$ characterization shows good uniformity
- Low subthreshold slope, symmetric $V_T$
- Mobility extracted by split-CV

 ![Graph showing I-V characteristics with $V_D=-1V, -0.1V, 0.1V, 1V$, $V_T=-0.45V, 0.6V$, $L_G=3\mu m$, and $S=65-70\, mV/\text{dec}$ for P-MOSFETs and $S=80-90\, mV/\text{dec}$ for N-MOSFETs.](image)

 ![Graph showing inverted layer mobility and inversion charge density for TmSiO/HfO$_2$ N-MOSFETs and P-MOSFETs.](image)
Results: low-field electron mobility

- Low-field mobility in N-MOSFETs is in line with scaled $\text{SiO}_x/\text{HfO}_2$ stacks.
Results: peak electron mobility

- Mobility improvement compared to SiO$_x$/HfO$_2$ stacks
- 20% increase in N-MOSFET peak mobility
Results: high-field electron mobility

- Mobility improvement compared to SiO$_x$/HfO$_2$ stacks
- 20% enhancement for N-MOSFETs at high field
Results: high-field hole mobility

- Mobility improvement compared to SiO$_x$/HfO$_2$ stacks
- 15% enhancement for P-MOSFETs at high field
Results: interpretation of the N mobility data

- Remote scattering mechanisms are modulated by IL thickness
- Thicker TmSiO IL (~0.8 nm) can reduce remote scattering from HfO$_2$
- Electron mobility in TmSiO/HfO$_2$ versus reference SiO$_x$/HfO$_2$:
  - Comparable low-field mobility
  - 20% higher peak and high-field mobility

![Graph showing mobility vs. inversion charge density](image)

Ando 2012
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- TmSiO IL can be integrated in HfO$_2$-based gate stacks
- Good electrical performance achieved for both N and P-MOSFETs
  - Subthreshold slope = 80-90 mV/dec for NFETs, 65-70 mV/dec for PFETs
- Low EOT achieved in gate-last CMOS process
  - 0.65 nm for NFETs, 0.8 nm for PFETs
- Observed electron/hole mobility improvement at high field
  - +20% for NFETs, +15% for PFETs
  - Likely consequence of the higher physical thickness of the IL
Acknowledgment

European Union ERC Advanced Grant 228229 "OSIRIS"

Swedish national research infrastructure for micro and nano fabrication

European Union, Network of Excellence Nanofunction (NoE: 257375)

Thank you for your attention