IL2236 Embedded Many-Core Architectures 7.5 credits

Arkitekturer för inbyggda mångkärniga system

Course syllabus for IL2236 valid from Spring 16

This is a translation of the Swedish, legally binding, course syllabus.

Grading scale: A, B, C, D, E, FX, F
Education cycle: Second cycle
Main field of study: Electrical Engineering

Intended learning outcomes

After studying the course, the students shall be able to do the following as learning outcomes:

- Describe and compare various on-chip bus protocols and arbitration schemes.
- Explain and apply concepts and design principles of interconnection networks in topology, routing, flow control, deadlock/livelock and quality-of-service (QoS).
- Describe and model on-chip pipelined routers, as well as describe and compare processor-network interface designs.
- Establish network performance evaluation setups, make qualitative and quantitative evaluation of network performance using theoretical and simulation methods.
- Describe real-time networking principles in embedded systems, explain and compare time-triggered and event-triggered protocols in general and industrial protocols such as CAN, FlexRay and TTP in particular.
- Explain and apply worst-case communication time analysis techniques in distributed embedded architectures.

Course main content

The course focuses on the communication problem of on-chip and off-chip many-core architectures in embedded systems. It teaches basic concepts and principles of on-chip bus and interconnection network, and presents details of on-chip router and network interface designs, network quality-of-service (QoS) provisioning and performance evaluation methodology. Moreover, it discusses realtime networking and worst-case communication time analysis in embedded many-core architectures and introduces industrial practices such as CAN, FlexRay and TTP.

The course consists of ten lectures, and 4 exercises, one of which can be in the mini-project form. An invited lecture from industry or academia may be organized.

The lectures are structured as three modules:

Module I: Concepts and principles

This module introduces the problems in many-core systems with focus on communication architectures. Concepts and principles of on-chip buses and interconnection networks will be presented. Particularly, network topology, routing and flow control, deadlock and livelock issues et cetera. will be investigated.

Module II: Design and evaluation

This module focuses on on-chip router and processor-network interface designs, QoS properties, and performance evaluation. The micro-architecture of a classic router will be detailed and network interfaces for both message passing and shared memory architectures will be presented. As a crucial component for network design, QoS properties of different design alternatives will be investigated. Furthermore, performance evaluation methodology will be systematically introduced.

Module III: Distributed realtime architectures

This module considers distributed many-core systems in embedded environments such as automotives and airplanes. Various media-access protocols for real-time networking will be studied. Particularly, industrial standards such as CAN, FlexRay and TTP will be introduced. Moreover, worst-case communication time analysis methods will be presented.

Language of instruction

Language of instruction is specified in the course offering information in the course and programme directory.

Eligibility

- Programming skill in one design language, e.g. C/C++, Python, Java, or SystemC (IL2206 Embedded Systems or IL2452 System Design Languages).
- Verilog/VHDL (e.g. IL2217 Digital Design with HDL).

Literature

- Willian J. Dally and Brian Towles, "Principles and Practices of Interconnection Networks". Morgan Kaufmann Publishers.
- Hermann Kopetz. "Real-Time Systems: Design Principles for Distributed Embedded Applications". Springer.
- Recommended manuscripts and research papers

Examination

- ANN1 - Homework Exercises, 3.0 credits, grading scale: P, F
- TEN1 - Examination, 4.5 credits, grading scale: A, B, C, D, E, FX, F