FIS3202 Computer Systems Architecture 10.0 credits

Datorsystemarkitektur

This is a translation of the Swedish, legally binding, course syllabus.

If the course is discontinued, students may request to be examined during the following two academic years

Establishment

Course syllabus for FIS3202 valid from Spring 2010

Grading scale

Education cycle

Third cycle

Specific prerequisites

Knowledge corresponding to course IS1200.

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

The overall objective with the course is to give knowledge and insights into the design of modern computers, in particular the processor design including parallel computational pipelines and advanced memory hierarchies.

The student should, for a passing grade, be able to>

*** account for the basic quantitative principles of computer design,**

*** explain the design and function of microprocessors with parallel computational pipelines and dynamic scheduling of instructions,**

*** explain the design and function of a memory hierarchy for the above mentioned microprocessor,**

*** explain the design and function of a multi-core processor with shared address space,**

*** identify and predict a program behaviour favoured by a certain microarchitecture of a processor,**

*** design and implement a simple parallel program with shared memory and explain its performance on a certain processor architecture with multiple cores,**

*** describe how simulation can be used to evaluate different architectural alternatives,**

*** propose and motivate a modification to a processor architecture which has potential to improve performance with the same power consumption,**

*** propose and motivate a modification to a processor architecture which has potential to lower the power consumption with the same performance**

Furthermore, the student should be able to plan and carry out a simple research study within the context of the course.

Course contents

*** Memory hiearchies, hardware for virtual memory management and memory protection**

*** Software and hardware methods for utilizing instruction level parallelism**

*** Orientation about thread level parallelism and hardware mechanisms to utilize thread level parallelism**

*** Orientation about shared memory and memory coherence**

Course literature

Computer architecture: A quantitative approach, John Hennessy, David Patterson

Upplaga: Fourth edition Förlag: Morgan Kaufmann År: 2006

ISBN: 0-12-370490-1

Laboration manuals, articles etc. distributed through the course web site.

Examination

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

Laboratory exercises on own computer

Forskningsrapport

The laboratory exercises may be accounted for orally or written. Peer review of written reports may occur.

All written reports will be checked for plagiarism.

Grading scale: P/F

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.