IL2203 Digital Design and Validation using Hardware Description Languages 9.0 credits

Digital design och validering med hårdvarubeskrivande språk

This is a translation of the Swedish, legally binding, course syllabus.

Establishment

The official course syllabus is valid from the autumn semester 2021 in accordance with Head of School decision: J-2021-0878.Decision date: 15/04/2021

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Electrical Engineering, Computer Science and Engineering

Specific prerequisites

- Basic digital technology equivalent to IE1204 Digital Design.
- Basic knowledge of the structure of microprocessors and instruction execution equivalent to IS1200 Division of Computer Systems, basic course.
- Basic knowledge of electric circuits equivalent to either IE1206 Embedded electronics, or EI1110 Electrical Circuit Analysis, Extended Course

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

After a passed course, the student should be able to

- use hardware description languages to model digital hardware
- mention and explain the different stages in the design flow for digital hardware
- point out the subset of a hardware description language that can be synthesized
- describe differences between the most common hardware description languages
- describe different architectures for digital hardware implementation
- design and validate digital hardware that is implemented on an FPGA
- explain the fundamental functionality of a hardware description language for modelling and validation of digital hardware
- use typical design and validation methods for combinatorial circuits, asynchronous and synchronous state machines and bus structures
- describe the different validation stages of digital hardware.

Course contents

- Introduction to hardware description languages
- Introduction to general system design flow and implementation techniques; FPGAs versus ASICs
- Modelling of digital systems by means of VHDL
- Construction and analysis of combinatorial and sequential components
- Asynchronous and synchronous state machines
- The subset of VHDL that can be synthesized
- Introduction to synthesis methodology
- Synthesis for FPGAs
- Microcontrollers/processors and data buses
- Introduction to Verilog and SystemVerilog
- Validation methods for embedded digital systems: Validation versus verification, randomised stimuli and constraints, code coverage, test coverage, regression test

Examination

- TEN1 - Written exam, 3.0 credits, grading scale: A, B, C, D, E, FX, F

- SEM1 - Seminars, 1.5 credits, grading scale: P, F
- LAB1 - Laboratory work, 3.0 credits, grading scale: P, F
- LAB2 - Laboratory work, 1.5 credits, grading scale: P, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

If the course is discontinued, students may request to be examined during the following two academic years.

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.