IL2204 DSP-Construction with HDL 7.5 credits

DSP-konstruktion med HDL

This is a translation of the Swedish, legally binding, course syllabus.

Establishment

Course syllabus for IL2204 valid from Autumn 2008

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Specific prerequisites

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

After finished course the student should be able to

1) use Control and Data Flow Graphs (CDFGs) to model and implement known digital signal processing functions (FIR/IIR/FFT) on FPGAs.

2) make calculations on the effects/limitations that the selection of datatype/resolution has on the implementations of known DSP-functions.

3) understand and utilize the addressing of memories to the DSP-functions for the optimization of them.

4) optimize the implementation wrt area/delay/latency/power consumption.

5) build prototypes of DSP-cores on FPGAs.

Course contents

Introduction to analog and digital filters. Applied signal processing.

Design methods for data intensive applications, for instance, within Digital Signal Processing and Telecommunication: Allocation, Scheduling, Binding, Pipelining, Retiming, Bit-serial Design.

Implementation methods for digital filter functions (FIR, IIR, FFT). FPGA-synthesis of filter functions. The DSP processor. DSP-cores as part of an embedded system. A/D and D/A-conversion.

Course literature

Lecture notes (pdf/ppt-format).
3 Laboration instructions (published on the course web page).
Additional material not contained in the course book.

Examination

- TEN1 - Examination, 3.0 credits, grading scale: A, B, C, D, E, FX, F
- LAB1 - Laboratory Work, 4.5 credits, grading scale: P, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

If the course is discontinued, students may request to be examined during the following two academic years.

Grading scale: A/B/C/D/E/Fx/F

Other requirements for final grade

One written exam (TEN1 3hp),
passed laboration course (LAB1 4.5hp) with 2 obligatory laborations (FIR-filter and FFT).

The laborations are driven in project form. The students are supposed to work independently on their own in groups of maximum two students, without any help from the lab assistants. The lab assistants are available for tool support only, and for checking finished lab projects.

For each lab, a short laboration report (~2-3 pages) documenting all results obtained should be submitted to the assistants before the assistants will come and check the simulations and the working FPGA prototype.

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.