IL2208 Electronic System Packaging 7.5 credits

Electronic System Packaging

This is a translation of the Swedish, legally binding, course syllabus.

Establishment

Course syllabus for IL2208 valid from Autumn 2008

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Electrical Engineering

Specific prerequisites

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

The objective of this course is to provide a coherent and pragmatic overview of relevant issues of physical architecture design of complex electronic system presented in such way that practicing electronics designers can communicate with experts in other fields and extract relevant design data for circuit and system design.

Course contents

This course provides a unified view of physical architecture of electronic systems from chip to cabinet via focus to interconnectivity and interconnections and their impact to performance and signal integrity and signal couplings. Our aim is to provide a coherent and pragmatic view for understanding the system performance constraints and their dependencies of the underlying technologies in order to define physical architecture of mixed signal systems. During the course we will

- Summarize the key interconnection technologies from chip to system with focus on the underlying principles and new technologies which will remain the basic for electronic design and manufacturing through the next decade
- Emphasize the interaction of chip and higher packaging level technologies for mixed signal system electrical design and system partitioning to different packaging technologies
- Analyse systematically the key electrical phenomena at chip, package and interconnection substrate levels defining the system signal integrity and robustness properties in order to define the future constraints to integration for communication and consumer electronic products.
- Emphasize the impact of deep sub micron CMOS technologies to system partitioning and packaging technologies.
- Introduce the early conceptual design for partitioning of the complex system to different packaging and interconnect hierarchies.

Course literature

Stephen H. Hall et al: High-Speed Digital System Design, Wiley Publishers, ISBN: 0-471-36090-2

Examination

- TEN1 - Examination, 4.5 credits, grading scale: A, B, C, D, E, FX, F
- LAB1 - Laboration Course, 3.0 credits, grading scale: P, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

If the course is discontinued, students may request to be examined during the following two academic years.

Other requirements for final grade

Laboratory course (LAB1; 3 hp)
Examination (TEN1; 4,5 hp)

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.