IL2222 Digital Circuit Design for Nanoscale CMOS 7.5 credits

Digital design av kretsar i nanoskala för CMOS

This is a translation of the Swedish, legally binding, course syllabus.

Establishment

Course syllabus for IL2222 valid from Autumn 2008

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Electrical Engineering

Specific prerequisites

120 university credits (hp) in engineering or natural sciences and documented proficiency in English corresponding to English A.

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

After having completed the course a student should be able to:

- explain the design solution and key properties of modern nanoscale CMOS circuits

- to analyze and select design solutions of nanoscale phenomena in digital circuit and micro architecture level.

- apply theory and practice for designing modern nanoscale CMOS digital circuits and logic system towards performance, yield optimization and variability mitigation in technologies such as power reduction, clocking/synchronization, and variability mitigation.

- be familiar with the use of modern Computer Aided Design tools

- search critically literature and Internet through IEEE Explore as well as work in a team ofdesign-ers.

Course contents

In this course we study in detail all the necessary phenomena relating to logic value changes inside the logic circuit with emphasis on advanced nanoscale phenomena. The key issues in this course are to understand the nature of performance parameters such as silicon area, speed and power consumption. The structure and contents are quite similar to VLSI design courses given at many universities. The main difference is in nanoscale phenomena and bringing up power consumption issues.

This course aims to analyze and design digital integrated circuits with advanced full cus-tom and standard cell techniques based on nanoscale CMOS. We emphasize the key new phenomena and design solutions adopted to handle nanoscale phenomena at circuit and micro architecture level.

Syllabus

Review of the IC development trends. The future of IC technologies is discussed. The technology scaling models and new device level phenomena of deep submicron MOS transistors is presented.

Review of the MOS transistor physics and device model, especially the key submicron device phenomena relevant to the VLSI circuit operations

A very simplified CMOS process flow is introduced. Nanoscale CMOS issues to circuit layouts and floorplans are presented

CMOS logic from power and performance perspective are analyzed.

Power consumption in CMOS and leakage power as well as voltage scaling issues are described

Performance optimizention through micro architecture design for data paths are described

Sequential logic circuit, registers, timing and clock distribution challenge are analyzed in modern CMOS circuits

Circuit techniques for data path structures are described. Different adder and multiplier implementation schemes are introduced. Pipelining is introduced. Impact of the Vdd scaling and associated pipelining and parallelization techniques for the reduction of the data path power consumption are described.

Metal wires and interconnect as design objects are described.

Variability reduction and design optimization techniques are introduced.

Memory and Network-on-Chip architectures .

Course literature

Up-to-date issues as published in Journal of Solid-state Circuits, and in proceedings of International Conference on Solid-State Circuits (ISSCC), and European Solid-State Circuits Conference (ESSCIRC). Access through IEEE Explore required

Examination

- TEN1 - Examination, 4.5 credits, grading scale: A, B, C, D, E, FX, F
- LAB1 - Laboratory Work, 3.0 credits, grading scale: P, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

If the course is discontinued, students may request to be examined during the following two academic years.

Other requirements for final grade

Passed assignments (LAB1, 3hp)
Written exam (TEN1, 4,5hp)

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.